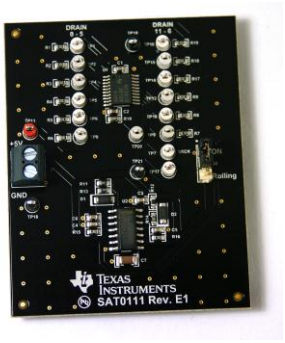
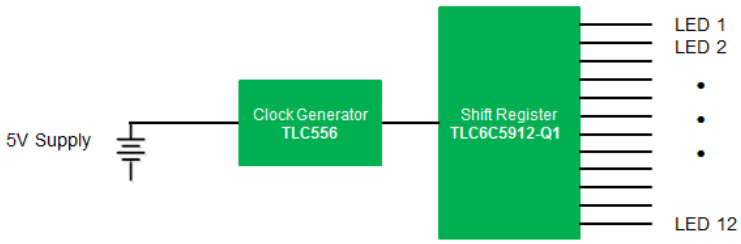
TIDA-00336 TI Design Test Data
Automotive LED Sequential Brake/Turn Light Reference Design

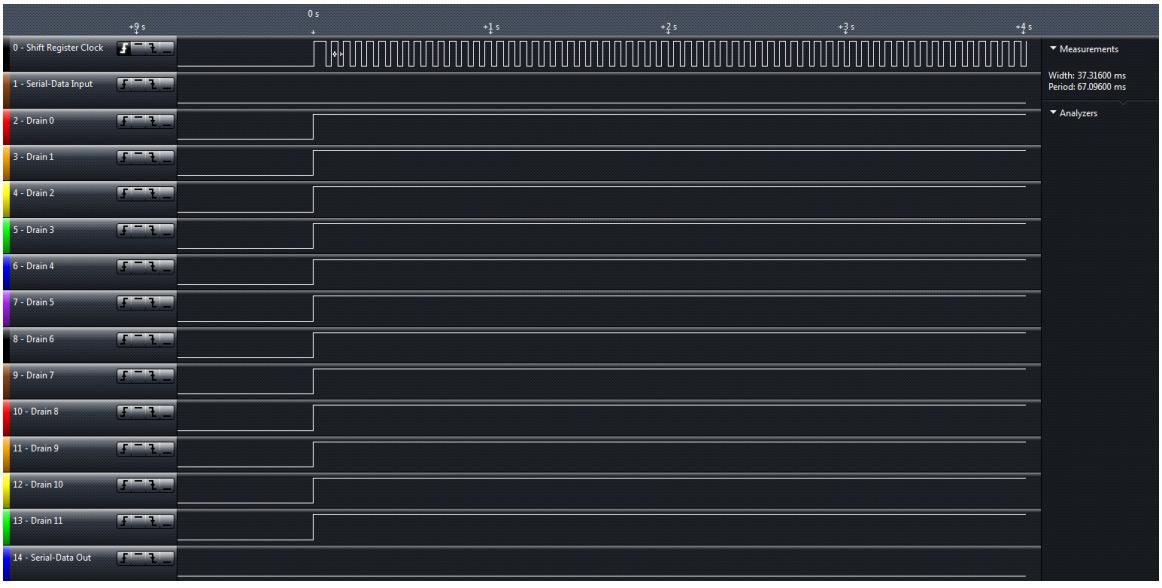
The following contains test data for the TIDA-00336 evaluation board collected on a Saleae 16-Channel logic analyzer and Tektronix MDO3024 oscilloscope. An Agilent E3644A power supply provided 5V DC to Vcc test pins on the evaluation board throughout testing. A photo of the evaluation board and block diagram for the system are included below.





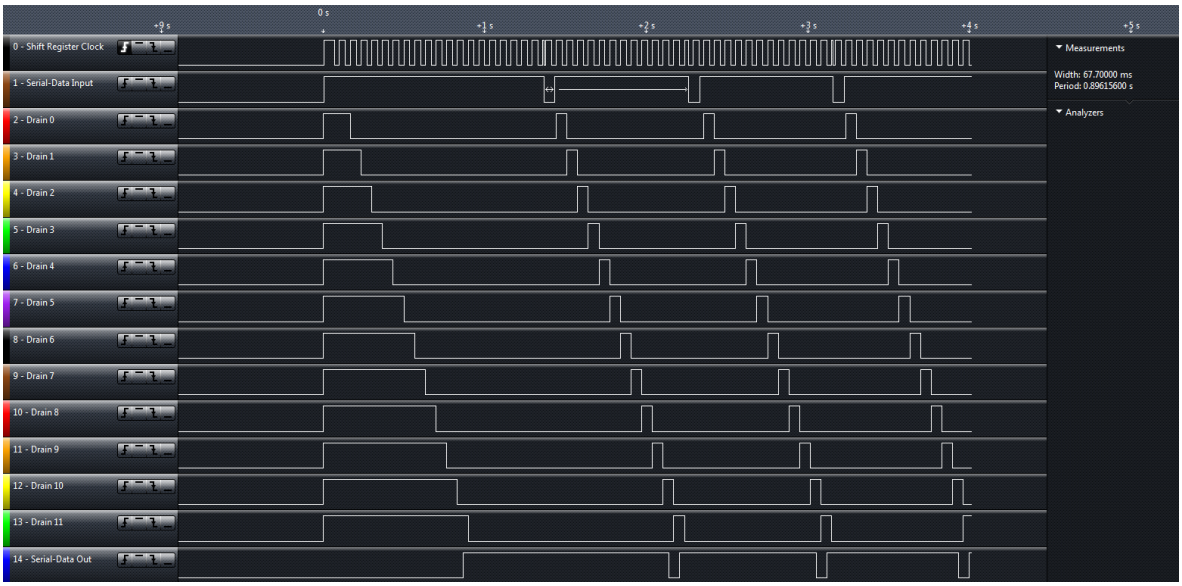
The design includes two modes of operation (ON and ROLLING) set by a jumper. ON operation sets each output to 5V. ROLLING operation cycles the state of the outputs sequentially.

A. Output logic states in ON operation.
With no load applied to the outputs and 5V DC supply, the design consumes approximately 1mA with jumper set to ON.



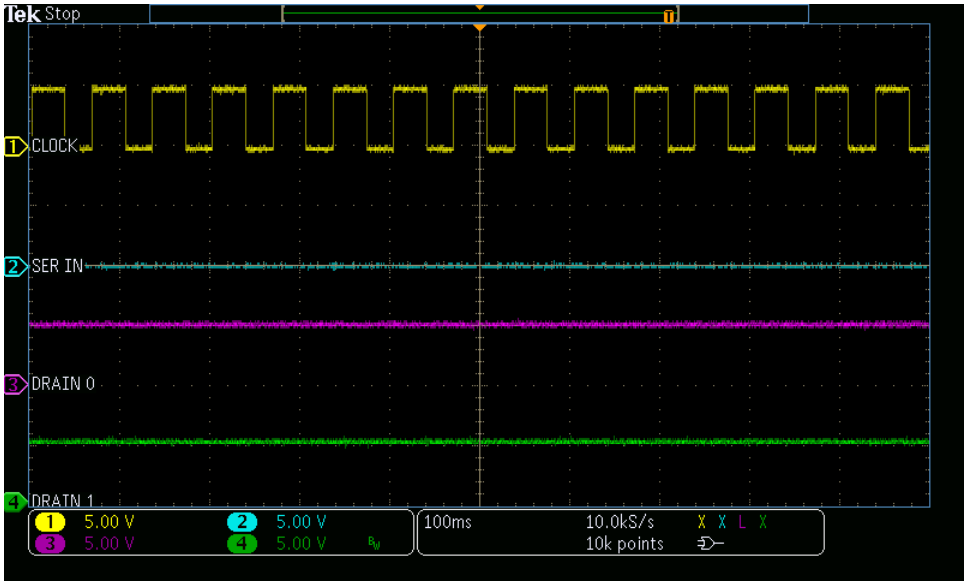
B. Output logic states in ROLLING operation.

With no load applied to the outputs and a 5V DC supply the design consumes approximately 6mA with jumper set to ROLLING.



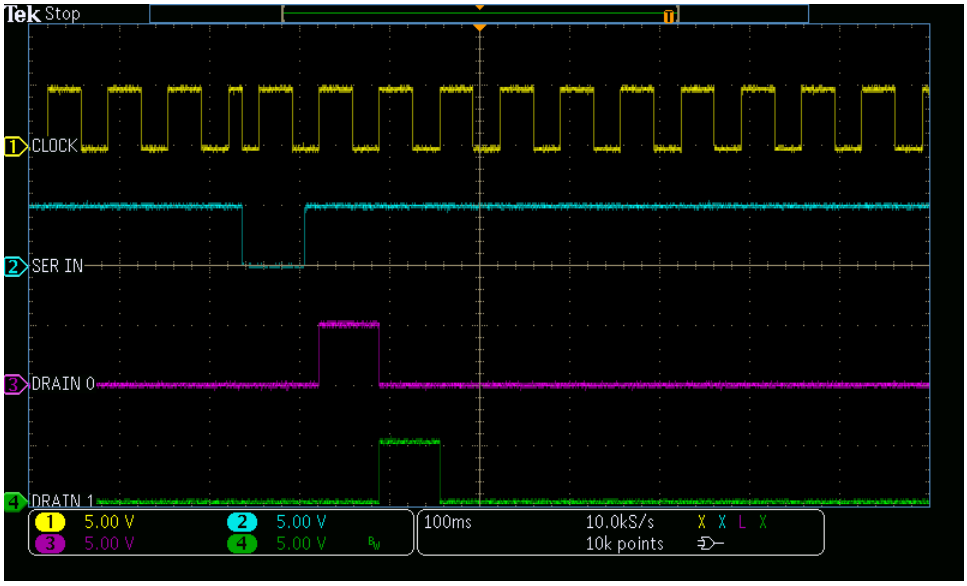
C. Oscilloscope captures of ON operation

The following capture contains voltage measurements for the Shift Register Clock (TP7), Shift Register Serial-data Input (TP20), Drain 0 (TP1), and Drain 1 (TP2) while jumper is set for ON operation mode.



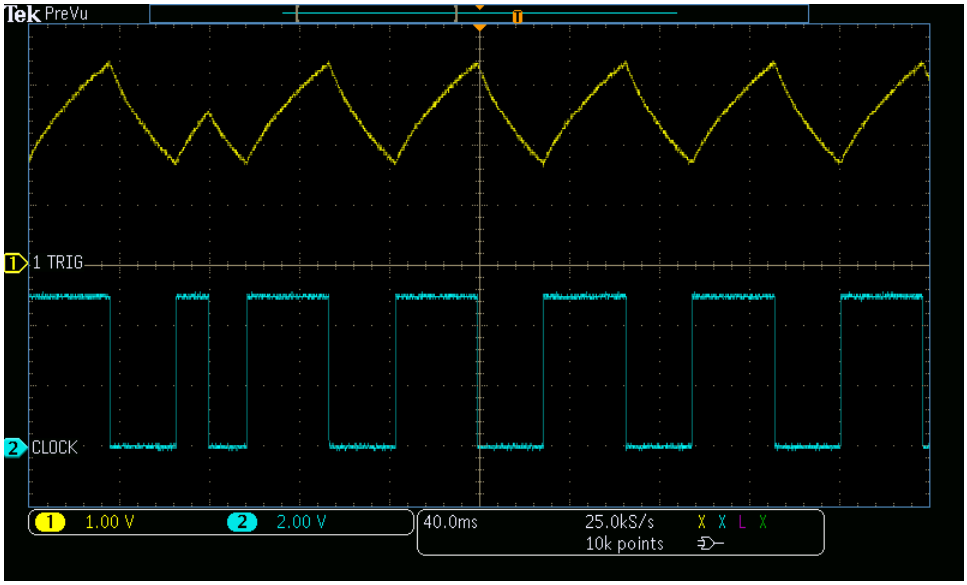
D. Oscilloscope captures of ROLLING operation

The following capture contains similar voltage measurements for the Shift Register Clock (TP7), Shift Register Serial-data Input (TP20), Drain 0 (TP1), and Drain 1 (TP2) while the jumper is set for ROLLING operation mode.



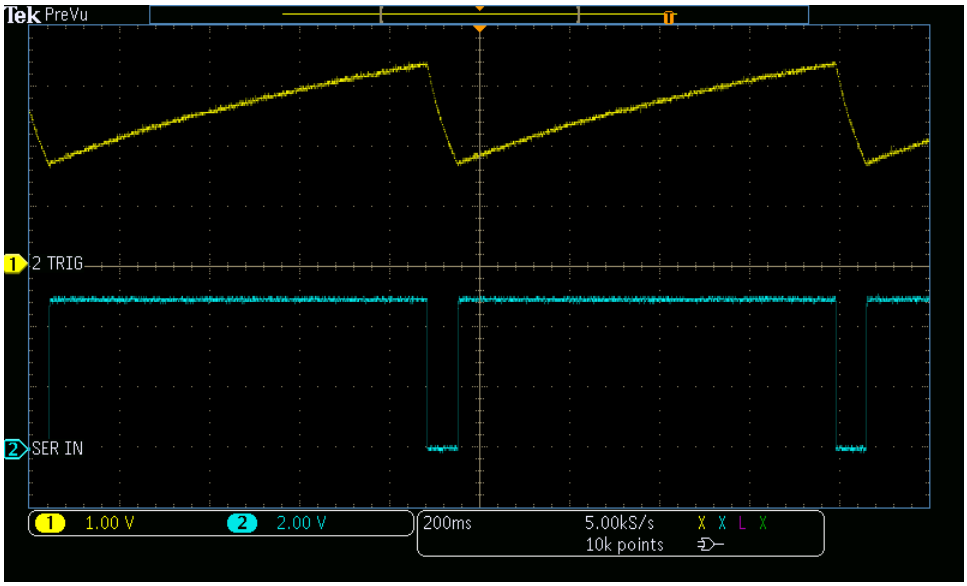
E. Timing waveforms for generating shift register clock input

In the figure below, 1 TRIG displays the voltage on pin 2 of the TLC556 (1 Trigger and 1 Threshold), while CLOCK represents the voltage on Shift Register Clock (TP7).



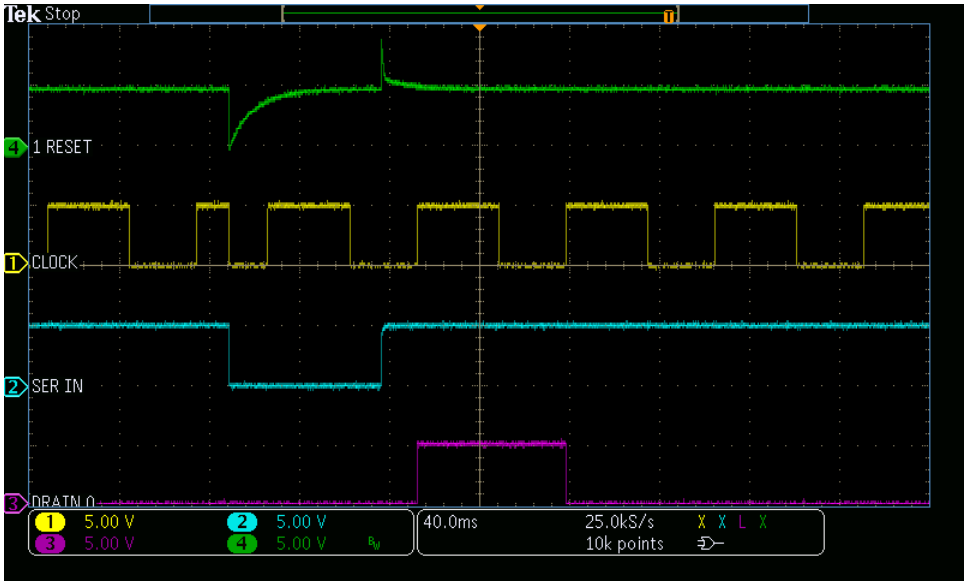
F. Timing waveforms for generating serial data input

The trace labelled TRIG 2 represents the voltage on pin 8 of the TLC556 (2 Trigger and 2 Threshold), while SER IN represents the voltage on Shift Register Serial-data Input (TP20)



G. Timing waveforms of periodic reset for clock synchronization

The following figure displays the correlation between the voltages on the Shift Register Serial-data Input (TP20), the reset pin for the timer responsible for the Shift Register Clock (1 RESET), and the Shift Register Clock (TP7) for synchronizing both 555 timers.



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