TI Designs

Thermocouple Analog Front End (AFE) Using RTD and Internal Temperature Sensor of ADS1220 for Cold Junction Compensation (CJC)

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Design Resources

TIDA-00168	Tool Folder Containing Design Files
ADS1220	Product Folder
MSP430™FR5949	Product Folder
REF5020	Product Folder
TPS71733	Product Folder
TCA9535	Product Folder

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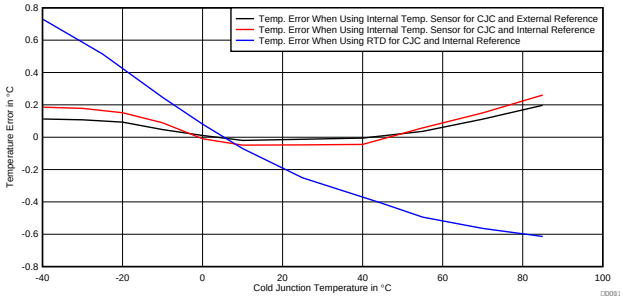
Design Features

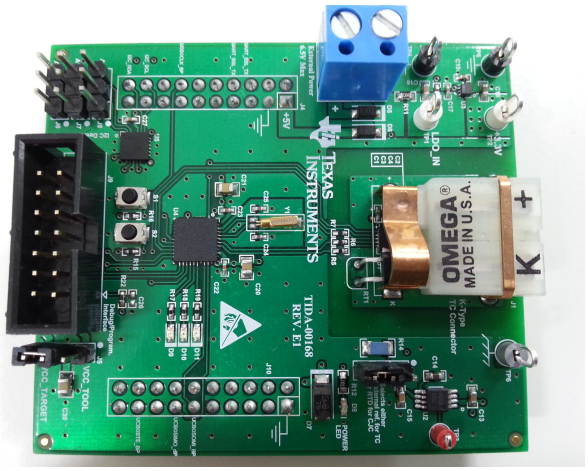
- Sensor Input: K-Type Thermocouple
- Temperature Range of –200°C to 1372°C
- Noise Free Resolution: 0.02ºC
- Cold Junction Compensation (CJC) Using Resistance Temperature Detectors (RTDs) or the Internal Temperature Sensor of ADS1220
- Designed to Meet IEC61000-4 Standards: Electrical Fast Transients (EFTs), Electrostatic Discharge (ESD), and Surge
- Operating Temperature Range of –40°C to 85°C

Featured Applications

- Factory Automation and Process Control
- Sensors and Field Transmitters
- Building Automation
- Portable Instruments

Temperature Error Versus Cold Junction Temperature





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1 Introduction

The sole objective of this reference design is to provide comprehensive details on how to design a simple, robust, and accurate analog front end (AFE) circuit for making precision temperature measurements with thermocouple sensors. This reference design explains the theory, operation, and complications involved and the step-by-step design.

This reference design also emphasizes topics like error analysis, the necessity of an anti-aliasing filter, biasing resistors for sensor diagnostics, CJC, linearization technique for sensor data, and the design challenges of printed circuit boards. Furthermore, the external protection circuitry complies with regulatory IEC61000-4 standards: EFT, ESD, and surge requirements. Electromagnetic compatibility (EMC) compliance to IEC61000-4 is necessary to ensure that the design not only survives but performs as intended in a harsh and noisy industrial environment.

This user sheet provides all of the relevant design files such as schematics, Bill of Materials (BOM), layer plots, altium files, gerber files, and software for the MSP430™ microcontroller unit (MCU).

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2 Design Summary

Table 1 lists the key design requirements and features.

Table 1. Design Requirements

PARAMETERS	SPECIFICATIONS AND FEATURES
Sensor Type	K-type thermocouple
Temperature Range	–200°C to 1375°C
Cold Junction Compensation Type	RTD Pt100 or internal temperature sensor
Analog-to-Digital Converter (ADC) Reference	Internal voltage reference when using RTD Pt100 for CJC
	External or internal voltage reference when using internal temperature sensor for CJC
Power Supply Voltage Range	Maximum up to 6.5 V
	3.3-V power supply from MSP430 debugging
Reverse Polarity Protection	Yes
Calibration	Offset and gain calibration for ADC and digital-to-analog converter (DAC)
Thermocouple Temperature Linearization	–200°C to 1375°C look-up table with 1°C resolution implemented in the MSP430 firmware to resolve non-linearity
RTD Temperature Linearization	–40°C to 85°C look-up table with 1°C resolution implemented in the MSP430 firmware to resolve non-linearity
Surge Transient Immunity	Designed to meet IEC 61000-4 standards
Operating Temperature	–40°C to 85°C (temperature of the board including the cold junction)
Interface Connectors	Two 20-Pin connectors compatible and pluggable with any MSP430 launch pad
	One 14-Pin connector for MCU debugging and programming using spy-bi-wire (SBW)
	One 2-Pin connector for external power supply

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3 System Description and Block Diagram

The front-end circuit biases a K-type thermocouple, filters out of bandwidth noise, reads the generated signal, amplifies the signal, and then converts analog input voltages into cold-junction compensated and linearized, 24-bit digital temperature readings. The module uses the National Institute of Standards and Technology (NIST) linearization tables based on the International Temperature Scale of 1990 (ITS-90) for thermocouple linearization.

The AFE circuit offers two solutions for CJC, using an on-chip temperature sensor or using an RTD Pt100 sensor. When using the on-chip temperature sensor, the user places the ADS1220 device close to the isothermal block. This placement reduces the external component count by using the on-chip sensor for a reference to the temperature measurement. The second solution, using an RTD Pt100 sensor, is useful when placing the ADS1220 device close to the isothermal block is impractical. Using the RTD Pt100 sensor increases the component counts. The AFE design also uses a low-noise, low-drift, precision voltage reference (REF5020) externally. This design allows the use of either RTD for CJC or external voltage reference when using a jumper setting. The MPS430 MCU provides the key computation of this AFE design. The ferroelectric-RAM (FRAM) contains all of the software that enables the MCU to perform all of the intended functions. The MCU interfaces with the ADS1220 device through the serial peripheral interface (SPI). Immediately after power up, the MCU performs the necessary initializations required to run, such as setting up the system clock, I/O port settings, enable and disable interrupts, and the initialization of SPI engines to begin communication with the ADC. After self-initialization, the MCU initializes the internal registers of the ADC as per the design requirements already captured and implemented in software. Figure 1 shows the components of the design in the conceptual schematic diagram.

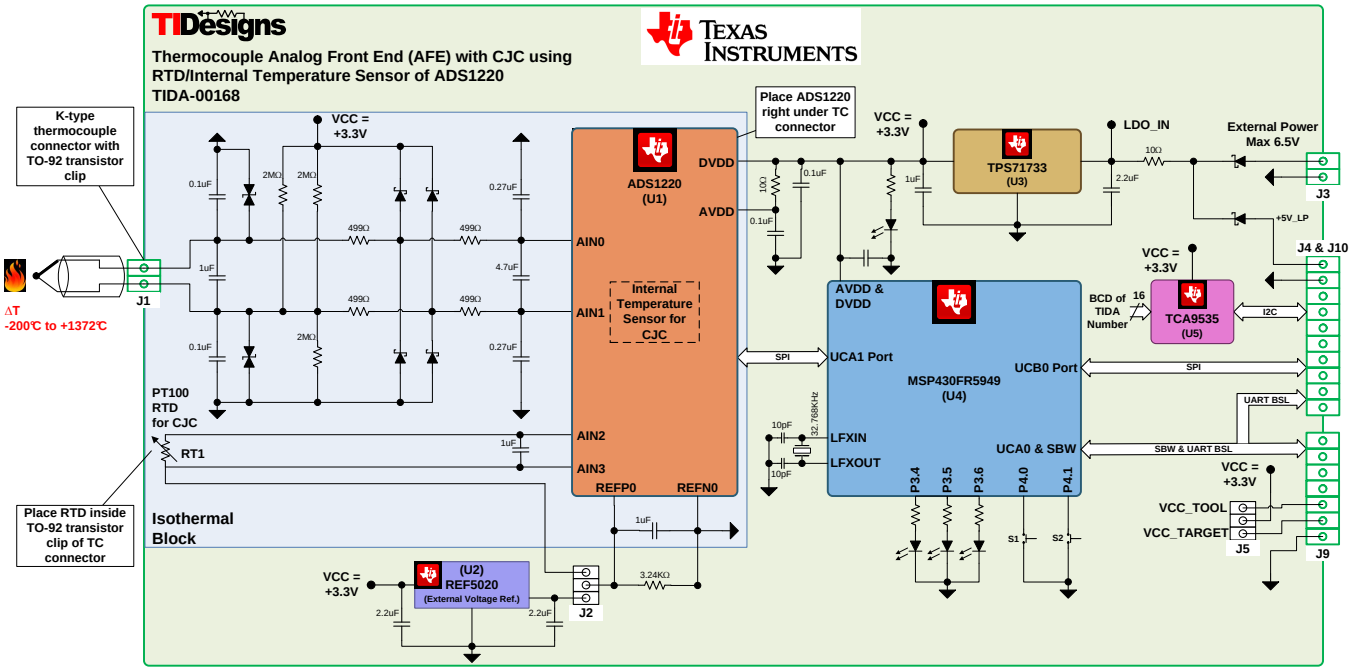

Figure 1. Conceptual Schematic Diagram

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4 System Design Theory

4.1 Thermocouple Theory

Temperature is the most essential process variable in the industry, which requires continuous measurement, monitoring, and control. Current industry standards demand an accurate, repeatable, and reliable temperature measurement to have a significant impact on product cost, product quality, process efficiency, and safety. All temperature sensors measure temperature by sensing a change in the material physical characteristics as a function of temperature. Temperature sensors are available in wide varieties:

- Thermocouple
- Resistance temperature detector (RTD)
- Thermistor
- Semiconductor temperature sensor integrated circuit

For many years, thermocouples were a straightforward choice of instrumentation and control-engineering in the process industry. In recent years, RTDs have challenged thermocouples as a means of temperature measurement. However, the use of thermocouples remains popular in applications that sense extremely high temperatures. Thermocouples have an important role in industrial thermometry. Thermocouples are of a simple construction, rugged, inexpensive, and one of the most commonly used temperature transducers covering a wide range of temperatures. A thermocouple is formed when two dissimilar metal wires bind together electrically to form two junctions as shown in Figure 2.

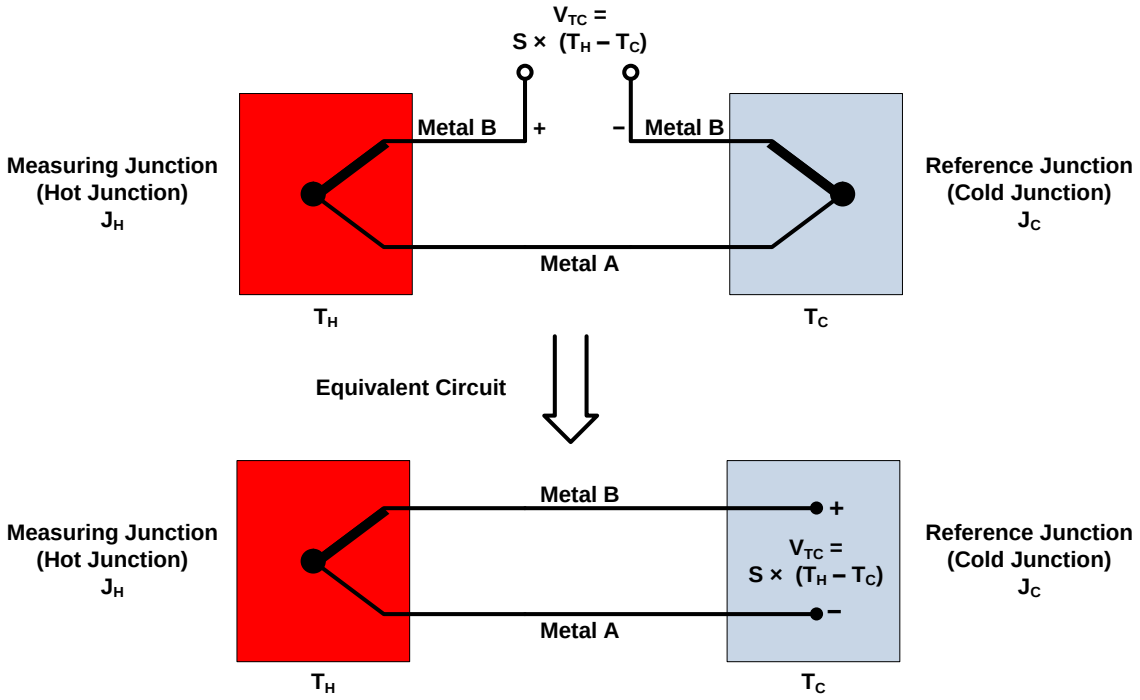

Figure 2. Simple Thermocouple

Whenever the two junctions formed by joining two dissimilar metals experience a temperature gradient, an open-circuit voltage develops. The produced voltage, first discovered by the German scientist Thomas Johann Seebeck in 1821, is called “Seebeck Voltage,” and this phenomenon is called the “Seebeck Effect.” Modern physics provides an explanation of the Seebeck phenomenon: the voltage potential arises because free-electrons at the hot end are more thermally agitated than the free-electrons at the cooler end. The more thermally agitated electrons on the hot end begin to diffuse toward the cooler end. This redistribution of electrons creates a negative charge at the cooler end and an equal positive charge at the hot end. The result is the production of an electrostatic-voltage between the two ends.

The magnitude and direction of the open-circuit voltage developed between the two ends is proportional to the temperature difference.

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$$V_{TC} = S \times (T_H - T_C)$$

Where

- V_{TC} is the Seebeck voltage in mV.
- S is the Seebeck coefficient or thermoelectric sensitivity in µV/ºC.
- T_H is the temperature of hot junction or measuring junction in ºC.
- T_C is the temperature of reference junction or cold junction in ºC. (1)

When designing with thermocouples, it is important to understand that thermocouples are bipolar, which means thermocouples can produce a positive or negative voltage depending on whether or not the measured temperature is higher or lower than the system temperature, respectively. Unlike other temperature sensors, thermocouples do not require excitation due to their inherent voltage-output.

Theoretically, all dissimilar metals exhibit the Seebeck effect, but only a few specific metal combinations are used to make most practical thermocouple sensors. These combinations were categorized and characterized into different calibration types by the NIST. Each calibration-type is designated by the capital letters indicating the composition and other different characteristics, as shown in Table 2 and Figure 3. Based on calibration type, the thermocouple has an individual sensitivity (µV/°C), a temperature range, accuracy, life-span, and nonlinearity over a temperature range.

Table 2. Different Type of Thermocouples

TYPE	TYPE E	TYPE K	TYPE J	TYPE R	TYPE S	TYPE T
JUNCTION MATERIAL	Nickel: 10% Chromium versus Constantan	Nickel: 10% Chromium versus Nickel: 5% Aluminum Silicon	Iron versus Constantan	Platinum: 13%, Rhodium versus Platinum (-)	Platinum: 10%, Rhodium versus Platinum (-)	Copper versus Constantan
SEEBECK COEFFICIENT AT 20°C	62 µV/°C	40 µV/°C	62 µV/°C	7 µV/°C	7 µV/°C	40 µV/°C
TEMPERATURE RANGE	–100°C to 1000°C	0°C to 1370°C	0°C to 760°C	0°C to 1450°C	0°C to 1750°C	–160°C to 400°C
GENERAL APPLICATION	Cryogenic use; nonmagnetic use	General purpose	Higher sensitivity	High resistance to oxidation and corrosion, calibration purposes	Standard for calibration for the melting point of gold	Often used in differential measurements

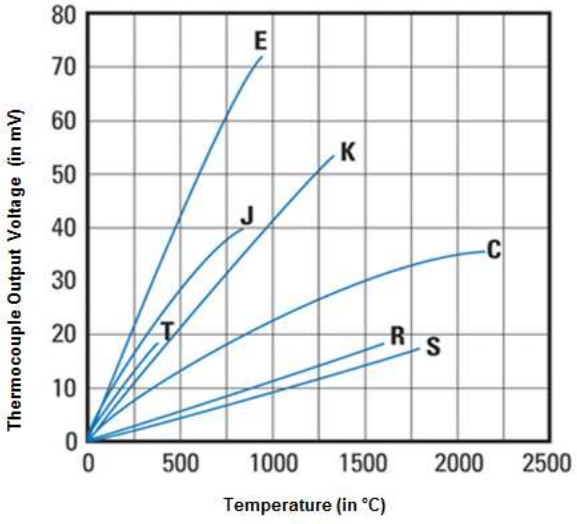

Figure 3. Thermocouple Output as Function of Temperature

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The Seebeck coefficient is a nonlinear function of temperature that causes nonlinearity in the thermocouple output voltage over the operating temperature range. Thermocouples are not uniformly linear across a temperature range, as shown in Figure 4. Always choose a thermocouple with less variation in the Seebeck coefficient.

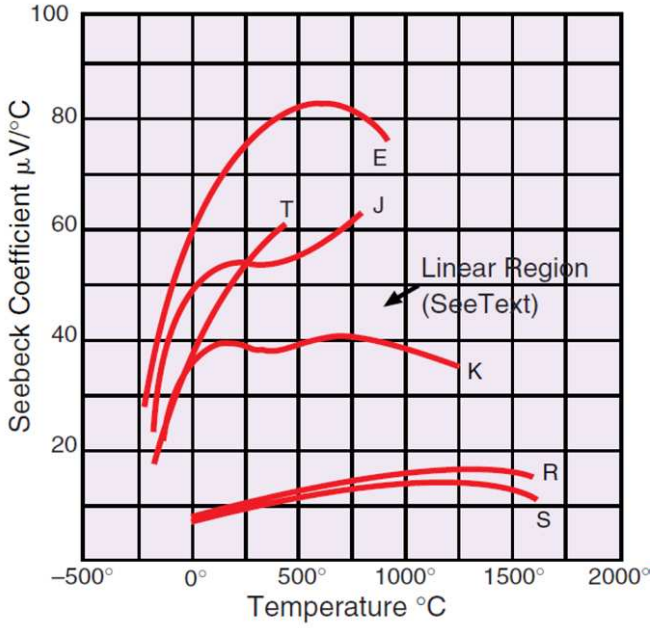

Figure 4. Seebeck Coefficient as Function of Temperature

4.2 Thermocouple Input Signal Conditioning

The use of thermocouples, despite their prevalence in the field of engineering, is often misunderstood and can result in many design challenges due to issues such as small output voltage, low sensitivity, and nonlinearity across the temperature range. Achieving an overall system accuracy of ±0.5ºC or better is difficult due to these signal conditioning issues. Users must design the interface of a thermocouple sensor AFE with extreme care to achieve a sufficient level of accuracy. A thermocouple signal chain consists of a thermocouple sensor in the front, a thermocouple connector, an isothermal block, overvoltage protection, biasing resistors, an anti-aliasing filter, an amplifier, an ADC, and sensor data linearization in the software. This AFE circuit addresses all of the challenges associated with the measuring of thermocouple temperature.

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4.2.1 Input Filter Design

4.2.1.1 Design Target

The main goal of the design is to keep the filter initial error contribution to the total error comparable to or smaller than the initial error of the thermocouple sensor. Due to the manufacturing limitations of the type-K thermocouple, which is mainly related to the purity of materials, the initial error of the thermocouple sensor (tolerance class 1) is typically less than 1.5°C and from –200°C to 375°C. The initial error is also better than 0.4% up to 1375°C, the maximum range of thermocouple temperatures.

With regard to errors such as noise and drift, the goal is to design a filter that does not degrade the performance of the ADS1220 device. For systems that work at a 20-SPS data rate at a gain of 32 V/V, the input-referred noise is 0.23 µV. The noise introduced by the filters must be less than that 0.23 µV, as Figure 5 shows.

Noise in μV_{RMS} (μV_{PP})
at AVDD = 3.3 V, AVSS = 0 V, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA ENABLED)							
	1	2	4	8	16	32	64	128
20	3.71 (13.67)	1.54 (5.37)	1.15 (4.15)	0.80 (3.36)	0.35 (1.16)	0.23 (0.73)	0.10 (0.35)	0.09 (0.41)
45	7.36 (29.54)	2.93 (13.06)	1.71 (9.28)	0.88 (4.06)	0.50 (2.26)	0.29 (1.49)	0.19 (0.82)	0.12 (0.51)
90	10.55 (47.36)	4.50 (20.75)	2.43 (11.35)	1.51 (6.65)	0.65 (3.62)	0.42 (2.14)	0.27 (1.22)	0.18 (0.85)
175	11.90 (63.72)	6.45 (34.06)	3.26 (17.76)	1.82 (11.20)	1.01 (5.13)	0.57 (3.09)	0.34 (2.14)	0.26 (1.60)
330	19.19 (106.93)	9.38 (50.78)	4.25 (26.25)	2.68 (14.13)	1.45 (7.52)	0.79 (4.66)	0.50 (2.69)	0.34 (1.99)
600	24.78 (151.61)	13.35 (72.27)	6.68 (39.43)	3.66 (19.26)	2.10 (12.77)	1.14 (6.87)	0.70 (4.76)	0.55 (3.34)
1000	37.53 (227.29)	18.87 (122.68)	9.53 (58.53)	5.37 (31.52)	2.95 (18.08)	1.65 (10.71)	1.03 (6.52)	0.70 (4.01)
2000	36.23 (265.14)	18.24 (127.32)	9.24 (65.43)	5.49 (37.02)	2.89 (18.89)	1.77 (12.00)	1.13 (7.60)	0.82 (5.81)

Figure 5. ADS1220 Input-Referred Noise in μV_{RMS} (μV_{PP})

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4.2.1.2 Importance of Input Filter

Signal conditioning is critical in any design. Any ADC, regardless of architecture, requires some amount of filtering on the inputs to reduce noise in the system, which is due to the effects of aliasing. The digital filter in delta-sigma ADCs significantly reduces the requirements of an external-analog filter, but still requires some filtering. A simple filter such as the one shown in Figure 6 creates a balanced differential filter.

The filter design using the ADS1220 device employs a simple first-order filter. The use of this first-order filter is due to the expected small-form factor and cost requirements of this reference design. Users implementing this filter can easily sequence the filter into higher-order filters to provide a greater immunity to high-frequency noise.

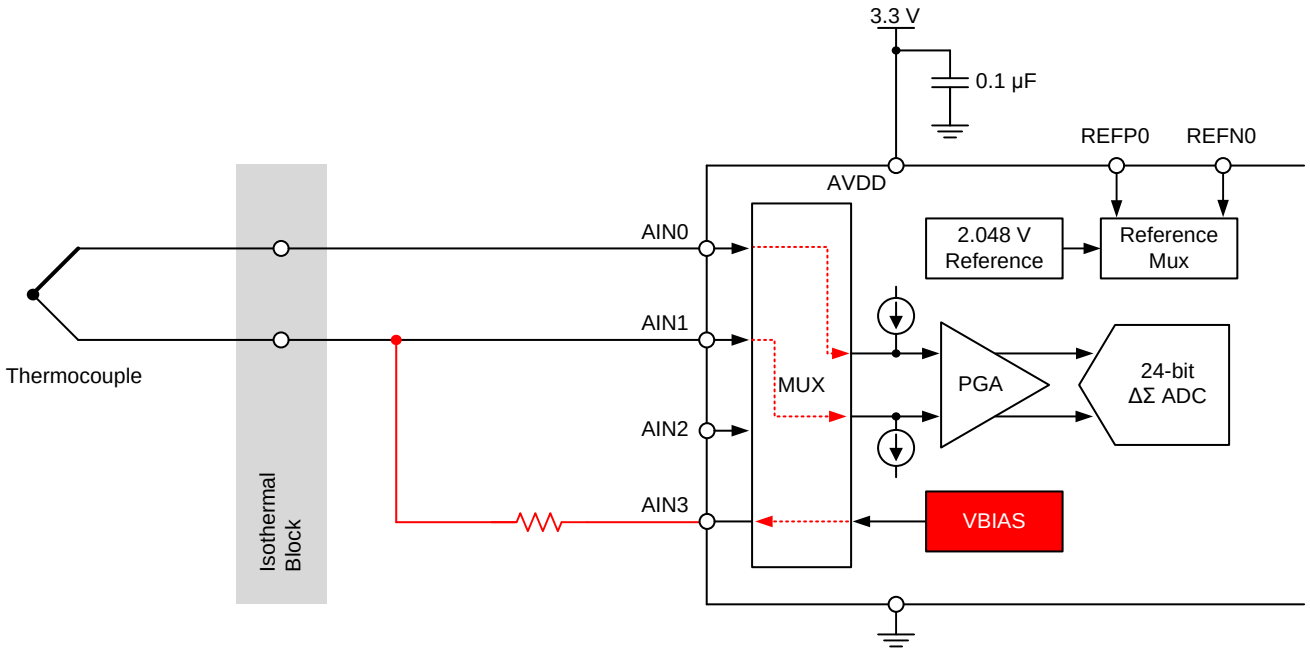

Figure 6. Signal Conditioning Using a First-Order Low-Pass Filter

NOTE: The accuracy of all selected capacitors is ±10%.

The accuracy of all selected resistors is ±1%. The drift of these resistors is ±100-ppm/°C.

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4.2.1.3 Selecting Differential-Mode and Common-Mode Capacitor Ratio

The differential filter is also great for reducing both common-mode and differential noise components. The resistors used to develop the filter also serve to limit current to the inputs of any device that follows the filter. When sized accordingly, the resistors enable better functionality to the inputs, protection against ESD, and long-term overvoltage conditions.

The filter shown in Figure 7 is an example of a structure commonly used for differential signals. There are a few important points to consider when selecting components. To avoid differential noise caused by mismatches in the common-mode capacitors, industry standards recommend using a differential capacitor that is at least ten times greater than the common-mode capacitors. TI spice-based simulators such as TINA™ simulate the mismatch in common-mode capacitors, as shown in Figure 8.

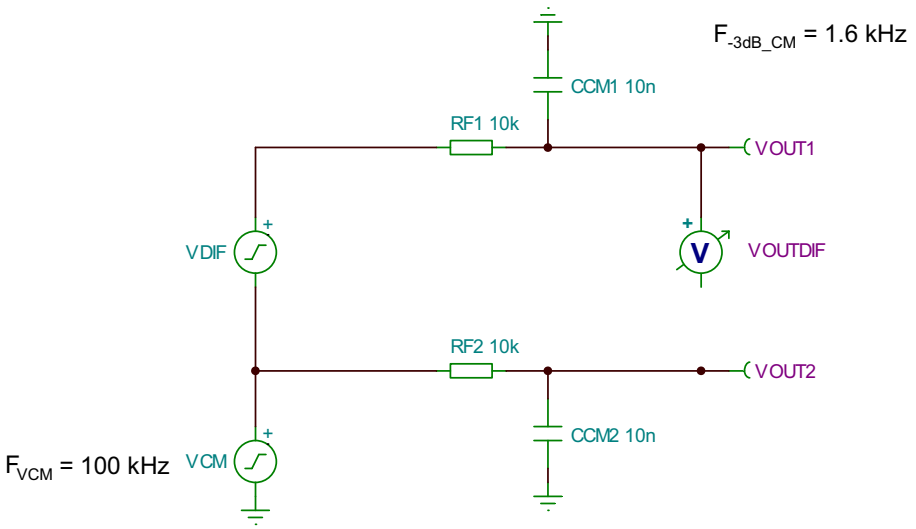

Figure 7. Common-Mode Filter Only

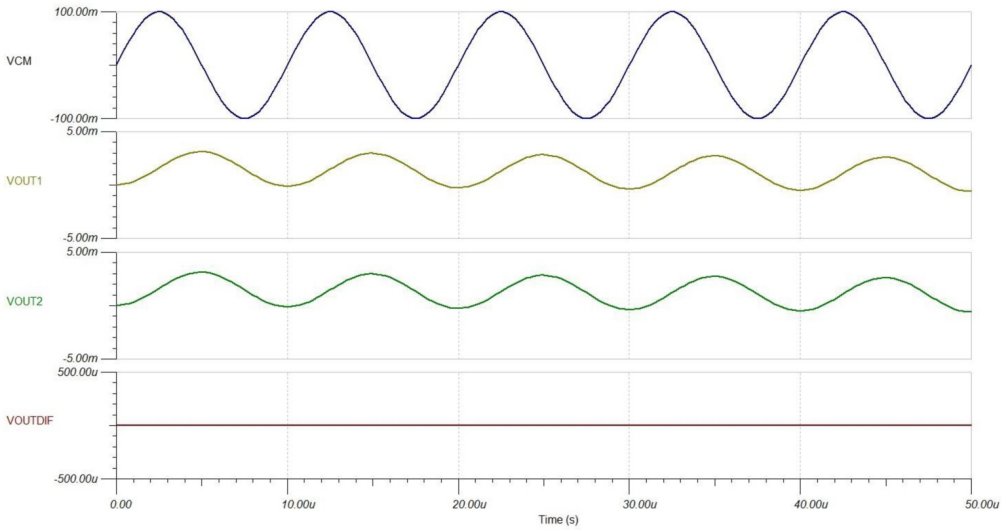

Figure 8. Ideally Matched Common-Mode Filter

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There is no differential output signal when using only the CM filter and with two matching C_{CM}.

The circuit in Figure 9 shows that when the two C_{CM} are mismatched by a difference of 1 nF, a large noise is introduced in the differential output. Figure 10 shows the addition of differential noise.

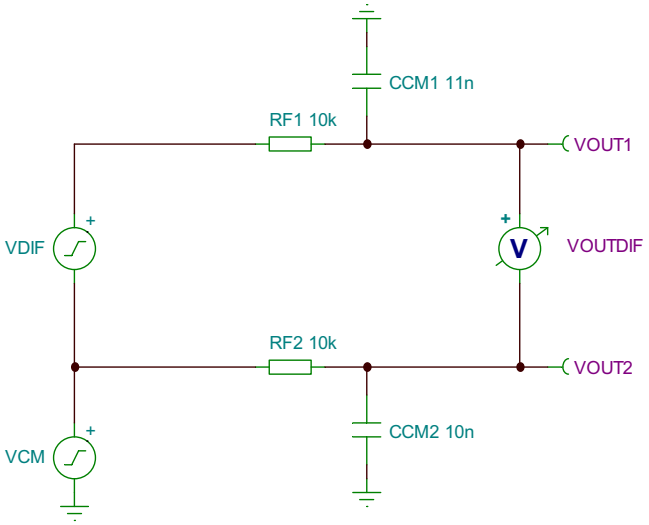

Figure 9. Mismatch in Common-Mode Capacitors

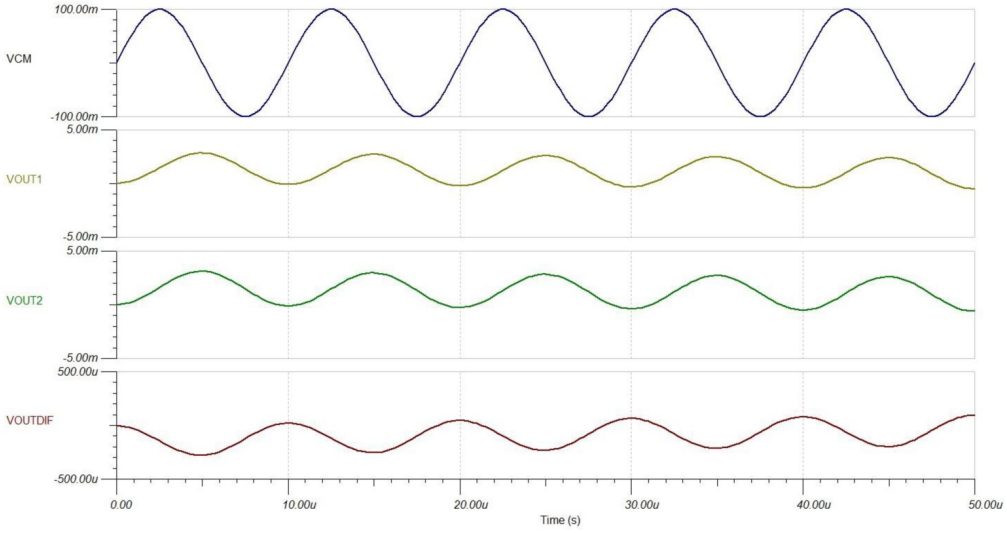

Figure 10. Differential Noise Due to Mismatches in Common-Mode Capacitors

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In Figure 11 the differential filter has been added. The value of the differential capacitor is the same as the CM capacitor. The addition of a DM capacitor reduces the noise caused by mismatched CM capacitors; however, the amount of noise generated is still considerable as Figure 12 shows.

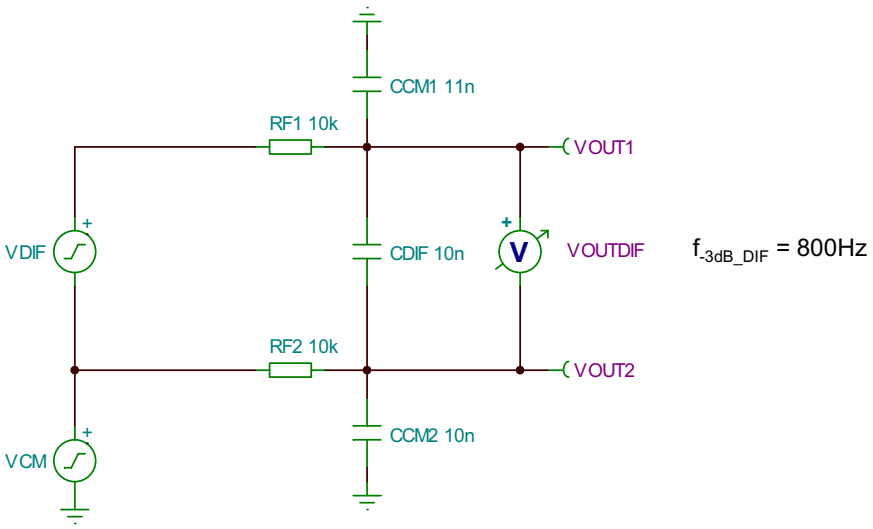

Figure 11. Adding a Differential-Mode Capacitor

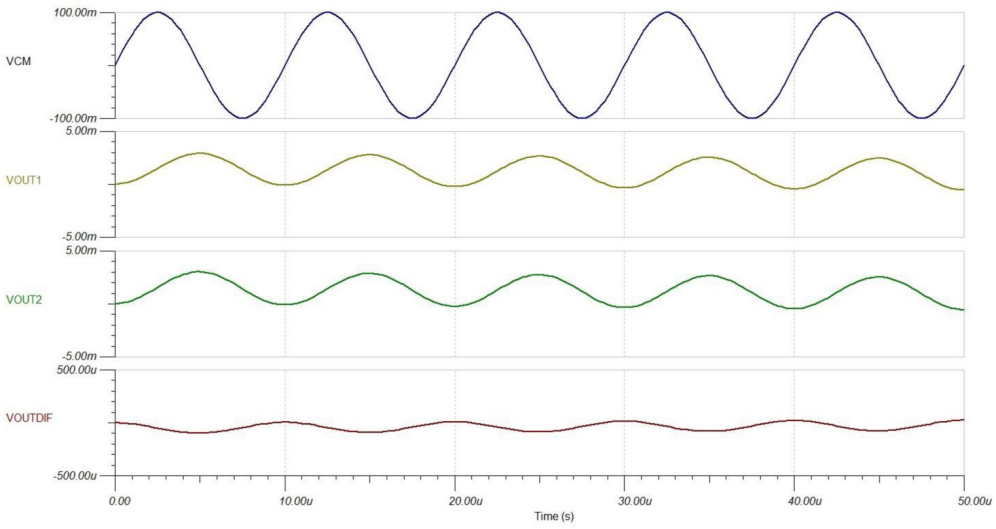

Figure 12. Differential-Mode Noise After Adding Differential-Mode Capacitor

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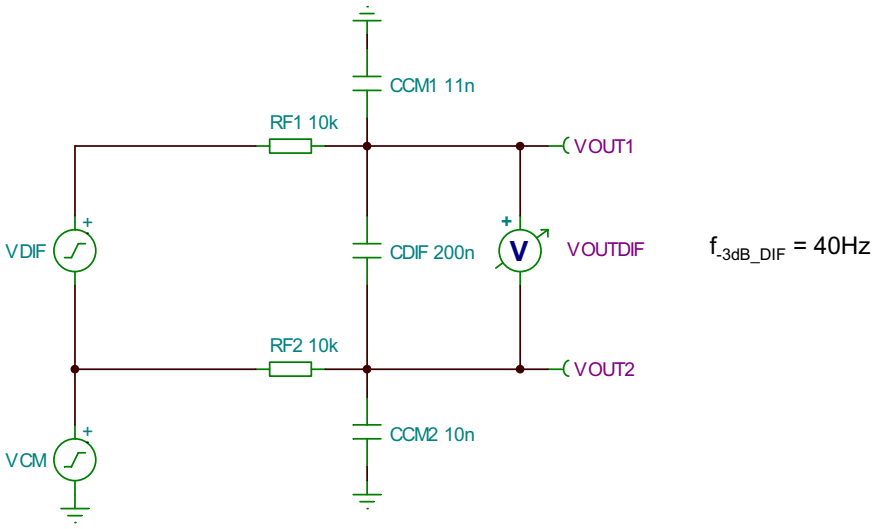

Figure 13. Increasing the Differential-Mode Capacitor

The circuit in Figure 13 shows that increasing the value of the DM capacitor 20 times larger than that of the CM capacitor greatly reduces the noise caused by mismatched CM capacitors, as shown in Figure 14. Increasing the value to this magnitude reduces the noise caused by mismatched CM capacitors. Set the differential filter capacitor to at least 10 times that of the amount of the CM capacitors to eliminate the mismatched noise in the CM capacitors.

$C_{DIFF} \geq 10 \times C_{CM}$

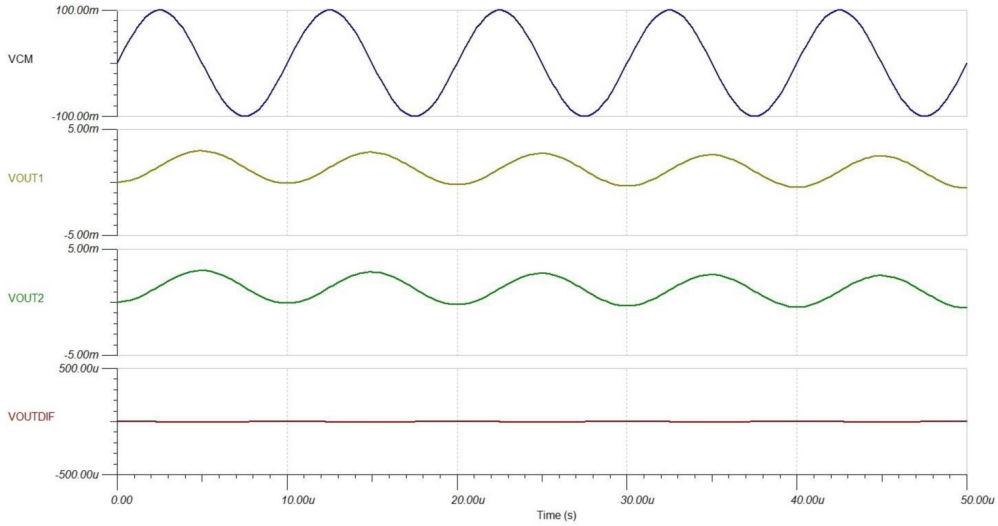

Figure 14. Differential-Mode Noise After Increasing Differential-Mode Filter Capacitor

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4.2.1.4 Input Filter Noise Contribution and Selecting Capacitor Values

The resistors in the input filters add a small amount of thermal noise. One way to reduce thermal noise in high-precision designs is to appropriately size the components. Components in this design are sized to limit the noise contribution lower than the input-referred noise (0.23 µV) of the front end. A low level of noise from these components can be useful as a means to employ dithering to the system, thereby obtaining higher resolution. Resistors generate a statistically Gaussian noise that is easy to average out, which enables a simple method to add dithering to the system. Using the Johnson-Nyquist equation for resistor noise:

$$v_n = \sqrt{4kTR\Delta f}$$

where

- $k = 1.38 \times 10^{-23}$ J/K
- T = 298 K

(2)

To find the total output noise, integrate the spectral density shown in Equation 2 over the noise bandwidth Δf. The RC circuit creates a one-pole filter for the noise.

Expressed in hertz, this noise bandwidth is:

$$\Delta f = \frac{1}{2\pi}\int_0^{\infty} \frac{d\omega}{1+(\omega C_1 R_{DIFF})^2} = \frac{\pi}{2\pi \times 2C_1 R_{DIFF}} = \frac{1}{4C_1 R_{DIFF}} \quad (3)$$

$$C_1 = (C_{DIFF} + \frac{C_{CM}}{2}) \quad (4)$$

$$R_{DIFF} = R_{F1} + R_{F2} \quad (5)$$

$$v_n = \sqrt{4kTR_{DIFF}\frac{1}{4C_1 R_{DIFF}}}$$

$$v_n = \sqrt{\frac{kT}{C_1}}$$

$$v_n^2 = \frac{kT}{C_1} \quad (6)$$

$v_n \le V_{RMS}$ of ADS1220, so

$$c_1 \ge \frac{kT}{0.0529(\mu V)^2} = 0.077\,\mu F \quad (7)$$

Equation 7 indicates that the resistor noise is not based on their own value, but rather depends on the value of the capacitor. The conditions for selecting the C_{DIFF} and C_{CM} are

$$c_1 = (C_{DIFF} + \frac{1}{2}C_{CM}) \ge 0.077\mu F, \text{ and}$$

$$C_{DIFF} = 10 \times C_{CM} \quad (8)$$

To satisfy the requirement in Equation 8, C_{DIFF} and C_{CM} are selected as 4.7 µF and 0.27 µF, respectively.

$$v_n = \sqrt{\frac{kT}{C_1}}$$

where

- C_1 = 4.7 µF + 0.135 µF = 4.835 µF

(9)

So,

$$v_n = 0.029\mu V \ll 0.23\ \mu V \quad (10)$$

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4.2.1.5 Filter Cutoff Frequency

Normally, the actual signal does not change quickly for a thermocouple (sensor bandwidth < 1 Hz). Therefore, using low cutoff filters is not unreasonable and generates a sufficient noise performance if quality capacitors are used; however, using low cutoff filters causes a reduced channel update rate. Use of the filter is important for the rejection of any noise that might be subjected to the ADC inputs, which are near the modulator sampling speed. The modulator sampling speed is usually hundreds or even thousands of times higher than the actual ADC output data rate. The data converter cannot digitally reject noises of higher frequencies. The use of analog input filtering is required to reject noises of higher frequencies, as shown in Figure 15, Figure 16, and Figure 17 . Delta-sigma ADCs specify the sampling frequency of the modulator to allow external filters to be designed accordingly. The ADS1220 device, for example, has a modulator sampling frequency of 256 kHz.

The input filter also performs as an anti-aliasing filter. In most systems, users can calibrate out errors introduced through input filters. However, for this uncalibrated example, the ADS1220 device has roughly 10 MΩ of differential input impedance, which increases the gain error as the sensor output and filter impedances increase. When selecting the filter for this design there is a trade-off between lowering the cutoff and using small-value components. Ideally, due to the low bandwidth of the sensor (< 1 Hz), users prefer a thermocouple design with a lower cutoff frequency and a higher-order filter. However, designing a high-order passive filter that is aggressive introduces large resistances in front of the ADC, which interacts with the differential input impedance of the ADS1220 device.

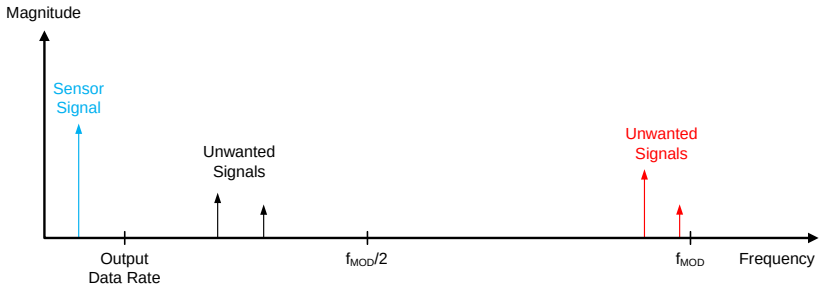

Figure 15. Unwanted Signal in the Frequency Domain

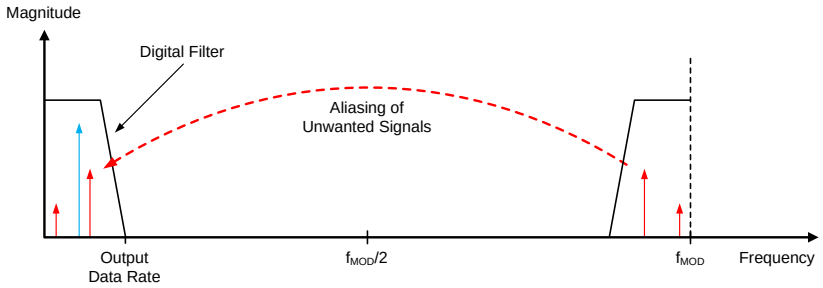

Figure 16. Aliasing After Sampling

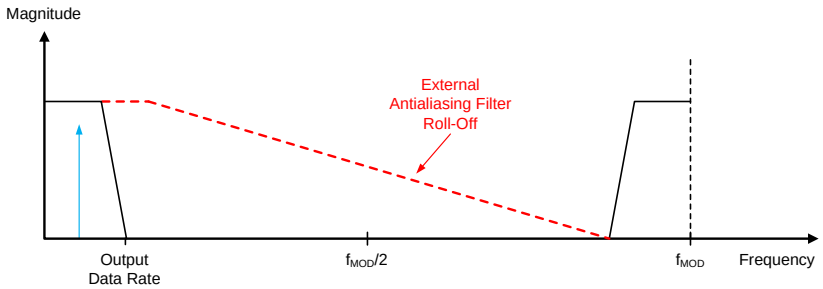

Figure 17. Anti-Aliasing Filter

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The inside digital filter cannot dispose of the aliasing signal brought on by the modulator. However, the input filter can act as an anti-aliasing filter. The goal of this design is to keep the signal rejection at 256 kHz and at least –80 dB. The –80 dB attenuation is arbitrary and depends on the expected noise in the environment where the system is deployed. The –80 dB shows that the injected undesirable signal of 5 mV attenuates to 0.5 µV.

Given that:

$$-80\,\text{dB} = 20\log[10^{-4}] \tag{11}$$

The filter must be able to reduce noise to 256 kHz by a factor of 10 000. The desired rejection is at 256 kHz of 80 dB. Calculate a cutoff frequency to achieve this rejection. Because the first-order filter in this design rejects at 20 dB per decade, the corresponding –3-dB frequency would be four decades down from 256 kHz or 25.6 Hz. The transfer function of the filter is:

$$\ddot{A} = \frac{\ddot{U}_o}{\ddot{U}_1} = \frac{1}{1 + j\omega R_{DIFF}\left(C_{DIFF} + \frac{1}{2}C_{CM}\right)} \tag{12}$$

If the attenuation at 256 kHz is –80 dB, the magnitude of the transfer function is:

$$\frac{1}{\sqrt{1 + \left(\omega R_{DIFF}\left(C_{DIFF} + \frac{1}{2C_{CM}}\right)\right)^2}} = \frac{1}{10000}$$

where

- $\omega = 2\pi \times 256$ kHZ
- $R_{DIFF} = (R_{F1} + R_{F2})$ (13)

and simplifying the equation

$$\frac{1}{2\pi \times 256\ \text{kHz} \times (R_{F1} + R_{F2}) \times \left(C_{DIFF} + \frac{C_{CM}}{2}\right)} = \frac{1}{10000}$$

$$\frac{1}{2\pi \times 25.6\ \text{kHz} \times (R_{F1} + R_{F2}) \times \left(C_{DIFF} + \frac{C_{CM}}{2}\right)} = 1 \tag{14}$$

So, the cutoff frequency is 25.6 Hz.

Consider the desired cutoff frequency when selecting actual component values. C_{DIFF} and C_{CM} are selected as 4.7 µF and 0.27 µF, respectively. With these components selected, Equation 14 can be re-arranged to solve for R_{F1} and R_{F2}. To cancel out any common-mode currents, R_{F1} and R_{F2} should be kept the same.

$$R_{F1} = R_{F2} = \frac{R_{DIFF}}{2} = \frac{1}{4\pi f_{C-DM}\left(C_{DIFF} + \frac{C_{CM}}{2}\right)} = \frac{1}{4\pi \times 25.6\,\text{Hz} \times \left(4.7\,\mu\text{F} + \frac{0.27\,\mu\text{F}}{2}\right)}$$

$$R_{F1} = R_{F2} = 643.24\ \Omega \tag{15}$$

Because R_{F1} and R_{F2} have values larger than 643 Ω, there is at least –80 dB of filter attenuation at 256 kHz.

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In addition to the filter cutoff frequency, the anti-aliasing filter must be able to protect the ADS1220 device in worst-case conditions. To select a suitable resistance for the protection, refer to the absolute maximum ratings section of the ADS1220 datasheet, which is shown in Table 3. The absolute maximum ratings section is included in all of the datasheets for TI data converters.

Table 3. ADS1220 Absolute Maximum Ratings

		VALUE		UNIT
		MIN	MAX	
AVDD to AVSS		–0.3	+7	V
DVDD to DGND		–0.3	+7	V
AVSS to DGND		–2.8	+0.3	V
Analog input current	Momentary	–100	+100	mA
	Continuous	–10	+10	mA

The ADS1220 device can withstand up to 10 mA of continuous current on any of its inputs and no more than 7 V. To limit the current to less than 10 mA, the series resistance must be:

$$\text{Series resistance } (R_{F1} \text{ and } R_{F2}) \geq \frac{\text{Overvoltage amount (V)}}{\text{Maximum rated continuous input current (A)}} = \frac{7\ \text{V}}{10\ \text{mA}}$$

$$R_{F1} = R_{F2} \geq \frac{7\ \text{V}}{10\ \text{mA}}$$

$$R_{F1} = R_{F2} \geq 700\ \Omega \tag{16}$$

This series resistance also meets the requirements of a 50–V momentary overvoltage according to the datasheet maximum ratings.

4.2.1.6 Filter Error Calculation

The anti-aliasing filter is the largest source of uncalibrated systematic error. The anti-aliasing filter presents a significant source of gain error to the system and must be calibrated out of most systems. Given that 1400 Ω of total series input resistance has been added to the signal chain (R_{F1} + R_{F2} = 2 × 700 Ω), the total series input resistance interacts with the approximate 10-MΩ differential input impedance of the ADS1220 and causes a gain error in the system. Based on these values, the user can expect the filter to cause the following error to the DC signal:

$$R_{DIFF} = R_{F1} + R_{F2}$$

$$\text{Error\%} = \frac{R_{DIFF}}{R_{DIFF} + \text{InputZ}} \tag{17}$$

The filter error should be smaller than the initial error of the K-type thermocouple.

$$\text{Error\%} \leq 0.4\%$$

$$\frac{R_{DIFF}}{R_{DIFF} + \text{InputZ}} \leq 0.4\% \tag{18}$$

$$R_{DIFF} = 2 \times R_{F1(2)} \leq 40\ \text{k}\Omega \tag{19}$$

So the range of R_{F1} and R_{F2} is:

$$700\ \Omega \leq R_{F1(2)} \leq 20\ \text{k}\Omega \tag{20}$$

This design uses a value of 1 kΩ for R_{F1} and R_{F2}. In addition to these errors, the drift of the selected resistor must be calculated. The selected components have a 100-ppm/°C drift. The initial or nominal operating temperature of the system is 25°C while the temperature range is from –40°C to 85°C; therefore, the maximum ΔT = 25 – (–40) = 65°C.

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The % drift of the resistor is,

$$100\,^{ppm}/_{\circ C} \times 65^{\circ}C = 0.65\% \tag{21}$$

The gain drift caused by the filter resistors can be given as:

$$\text{Gain drift} = (\text{Error\%(drift)} - \text{Error\%}) \times 1000000$$

$$= \left(\frac{R_{DIFF}(1 + 0.65\%)}{R_{DIFF}(1 + 0.65\%) + \text{InputZ}} - \frac{R_{DIFF}}{R_{DIFF} + \text{InputZ}}\right) \times 1000000 \tag{22}$$

For a 1-KΩ resistor, the gain drift is equal to 2.25 ppm.

To avoid degradation of the front-end performances, compare this 2.25-ppm gain drift to the gain drift of the ADS1220 device:

$$1^{ppm}/_{\circ C} \times 65^{\circ}C = 65 \text{ ppm}$$

$$\text{Gain drift} = 2.25 \text{ ppm} \ll 65 \text{ ppm} \tag{23}$$

The gain drift due to filter resistors is less than the gain drift of the ADS1220 device.

4.2.1.7 Differential Input Current Error Calculation

The thermocouple and the filters are connected to AIN0 and AIN1. Differential input currents flow through the resistors and generate a voltage error, resulting in a set limit to the upper value of the filter resistors.

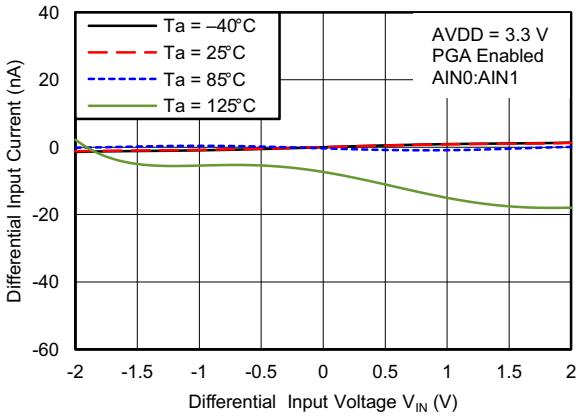

Figure 18. Differential Input Current Versus Differential Input Voltage (PGA Enabled)

Figure 18 shows that the differential current is from –40°C to 85°C, with respect to temperature. With a maximum input current of 1 nA and R_{DIFF} = 1 kΩ + 1 kΩ = 2 kΩ

$$V_{error} = I_{DIFF} \times R_{DIFF} = 2\ \mu V \tag{24}$$

Because of the uncontrollable and non-characterized nature of the current, the above error cannot be calibrated out.

The actual filter cutoff with these values becomes 16 Hz with a 256-kHz filter rejection of 83.8 dB. Filter error% is 0.02%. This error scales with input signal, so at a 0-V differential input, there is no error. However, the largest thermocouple voltage from the omega K-type thermocouple of a 54.89-mV signal attenuates to:

$$V_{Actual} \times (1 - \text{Error\%}) = V_{Measured}$$

$$54.89\,mV \times (100\% - 0.02\%) = 54.879\,mV \tag{25}$$

This 11 µV of error corresponds to roughly 0.27°C of error at 1375°C and scales linearly with temperature. As a benchmark, this correspondence indicates that at 1375°C every 0.1% of error contributes about 1.39°C of total system error.

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4.2.1.8 Input Filter Resistor Accuracy Error Calculation

The accuracy of the R_{DIFF}, C_{DIFF}, and C_{CM} influences the attenuation at 256 kHz. Substitute the values of R_{DIFF}, C_{DIFF}, and C_{CM} in Equation 26; the amplitude of the transfer function is:

$$\left|\ddot{A}\right| = \frac{1}{\sqrt{1 + (\omega R_{DIFF} + \frac{C_{CM}}{2}))^2}}$$

$$\left|\ddot{A}\right| = \frac{1}{\sqrt{1 + (2\pi \times 256\ \text{kHz} \times 2\ \text{k}\Omega \times (1 - 1\%) \times (4.7 + 0.135)\mu\text{f} \times (1 - 10\%))^2}}$$

$$\left|\ddot{A}\right| = \frac{1}{13851.72}$$

$$-20\log\left|\ddot{A}\right| = -82.8\text{dB} \tag{26}$$

The attenuation at 256 kHz can be lower, but is still below –80 dB and does not influence the result of the anti-aliasing filter being used.

Alternatively, the accuracy of R_{F1} and R_{F2} creates a mismatch in the value of the two resistors. Mismatched values for R_{F1} and R_{F2} cause any common-mode input to be transferred as a differential-mode at the ADS1220 input.

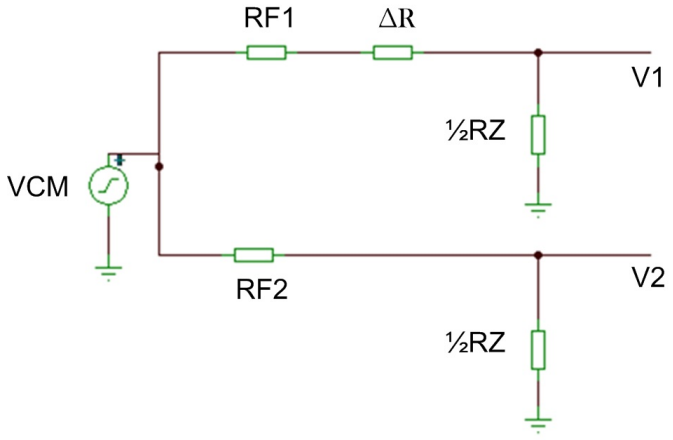

Figure 19. Simplified Circuit of RF1 and RF2 Mismatch

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Because the accuracy of R_{F1} and R_{F2} is ±1%, the largest value for ΔR is:

$$\Delta R_{MAX} = R_{F1}(1+1\%) - R_{F2}(1-1\%) = 20\ \Omega$$

$$R^{*}_{F1} = R_{F1}(1+1\%) = 1010\ \Omega, \quad R^{*}_{F2} = R_{F1}(1-1\%) = 990\ \Omega$$

$$RZ = \sim 10\ M\Omega \tag{27}$$

Using the maximum allowed common-mode voltage:

$$V_{cm} = V_{DD} - 0.2\,V = 3.1\,V$$

$$V1 = \frac{V_{cm}}{R_{F1} + \Delta R + \frac{1}{2}RZ} \times \frac{1}{2}RZ = 3.099374\,V$$

$$V2 = \frac{V_{cm}}{R_{F1} + \frac{1}{2}RZ} \times \frac{1}{2}RZ = 3.099386\,V$$

$$V_{Error} = V2 - V1 = 12.79\ \mu V \tag{28}$$

The error in Equation 28 is significant. Introducing the R_{B1} and R_{B2} biasing resistors to constrain the V_{CM} attenuates the error.

4.2.2 Selecting PGA Gain for Thermocouple Channel

In this design, the K-type thermocouple measures temperature from –200ºC to 1372ºC and with an output-voltage of –6.035 mV to 54.886 mV as per the NIST Monograph 175 revised to the ITS-90 thermocouple reference table. The PGA must amplify the small-signal output voltage of a thermocouple before reaching ΔΣ ADC for conversion. Use the largest possible input signal that can occur in the application. Choose the PGA gain that results in an ADC input signal with a value less than V_{REF} at the maximum thermocouple temperature. The largest possible gain yields the best resolution per °C.

$$V_{TC(MAX)}\ \text{at}\ +1372°C = +54.886\ mV$$

$$\text{Internal}\ V_{REF} = \text{External}\ V_{REF} = +2.048\,V$$

$$\text{PGA GAIN} = \frac{V_{REF}}{V_{TC(MAX)}\ \text{at}\ +1372°C} = \frac{+2.048\,V}{+54.886\ mV} = 37.314\,V/V \tag{29}$$

The next, smallest possible PGA gain that can be chosen in ADS1220 is 32 V/V. This gain can be achieved by setting GAIN [2:0]: Gain Configuration bits to 101b in configuration register 0.

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4.2.3 PGA Operation and Common-Mode Voltage Limitation

The ADS1220 device features a low-noise, low-drift PGA with high input impedance. The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128 V/V by adjusting radio frequency (R_F) internally. View a simplified diagram of the PGA in Figure 20. The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the PGA gain. The PGA input is equipped with an electromagnetic interference (EMI) filter. The A1 and A2 are not rail-to-rail amplifiers; therefore, outputs of PGA (OUT_P and OUT_N) must be within (AVSS + 0.2 V) and (AVDD – 0.2 V) constantly for amplifiers (A1 and A2) to stay in the linear operating range. Equation 30 defines a few terms:

$$\text{Differential input voltage} = V_{IN} = (V_{INP} - V_{INN})$$

$$\text{Differential input voltage} = V_{OUT} = (V_{OUTP} - V_{OUTN}) = \text{GAIN} \times V_{IN}$$

$$\text{Input output common-mode voltage} = V_{CM} = \frac{(V_{INP} - V_{INN})}{2} = \frac{(V_{OUTP} - V_{OUTN})}{2}$$

$$\text{PGA gain} = \text{GAIN} = \left(1 + \frac{2R_F}{R_G}\right) \tag{30}$$

NOTE: All the absolute voltages are referenced to AVSS.

So

$$V_{OUTP} = V_{CM} + \frac{\text{GAIN} \times V_{IN}}{2} \le \text{AVDD} - 0.2\,\text{V}$$

$$V_{CM} \le \text{AVDD} - 0.2\,\text{V} - \frac{\text{GAIN} \times V_{IN}}{2} \tag{31}$$

Similarly

$$V_{OUTN} = V_{CM} + \frac{\text{GAIN} \times V_{IN}}{2} \ge \text{AVSS} + 0.2\,\text{V}$$

$$V_{CM} \ge \text{AVSS} + 0.2\,\text{V} + \frac{\text{GAIN} \times V_{IN}}{2} \tag{32}$$

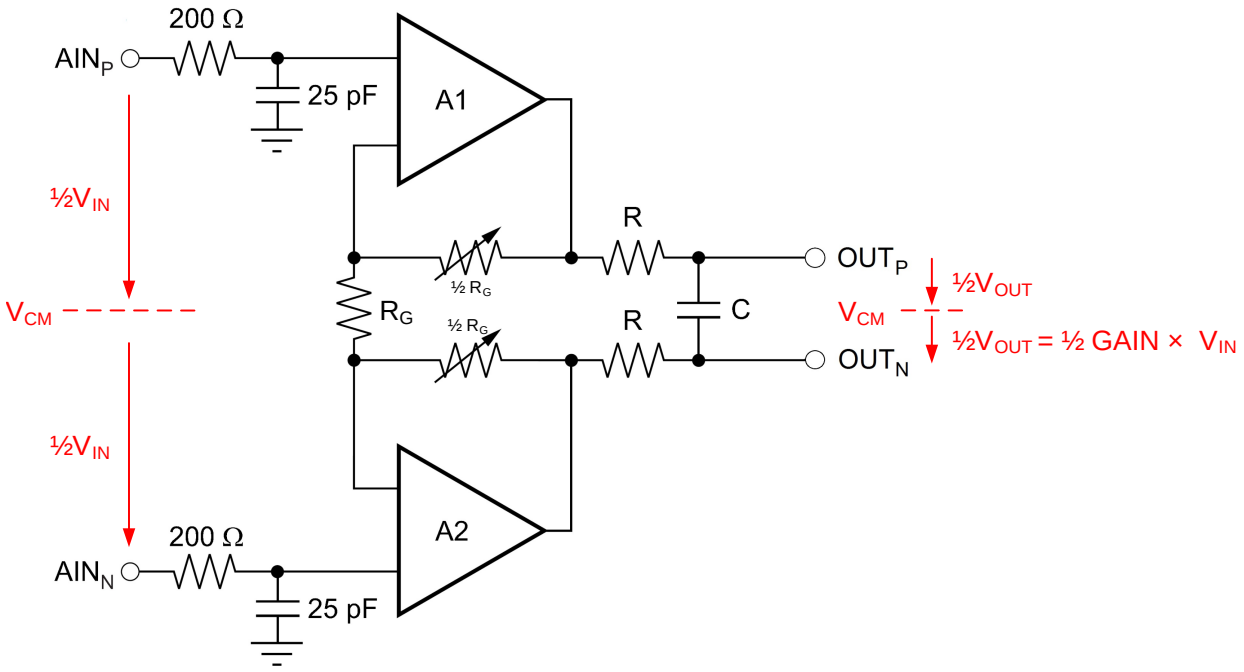

Figure 20. Simplified Diagram of PGA

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As with any PGA, the input voltage must remain within a specified voltage range of the common-mode input. The common-mode input voltage (V_{CM}) must remain within the minimum and maximum limits as shown Figure 21.

ANALOG INPUTS			
Full-scale input voltage (V_{IN} = ADCINP – ADCINN)		$\pm V_{REF}/PGA$ (1)	V
Common-mode input range		AVSS + 0.2 V + $\frac{(V_{IN})(Gain)}{2}$ AVDD – 0.2 V – $\frac{(V_{IN})(Gain)}{2}$	V

Figure 21. Common-Mode Input Voltage Range

To better understand PGA operation and subsequent common-mode voltage limitations, refer to the following examples.

Good Example #1:

If GAIN = 1, V_{INP} = 1.2 V, and V_{INN} = 0.2 V for the circuit shown in Figure 22 , then determine the values for V_{OUTP}, V_{OUTN}, V_{CM}, and $V_{CM\ (MIN)}$.

Requirement:

$$V_{CM(MIN)} = \left[0\ V + 0.2\ V + \frac{1 \times 1\ V}{2}\right] = 0.7\ V \tag{33}$$

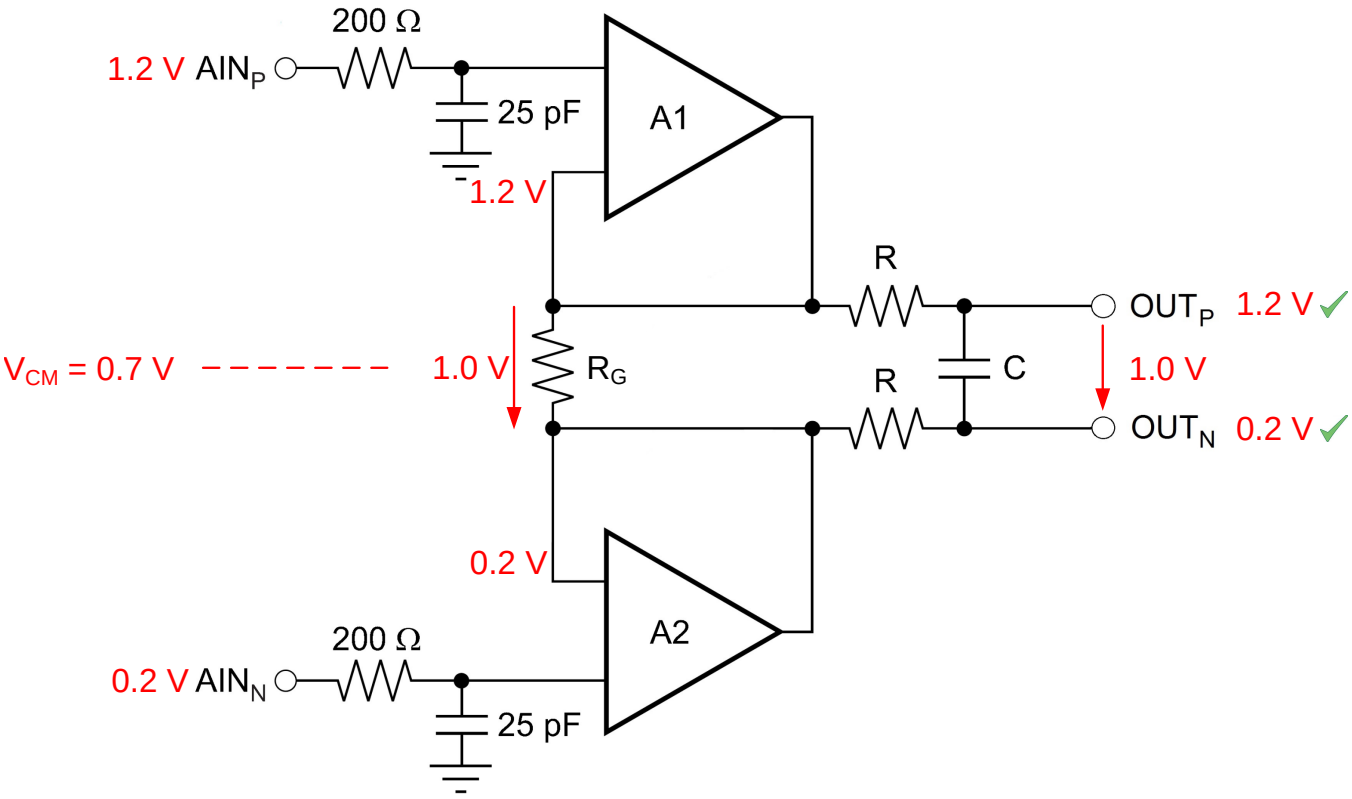

Figure 22. PGA Operation and Common-Mode Limitation — Good Example #1

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Bad Example #1:

If GAIN = 1, V_{INP} = 1.1 V, and V_{INN} = 0.1 V for the circuit shown in Figure 23, then determine the values for V_{OUTP}, V_{OUTN}, V_{CM}, and $V_{CM\ (MIN)}$.

Requirement:

$$V_{CM(MIN)} = \left[0\ V + 0.2\ V + \frac{1 \times 1\ V}{2}\right] = 0.7\ V \quad (34)$$

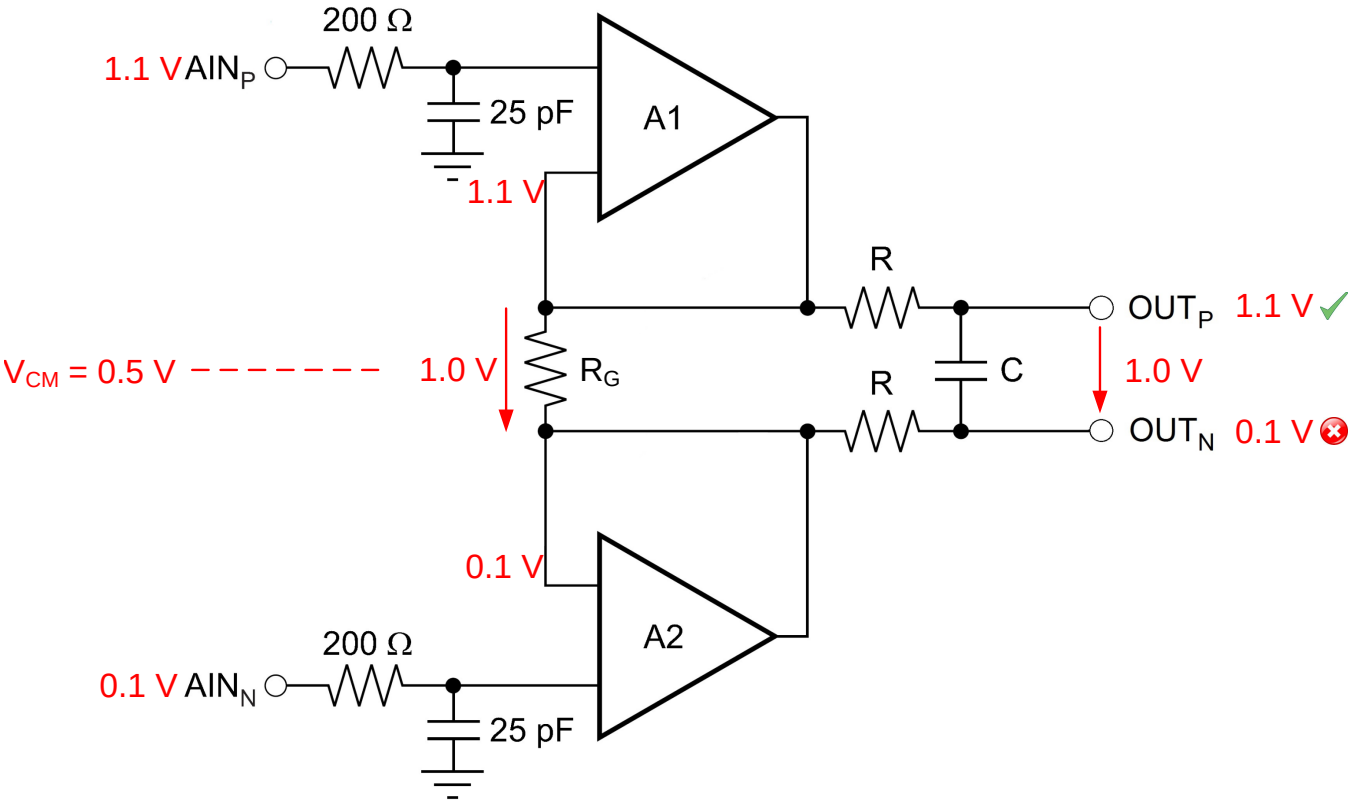

Figure 23. PGA Operation and Common-Mode Limitation — Bad Example #1 (Violation)

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Good Example #2:

If GAIN = 2, V_{INP} = 1.1 V, and V_{INN} = 1.0 V for the circuit shown in Figure 24, then determine the values for V_{OUTP}, V_{OUTN}, V_{CM}, and $V_{CM\ (MIN)}$.

Requirement:

$$V_{CM(MIN)} = \left[0\ V + 0.2\ V + \frac{2 \times 0.1\ V}{2}\right] = 0.3\ V \tag{35}$$

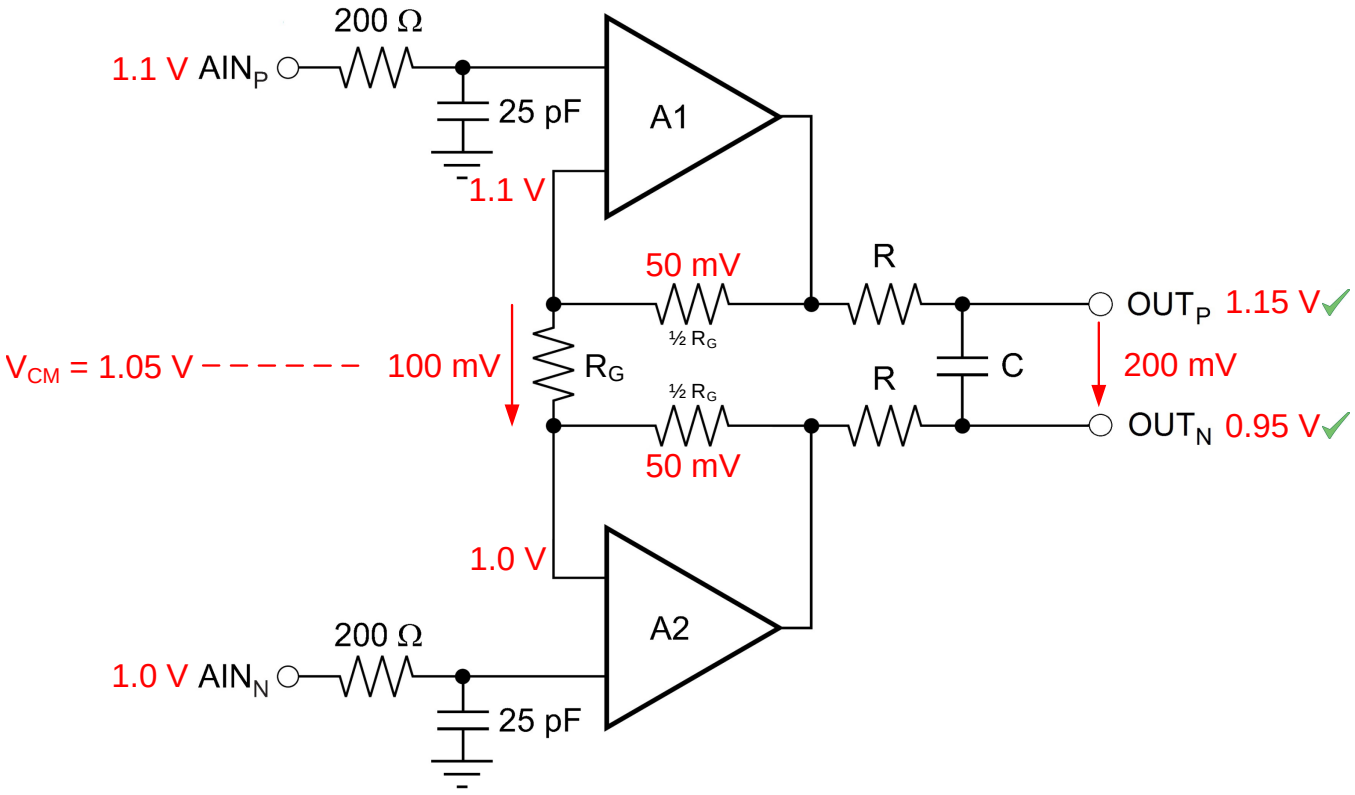

Figure 24. PGA Operation and Common-Mode Limitation — Good Example #2

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Bad Example #2:

If GAIN = 2, V_{INP} = 1.0 V, and V_{INN} = 0.0 V for the circuit shown in Figure 25, then determine the values for V_{OUTP}, V_{OUTN}, V_{CM}, and $V_{CM\ (MIN)}$.

Requirement:

$$V_{CM(MIN)} = \left[0\ V + 0.2\ V + \frac{2 \times 1.0\ V}{2}\right] = 1.2\ V \tag{36}$$

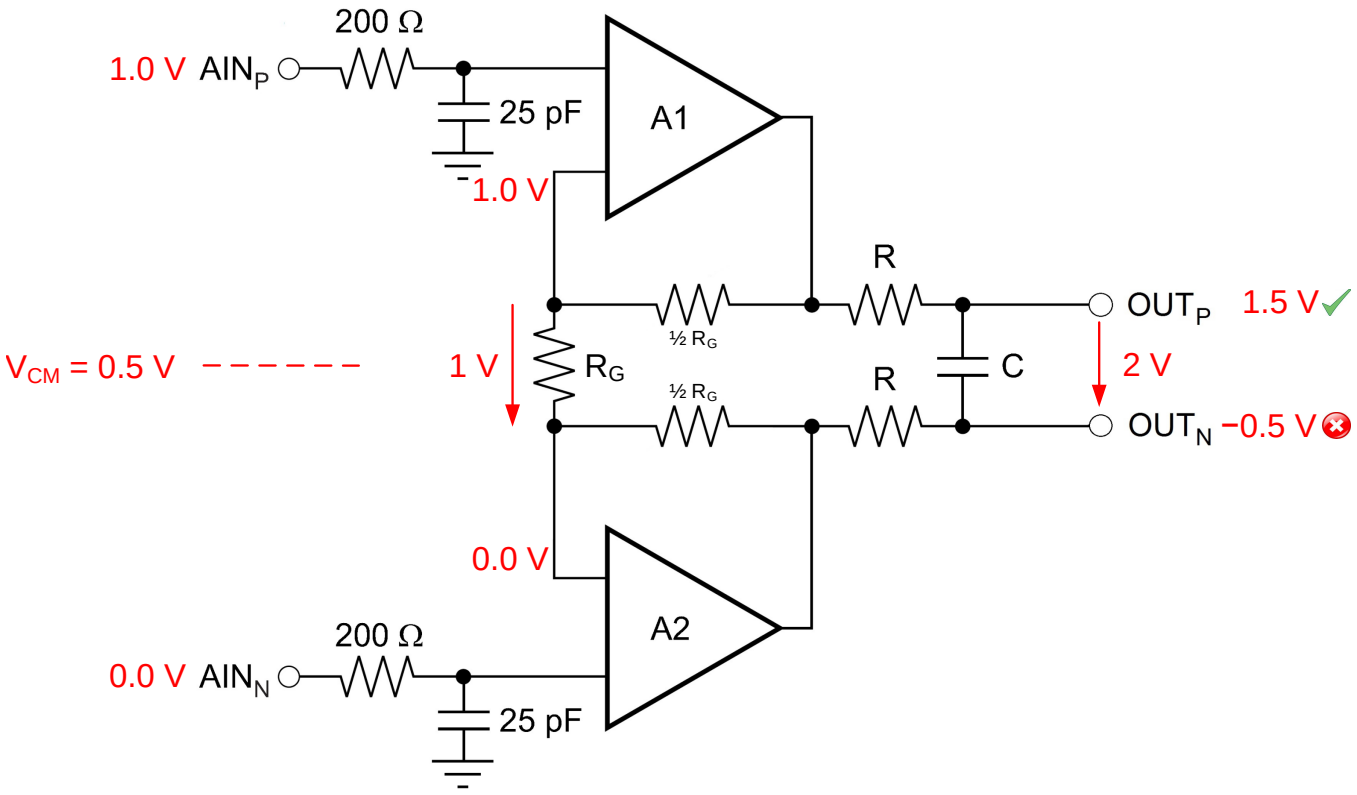

Figure 25. PGA Operation and Common-Mode Limitation — Bad Example #2 (Violation)

Therefore, the minimum and maximum common-mode voltage limits for a K-type thermocouple can be given by Equation 37:

$$\left[0\ V + 0.2\ V + \frac{+54.886\ mV \times 32}{2}\right] \le V_{CM} \le \left[3.3\ V - 0.2\ V - \frac{+54.886\ mV \times 32}{2}\right]$$

$$1.0782\ V \le V_{CM} \le 2.222\ V \tag{37}$$

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4.2.4 Biasing Resistors

In the case of a floating signal source and differential measurement, take care to ensure that the common-mode voltage level of the signal remains in the common-mode input range of the measurement device with respect to the measurement system ground. In the input stage of a data acquisition device, the input bias currents can move the voltage level of the floating source out of the valid range. Use resistors to bias this voltage to a reference, as shown in Figure 28.

These resistors are called bias resistors and provide a DC path from the device inputs to the measurement system ground. Bias resistors must have a large enough value to allow the source to float with respect to the measurement system ground and not load the signal source. Likewise, the biasing resistors R_{B1} and R_{B2} are used to set the common-mode voltage of the thermocouple within the specified common-mode voltage range of the PGA (in this example, to mid-supply AVDD/2). Mid-supply AVDD/2 is often an ideal common-mode voltage for most devices like ADCs, operational amplifiers, and PGAs. If the application requires the thermocouple to be biased to GND, a bipolar supply (for example, AVSS = –2.5 V and AVDD = +2.5 V) must be used for the ADS1220 device to meet the common-mode voltage requirement.

It is important to understand the consequence of not using biasing resistors. Without the biasing resistors, the thermocouple output-voltage is purely differential. If not biased to any reference level, the common-mode voltage can be anywhere from AVSS to AVDD (in this example, 0 V to 3.3 V), thus indicating that the condition for common-mode voltage can be violated. Consequently, the non-ideal common-mode rejection ratio (CMRR) of the device results in an input offset voltage error. According to the ADS1220 datasheet, the CMRR is at least 90 dB as shown in Figure 26. The CMRR can be defined by the following Equation 38.

$$\mathrm{CMRR}_{\mathrm{Measured}}\,(\mathrm{dB}) = 20\log_{10}\left(\frac{\Delta V_{CM}}{\Delta V_{OS}}\right) \tag{38}$$

where

- ΔV_{CM} = Change in common-mode voltage
- ΔV_{OS} = Change in input offset voltage

V_{IO}	Offset voltage (input-referred)	PGA disabled, T_A = +25°C, differential inputs		±4		µV
		PGA = 1, T_A = +25°C, differential inputs	–30	±4	30	µV
		PGA = 2…128, T_A = +25°C, differential inputs		±4		µV
	Offset drift	PGA = 1…128, T_A = –40°C to +85°C (4)		0.08	0.3	µV/°C
		PGA = 1…128, T_A = –40°C to +125°C		0.25		µV/°C
	Offset match	Match between any two inputs		±20		µV
GE	Gain error	PGA = 1…128, T_A = +25°C	-0.1%	±0.015%	0.1%	
	Gain drift	PGA = 1…128, T_A = –40°C to +125°C (4)		1	4	ppm/°C
NMRR	Normal-mode rejection ratio (5)	50 Hz ±3%, DR = 20 SPS, external CLK, bit 50/60 = 10	105			dB
		60 Hz ±3%, DR = 20 SPS, external CLK, bit 50/60 = 11	105			dB
		50 Hz or 60 Hz ±3%, DR = 20 SPS, external CLK, Bit 50/60 = '01'	90			dB
CMRR	Common-mode rejection ratio	At dc and PGA = 1	90	105		dB
		f_{CM} = 50 Hz, DR = 2000 SPS (4)	95	115		dB
		f_{CM} = 60 Hz, DR = 2000 SPS (4)	95	115		dB

Figure 26. ADS1220 Offset Voltage and CMRR Ratings

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Now

$$\Delta V_{CM} = V_{CM} - \frac{AVDD}{2} \tag{39}$$

Considering the worst case, V_{CM} = AVDD = 3.3 V

$$\Delta V_{CM} = 3.3\,V - \frac{3.3\,V}{2} = 1.65\,V$$

$$\Delta V_{OS} \le \Delta V_{CM} \times 10^{\frac{-CMRR(dB)}{20}}$$

$$\Delta V_{OS} \le 52.18\,\mu V \tag{40}$$

Without biasing resistors, there is an offset voltage error of 52.18 µV at the input, which is greater than the maximum intrinsic value of the input offset voltage of the ADS1220 device (which is 30 µV in a worst-case scenario). The R_{B1} and R_{B2} biasing resistors must be included in the design due to the introduction of this offset voltage error. Be cautious when choosing the values of the biasing resistors so that the biasing current does not degrade the measurement accuracy. The biasing current flows through the thermocouple where the current can cause self-heating and additional voltage drops in the thermocouple leads. Select a value for the biasing resistors that is as high as possible without introducing excessive thermal noise. A higher value for biasing resistors is desirable to avoid influencing the filter transfer function.

To determine the common-mode input voltage set by the design, replace the thermocouple by its Thevenin's equivalent circuit where V_{TC} is a function of the Seebeck coefficient and the temperature difference (ΔT) between the two junctions, as shown in Figure 27. R_{TC} is the thermocouple wire resistance, which is a function of wire resistivity, length, and gauge. This design has two options for connecting the biasing resistors to the thermocouple lead wires as shown in Figure 28. There are different advantages and disadvantages to both options.

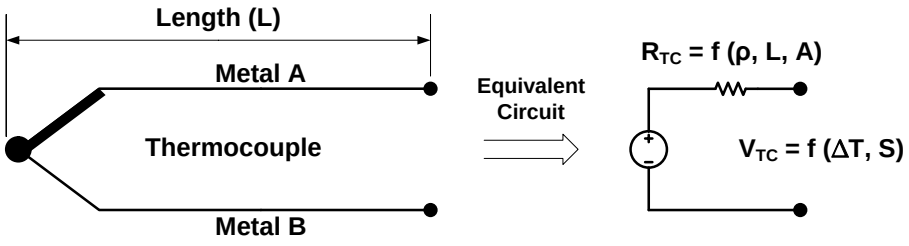

Figure 27. Thermocouple Equivalent Circuit

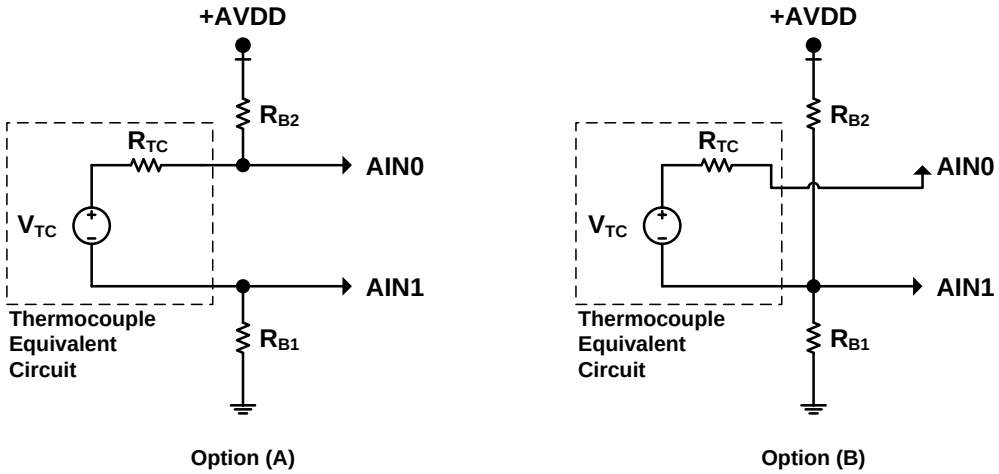

Figure 28. Thermocouple Biasing Options Using Pull-Up and Pull-Down Resistors

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4.2.4.1 Common-Mode Input Voltage for Option A

This circuit configuration has a pull-up resistor on one lead wire and a pull-down resistor on the other lead wire of the thermocouple.

$$V_{CM\_A} = \frac{AIN0 + AIN1}{2} = \frac{\left[V_{TC} + \left(R_{TC} + 2 \times R_{PD}\right) \times \left\{\frac{3.3\,V - V_{TC}}{R_{TC} + R_{PU} \times R_{PD}}\right\}\right]}{2} \quad (41)$$

If $R_{PU} = R_{PD}$, then

$$V_{CM\_A} = \frac{\left[V_{TC} + \left(R_{TC} + 2 \times R_{PD}\right) \times \left\{\frac{3.3\,V - V_{TC}}{R_{TC} + 2 \times R_{PD}}\right\}\right]}{2} = \frac{3.3\,V}{2}$$

$$V_{CM\_A} = 1.65\,V \quad (42)$$

This result is well within the allowed common-mode input voltage limits.

This circuit configuration has the following advantages.

1. Detects an open thermocouple sensor on-the-fly by implementing a check on every measured reading in the software.
2. Maintains balance in the input anti-aliasing filter.

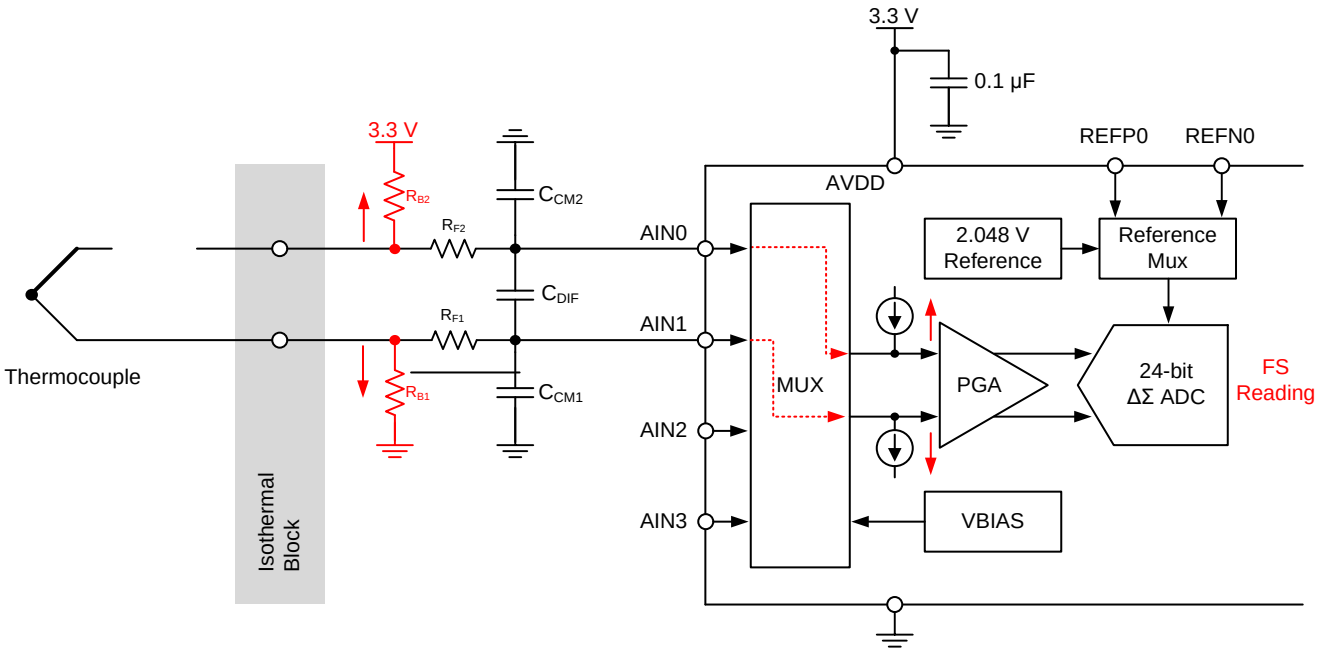

Figure 29. Thermocouple Wire Break Detection and Biasing Resistors

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As Figure 32 shows, the only disadvantage of this circuit configuration is the flow of the biasing current through the long leads of the thermocouple, which introduces an additional offset voltage error and causes self-heating.

To minimize the additional offset voltage error and self-heating, the biasing resistor must be chosen in the range of a few mega ohms (MΩ).

The noise introduced by R_{B1} and R_{B2} can be represented with a series voltage source as Figure 30 shows.

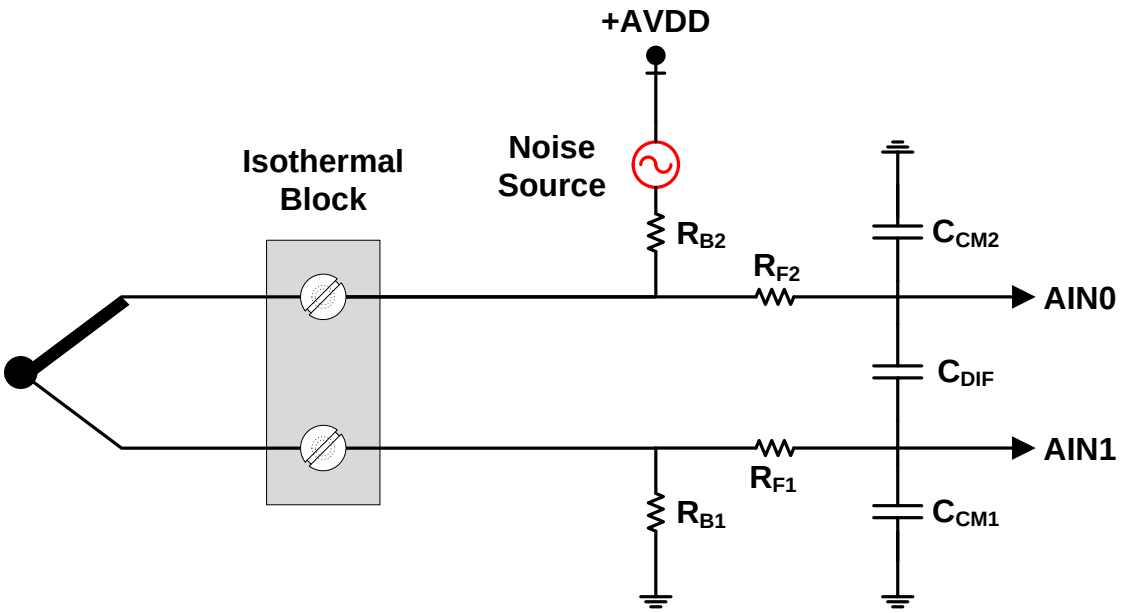

Figure 30. Biasing Resistors Noise Model

Figure 31 shows that simplifying the circuit is possible after some considerations. At the first approximation, the thermocouple can be seen as a short. AVDD is a DC power supply and can be used as a ground for AC analysis or noise analysis. R_{B1} and R_{B2} become parallel to each other for noise. The complete symmetry of the circuit indicates that node AIN0 and AIN1 are at the same voltage level. This shared voltage level indicates that C_{DIFF} has a voltage drop of 0 V; therefore, C_{CM1} is parallel to C_{CM2}.

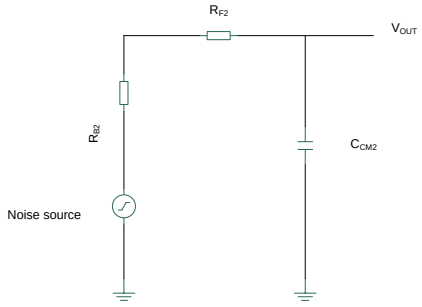

Figure 31. Simplified Circuit for Bias Resistor Noise

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Noise contribution by the biasing resistors must be kept less than the input-referred noise of the ADS1220 (0.23 µV). Using the Johnson-Nyquist equation for resistor noise:

$$v_n = \sqrt{4kTR\Delta f}$$

where

- v_n = 0.23 µV, T = 298 K

(43)

$$\Delta f = \frac{1}{2\pi}\int_0^{\infty} \frac{d\omega}{1+(\omega 2 \times C_{CM} R_1)^2} = \frac{\pi}{2\pi \times 4C_{CM}R_1} = \frac{1}{8C_{CM}R_1}$$

$$R_1 = \frac{R_{B1}}{2} + R_{F1} \times 2$$

$$v_n = \sqrt{4kTR_1 \frac{1}{8C_{CM}R_1}}$$

$$v_n = \sqrt{\frac{kT}{2C_{CM}}}$$

$$v_n^2 = \frac{kT}{2C_{CM}}$$

(44)

$v_n \le V_{rms}$, so

$$C_{CM} \ge \frac{kT}{0.0529(\mu V)^2 \times 2} = 0.0385\ \mu F$$

(45)

As Equation 45 shows, the noise caused by biasing resistors does not relate to their value, but relates to the value of C_{CM}. The 0.27-µF value attributed to C_{CM} is larger than what is needed. Therefore, based on noise considerations, there is no limit on the value for R_{B1}.

The main constraint on the biasing resistors stems from the current the biasing resistors inject into the thermocouple. A value of 2 MΩ is selected for this design. At this value, the current that flows on the thermocouple can be calculated in Equation 46:

$$I_{Error} = \frac{AVDD}{R_{B1} + R_{B2}} = \frac{3.3\,V}{4\ M\Omega} = 0.825\ \mu A$$

(46)

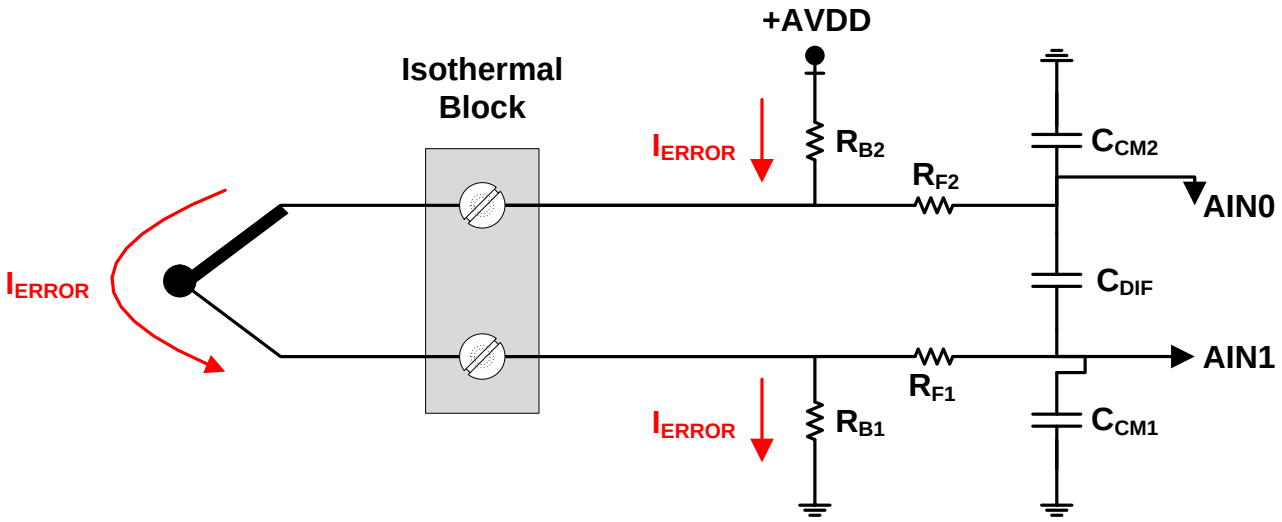

Figure 32. Error and Biasing Current Through Thermocouple Wires

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The input-referred error depends on the current and on the total wire resistance of a thermocouple as summarized in Table 4.

Table 4. Thermocouple Lead Resistance By Type and Wire Size

AMERICAN WIRE GAUGE (AWG) NUMBER	DIAMETER (INCHES)	ISA TYPE K CHROMEL-P/ ALUMEL	ISA TYPE J IRON/ CONSTANT AN	ISA TYPE T COPPER/ CONSTANT AN	ISA TYPE E CHRMOMEL/ CONSTANT AN	ISA TYPE N NICROSIL/ NISIL	ISA TYPE S PT-PT 10% RH	ISA TYPE R PT-PT 13% RH
8	.1285	.0365	.2185	.0186	.0437	.0485	.011	.011
12	.0808	.0916	.0533	.0455	.1099	.1225	.028	.029
14	.0641	.1466	.085	.0735	.1752	.1947	.045	.047
16	.0508	.2331	.136	.117	.2775	.3100	.071	.073
18	.0403	.3706	.218	.1874	.4454	.4926	.116	.119
20	.0320	.5894	.349	.2991	.7030	.7812	.185	.190
22	.0253	.9368	.544	.4751	1.1206	1.2498		
24	.0201	1.4901	.878	.7526	1.78	1.980	.464	.478
26	.0159	2.3811	1.405	1.204	2.836	3.164	.740	.760
28	.0126	3.768	2.235	1.9159	4.512	5.039		
30	.0100	5.984	3.551	3.0431	7.169	8.000	1.85	1.91

Assuming a type-K thermocouple has an AWG number of 26 with a 10-m (32-feet) length:

$R_{TC} = 32 \times 2.3811 = 76\ \Omega$

So the resulting voltage error is:

$0.825\ \mu A \times 76\ \Omega = 62.7\ \mu V$

This voltage error corresponds to approximately 1.58°C and cannot be neglected in comparison to the offset error of the ADS1220 device (4 µV typically, 30 µV maximum). This voltage error is an offset and can be calibrated out at the system level.

The bias resistor drift also introduces a non-systematic error. The offset drift of the ADC is typically 0.08 µV/°C and 0.3 µV/°C at the maximum. For example, consider thermocouple resistance R_{TC} = 100 Ω and a drift of R_{B1}

$$\frac{100\ \text{ppm}}{^\circ\text{C}} \times 65^\circ\text{C} = 0.65\%$$

$$I_{\text{Offset Drift}} = \frac{3.3\,\text{V}}{4\,\text{M}\Omega(1 - 0.65\%)} - 0.825\ \mu\text{A} \tag{47}$$

So the resulting error is

$$100\ \Omega \times 0.0054\ \mu\text{A} = 0.54\ \mu\text{V} \tag{48}$$

Because thermocouple wire resistance can go as high as a few kΩ, the offset drift deteriorates the performance of ADS1220. The topology must be improved to avoid this deterioration of performance.

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4.2.4.2 Common-Mode Input Voltage for Option B

This circuit configuration has a pull-up resistor and a pull-down resistor on the same lead wire of the thermocouple as shown in Figure 33.

$$V_{CM\_B} = \frac{AIN0 + AIN1}{2} = \frac{\left[V_{TC} + 2 \times R_{PD} \times \left\{\frac{3.3\ V}{R_{PU} + R_{PD}}\right\}\right]}{2} \quad (49)$$

If $R_{PU} = R_{PD}$, then

$$V_{CM\_B} = \frac{3.3\,V + V_{TC}}{2} \quad (50)$$

In option B the common-mode input voltage varies and depends on the output-voltage of the thermocouple.

$V_{TC\ (MIN)}$ at –200ºC = –6.035 mV

and, $V_{TC\ (MAX)}$ at 1372ºC = 54.886 mV

then

$$\frac{\left(3.3\ V + V_{TC(MIN)}\right)}{2} \le V_{CM\_B} \le \frac{\left(3.3\,V + V_{TC(MAX)}\right)}{2}$$
$$1.647\ V \le V_{CM\_B} \le 1.6774\ V \quad (51)$$

The result of Equation 51 is within the allowed limits of the common-mode input voltage.

Now

$$\Delta V_{CM\_B} = V_{CM\_B} - \frac{AVDD}{2} = 27.443\ mV$$
$$\Delta V_{OS\_B} = \Delta V_{CM\_B} \times 10^{\frac{-CMRR(dB)}{20}} = 0.86\ \mu V \quad (52)$$

Compared to the offset voltage of the ADS1220 device, 4 µV and 30 µV maximum, this offset voltage is acceptable.

The advantage of this configuration is the absence of a bias current flowing through the thermocouple.

This circuit configuration has the following disadvantages.

1. Cannot detect an open thermocouple sensor on-the-fly. The configuration requires the use of a separate diagnostic cycle to turn on the burn-out current sources. The burn-out current sources cause additional offset voltage error if left unengaged.
2. A small change in the common-mode of the input signal which is no longer biased at AVDD/2.

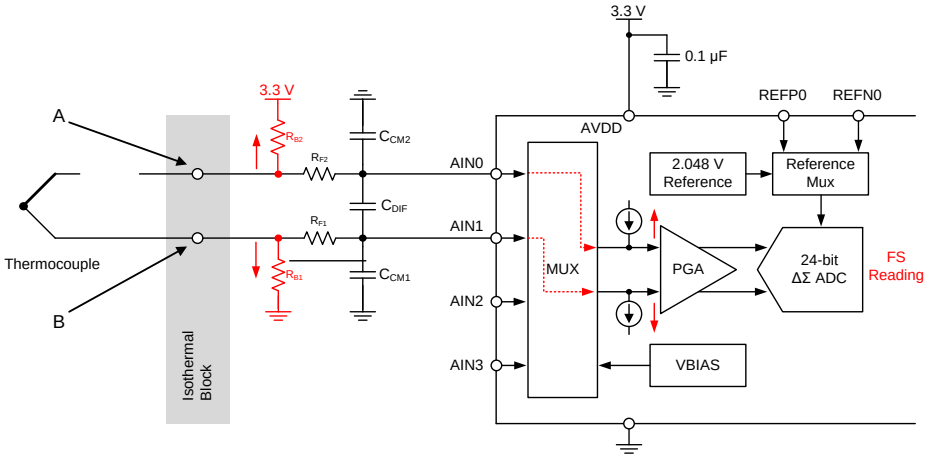

Figure 33. Improved Biasing Circuit

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4.2.5 Input Filter Design

Summarizing all of the above contributions:

1. Noise due to R_F : 0.029 µV
2. Noise due to R_B : 0.0872 µV
3. Inaccuracy of capacitor : 0.001 µV
4. Filter error : 11 µV
5. R_F mismatch : 0.18 µV
6. Inaccuracy of R_F : 0.11 µV
7. Drift of R_F : 0.123 µV
8. Offset error : 0.86 µV
9. Inaccuracy of R_B : 0.529 µV

$$\text{Total filter error} = \sqrt{0.029^2 + 0.0872^2 + 0.001^2 + 11^2 + 0.18^2 + 0.11^2 + 0.123^2 + 0.86^2 + 0.529^2} = 11.05\,\mu\text{V} \quad (53)$$

The total filter error corresponds to a temperature error of approximately 0.279ºC

Most of this filter error is deterministic and can be calibrated out. After calibrating out, only the drift and noise remain.

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4.3 Cold Junction Compensation (CJC)

Using Internal Temperature Sensor for CJC

The ADS1220 device integrates a high-precision temperature sensor that is useful when measuring the temperature of the cold junction as shown in Figure 34. To measure the internal temperature of the ADS1220 device, set the device mode to internal temperature sensor by adjusting the bit test set (TS) to '1' in the configuration register. A precise board layout is critical to achieve sufficient thermal conductivity between the cold junction and the ADS1220 package as shown in Figure 36; a careful consideration of board layout also ensures optimal performance of the device.

The ADS1220 device does not perform automatic cold-junction compensation of the thermocouple. This compensation must be done in the microcontroller that interfaces with the ADS1220 device. The microcontroller requests one or more readings of the thermocouple voltage from the ADS1220 and then sets the device to internal temperature sensor mode (TS = 1) to acquire the temperature of the cold junction. Use the microcontroller to implement calculations that can compensate for the cold junction temperature.

Using the integrated temperature sensor is not possible in every application (for example, if the accuracy is not sufficient or if the ADS1220 device cannot be placed close enough to the cold junction). When using the integrated temperature sensor is impossible, use the additional analog input channels of the ADS1220 device with a thermistor or RTD to measure the cold junction temperature.

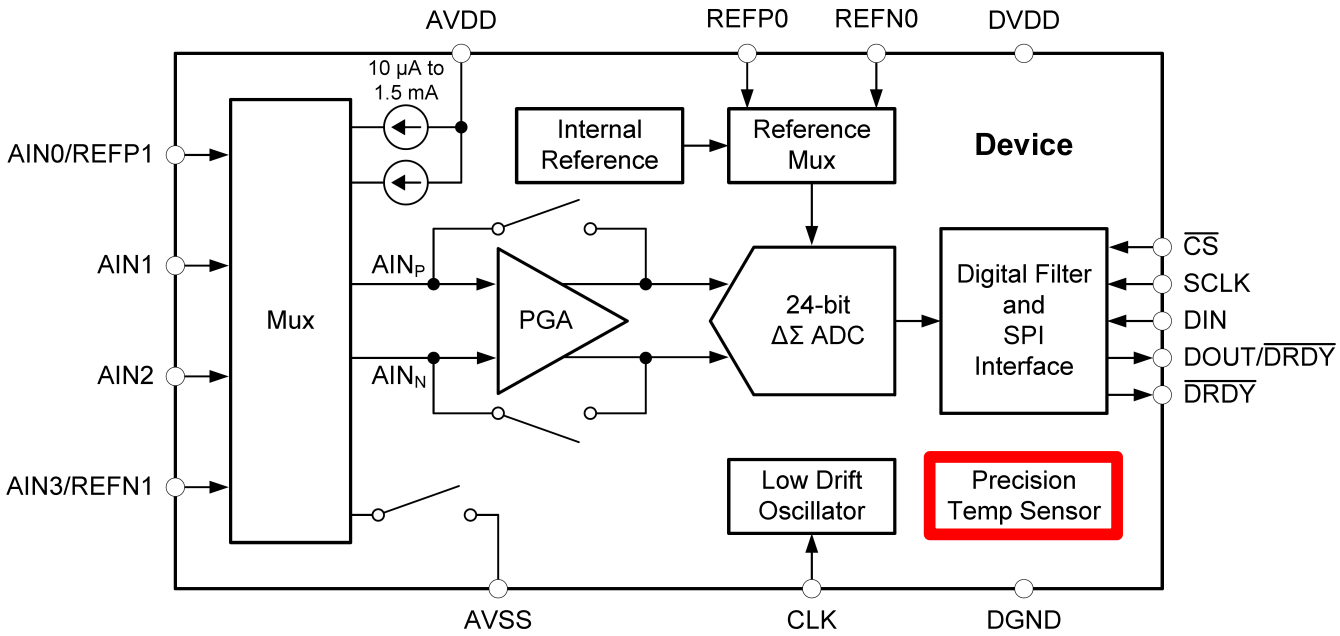

Figure 34. ADS1220 Internal Temperature Sensor

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TEMPERATURE SENSOR					
Temperature sensor resolution	Conversion resolution		14		Bits
	Temperature resolution		0.03125		°C
Temperature sensor accuracy	T_A = 0°C to +75°C	–0.5	±0.25	0.5	°C
	T_A = –40°C to +125°C	–1	±0.5	1	°C
	vs analog supply voltage		0.0625	0.25	°C/V

Figure 35. ADS1220 Internal Temperature Sensor Specifications

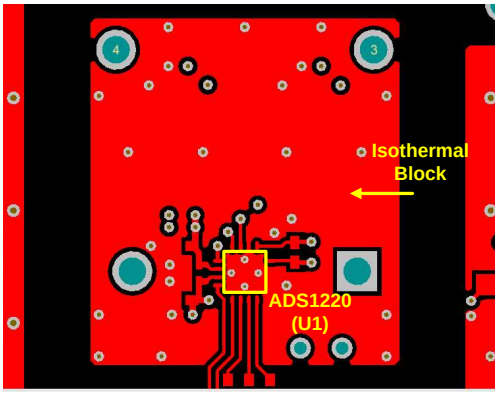

Figure 36. Placement of ADS1220 In the Isothermal Block for CJC

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4.3.1 Using RTD for CJC

An RTD can be used for CJC. To measure the temperature of the cold junction, place the Pt100 RTD (in a TO-92 package) inside the transistor retainer clip of the thermocouple connector, as shown in Figure 37. The voltage measured across the RTD is proportional to the temperature (which is determined by characteristics of the RTD). The reference voltage for the ADC is also derived from the IDAC and external precision reference resistor. This external precision resistor determines the reference voltage to the ADC in addition to the input common-mode of the PGA. This ratiometric approach ensures a more effective number of bits (ENOB) because the noise in the IDAC reflects in the reference as well as in the input, and thus tends to cancel-off. This design uses a three-wire RTD configuration despite the close proximity between the ADS1220 device and RTD Pt100 sensor. Therefore, IDAC1 = IDAC2 = 250 µA.

Choosing R_{REF} = 3.24 kΩ, a ±0.1% tolerance or better, and a 25-ppm/°C drift or less results in a common-mode voltage close to the mid-supply (AVDD + AVSS) / 2.

V_{REF} = 2 × IDAC × R_{REF} = 2 × 250 µA × 3.24 KΩ = 1.62 V

The operating temperature range for the circuit is –40°C to 85°C, which corresponds to a resistance of 84.27 Ω to 130.9 Ω when referring to the PT100 RTD table. The resulting minimum and maximum voltage inputs are:

$V_{RTD\ (MIN)}$ at –40 °C = 84.27 Ω × 250 µA = 21.0675 mV

$V_{RTD\ (MAX)}$ at 85 °C = 130.9 Ω × 250 µA = 32.725 mV

$$\text{PGA GAIN} = \frac{V_{REF}}{V_{RTD(MAX)} \text{ at } +85^{\circ}\text{C}} = \frac{+1.62\ \text{V}}{+32.725\ \text{mV}} = 49.5\ \text{V/V} \tag{54}$$

A 32-V/V PGA gain is the minimum that can be selected for the ADS1220 device. Achieve this PGA gain by setting GAIN [2:0]: Gain Configuration bits to 101 bits in configuration register 0.

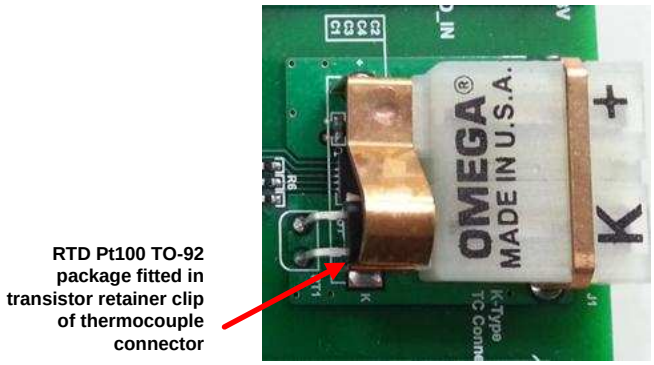

Figure 37. Placement of RTD Pt100 Sensor Inside Transistor Retainer Clip

4.4 System Error Analysis

Refer to TIDA-00189 to learn more about the thermocouple channel and calculations for RTD channel errors.

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5 Getting Started With Hardware

5.1 Hardware

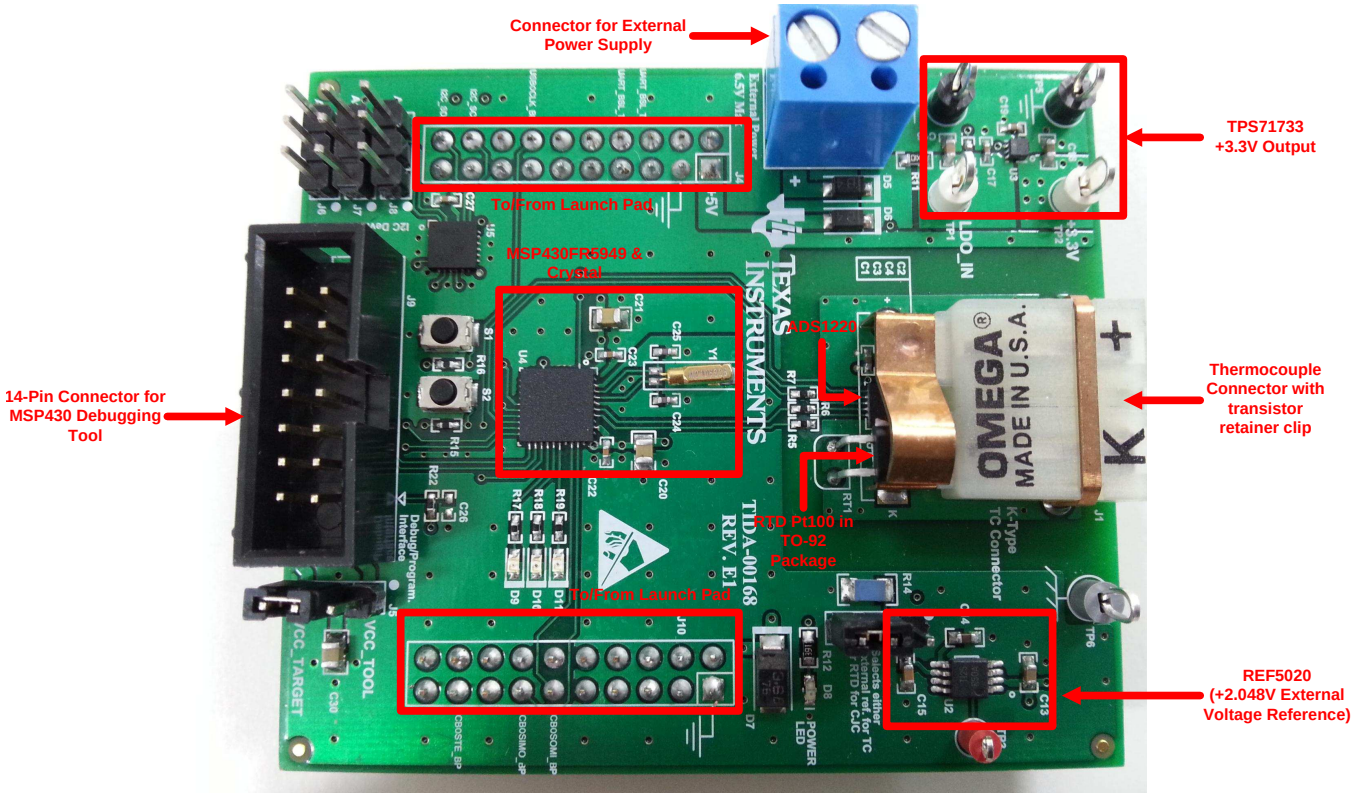

Figure 38. Board Top View

Table 5. Connector, Test Points, and Switches

CONNECTORS, TEST POINTS (TPs), AND SWITCHES	DESCRIPTION
J1	Thermocouple connector
J2	Selects either RTD for CJC or external voltage reference for ADC
J3	External power supply input (must not exceed 6.5 V)
J4, J10	To interface to TI launch pads
J5	Selects either VCC_TOOL or VCC_TARGET
J6, J7, J8	To set the I2C device address for the IO expander
J9	MSP430 debugging tool (SBW) and UART
TP1	LDO input
TP2	3.3-V LDO output
TP3	Temperature output of REF5020
TP4, TP5	GND
TP6	Chassis
S1, S2	General purpose

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For the initial board setup the following equipment is required:

1. TIDA-00168 board with the MSP430 device pre-programmed
2. 6-V battery or power supply
3. KEITHLEY™ model 2450 SourceMeter® to provide the temperature equivalent voltage
4. HP 3458A 8½ digit multimeter
5. Oscilloscope (optional)

Connections:

1. Configure the jumpers on the board as follows:
   - - J2: 1-2 to use external voltage reference REF5020 for ADC
   - - J2: 2-3 to use RTD in ratiometric configuration for CJC
   - - J5: 1-2 to power up the board from the MSP430 debugging tool
   - - J5: 2-3 to power up the board using an external power supply
2. Connect a 6-V battery or power supply to J3 — make sure the input power supply does not exceed 6.5 V
3. Connect the voltage output of the KEITHLEY 2450 SourceMeter (–7 mV to 56 mV) to the thermocouple input J1 (a thermocouple type-K can connect to J3, as well)
4. Verify the following voltages between
   - - TP2 and (TP4 or TP5) : approximately 3.3 V
   - - J2 pin-1 and (TP4 or TP5) : approximately 2.048 V

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6 Software Update

For MSP430 firmware updates, Code Composer Studio™ (CCStudio) is recommended. Code Composer Studio is an integrated development environment (IDE) for Texas Instruments (TI) embedded processor families. CCStudio comprises a suite of tools used to develop and debug embedded applications. CCStudio includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system, and many other features. The intuitive IDE provides a single-user interface that guides through each step of the application development flow.

For programming and debugging, the MSP430 implements an embedded emulation module (EEM). The EEM is accessed and controlled through either a 4-wire joint test action group (JTAG) mode or a spy-bi-wire mode. This reference design supports the spy-bi-wire mode only. For more details on how the features of the EEM can be used in conjunction with (CCS), see the advanced debugging using the enhanced emulation module (SLAA393). The 2-wire interface is made up of the spy-bi-wire test clock (SBWTCK) and the spy-bi-wire test data input/output (SBWTDIO) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the RST/NMI pin of the device. For programming and debugging purposes the SBWTCK, SBWTDIO, VCC, and GND from the debugger must be connected on J5.

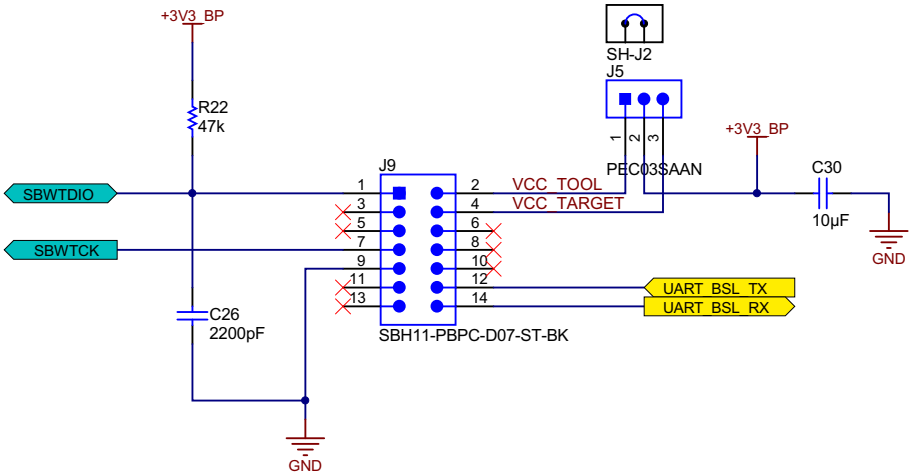

Figure 39. Spy-Bi-Wire Interface for Debugging and Programming of MCU

To program and debug code in the reference design, a MSP430 debugger interface (such as the MSP-FET430UIF) can be used with the proper connections.

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Power during debugging

CAUTION

Take special care during debugging operations to avoid damages due to conflicts between different power domains (TPS71733 power and debugger tools power). Read the following section carefully.

If using the locally-generated 3.3-V supply from the TPS71733 during debugging operations, make sure the VCC_Target pin from the debugger interface is connected to the VCC. In the condition that power from the debugger interface is used and there is no local power, make sure that the VCC_Tool pin from the debugger interface is connected to the VCC and disconnect the VCC_Target pin. Refer to Figure 40.

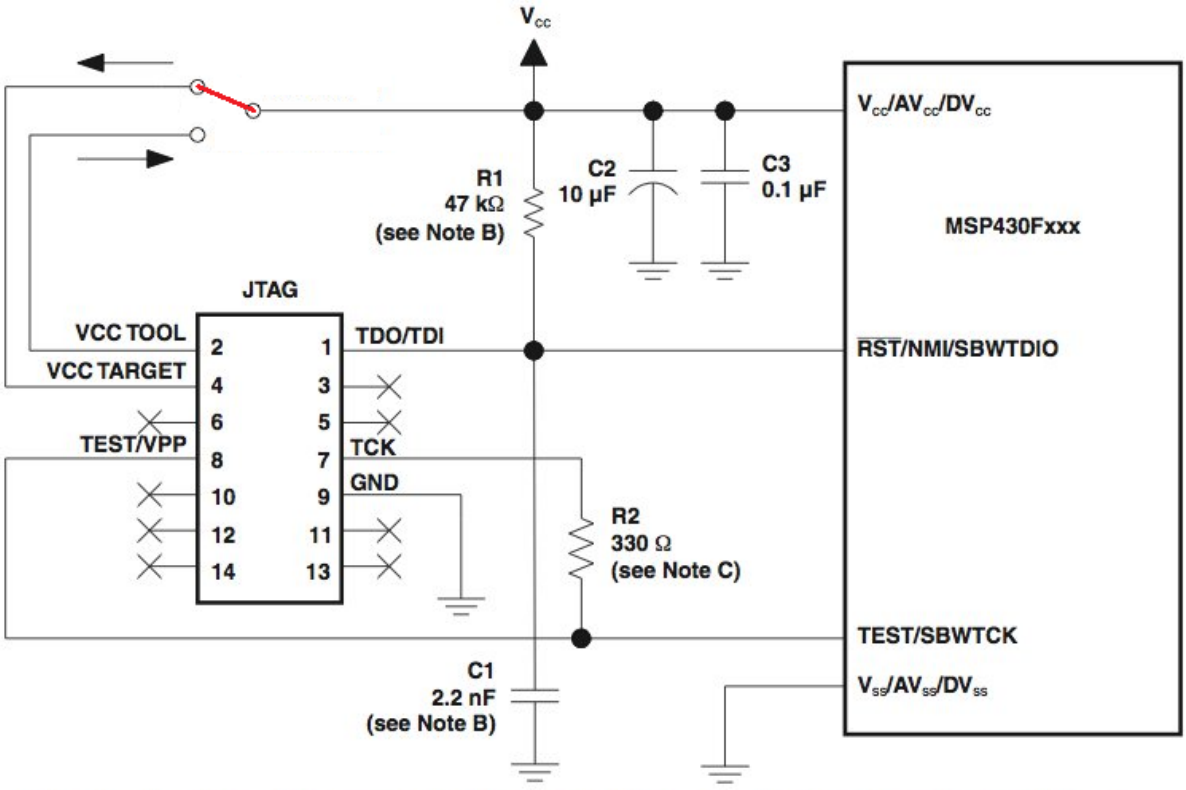

Figure 40. Power Supply Connection During Debugging

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7 Verification and Measured Performance

7.1 Test Setup

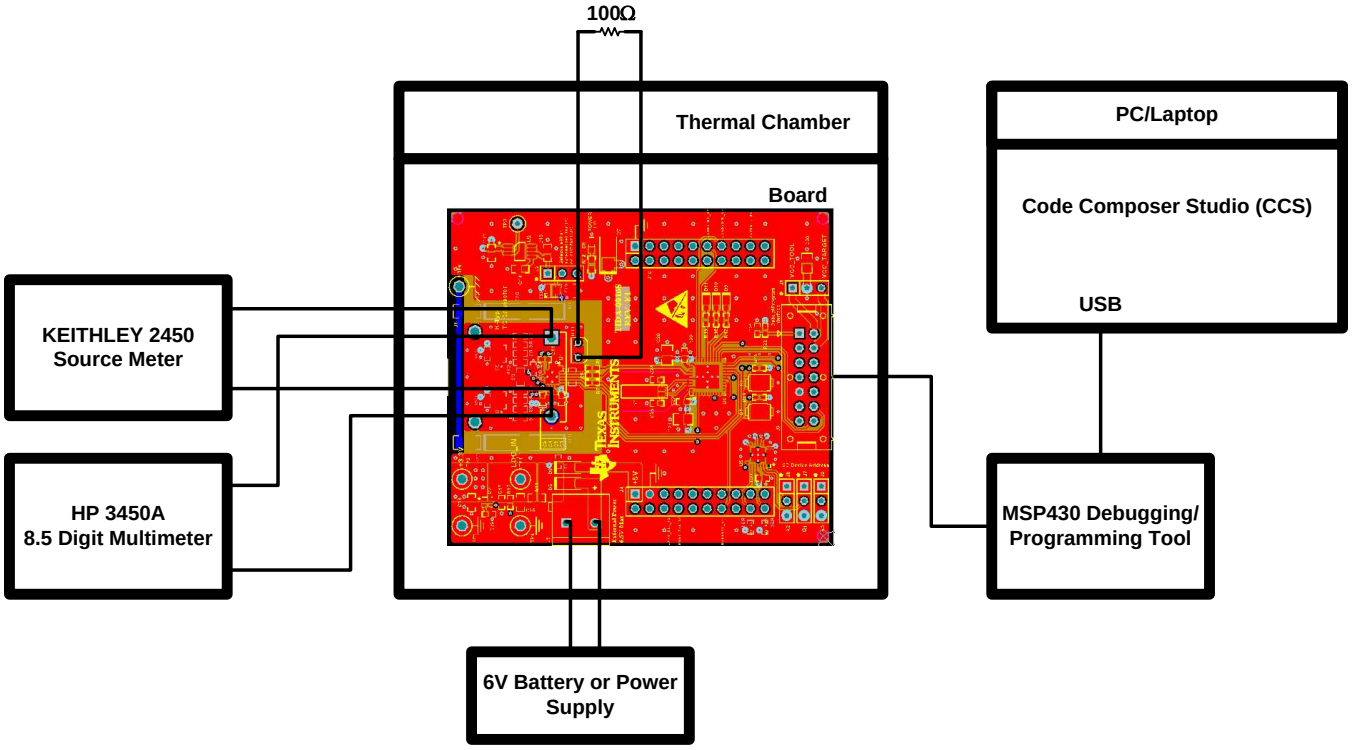

Figure 41. Test Setup

NOTE:

1. This design provides a thermocouple temperature from the equivalent voltage according to the type-K table, which validates a cold junction temperature of 0°C. Therefore, the onboard RTD Pt100 sensor that measures the CJC is replaced with the high-precision 100-Ω resistor, which is equivalent to 0°C.
2. The test data in the following sections measures at room temperature using calibrated lab equipment unless otherwise specified.

7.2 Noise Histogram for Thermocouple Channel

Use the histogram corresponding to the ADC output code to approximate the peak-to-peak noise of the acquisition system. In this design, the thermocouple inputs are shorted together. Conifgure the ADS1220 for continuous conversion mode at a 20-SPS data rate in the software. To generate the histogram plot for this design, the MSP430 MCU recorded 1024 samples.

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7.2.1 Noise Histogram With Internal Voltage Reference

The peak-to-peak spread of the codes in the histogram of Figure 42 is approximately 209 codes. Equation 55 calculates the least-significant bit (LSB) size of the ADC, which is then used to translate the peak-to-peak noise voltage:

$$1\,\text{LSB} = \frac{2.048}{32 \times (2^{24} - 1)} = 3.815\ \text{nV}$$

$$\text{Peak-to-peak noise} = 1\,\text{LSB} \times \text{ADC code spread} = 3.815\ \text{nV} \times 209 = 0.797\ \mu V_{PP} \quad (55)$$

The peak-to-peak noise (0.797 μV_{PP}) of the acquisition system is in close proximity to the ADC's peak-to-peak noise (0.73 µV) given in the datasheet.

Calculate the total noise in terms of degrees Celsius using the peak-to-peak noise as illustrated in Equation 56 :

$$\text{Noise (in °C)} = \frac{\text{Noise voltage (in } \mu V_{PP})}{\text{Thermocouple sensitivity (in } \mu \frac{V}{°C})} = \frac{0.797\ \mu V_{PP}}{39.77\ \mu \frac{V}{°C}} = 0.02°C \quad (56)$$

Reduce the noise further by implementing additional averaging or filtering in the software.

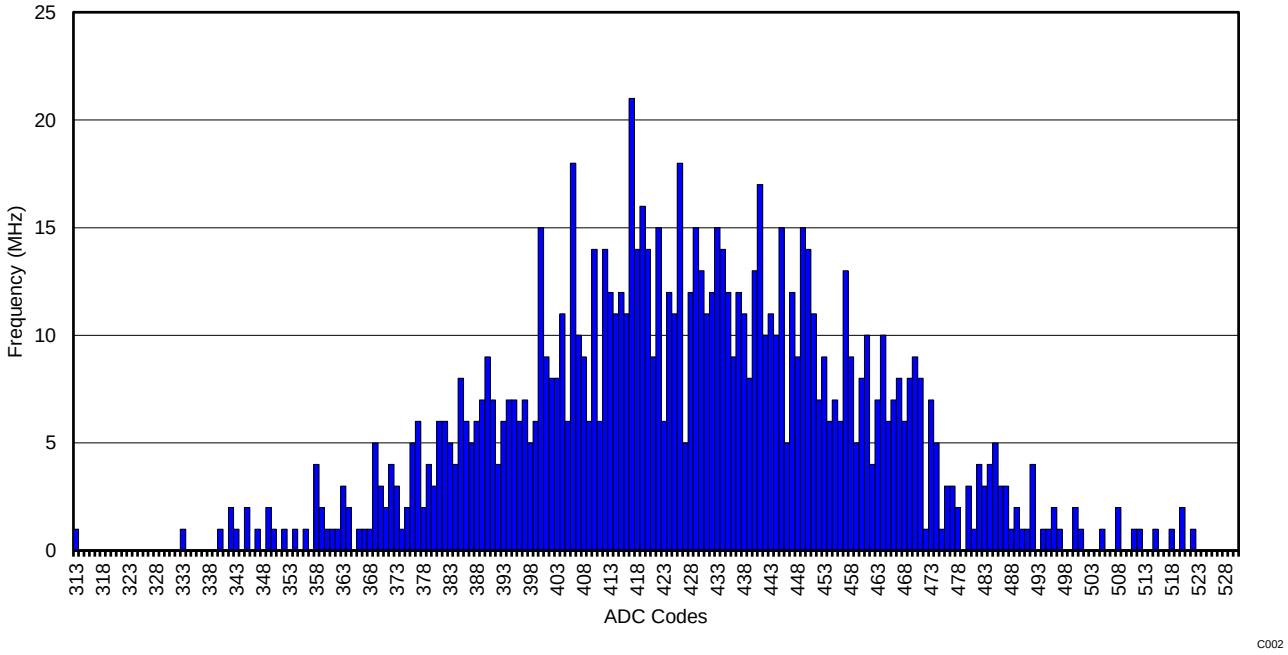

Figure 42. Raw ADC Code Distribution With Internal Voltage Reference

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7.2.2 Noise Histogram With External Voltage Reference

The peak-to-peak spread of the codes in the histogram of Figure 43 is approximately 214 codes. Equation 57 calculates the least-significant bit (LSB) size of the ADC, which is then used to translate the peak-to-peak noise voltage:

$$1\,\text{LSB} = \frac{2.048}{32 \times (2^{24} - 1)} = 3.815\ \text{nV}$$

$$\text{Peak-to-peak noise} = 1\,\text{LSB} \times \text{ ADC code spread} = 3.815\ \text{nV} \times 214 = 0.8164\ \mu V_{PP} \quad (57)$$

The peak-to-peak noise (0.8164 μV_{PP}) of the acquisition system is in close proximity to the ADC's peak-to-peak noise (0.73 µV) given in the datasheet.

Calculate the total noise in terms of degrees Celsius using the peak-to-peak noise as illustrated in Equation 58:

$$\text{Noise (in °C)} = \frac{\text{Noise voltage (in } \mu V_{PP})}{\text{Thermocouple sensitivity (in } \mu \frac{V}{°C})} = \frac{0.8164\ \mu V_{PP}}{39.77\ \mu \frac{V}{°C}} = 0.0205°C \quad (58)$$

Reduce the noise further by implementing additional averaging or filtering in the software.

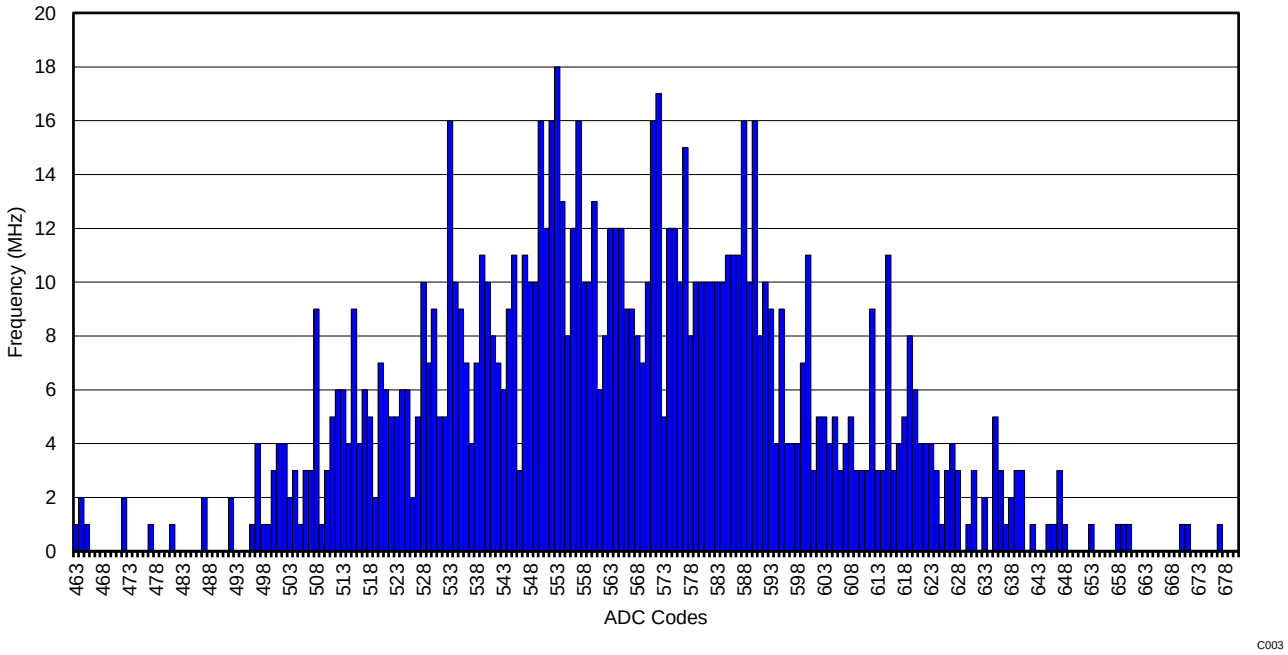

Figure 43. Raw ADC Code Distribution With External Voltage Reference

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7.3 Temperature Error of RTD Channel

Plot the temperature error for the RTD channel by replacing the RTD Pt100 sensor with a high-precision 100-Ω resistor. In this design multiple readings of ambient temperature were taken at 25ºC. The RTD channel error directly impacts the overall system accuracy. The temperature error graph in Figure 44 exclusively shows the error due to the measurement system.

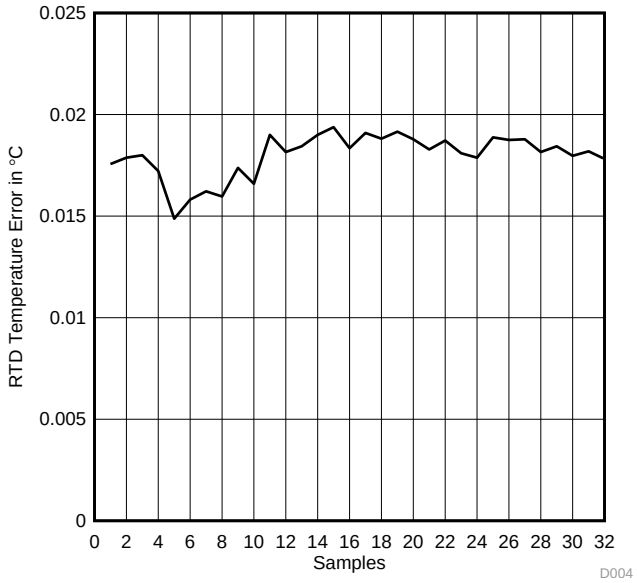

Figure 44. RTD Temperature Error at 25ºC

7.4 Temperature Error for Thermocouple Channel Without CJC

To test the thermocouple channel of the ADS1220 device, transfer the equivalent thermocouple voltages to the input. Calculate the equivalent thermocouple voltages with either the formula for a given type of thermocouple or with a table. Calculations by formula and table are only valid when the junction temperature is equal to 0°C. To eliminate the uncertainty of the junction temperature, replace the PT100 element with a high-precision 100-Ω equivalent to 0°C. Additionally, the MSP430 provides the pure temperature cycle (TC) temperature without the calculation of the cold junction. All of the tests covered under Section 7.4 use the test setup shown in Figure 41. The equivalent thermocouple voltages sweep from –200°C to 1370°C in several steps.

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7.4.1 Temperature Error With Internal Reference

Figure 45, Figure 46, Figure 47, Figure 48, and Figure 49 show the temperature error at three different ambient temperatures with and without gain calibration when using the ADCs internal voltage reference. The temperature error shown in the graph is solely due to the TC channel and does account for the RTD channel.

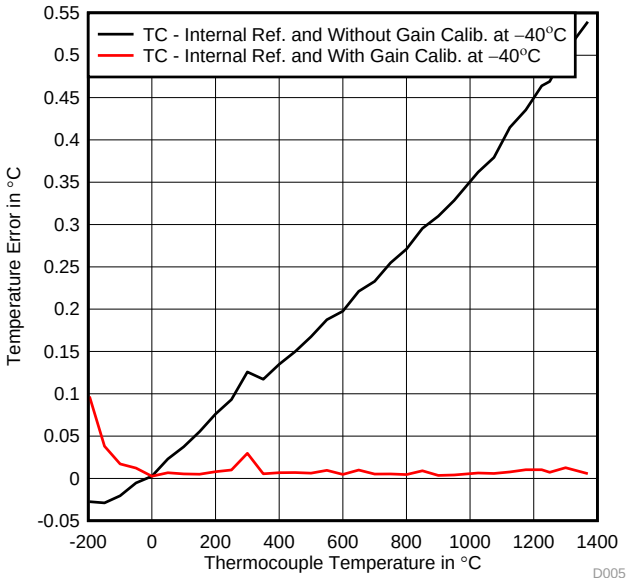

Figure 45. Thermocouple Temperature Error With and Without Gain Calibration at –40°C Using Internal Voltage Reference

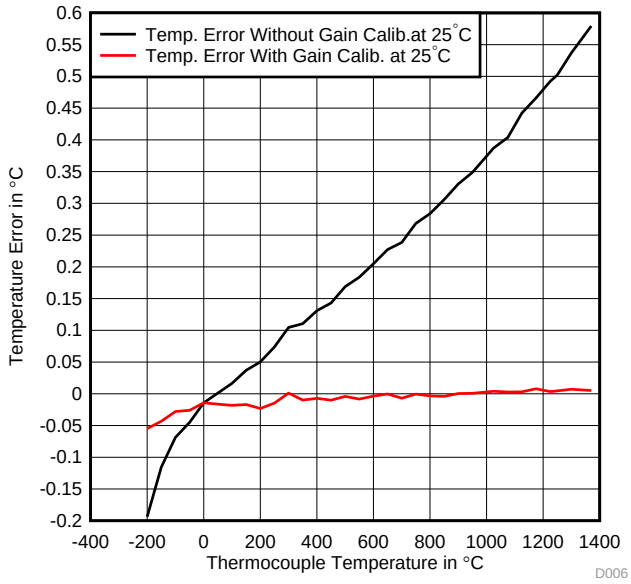

Figure 46. Thermocouple Temperature Error With and Without Gain Calibration at 25°C Using Internal Voltage Reference

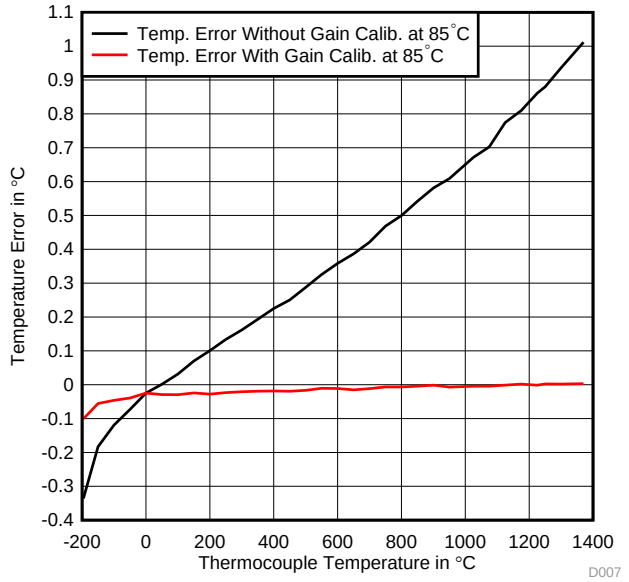

Figure 47. Thermocouple Temperature Error With and Without Gain Calibration at 85°C Using Internal Voltage Reference

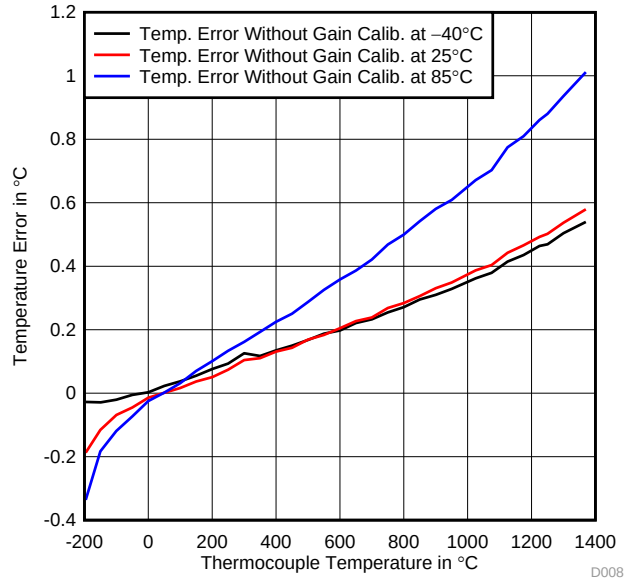

Figure 48. Thermocouple Temperature Error Without Gain Calibration at –40°C, 25°C, and 85°C Using Internal Voltage Reference

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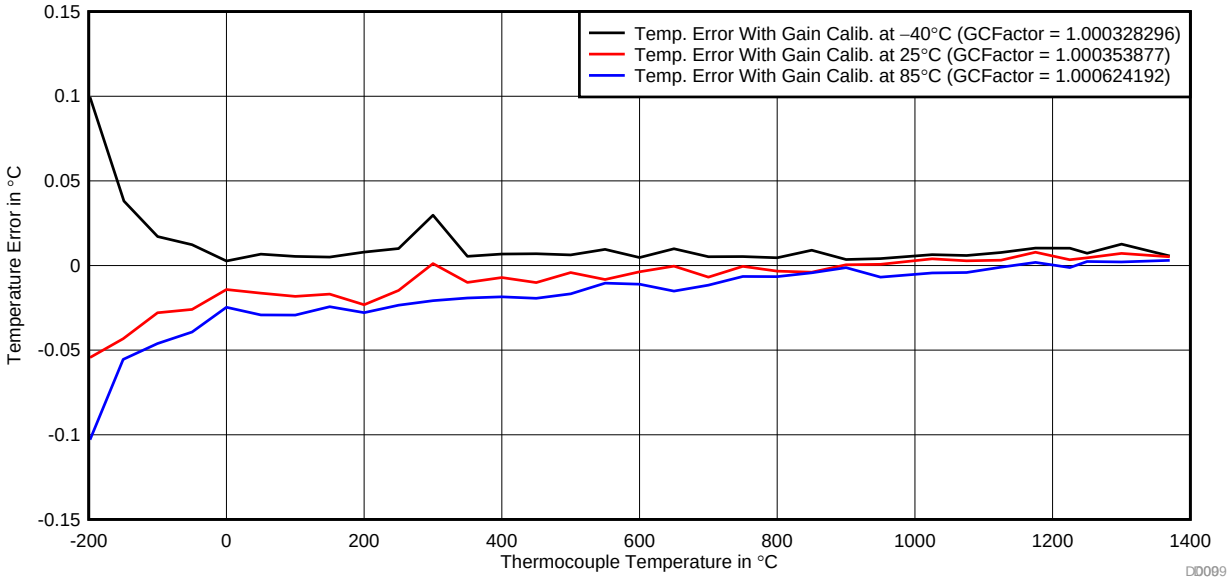

Figure 49. Thermocouple Temperature Error With Gain Calibration at –40°C, 25°C, and 85°C Using Internal Voltage Reference

7.4.2 Temperature Error With External Reference

Figure 50, Figure 51, Figure 52, Figure 53, and Figure 54 show the temperature error at three different ambient temperatures with and without gain calibration when using external voltage reference. The temperature errors shown in the graphs are due to the TC channel and do not account for the RTD channel.

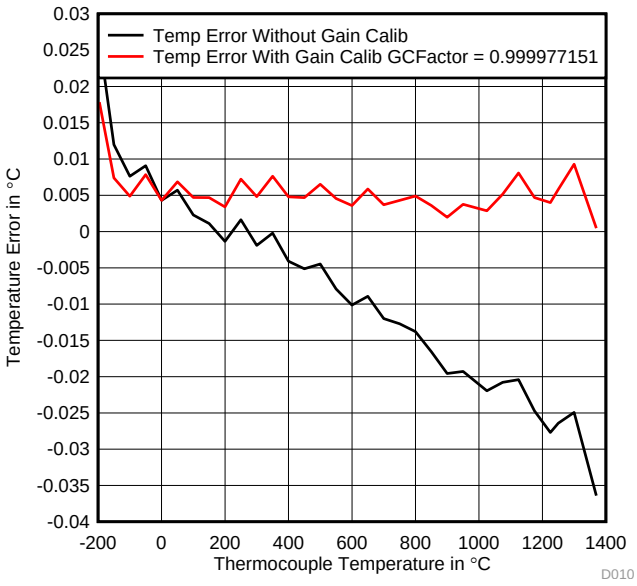

Figure 50. Thermocouple Temperature Error With and Without Gain Calibration at –40°C Using External Voltage Reference

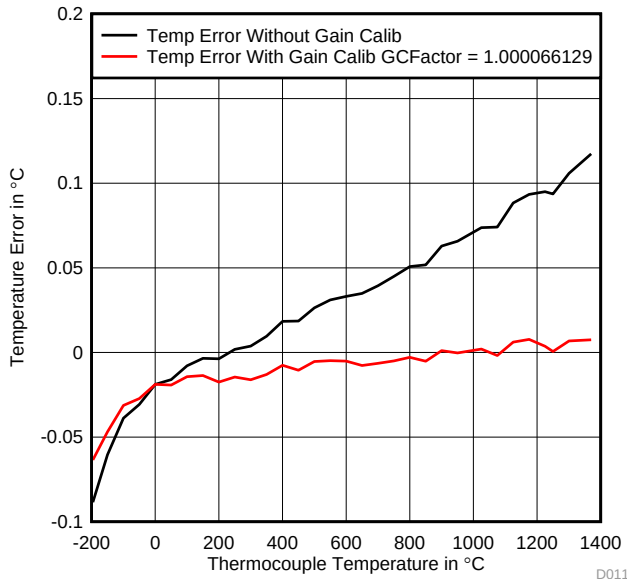

Figure 51. Thermocouple Temperature Error With and Without Gain Calibration at 25°C Using External Voltage Reference

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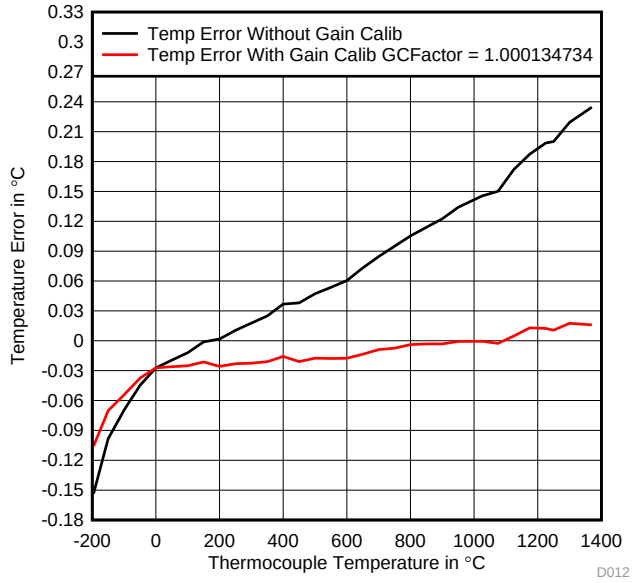

Figure 52. Thermocouple Temperature Error With and Without Gain Calibration at 85°C Using External Voltage Reference

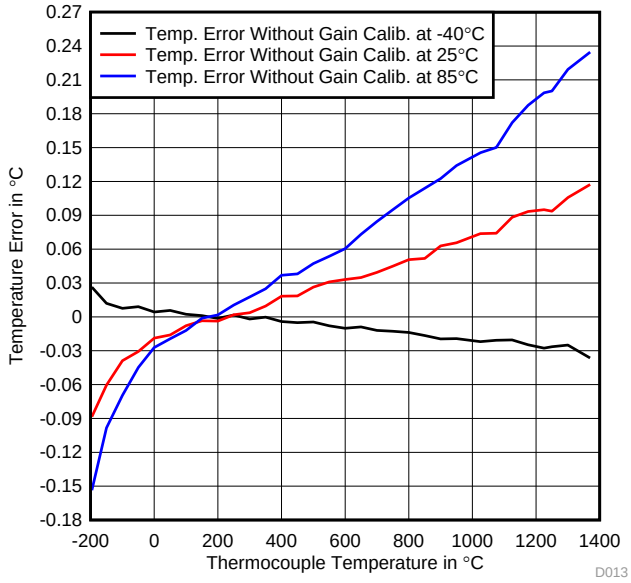

Figure 53. Thermocouple Temperature Error Without Gain Calibration at –40°C, 25°C, and 85°C Using External Voltage Reference

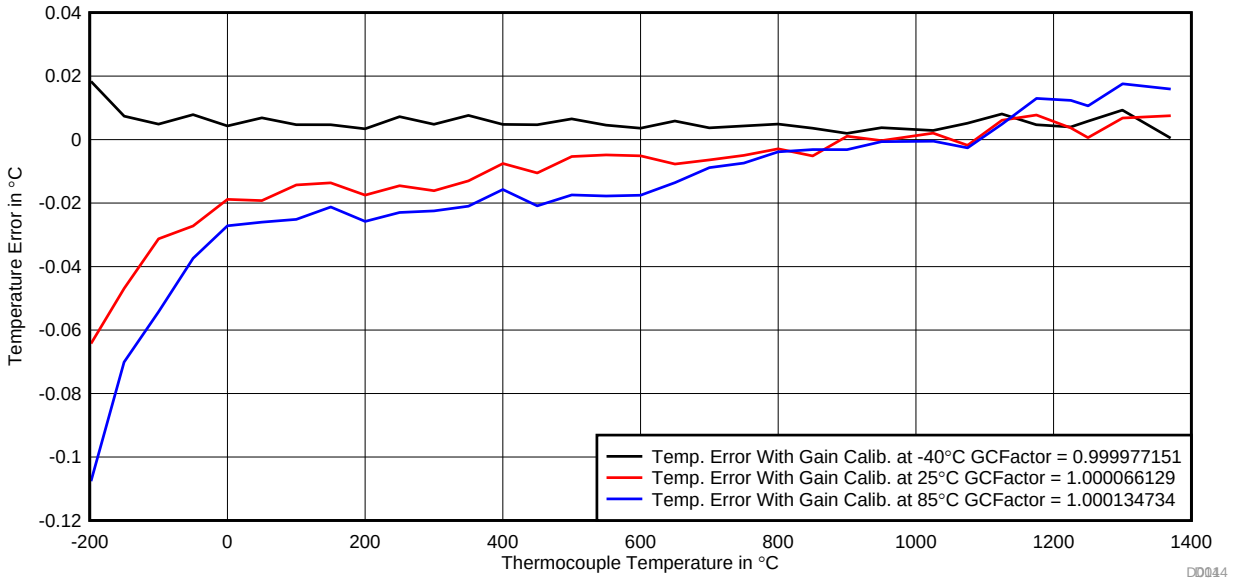

Figure 54. Thermocouple Temperature Error With Gain Calibration at –40°C, 25°C, and 85°C Using External Voltage Reference

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7.5 Oil Bath Testing

An excellent way to test the accuracy of the RTD and CJC of the on-chip with the completed board is to place the ADS1220 and cold junction into a temperature-controlled environment. The next step is to place the other end of the thermocouple into an established, constant source of temperature such as a thermal bath. View this experimental setup in Figure 55.

When performing this experiment, try to simulate the actual environment in which the system board is to be used. If the ADS1220 and cold junction are within an enclosure without significant air currents, using a simple oven may be sufficient. To benchmark the system performance in applications that must endure high-air currents, a temperature forcing system can be useful. The accuracy of the oven or temperature forcing system used on the ADS1118 system board and cold junction does not need to be highly accurate. However, the other end of the thermocouple must be maintained at a constant and accurate temperature.

A good example for achieving this constant temperature is to use a thermal bath or a well-insulated bath of ice water. To perform this experiment, sweep the temperature of the ADS1220 PCB and thermocouple cold junction while maintaining a constant temperature at the end of the thermocouple in the thermal bath. Record the temperature measurements of the thermocouple and plot the temperature errors against the cold junction temperature (oven temperature) for different options.

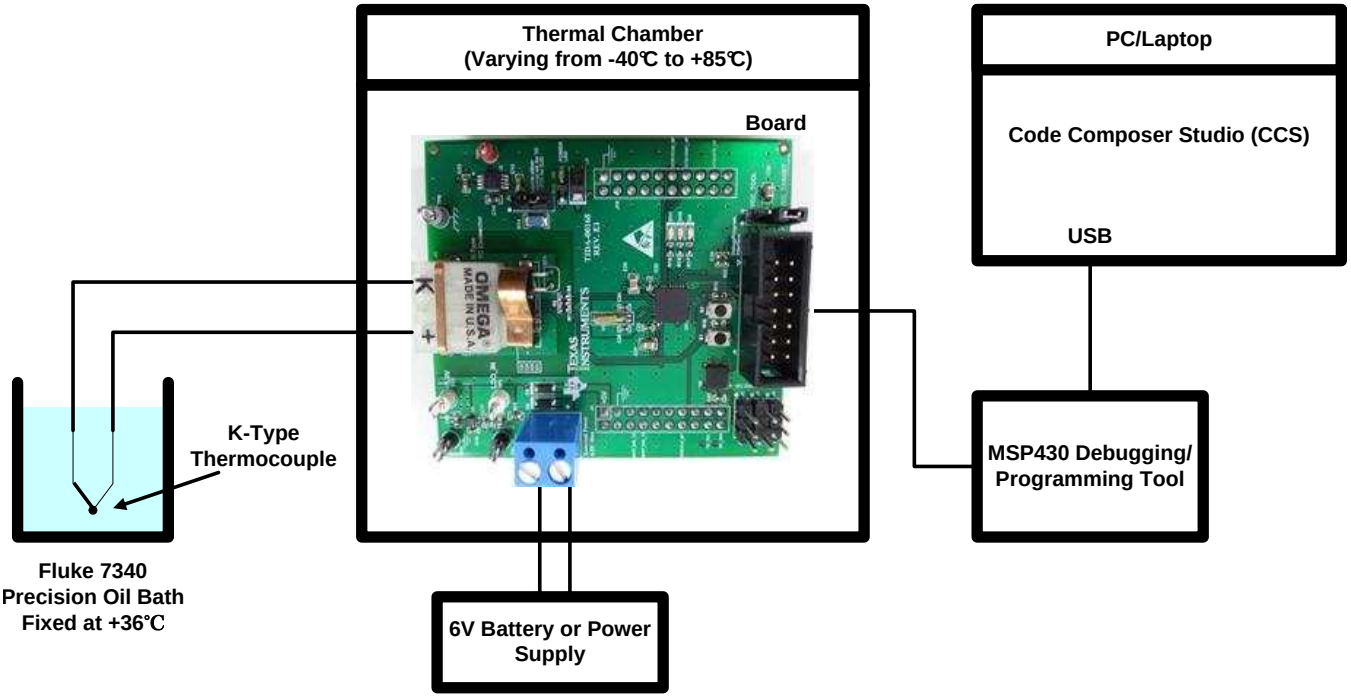

Figure 55. Experimental Setup With Varying Cold Junction Temperature

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Figure 56 shows the plot of the thermocouple measurements against the cold junction temperature obtained in this experiment. Use this setup to reveal inaccuracies that arise because of changes to the system board temperature, cold junction temperature, and ADS1220 temperature. This design obtains results without the use of gain calibrations and includes all errors as a result of the reference voltage drift, RTD sensor, internal temperature sensor, and isothermal block.

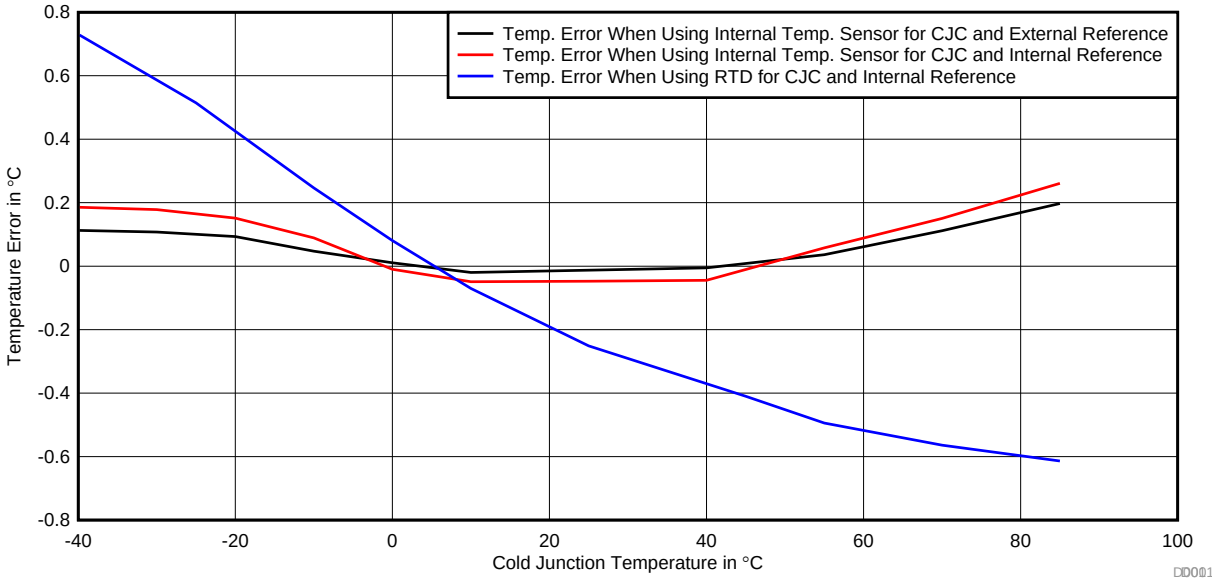

Figure 56. Thermocouple Temperature Error With Varying Cold Junction Temperature of the Board

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8 Design Files

8.1 Schematics

To download the schematic, see the design files at TIDA-00168.

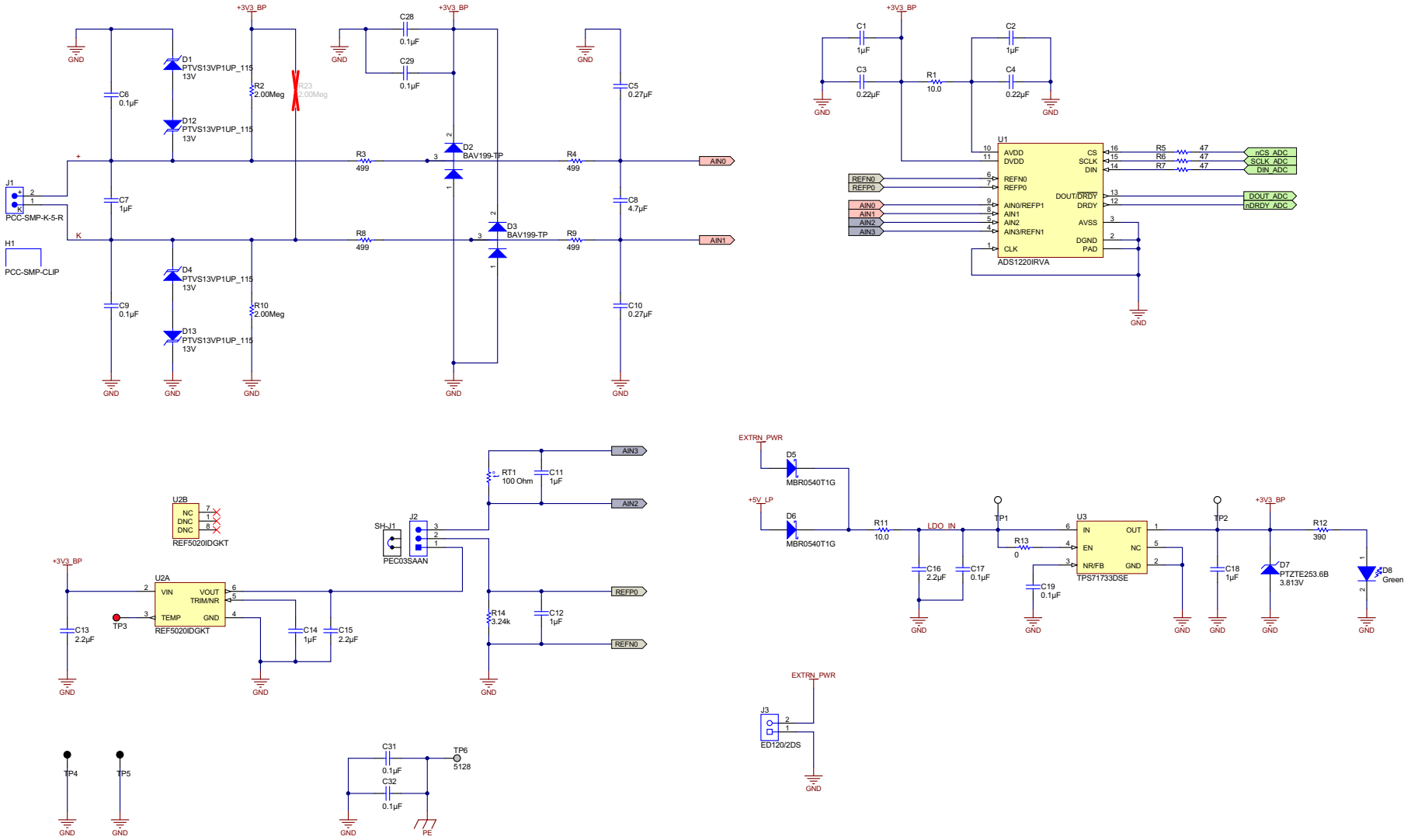

Figure 57. Schematic Page 1

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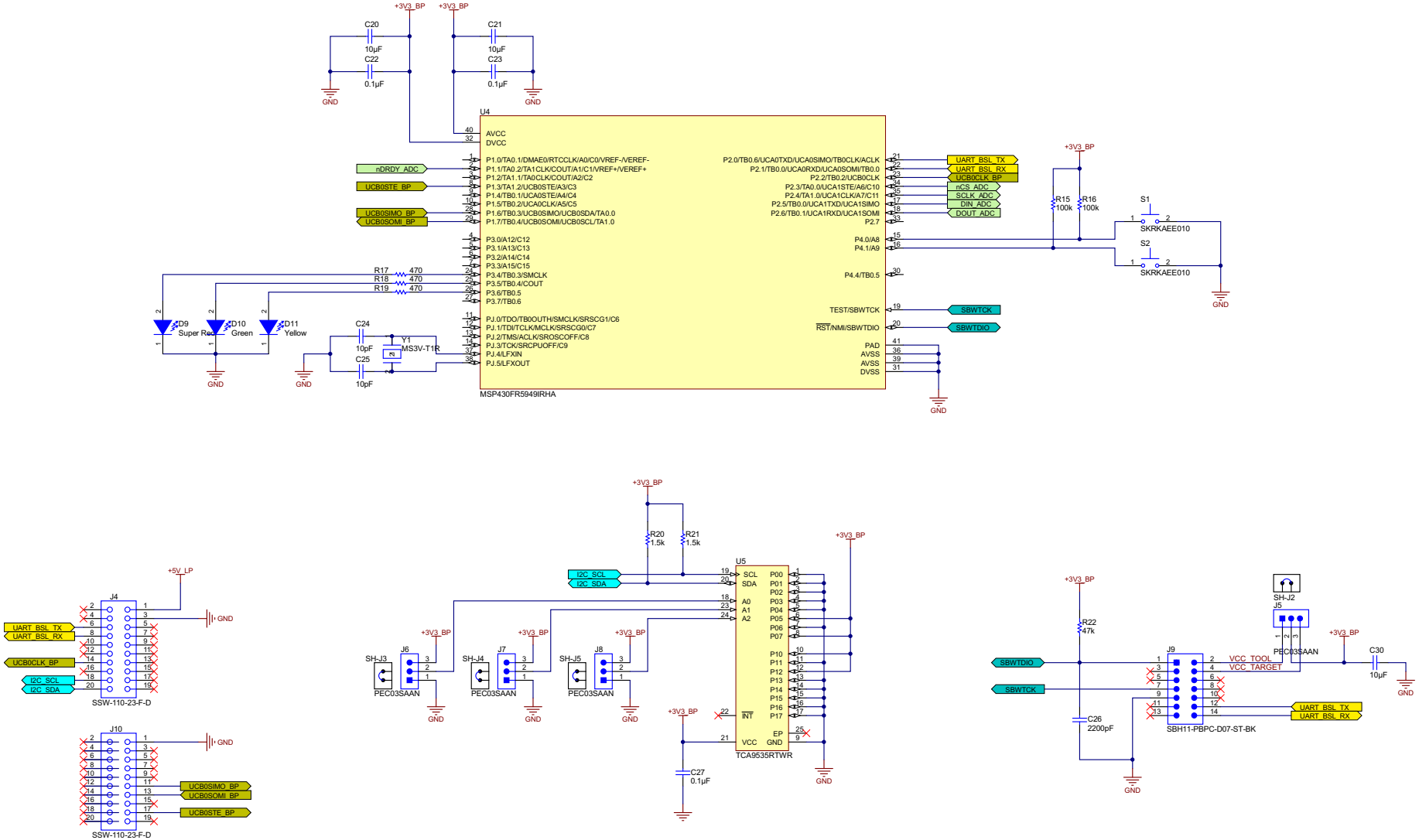

Figure 58. Schematic Page 2

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8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00168.

Table 6. BOM

FITTED	DESCRIPTION	DESIGNATOR	FOOTPRINT	MANUFACTURER	PARTNUMBER	QTY	ROHS
Fitted	CAP, CERM, 2200 pF, 6.3 V, ±10%, X7R, 0402	C26	0402	MuRata	GRM155R70J222KA01D	1	Y
Fitted	CAP, CERM, 10 µF, 10 V, ±10%, X7R, 0805	C30	0805	MuRata	GRM21BR71A106KE51L	1	Y
Fitted	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 0603	C7	0603	Taiyo Yuden	UMK107AB7105KA-T	1	Y
Fitted	CAP, CERM, 4.7 µF, 6.3 V, ±10%, X5R, 0603	C8	0603	MuRata	GRM188R60J475KE19D	1	Y
Fitted	LED, Green, SMD	D10	LED_0603	Wurth Elektronik eiSos	150060VS75000	1	Y
Fitted	LED, Yellow, SMD	D11	LED_0603	Wurth Elektronik eiSos	150060YS75000	1	Y
Fitted	Diode, Zener, 3.813 V, 1 W, SMA	D7	SMA	Rohm	PTZTE253.6B	1	Y
Fitted	LED, Green, SMD	D8	1.7 × 0.65 × 0.8 mm	OSRAM	LG L29K-G2J1-24-Z	1	Y
Fitted	LED, Super Red, SMD	D9	LED_0603	Wurth Elektronik eiSos	150060SS75000	1	Y
Fitted	Mounting bracket for PCC-SMP	H1		Omega	PCC-SMP-CLIP	1	Y
Fitted	Circuit Board Thermocouple Connector, Miniature Size, Type-K, Horizontal installation, TH	J1	20.8 × 6.3 × 15.5 mm	Omega	PCC-SMP-K-5-R	1	Y
Fitted	Terminal Block 5.08 mm Vert 2POS, TH	J3	TERM_BLK, 2pos, 5.08 mm	On-Shore Technology	ED120/2DS	1	Y
Fitted	Header (shrouded), 100 mil, 7 × 2, Gold plated, TH	J9	7 × 2 Shrouded Header	Sullins Connector Solutions	SBH11-PBPC-D07-ST-BK	1	Y
Fitted	RES, 390 Ω, 5%, 0.1 W, 0603	R12	0603	Yageo America	RC0603JR-07390RL	1	Y
Fitted	RES, 0 Ω, 5%, 0.063 W, 0402	R13	0402	Vishay-Dale	CRCW04020000Z0ED	1	Y
Fitted	RES, 3.24 kΩ, 0.1%, 0.333 W, 1206	R14	1206	TT Electronics/IRC	PFC-W1206R-12-3241-B	1	Y
Fitted	RES, 47 kΩ, 5%, 0.063 W, 0402	R22	0402	Vishay-Dale	CRCW040247K0JNED	1	Y
Fitted	Temperature Sensor, 100 Ω, TC = 3850 ppm, TO-92, TH	RT1	TO-92, 2pin	Heraeus Sensor Technology	32209210	1	
Fitted	Test Point, Miniature, Red, TH	TP3	Red Miniature Testpoint	Keystone	5000	1	Y

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Table 6. BOM (continued)

FITTED	DESCRIPTION	DESIGNATOR	FOOTPRINT	MANUFACTURER	PARTNUMBER	QTY	ROHS
Fitted	Test Point, Multi-Purpose, Grey, TH	TP6	Grey Multi-Purpose Testpoint	Keystone	5128	1	Y
Fitted	Low-Power, Low-Noise, 24-Bit Analog-to-Digital Converter for Small Signal Sensors, RVA0016A	U1	RVA0016A	Texas Instruments	ADS1220IRVA	1	Y
Fitted	Low-Noise, Very Low-Drift, Precision Voltage Reference, –40 to 125°C, 8-Pin MSOP (DGK), Green (RoHS and no Sb/Br)	U2	DGK0008A	Texas Instruments	REF5020IDGKT	1	
Fitted	Low-Noise, High-Bandwidth PSRR Low-Dropout 150 mA Linear Regulator, DSE0006A	U3	DSE0006A	Texas Instruments	TPS71733DSE	1	Y
Fitted	MSP430FR5949 16 mHz Ultra-Low Power Microcontroller featuring 64 KB FRAM, 2 KB SRAM, 33 IO, RHA0040B	U4	RHA0040B	Texas Instruments	MSP430FR5949IRHA	1	Y
Fitted	Remote 16-Bit I2C and SMBus, Low-Power I/O Expander with Interrupt Output and Config Register, 1.65 to 5.5 V, –40 to 85°C, 24-Pin QFN (RTW), Green (RoHS & no Sb/Br)	U5	RTW0024B	Texas Instruments	TCA9535RTWR	1	
Fitted	Crystal, Tuning Fork, 30 kHz to 200 kHz, SMD	Y1	6.7 × 1.40 mm	Micro Crystal AG	MS3V-T1R	1	
Fitted	CAP, CERM, 1 µF, 10 V, ±10%, X7R, 0603	C14, C18	0603	MuRata	GRM188R71A105KA61D	2	Y
Fitted	CAP, CERM, 10 µF, 6.3 V, ±10%, X7R, 0805	C20, C21	0805	MuRata	GRM21BR70J106KE76L	2	Y
Fitted	CAP, CERM, 10 pF, 50 V, ±5%, C0G/NP0, 0402	C24, C25	0402	MuRata	GRM1555C1H100JA01D	2	Y
Fitted	CAP, CERM, 0.22 µF, 6.3 V, ±10%, X5R, 0402	C3, C4	0402	MuRata	GRM155R60J224KE01D	2	Y
Fitted	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, 1206	C31, C32	1206	AVX	12061C104KAT2A	2	Y
Fitted	CAP, CERM, 0.27 µF, 6.3 V, ±10%, X5R, 0402	C5, C10	0402	MuRata	GRM155R60J274KE01D	2	Y
Fitted	Diode, Switching, 70 V, 0.215 A, SOT-23	D2, D3	SOT-23	Micro Commercial Components	BAV199-TP	2	Y

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Table 6. BOM (continued)

FITTED	DESCRIPTION	DESIGNATOR	FOOTPRINT	MANUFACTURER	PARTNUMBER	QTY	ROHS
Fitted	Diode, Schottky, 40 V, 0.5 A, SOD-123	D5, D6	SOD-123	ON Semiconductor	MBR0540T1G	2	Y
Fitted	Connector, Receptacle, 100 mil, 10 × 2, Gold plated, TH	J4, J10	HEADER, RECEPTACLE, 100 mil, 10 × 2	Samtec, Inc.	SSW-110-23-F-D	2	Y
Fitted	RES, 10.0 Ω, 1%, 0.1 W, 0603	R1, R11	0603	Vishay-Dale	CRCW060310R0FKEA	2	Y
Fitted	RES, 100 kΩ, 5%, 0.063 W, 0402	R15, R16	0402	Vishay-Dale	CRCW0402100KJNED	2	Y
Fitted	RES, 2.00 MΩ, 1%, 0.063 W, 0402	R2, R10	0402	Vishay-Dale	CRCW04022M00FKED	2	Y
Fitted	RES, 1.5 kΩ, 5%, 0.063 W, 0402	R20, R21	0402	Vishay-Dale	CRCW04021K50JNED	2	Y
Fitted	Switch, Push Button, SMD	S1, S2	2.9 × 2.0 × 3.9 mm SMD	Alps	SKRKAEE010	2	Y
Fitted	Test Point, Multi-Purpose, White, TH	TP1, TP2	White Multi-Purpose Testpoint	Keystone	5012	2	Y
Fitted	Test Point, Multi-Purpose, Black, TH	TP4, TP5	Black Multi-Purpose Testpoint	Keystone	5011	2	Y
Fitted	CAP, CERM, 2.2 µF, 10 V, ±10%, X7R, 0603	C13, C15, C16	0603	MuRata	GRM188R71A225KE15D	3	Y
Fitted	RES, 470 Ω, 5%, 0.063 W, 0402	R17, R18, R19	0402	Vishay-Dale	CRCW0402470RJNED	3	Y
Fitted	RES, 47 Ω, 5%, 0.063 W, 0402	R5, R6, R7	0402	Vishay-Dale	CRCW040247R0JNED	3	Y
Fitted	CAP, CERM, 1 µF, 10 V, ±10%, X5R, 0402	C1, C2, C11, C12	0402	MuRata	GRM155R61A105KE15D	4	Y
Fitted	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0402	C6, C9, C28, C29	0402	TDK	C1005X7R1H104K050BB	4	Y
Fitted	Diode, TVS, Uni, 13 V, 600 W, SMD, 2-Leads, Body 4 × 2.7 mm, Height 1.1 mm	D1, D4, D12, D13	SMD, 2-Leads, Body 4.0 × 2.7 mm, Height 1.1 mm	NXP Semiconductor	PTVS13VP1UP_115	4	Y
Fitted	RES, 499 Ω, 1%, 0.063 W, 0402	R3, R4, R8, R9	0402	Vishay-Dale	CRCW0402499RFKED	4	Y
Fitted	CAP, CERM, 0.1 µF, 10 V, ±10%, X7R, 0402	C17, C19, C22, C23, C27	0402	MuRata	GRM155R71A104KA01D	5	Y
Fitted	Header, 100 mil, 3 × 1, Tin plated, TH	J2, J5, J6, J7, J8	Header, 3 PIN, 100 mil, Tin	Sullins Connector Solutions	PEC03SAAN	5	Y
Fitted	Shunt, 100 mil, Gold plated, Black	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5	Shunt	3M	969102-0000-DA	5	Y

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Table 6. BOM (continued)

FITTED	DESCRIPTION	DESIGNATOR	FOOTPRINT	MANUFACTURER	PARTNUMBER	QTY	ROHS
Fitted	Fiducial mark. There is nothing to buy or mount.	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial	N/A	N/A	6	
Not Fitted	RES, 2.00 MΩ, 1%, 0.063 W, 0402	R23	0402	Vishay-Dale	CRCW04022M00FKED	0	Y

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8.3 Layer Plots

To download the layer plots, see the design files at TIDA-00168.

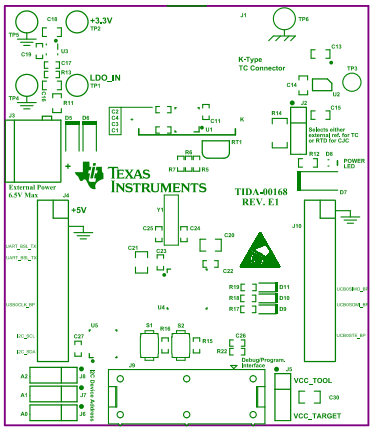

Figure 59. Top Overlay

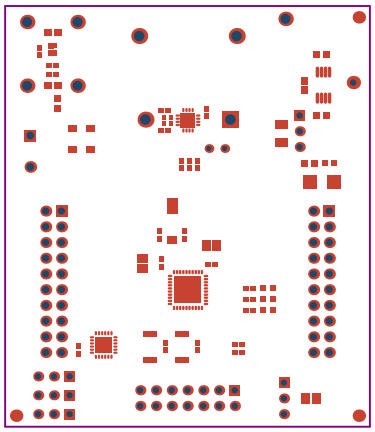

Figure 60. Top Solder Mask

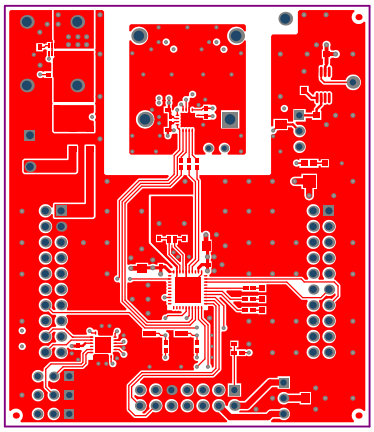

Figure 61. Top Layer

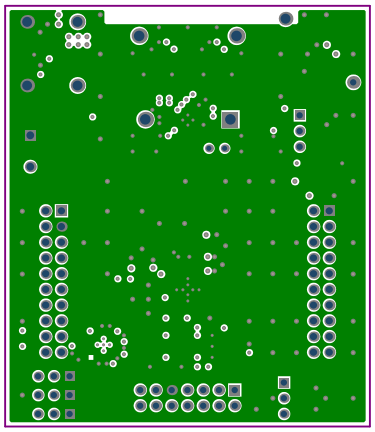

Figure 62. GND Plane

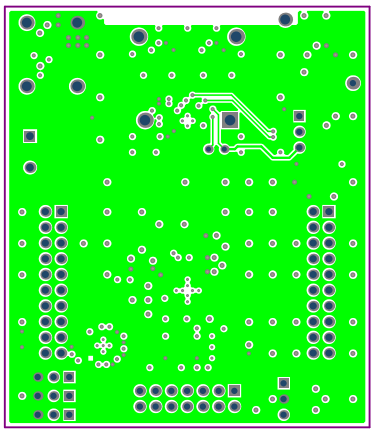

Figure 63. VCC Plane

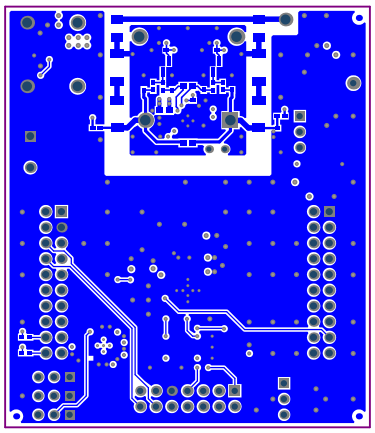

Figure 64. Bottom Layer

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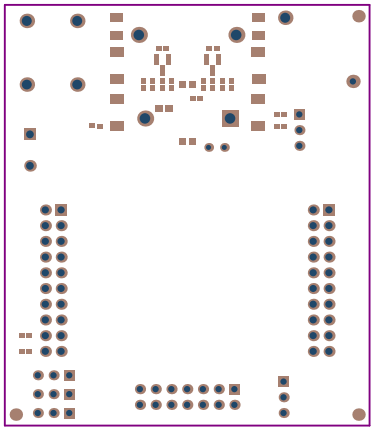

Figure 65. Bottom Solder Mask

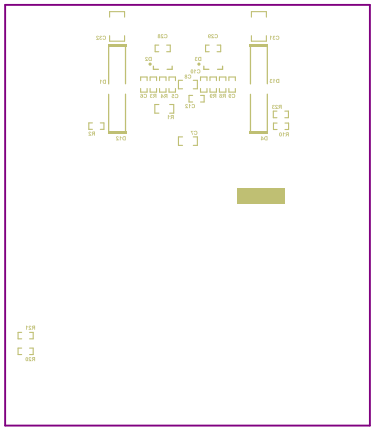

Figure 66. Bottom Overlay

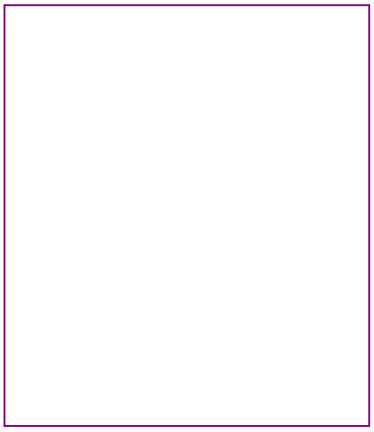

Figure 67. Board Outline

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00168.

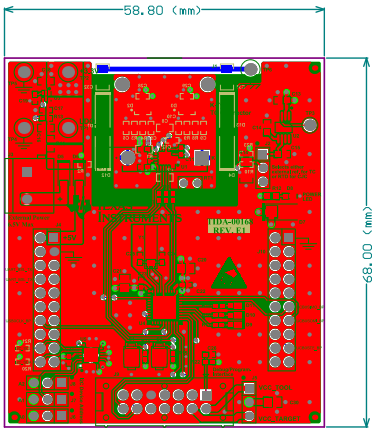

Figure 68. Multilayer Composite Print

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8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00168.

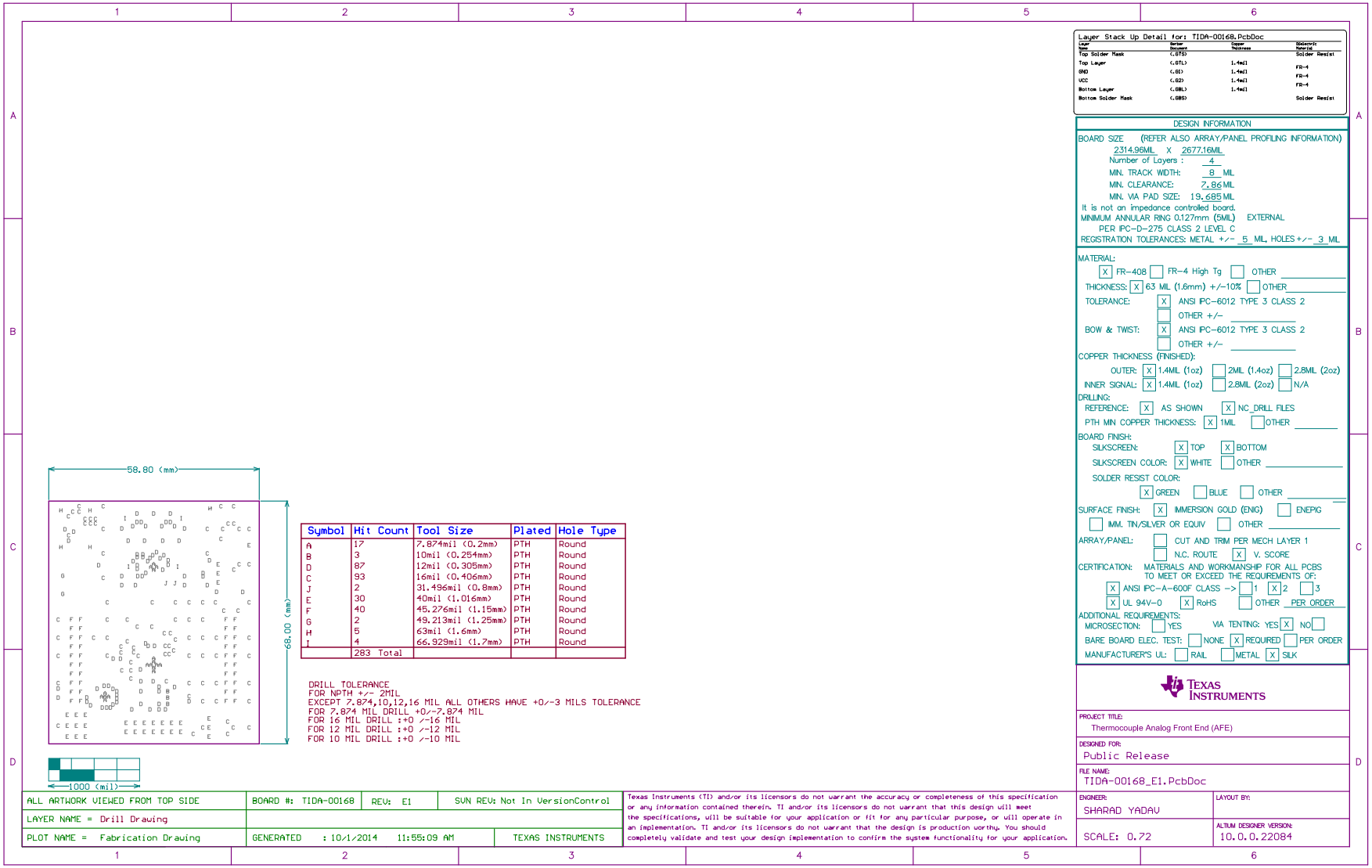

Figure 69. Fabrication Drawing

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8.6 Assembly Drawings

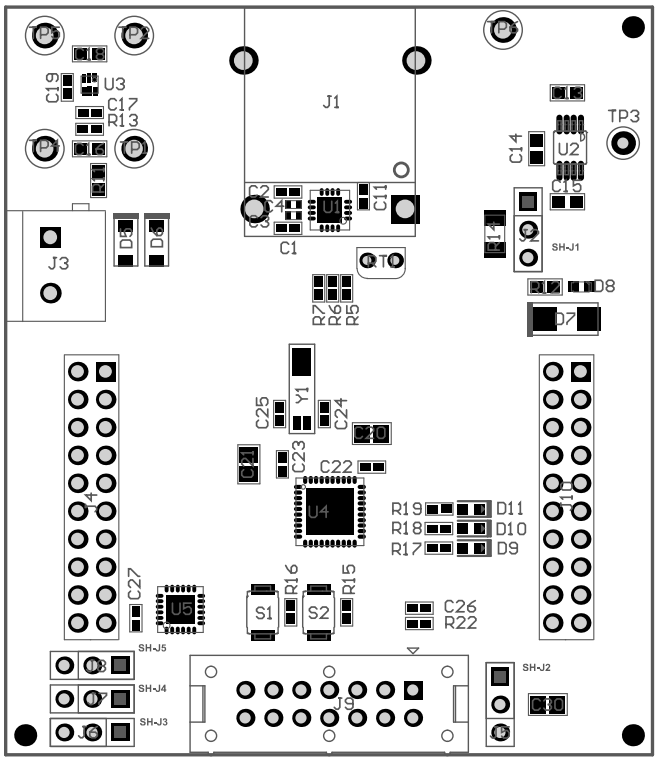

Figure 70. Top Assembly Drawing

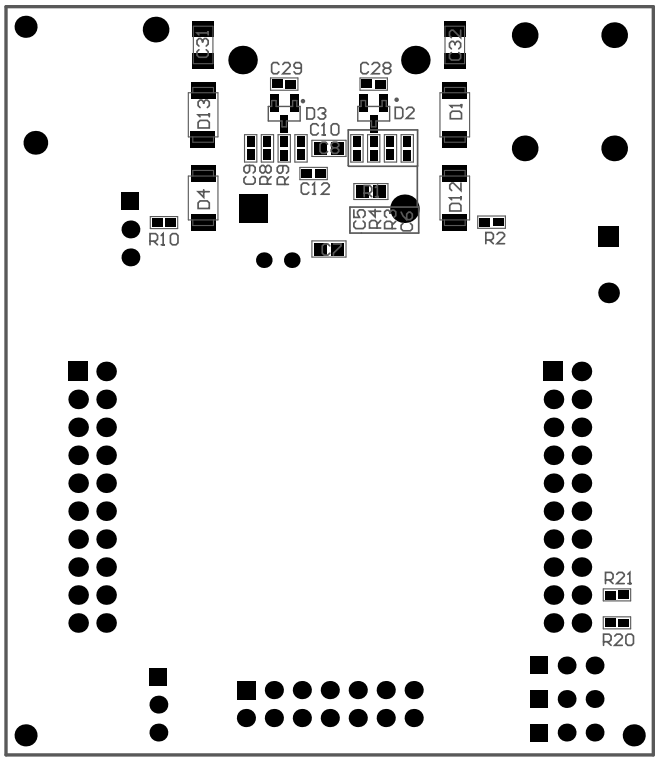

Figure 71. Bottom Assembly Drawing

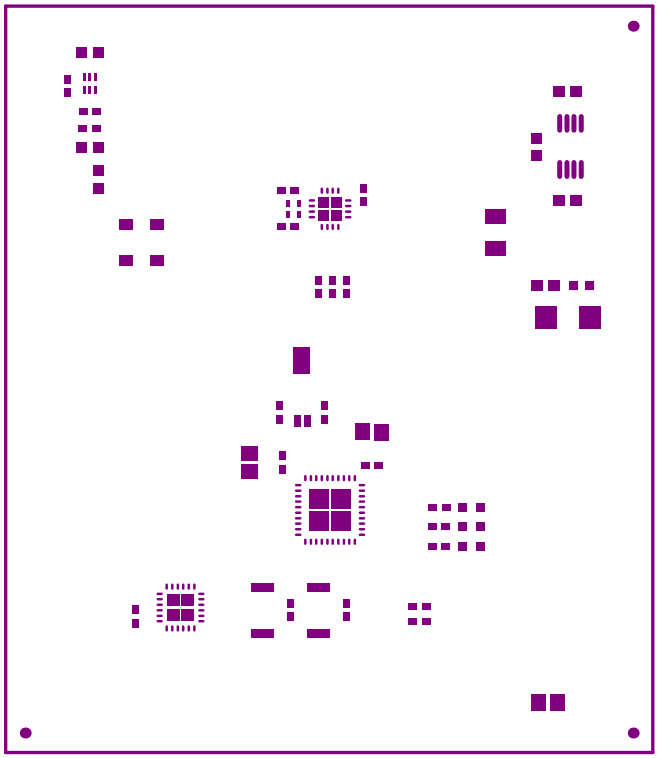

Figure 72. Top Paste

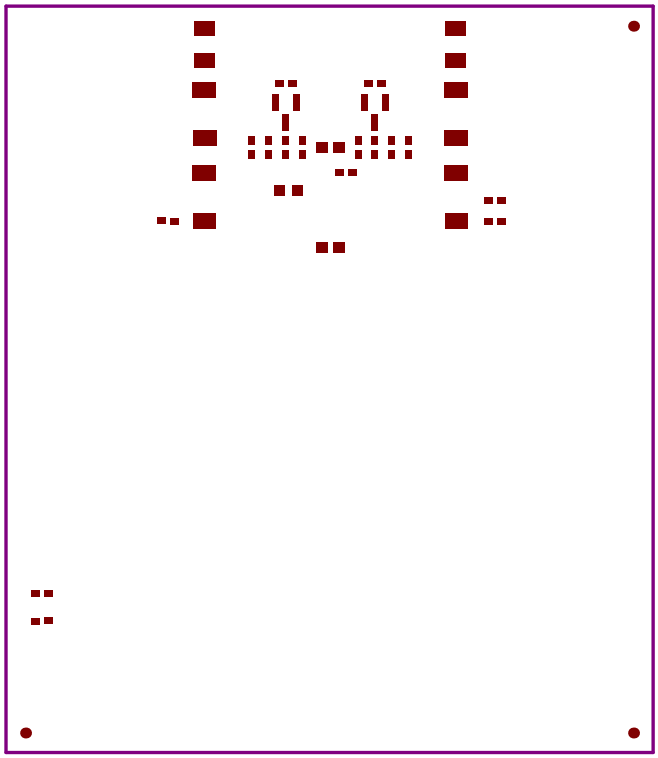

Figure 73. Bottom Paste

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8.7 Software Files

To download the software files, see the design files at TIDA-00168.

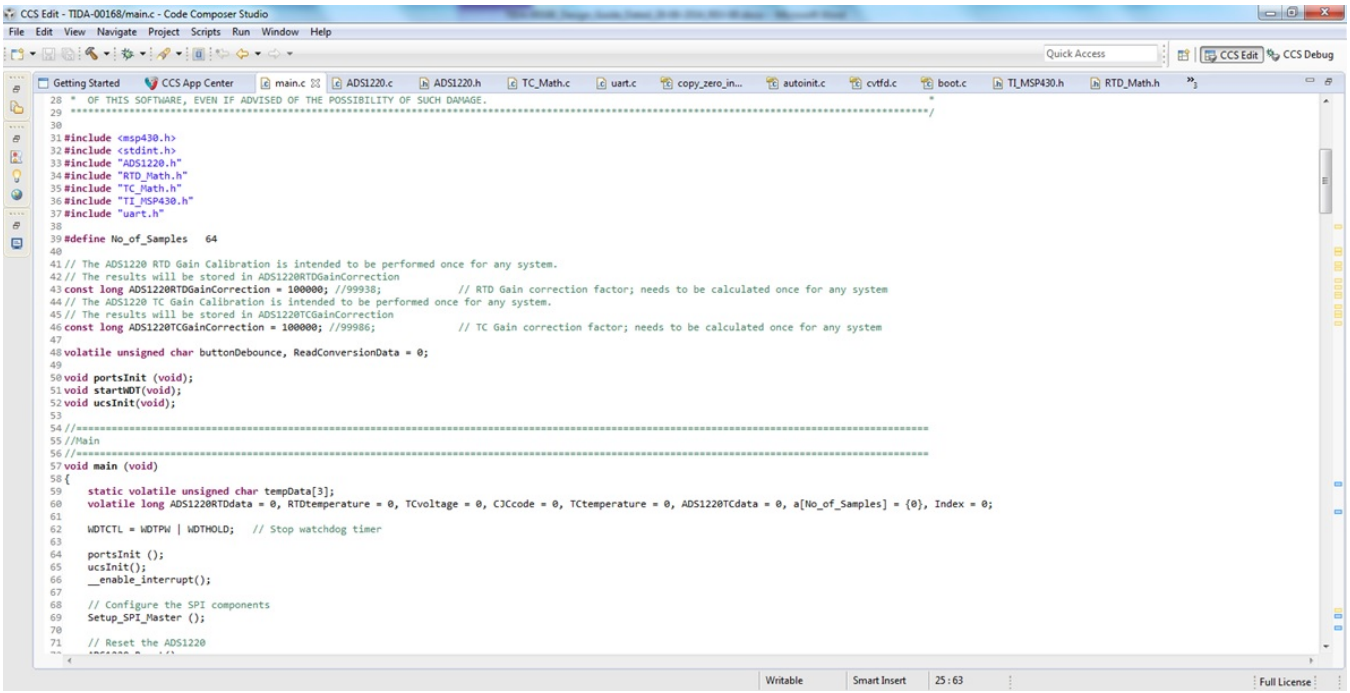

Figure 74. Code Composer Studio Screen Capture

9 References

1. Texas Instruments, *Example Temperature Measurement Applications Using the ADS1247 and ADS1248*, Application Report (SBAA180)
2. Texas Instruments, *Advanced Debugging Using the Enhanced Emulation Module*, Application Report (SLAA393)
3. Texas Instruments, *Precision Thermocouple Measurement with the ADS1118*, Application Report (SLAU509)
4. Texas Instruments, *Isolated Loop Powered Thermocouple Transmitter Reference Design*, Tool Folder (TIDA-00189)
5. Thermibel, *Conversion of RTD Pt100* (http://www.thermibel.be/documents/pt100/conv-rtd.xml?lang=en)

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