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Uniquely Efficient Isolated DC/DC Converter for Ultra-Low Power and Low-Power Applications

TI Designs

TI Designs provide the foundation that you need including methodology, testing, and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00349	Tool Folder Containing Design Files
TPS60402	Product Folder

TI E2E™ Community

ASK Our E2E Experts
WEBENCH® Calculator Tools

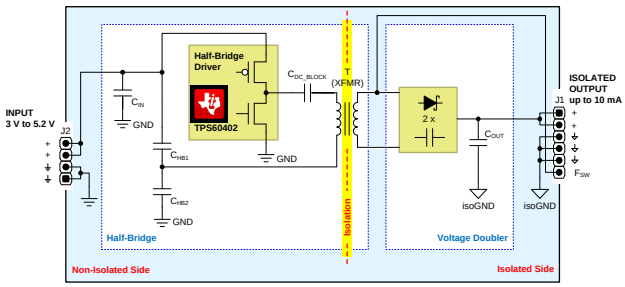
Design Features

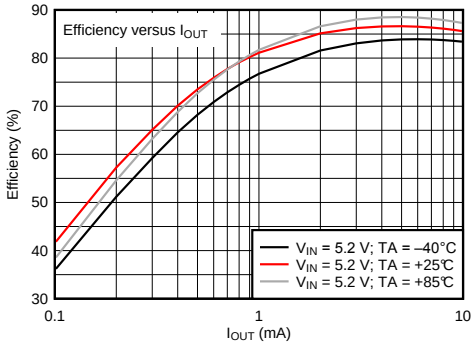
- Isolated DC/DC Converter for up to 60-mW Output Power
- Highly Efficient Design
  - Up to 86% With 5-V Input
  - Up to 82% With 3.3-V Input
  - Open-Loop, Optocoupler-less Design
- Characterized Over 3.0- to 5.2-V Input and for Output Currents up to 10 mA
- Synchronization Output and Fixed Switching Frequency Enable Use in Noise Sensitive Applications
- Flexible Configurable Board Enables Easy Evaluation and Modification

Featured Applications

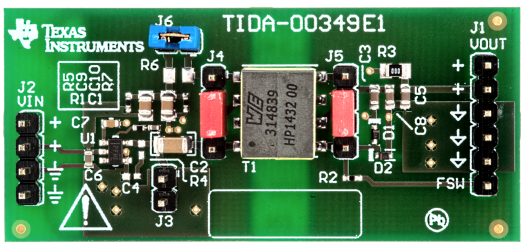
- Factory Automation and Process Control
- Loop Powered 4- to 20-mA Transmitters and Other Sensors and Field Transmitters
- Building Automation
- Portable Instrumentation

TIDA-00349 Block Diagram





Board Image



1 Introduction

The objective of this TI design is to provide a turn-key solution for an isolated DC/DC converter with a uniquely high efficiency at ultra-low power and low power levels of up to 60 mW. This design (TIDA-00349) is characterized at −40°C, +25°C, and +85°C and over an input voltage range from 3 V to 5.2 V and for output currents up to 10 mA. A low switching frequency of 60 kHz, which is independent of the load, enables the use of this design in noise-sensitive applications and is a major prerequisite for keeping the switching losses low. A low switching frequency also helps to achieve a uniquely high efficiency at low power levels. Additionally, Schottky diodes on the secondary side of the circuit assist in providing more than an 85% efficiency for a 5-V input operation at 15 mW to 50 mW of output power and more than 80% efficiency for a 3.3-V operation at a 3- to 20-mW power level.

The isolated DC/DC converter uses an open-loop control approach that simplifies the design and makes the optocoupler superfluous.

The single-sided, populated PCB is a convenient tool for evaluation of the design. An optimized number of headers and jumpers provide an easy way for modifying the board and adapting it to different requirements for a wide variety of applications.

2 System Description

Low power, isolated DC/DC converters such as this TIDA-00349 Design are currently used in a large variety of applications, such as factory automation, process control, building automation, and portable instrumentation.

One of the main purposes of using this design is the avoidance of ground loops in signal conditioning and data transmission applications. The design can also be used in similar cases where the functional isolation of the used transformer is sufficient. Other uses for this design may require the use of a modified transformer to fulfill more stringent isolation requirements.

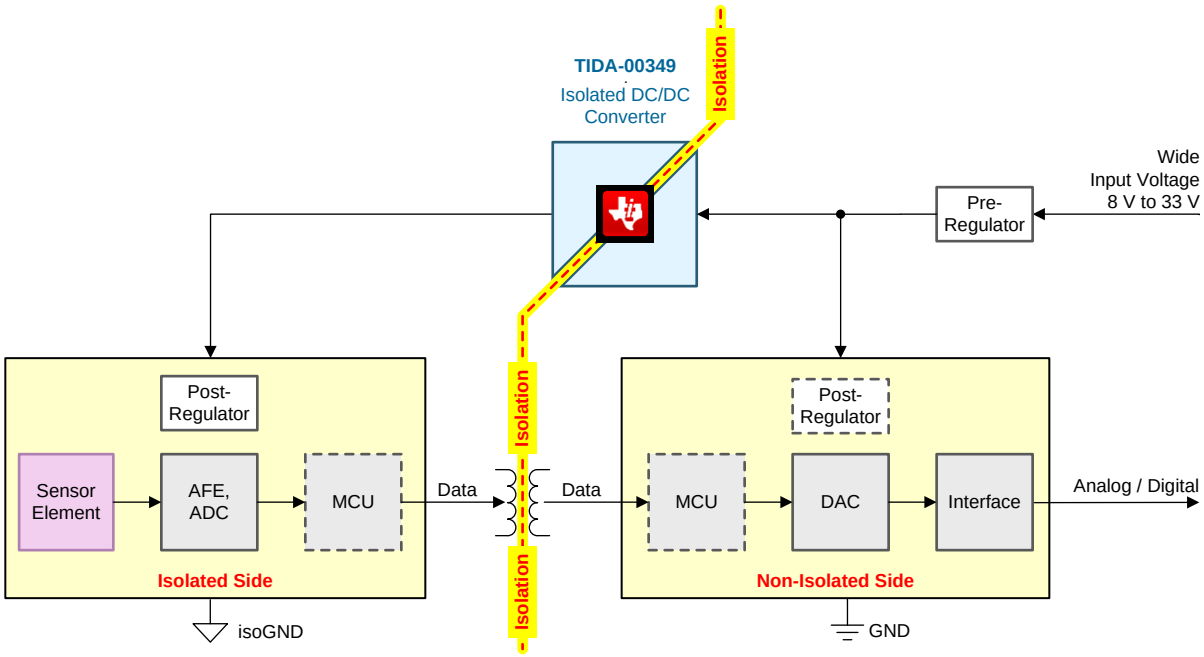


Figure 1. TIDA-00349 Used in Typical Sensor Transmitter System

While solutions for high efficiency isolated DC/DC converters addressing an output power range above hundreds of milliwatts are already available [1], the TIDA-00349 reference design is able to achieve a uniquely high power conversion efficiency even at much lower output power levels, ranging from some tens of milliwatts down into the sub-milliwatt range. This efficiency allows applications with limited input power budgets to benefit greatly from this design, such as loop powered 4- to 20-mA transmitters or bus powered applications where the bus power is limited.

Figure 1 shows a typical sensor transmitter application where the TIDA-00349 device powers the signal conditioning and signal processing of the isolated side. A pre-regulated voltage powers the TIDA-00349 to enable its use in systems that are powered from higher voltages than the targeted 3- to 5.2-V input voltage range of this reference design.

3 Design Features

Table 1 shows the specifications and features of the TIDA-00349 reference design.

Table 1. Key System Specification

PARAMETERS		SPECIFICATIONS AND FEATURES
Input	Nominal input voltage range	3- to 5.2-V DC
	Maximum input current (V_{IN} = 5.2 V; I_{OUT} = 10 mA)	< 14 mA
Output[1]	Output voltage[2] / Efficiency[2]	
	V_{IN} = 3 V; TA = 25°C, I_{OUT} = 100 µA	3.28 V / 54%
	I_{OUT} = 1 mA	3.18 V / 80%
	I_{OUT} = 10 mA	2.83 V / 76%
	V_{IN} = 5.2 V; TA = 25°C, I_{OUT} = 100 µA	6.04 V / 42%
	I_{OUT} = 1 mA	5.94 V / 81%
	I_{OUT} = 10 mA	5.60 V / 85%
General	Type of converter	Half-bridge on primary Voltage doubler on secondary
	Loop control	Open-loop, optocoupler-less
	Switching frequency	60 kHz
	Transformer insulation dielectric	Functional 1500-V AC 1 min 1875-V AC 1 sec
Environment	Temperature range	−40 °C to +85 °C
PCB	Form factor (L x W)	55.9 mm x 25.4 mm
	Number of layers	Two layers, single-side populated

(1) Can be modified by changing turns ratio of transformer
(2) Values are typical

4 Block Diagram

Figure 2 shows the block diagram of the design. The block diagram shows a half bridge driving the primary winding of the transformer on the non-isolated side and a voltage doubler circuit on the isolated side. Each side has a dedicated ground (GND on the non-isolated side, isoGND on the isolated side). Furthermore, the output header (J1) of the isolated side provides a dedicated pin (FSW). The switching frequency is available on that dedicated pin for test purposes or for synchronizing other system parts to the fixed switching frequency of the half-bridge.

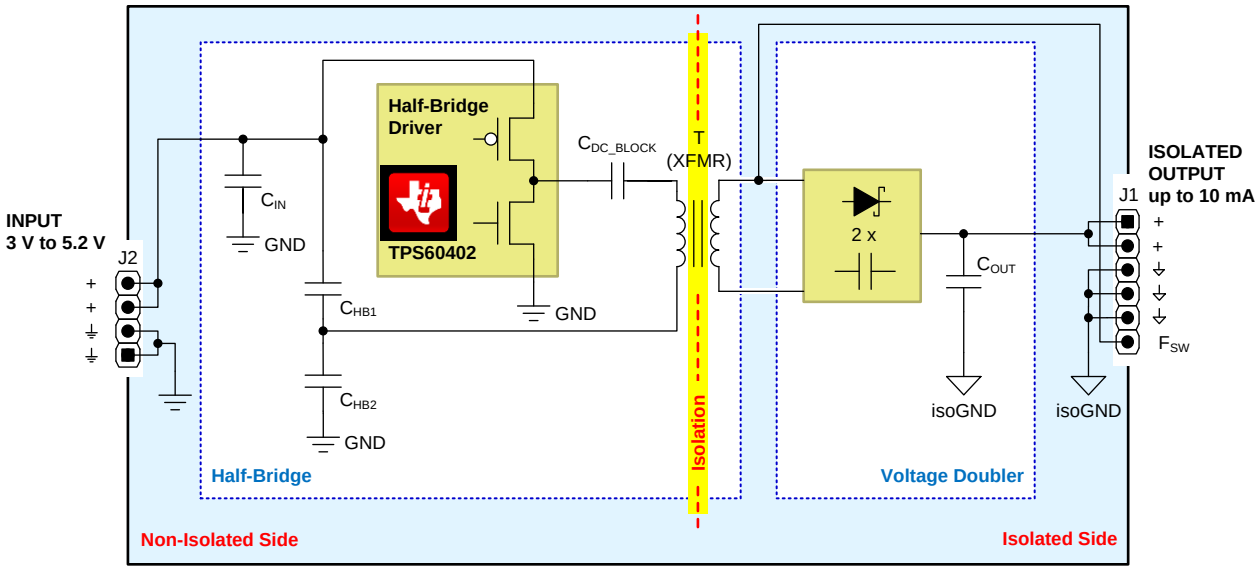


Figure 2. TIDA-00349 Block Diagram

Half-bridge circuit:

To best utilize the transformer and to achieve a high efficiency, this reference design uses an open-loop control approach to drive the primary side of the transformer with a fixed 50% duty cycle in both directions of the hysteresis curve of the core of the transformer. This open-loop control approach ensures that the isolated DC/DC converter is always working at an optimal operating condition—energy transfer from the primary to the secondary side of the transformer takes place over the full period of the switching frequency. As a result, the output voltage of the complete design depends on the input voltage and on the turns ratio of the windings of the transformer.

C_{IN} serves as an input bypass capacitor. C_{HB1} and C_{HB2} are the capacitors of the capacitive voltage divider, providing a fixed voltage of V_{IN} / 2 to one end of the primary winding of the transformer. The other end of the winding is driven by an integrated half-bridge stage inside the half-bridge driver. A dedicated capacitor, C_{DC_BLOCK}, blocks any DC voltage on the primary winding that might otherwise cause flux walking and saturation of the transformer core. The transformer T is the main passive component of the design and provides the isolation between the primary (non-isolated) side and the secondary (isolated) side. The transformer construction determines the class of isolation, which is functional isolation in the case of this design.

Voltage doubler:

This reference design uses a voltage doubler on the isolated side because, in a half-bridge topology, the voltage applied across the primary winding of the transformer is only V_{IN} / 2. Use of the voltage doubler is also intended to simplify the transformer design by using a minimum number of turns. The voltage doubler consists of two Schottky diodes and two capacitors. Each of those two capacitors is charged to the peak of the voltage of the secondary winding and then added together up to twice the value of the secondary winding voltage by the output capacitor C_{OUT}. The voltage losses caused by the two Schottky diodes are compensated by the turns ratio of the transformer windings.

The circuit blocks are easy to identify in the PCB assembly view (Figure 3).

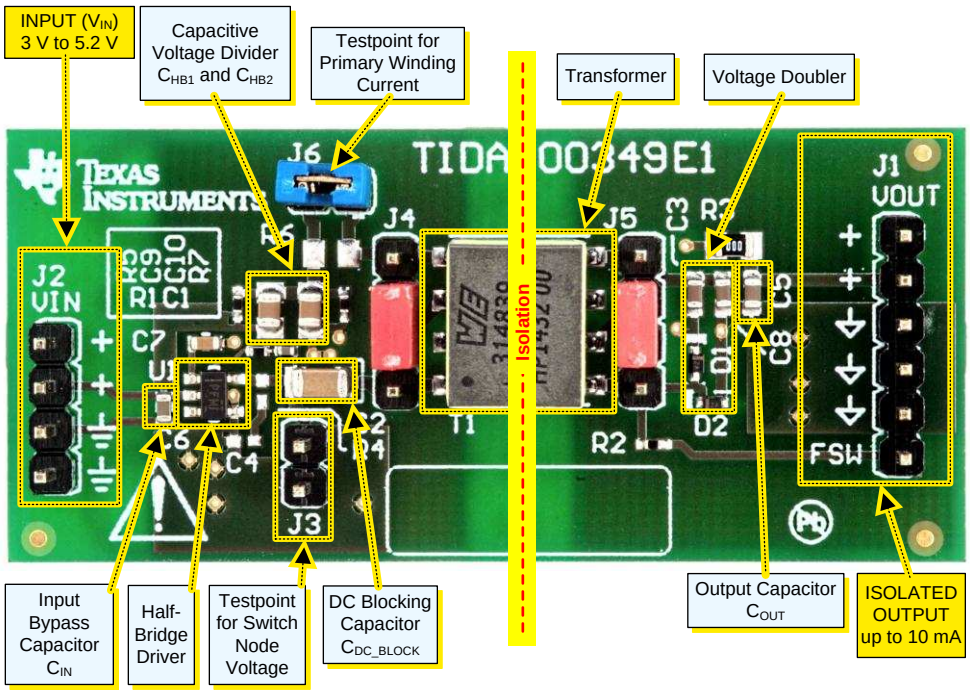


Figure 3. TIDA-00349 PCB Assembly View

5 Circuit Design and Component Selection

The following subsections describe the details of the main blocks of the TIDA-00349 design. Beside the technical descriptions, these sections provide an in-depth view into the design challenges and an explanation of the component selection process.

5.1 General Design Challenges for the Complete Design

Although there are countless converter ICs, transformers, MOSFETs, diodes, and different power topologies available [2], their usage is very limited for the specific case of low and ultra-low output power that this design targets. All of the different power solutions can cover output-power ranges from some hundreds of milliwatts up to a figure in the kilowatts, in theory.

However, the extreme low-power level of this design requires a new, more focused approach when it comes to achieving high power conversion efficiency levels. Even small losses must be considered, as they reduce the achievable efficiency significantly, especially at a very-low output power level. Taking an example of a 5-V input operation and a hypothetical no-load quiescent current of 100 µA, the resulting 500 µW can be considered a no-load power loss.

Also, if a 500-µW load is present at the output of the isolated DC/DC converter, additional load dependent losses must be added to the 500-µW no-load power loss. This process results in driving the efficiency further below the 50% point, which Figure 4 shows for a 500-µW output power and 500-µW loss case.

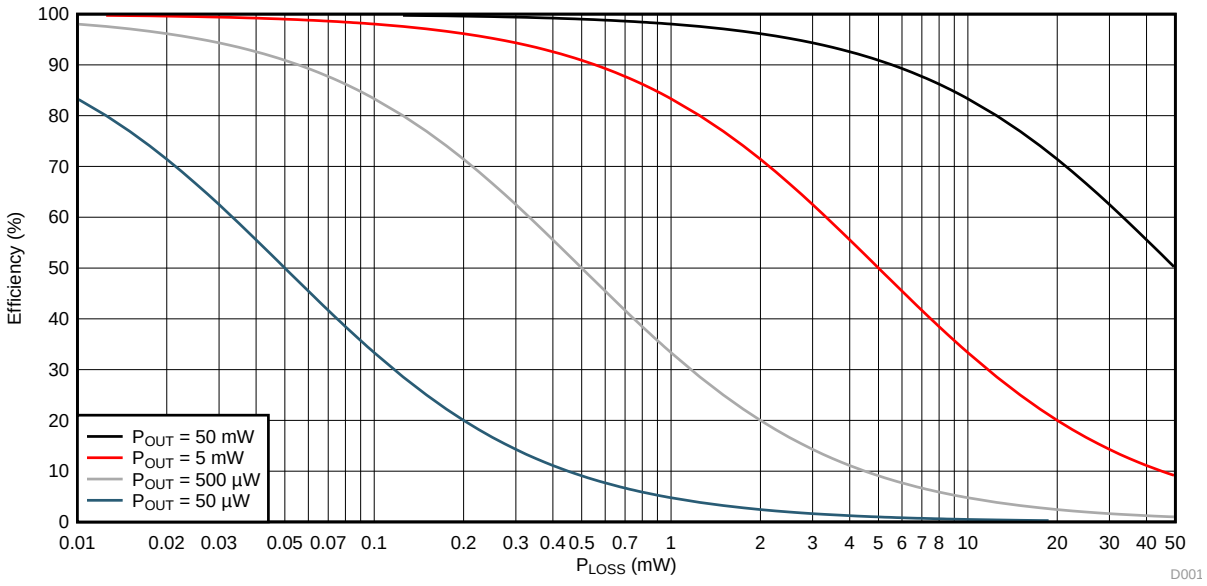


Figure 4. Efficiency at Different Output Power and Power Loss Levels

Reducing the different kinds of losses is one of the key objectives in this design. To name just some of those losses:

- Forward voltage (V_F) of diodes on the secondary side—especially critical in low output voltage applications when operating at low temperatures
- Reverse current of diodes on the secondary side—especially important in ultra-low power applications when operating at high temperatures
- Frequency-dependent switching losses—rising up proportionally with switching frequency
- Load-dependent conduction losses—important to consider at high output currents
- Magnetizing current—independent of load current but might exceed the load current, especially in ultra-low power applications (causes additional load-independent conduction losses)
- Core losses—increases with switching frequency

Besides focusing on minimizing the losses, other challenges to the designs are:

- The transformer saturation current and the V-µs limits must not be exceeded (see Figure 10)
- The use of a constant switching frequency over all load conditions to minimize negative impact on the accuracy and performance of systems that are sensitive to noise and switching frequency changes

Taking all of these challenges into account, the final solution is a compromise between size and efficiency. Therefore, simply assuming that the ultra-small output power automatically enables ultra-small transformers does not work.

5.2 Isolated DC/DC Converter—Selection of Control Approach

Section 3 already provides the basic control approach as an open-loop, optocoupler-less isolated DC/DC converter. In this design, open-loop isolated DC/DC conversion means that a known and stable DC input voltage is simply converted into an isolated DC output voltage without any control loop.

Figure 5 and Table 2 provide an in-depth comparison of open-loop control versus regulated DC/DC converters. Table 2 highlights the advantages of each approach using the green colored cells.

While regulated converters can be directly powered from a non-regulated power rail, open-loop converters require pre-regulation unless a stable power rail is already available in the system. Similarly, open-loop converters require post regulation in all cases where the load requires a stable voltage independent of input voltage or significant output current changes.

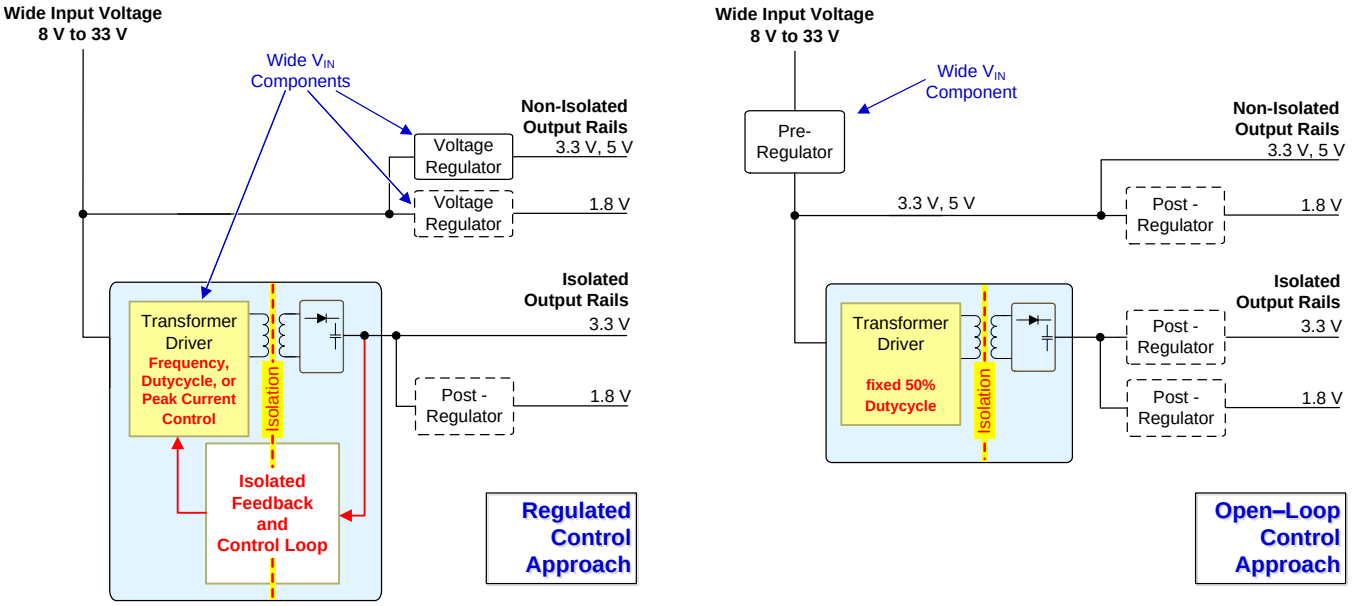


Figure 5. Regulated Versus Open-Loop Isolated DC/DC Converters and Their Impact on the Complete System Design

Open-loop converters operate their power stage with a fixed duty cycle, mostly 50%. Therefore there is a more or less continuous power transfer from the primary to the secondary side over the complete switching period, especially when the open-loop control is complemented with the use of double ended power topologies. This approach enables optimization of the power stage design to this known operating point and provides therefore the most efficient power transfer from the primary to the secondary side. In addition it helps to reduce the input ripple current which leads to less EMI. Because open-loop converters are usually powered off a constant input voltage, their EMI signature changes only with their load condition but do not depend on input voltage changes of the system's variable input voltage.

Because there is no control loop, designing open-loop converters is simpler, as there is no concern to loop stability. The fact that any increase or decrease of input voltage leads to an increase or decrease in input current means that the incremental input impedance of open-loop converters is positive; whereas the incremental input impedance is negative for any regulated DC/DC converters. The negative impedance of regulated converters requires special care to ensure loop stability when designing input ripple filters or

when using cascades of regulated converters. On the other hand, regulated converters provide a stable output voltage, which can be considered to be independent of the input voltage and the output current. However, open-loop converters provide an output voltage that shows a clear dependency on the input voltage. This output voltage is based on the fixed duty cycle used so that the voltage conversion ratio is mainly a function of the transformer winding ratio. Additionally, there are minor load and temperature-dependent influences of the output voltage in open-loop converters due to the voltage losses in the output rectifiers (diodes), switches (MOSFETs), and copper resistance of the windings. The load-dependent losses in the switches and in the copper resistance of the windings can be neglected, especially for the low-current ranges applicable to this design.

After considering the pros and cons of the two control approaches, the open-loop approach was selected for this design.

Table 2. Control Approach for Isolated DC/DC Converters

#	CHARACTERISTIC	REGULATED	OPEN-LOOP
1	Input voltage	Can vary over a wider range	Must be stable or within a narrow range
2	Output voltage	Stable, not a function of V_{IN} and I_{OUT}	Function of V_{IN}, additional minor dependency on I_{OUT}
3	Isolated feedback and control loop needed?	Yes	—
4	Variable control parameter	Switching frequency, duty cycle, or peak current	—
5	Stability of optimum operating point	V_{IN} and I_{OUT} change operating point	Always works at optimum operating point
6	Incremental input impedance	Negative	Positive
7	Loop stability concerns	Yes	—
8	Input current ripple	High; magnitude depends on V_{IN} and I_{OUT}	Lower; magnitude depends on I_{OUT} only
9	EMI signature (conducted EMI)	Depends on V_{IN} and I_{OUT}	Depends on I_{OUT} only
10	Post regulator	—	A post regulator is required when V_{OUT} must be stable and when the requirement that V_{OUT} must be independent of V_{IN} and I_{OUT} exists

5.3 Isolated DC/DC Converter—Selection of Power Topology

With the decision for the control approach having been made, the user can select the best-fitting topology for the isolated power stage of the DC/DC converter. The selection process considers not only the features of the different topologies, but also the available DC/DC converter ICs for the respective topology to be selected.

Isolated DC/DC converters can generally be grouped into either single-ended or double-ended topologies, depending on the use of the B-H curve of the transformer core [3].

Figure 6 shows the basic **single-ended topologies**. In the single-ended topologies, such as those used in forward or flyback converters, the magnetic flux swings in only one quadrant of the B-H curve, underutilizing the core.

To avoid the saturation of the transformer core, the standard **forward converter** requires a transformer that must have an extra reset-winding alongside the standard primary and secondary transformer windings (N_P and N_S). The purpose of this extra reset winding and the diode (D3) is to bring the magnetic flux back after each switching period to the value where the magnetic flux started. Furthermore, the ON-time is limited to less than 50% of the total switching period. The ON–time is the time during which the primary switch (MOSFET Q1) is ON and energy transfers from the primary side to the secondary side. - An additional storage inductor (L) is used as a magnetic storage element, providing a current to the output capacitor and the load through the freewheeling diode (D2) even during the OFF-time of Q1.

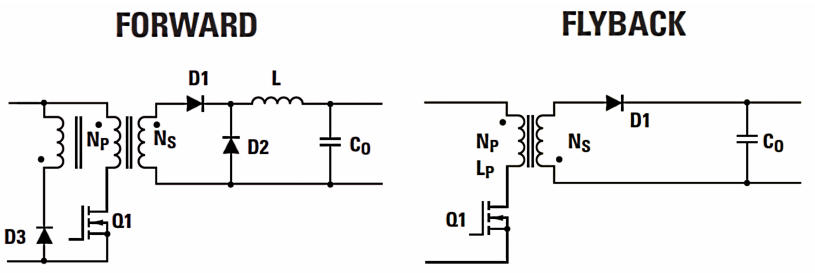


Figure 6. Basic Single-Ended Topologies

Flyback converters store energy in the air-gap of the core and, therefore, require a specific minimum core size of the transformer. The flyback “transformer” itself is not a real transformer and is a misnomer. A more accurate expression for the flyback transformer is “coupled inductors”. There is no direct or instantaneous energy transfer from the primary to the secondary side, as with the forward topology. During the ON-time of Q1 the energy stores in the air gap of the core of the coupled inductors by the current flow in the primary winding (N_P) of the flyback topology. This stored energy then releases to the output through the secondary winding (N_S) and the diode (D1). This process of energy transfer starts immediately when Q1 is switched OFF and continues until the secondary winding current has fallen to zero. The secondary winding current charges the output capacitor C_O and directly provides a current to the load during this time interval. The output capacitor C_O is partially discharged by the load at all other time intervals due to the missing direct energy transfer from the primary to the secondary side. The flyback is based on two energy storage elements: storing magnetic energy in the air gap of the magnetic core and further using the output capacitor as a capacitive storage element.

The forward topology and the flyback topology draw current during the ON-time of their switch (Q1) only; as a result, the forward and flyback topologies have a higher input ripple current and an increased RMS-current when compared with the double-ended topologies.

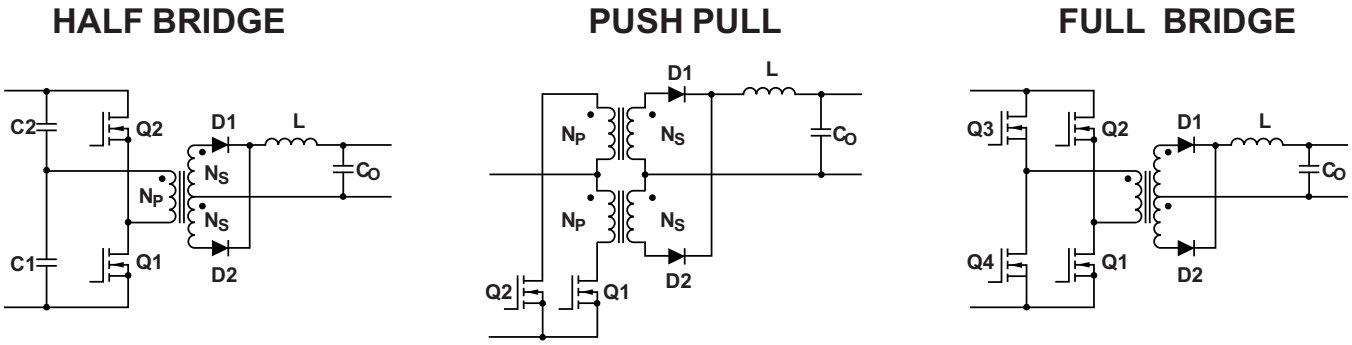


Figure 7. Basic Double-Ended Topologies

By using one of the **double-ended topologies** that Figure 7 show, the user can expect a better efficiency.

The double-ended topologies in Figure 7 derive from the previously mentioned forward converter, involving a direct energy transfer from the primary to the secondary side during the ON-time of the switches (Q1 to Q4). There is no storage of magnetic energy in the transformer as is mandatory for the basic operation of the flyback.

The double-ended topologies actively drive the core of the transformer in two opposite directions, ensuring the full and best utilization of the transformer core. The bi-directional drive of the core also provides an easy method for demagnetizing the core, making an extra reset-winding no longer necessary (as is the case with the standard forward topology). Driving the switches of the double-ended topologies with a fixed 50% duty cycle—as intended in open-loop converters—forces the input and output currents to be continuous over the total switching period, showing a lower ripple and lower RMS current when compared with the single-ended topologies.

Due to the advantages of the double-ended topologies, the aforementioned single-ended topologies were not further considered for the selection process. Likewise, the advanced double-ended topologies such as the full bridge were not considered due to the increased complexity level and the requirement to drive four switches, which leads to an increase in switching losses.

The half-bridge and the push-pull are selected last for a more detailed investigation. The storage inductor (L) on the secondary is considered to be superfluous (further simplifying the topologies) because of the continuous current flow when operated as open-loop converters, controlling the switches (Q1 and Q2) with a fixed 50% duty cycle.

Running with a 50% duty cycle is commonly used in low-power, isolated, non-regulated DC/DC converters like the ones based on the SN6501 device [1], which is optimized for an output power efficiency in the range of tens of milliwatts up to 1 W, as Figure 8 shows.

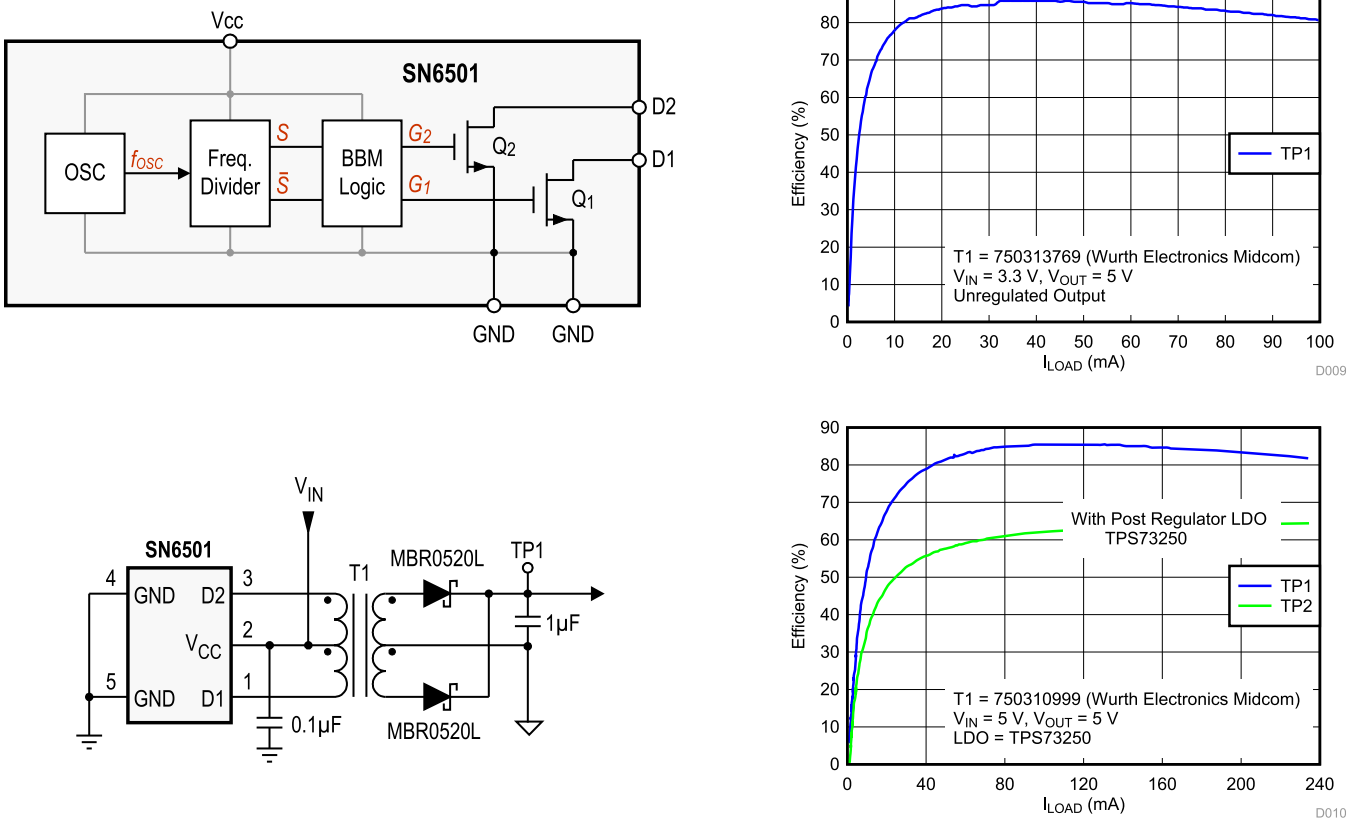


Figure 8. SN6501 Device—Block Diagram, Schematic, and Efficiency

Although the omission of a storage inductor on the secondary side simplifies the design in general, the greater design challenge is the power transformer itself. The symbol of the transformer in schematics appears to be as simple as the ideal transformer (Figure 9); however, a simplified model of a real transformer shows additional components that comprise each real transformer.

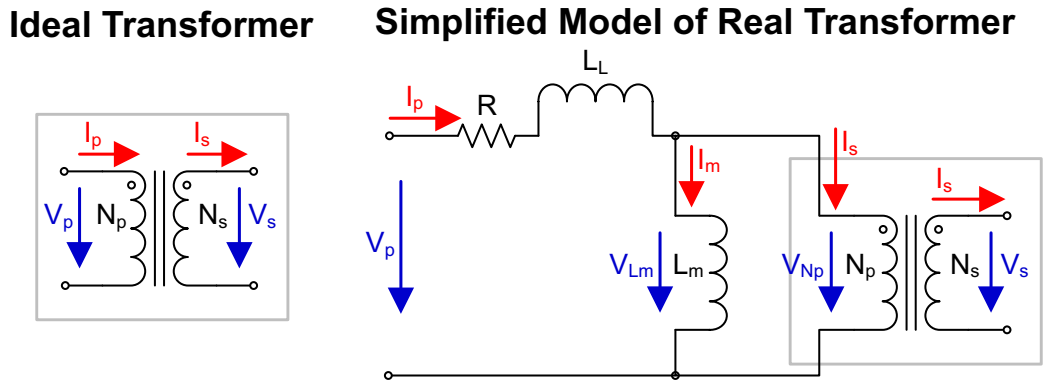


Figure 9. Ideal Transformer Versus Simplified Model of Real Transformer

The basic equations describing an **ideal transformer** are simple, well known, and understood. In the simplest case, an ideal transformer consists only of one primary and one secondary winding. Each winding has a respective number of turns and is linked by a magnetic core together. As a result, the turns ratio (n) can be calculated.

$$n = \frac{N_p}{N_s}$$

where

- n is the primary-to-secondary turns ratio
- N_p is the number of primary turns
- N_s is the number of secondary turns

(1)

The turns ratio does not only define the relation between the number of turns of the two windings, but also defines the relation of the related voltages and currents.

$$n = \frac{N_p}{N_s} = \frac{V_p}{V_s} = \frac{I_s}{I_p}$$

where

- V_p is the voltage across the primary winding
- V_s is the voltage across the secondary winding
- I_p is the current through the primary winding
- I_s is the current through the secondary winding

(2)

This can be rearranged to get the most important relations.

$$\frac{V_p}{V_s} = \frac{N_p}{N_s} = n$$

(3)

The ratio of the voltages on both sides equals the ratio of the number of turns of the respective windings.

$$\frac{I_p}{I_s} = \frac{N_s}{N_p} = \frac{1}{n}$$

(4)

The ratio of the currents on both sides equals the reverse ratio of the number of turns of the respective windings.

The normal use case of a transformer assumes that a voltage V_p is applied to the primary side and appears multiplied by 1/n on the secondary side as the voltage V_s.

$$V_s = \frac{V_p}{n}$$

(5)

The current I_s drawn by a load on the secondary side appears multiplied by 1/n on the primary side as the current I_S' , which is called the *reflected current from the secondary*.

$$I_s' = \frac{I_s}{n} \tag{6}$$

Therefore, the current through the primary winding of a **real transformer** is the sum of the reflected current from the secondary side and the current of the magnetizing inductance of the primary-side winding.

$$I_p = I_s' + I_m \tag{7}$$

Note that using Equation 1 for the calculation of the turns ratio n (as used in this document) is only one possible way to define the turns ratio. Some literature defines the turns ratio to the exact contrary, as a secondary-to-primary turns ratio.

NOTE: Equation 2 through Equation 7 are valid for the AC signals and an ideal transformer only. This validity corresponds with the common knowledge that a transformer does not work with a DC whatsoever. The questions regarding the borderline between AC and DC forces a more detailed look into a simplified model of a real transformer.

The ideal transformer can thoroughly explain the ratio between voltages, currents, and number of turns on the primary and secondary side. However, the ideal transformer is missing the explanation of the inductive behavior which needs to be expected from practical experience, whenever a number of turns are wound, especially on a magnetic core.

An explanation of the inductive behavior comes with the simplified model of the real transformer, which takes the described ideal transformer and adds the magnetizing inductance L_m.

Since the design of a real transformer aims at keeping the other added components like the parasitic leakage inductance L_L orders of magnitude lower (compared to L_m), the effect of L_L can be neglected for the purpose of this discussion and for the sake of simplicity. The effect of the winding resistance R shown in series to L_L on the primary side can also be neglected for the purpose of this discussion.

The simplified model of the real transformer shows the magnetizing inductance L_m connected in parallel to the primary winding of the ideal transformer block. In this configuration, L_m represents the inductive properties of the primary winding wound on a magnetic core of specific dimensions and with specific magnetic properties. L_m can be calculated according to Equation 8 or Equation 10 and can be measured on the primary winding of the real transformer if the secondary winding is disconnected.

$$L_m = \frac{\mu \times A_C \times N_p^2}{l_C} \tag{8}$$

with

$$\mu = \mu_0 \times \mu_r \tag{9}$$

Core manufacturers often combine all the magnetics and mechanical size-related properties into a single term called A_L value or *inductance factor* to simplify the calculation to Equation 10.

$$L_m = A_L \times N_p^2 \tag{10}$$

A_L needs to be

$$A_L = \frac{\mu \times A_C}{l_C} \tag{11}$$

Due to Equation 8 and Equation 11 where

- L_m = magnetizing inductance
- μ = core permeability
- μ_0 = permeability of free space = $4\pi \times 10^{-7}$ H/m
- μ_r = relative permeability of core material
- A_C = core cross section
- l_C = core magnetic path length
- A_L = inductance factor or A_L–value (12)

The core links the primary and secondary winding together, and the magnetizing inductance models the magnetization of the core *as a real, physical inductor*. Unfortunately, the magnetizing inductance shows undesirable characteristics of inductors—saturation and hysteresis—as well (Fundamentals of Power Electronics). Both characteristics are represented by the hysteresis curve of the magnetizing inductance. The hysteresis causes hysteretic losses, while the saturation places a limit for the maximum current flow through the inductor or for the applied product of volt-seconds (V-s) to that inductor, respectively.

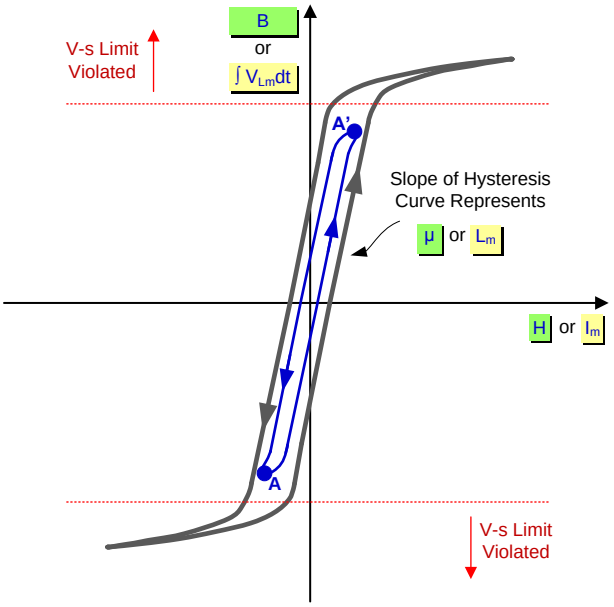


Figure 10. Hysteresis Curve of Ferrite and of Specific Inductor

The gray hysteresis curve in Figure 10 is also known as the B-H curve and is used to characterize the core material itself. The slope of the curve represents the permeability, μ in this case. Applying the "Transformation of Axes" as described [5] in Section 1 of the Magnetics Design Handbook, the vertical axis can also be used for the V-s applied to a specific inductor when the horizontal axis is used for the current flowing through this specific inductor. This specific inductor is in this case the magnetizing inductance L_m of the transformer and is then represented by the slope of the hysteresis curve as well. The horizontal axis is then specifically showing the magnetizing current I_m.

The blue curve is representing the so-called *minor loop* that is the practical range of excursion used in real applications.

If the applied V-s product (or the flux-density B) violates a certain limit (the red dotted lines), then the slope changes from a linear to a nonlinear behavior. Any further increase in the applied V-s will cause a drastic increase of the magnetizing current. The inductive characteristic diminishes, leaving finally, only the copper resistance of the winding. A drastic increase of the magnetizing current also causes shorting of the primary side of the ideal transformer block used in the simplified model of the real transformer. Any voltage applied to the magnetizing inductance can cause such an effect, no matter how small. The question is just how long the voltage is applied. This information explains why transformers can work for AC signals only, but not for DC signals.

Even AC signals can cause this effect if the AC signals violate the V-s limit of the specific inductor. Such a violation can happen, if the magnitude of the voltage is too large or the time the voltage is applied is too long (for example, when operated at low frequency). The violation can also happen if the AC signal has a DC voltage superimposed. To avoid this situation, the V-s applied to an inductor (or to the flux in the core) needs to be balanced. Therefore, any positive V-s excursion in one direction needs to be cancelled out by exactly the same excursion in the opposite direction. Otherwise, the so-called *flux walking* can happen. Flux walking can drive the core earlier or later into saturation.

The high efficiency goal for the design of the isolated DC/DC includes the need of a low switching frequency to minimize the switching losses. With low switching frequency, any voltage on the primary winding of the transformer is applied for a longer time (compared to using a higher switching frequency). Therefore, the power topology applying the lower voltage to the primary winding of the transformer — the half-bridge topology — was selected. Table 3 provides further details.

The applied voltage for the half bridge is exactly one half of the voltage, which would be applied using a push-pull topology. Furthermore, the half bridge is providing another simple measure to avoid flux imbalance and flux walking, simply by the use of a DC-blocking capacitor. Additionally, the half bridge eases the transformer design. On the primary side, there is only a standard single winding needed versus a tapped winding as needed with a push-pull transformer. The single winding of the half bridge is used 100% of the time. In contrast, each one of the two halves of the primary winding of the push-pull is used only 50% of the time.

Table 3. Isolated DC/DC—Selection of Power Topology

PARAMETER	PUSH-PULL	HALF-BRIDGE
Voltage stress of primary side switches	2 x V_{IN}	V_{IN}
Voltage across primary winding	V_{IN}	V_{IN} / 2
Relative V-µs (Referred to push-pull, same switching frequency, same ON-time)	1	0.5
Core utilization	Bi-directional (double-ended)	Bi-directional (double-ended)
Structure of primary winding	Center tapped winding	Standard single winding
Structure of secondary winding	Usually center tapped winding	Standard single winding
Copper utilization	50%	100%
Avoidance of flux imbalance	Positive temperature coefficient of the MOSFET RDSon	Positive temperature coefficient of the MOSFET RDSon
		DC blocking capacitor

5.4 Isolated DC/DC Converter—Selection of Transformer Driver

Special care was taken for the selection of the best-suited device for driving the power transformer.

Key Specifications for Selecting a Transformer Driver

- High efficiency
  - *Low-switching frequency* is a prerequisite to ensure lowest switching losses. However, the disadvantage comes when avoiding violation of the V-s limit of the transformer, while at the same time, trying to achieve the smallest solution size. This disadvantage is related to the inductance values of the transformer, which will rise with a low-switching frequency, which can directly be translated into larger physical transformer size. The same size relation applies to the capacitors needed on the input and output of the isolated power stage. However, the size impact for the capacitors is not as severe as the size impact for the transformer. There is a cost impact when trying to obtain the same physically-sized capacitor with a much larger capacitor value. A tradeoff between efficiency and solution size needs to be found.
  - *Low quiescent current (Iq)*: Due to the low output power level, the current consumption of the converter itself has a major influence on the efficiency.
- *High integration level*: needed for smallest size solution. The integration of the switches (FETs) is highly desirable.
- *Fixed switching frequency*: preferable from a noise and system accuracy perspective. The standard approach of operating the DC/DC converter in a PFM-, SKIP- or BURST-mode to achieve highest efficiency at the needed low output power level (from 5 to 10 mW) is not desirable. The result would be a mix of different frequencies, which is directly opposite of the goal of best-system accuracy performance.

After taking into account all the specifications need for a device driving the power transformer, the TPS60400 family, as shown in Figure 11, was selected.

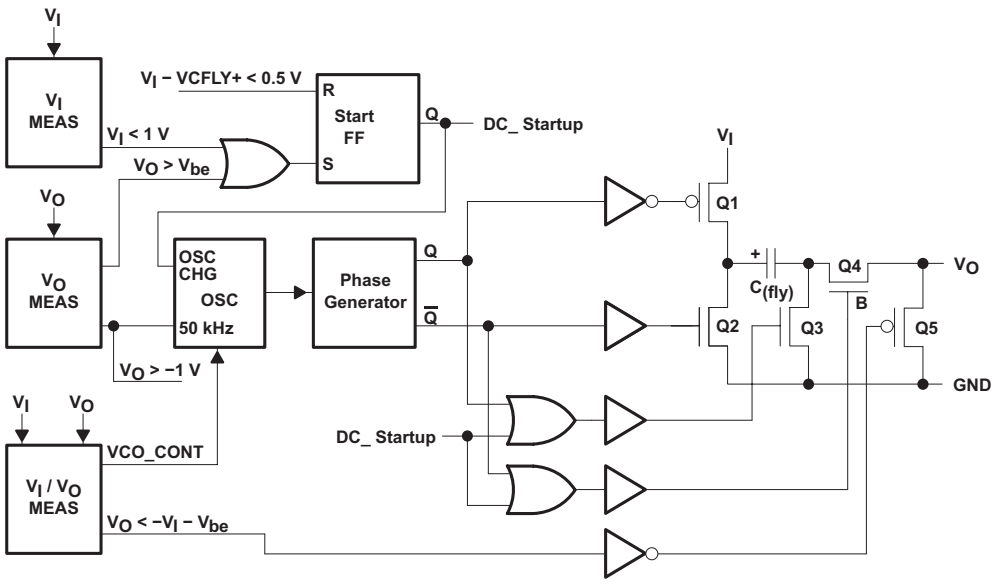


Figure 11. TPS60400 Family—Functional Block Diagram

The primary applicable and beneficial specifications of the TPS60400 device family can be summarized as follows:

- Input voltage range from 1.6 V to 5.5 V
- Small 5-pin SOT23 package
- Integrated switches (FETs)
- Internal fixed frequency oscillator (for TPS60401 to TPS60403)
- Multiple switching frequency versions, as shown in Table 4
- Devices available with quiescent current down to 65 μA

Table 4. TPS60400 Family—Device Versions

PARAMETER	TPS60400	TPS60401	TPS60402	TPS60403
Switching frequency (typ)	Variable switching frequency 50 kHz to 250 kHz	20 kHz	50 kHz	250 kHz
Quiescent current (typ)	125 µA	65 µA	120 µA	425 µA

The TPS60402 was selected from the TPS60400 family. With a 50-kHz switching frequency, the TPS60402 offers a good trade-off between efficiency and solution size.

5.5 Isolated DC/DC Converter—Further Device Selection and Circuit Implementation

Figure 12 shows how the internal circuitry of U1 (TPS60402) is used to drive a half-bridge transformer (T1).

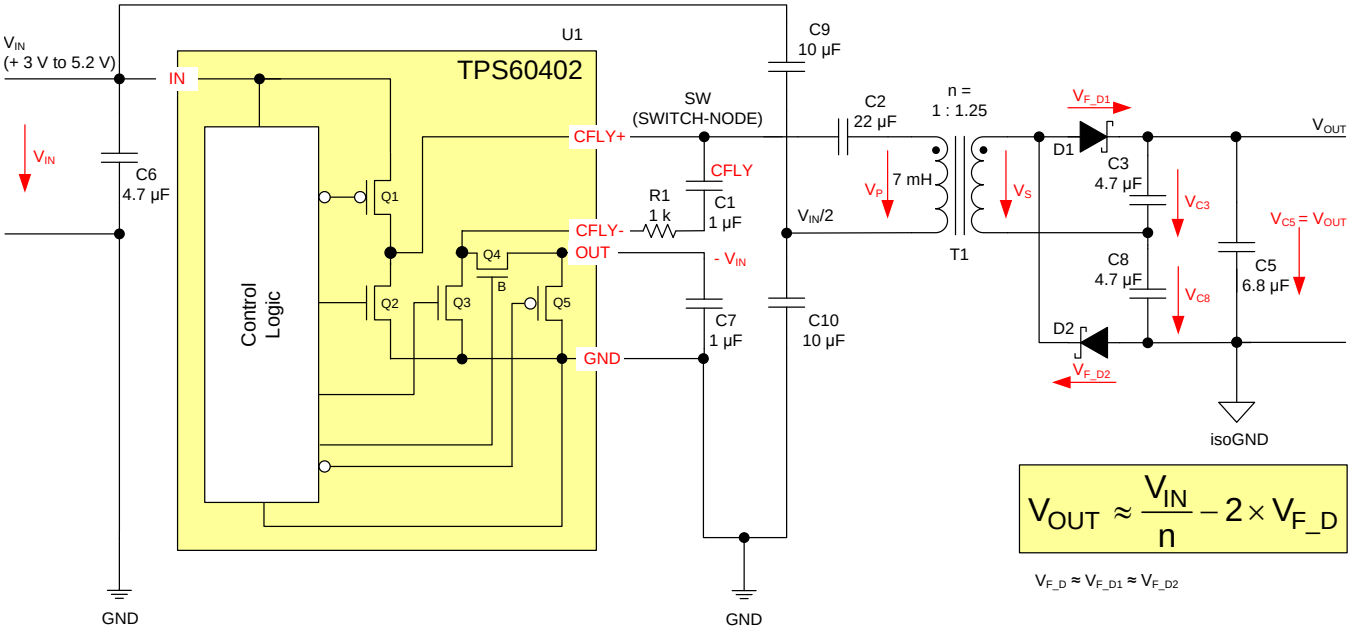


Figure 12. Simplified Schematic of Isolated DC/DC Converter

The switches (MOSFETs) Q1 and Q2 of the TPS60402 form one leg (the left leg) of the bridge. Q1 and Q2 drive the dot end of the transformer T1 primary winding through the CFLY+ pin (SWITCH-NODE SW) and the DC-current blocking capacitor C2 with a square-wave-like voltage. Both MOSFETs are switched ON alternately. Each MOSFET is ON for almost 50% of the period T. The basic operation of this circuitry can be divided into two main time intervals with identical length. Table 5 describes the state of the switches, diodes, and the direction of the magnetic excursion in the core of the transformer during each of the intervals.

Table 5. Half Bridge DC/DC Converter—State of Switches and Diodes During Each Time Interval

TIME INTERVAL	Q1	Q2	Q3	Q4	VP	D1	D2	CORE DRIVE
1	On	Off	On	Off	$V_{IN} - V_{IN} / 2$	On	Off	A to A’
2	Off	On	Off	On	$-V_{IN} / 2$	Off	On	A’ to A

The core drive represents the magnetic excursion and refers to the blue line and blue dots A and A', highlighting the minor loop in Figure 10.

A short dead time between the two time intervals prohibits cross conduction, respectively the shoot-through of Q1 and Q2. The voltage level on the CFLY+ pin toggles between 0 V (GND) and V_{IN}.

Q3, Q4, CFLY (C1), and C7 complement Q1 and Q2 to eventually form an inverting charge pump circuit, which is the conventional use of the TPS60402 device. Q3, Q4, CFLY (C1), and C7 are not required to drive the half-bridge transformer, but are required to satisfy the standard operating conditions of the TPS60402. The TPS60402 device requires a negative voltage on its OUT pin, which requires the circuitry connected to the device to be complete, as in the typical application of the device. However, the capacitors have been minimized in value, eventually resulting in an increased output voltage ripple on the OUT-pin of the device U1. This increased ripple is acceptable because this voltage is the negative voltage not used in the design.

Resistor R1 is connected in series to the flying capacitor C1, significantly reducing the inrush current and the continuous operating losses for the generation of the unused negative voltage. Figure 13 shows the waveforms of the charge pump operation, simulated with TINA-TI™ software [6]. The brown curve shows the CFLY+ pin of the TPS60402 device, acting as the primary side switch-node (SW). The switch-node toggles with a duty cycle of 50% and a typical frequency of 60.8 kHz between the input voltage V_{IN} and GND (0 V), as the V_SW curve shows. The purple V_C7 curve shows the negative output voltage generated by the TPS60402, which is not further used by the complete circuitry of this design. The ripple voltage is in the range of 550 μV_{p-p} only. Similarly, the blue voltage V_C1 curve shows a ripple of roughly 500 μV_{p-p} across the flying capacitor (C1)

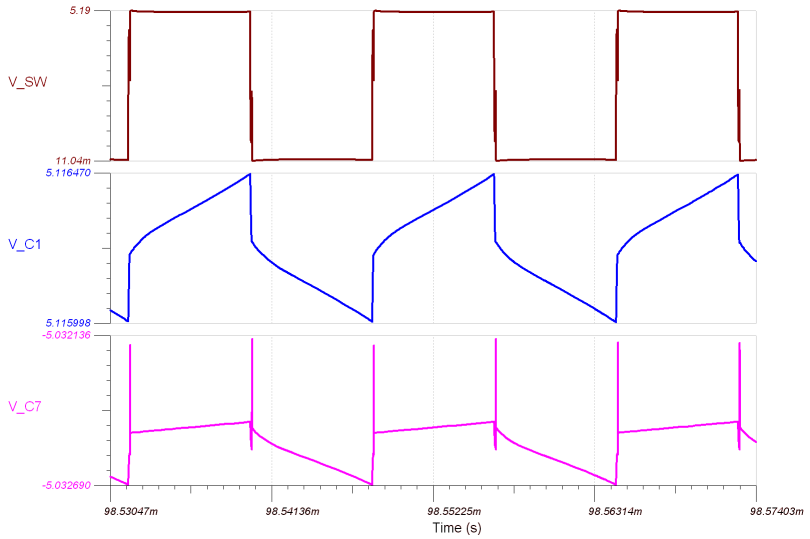


Figure 13. Charge Pump Waveforms for V_{IN} = 5.2 V and I_{OUT} = 10 mA

The other leg of the bridge is formed by C9 and C10, a capacitive voltage divider keeping the non-dot end of the primary winding of the transformer at a constant voltage of V_{IN} / 2. The resulting voltages $V_{p@1}$ and $V_{p@2}$ across the primary winding of the transformer during the two intervals can be calculated using Equation 13.

$$V_{P@1} = V_{IN} - \frac{V_{IN}}{2} = \frac{V_{IN}}{2}$$

$$V_{P@2} = -\frac{V_{IN}}{2}$$

where

- $V_{p@1}$ is the voltage across the primary winding during time interval 1
- $V_{p@2}$ is the voltage across the primary winding during time interval 2 (13)

The equations for calculating the voltages on the secondary side of the transformer derive from Equation 5.

$$V_{s@1} = \frac{V_{p@1}}{n}$$

$$V_{s@2} = \frac{V_{p@2}}{n}$$

where

- $V_{s@1}$ is the voltage across the secondary winding during time interval 1
- $V_{s@2}$ is the voltage across the secondary winding during time interval 2
- n is the primary-to-secondary turns ratio (14)

Depending on the time interval and the resulting polarity on the primary winding, the voltage on the secondary winding shows up with positive and negative polarity also. Therefore, during each of the time intervals, only one of the two diodes is biased in forward direction, whereas the other diode is reverse biased. The forward-biased diode peak rectifies the voltage of the secondary winding and charges the capacitors (C3 and C8) to their respective voltages.

$$V_{C3} = V_{S@1} - V_{F\_D1}$$

$$V_{C8} = -V_{S@2} - V_{F\_D2}$$

where

- V_{F_D1} is the forward voltage drop of the diode D1
- V_{F_D2} is the forward voltage drop of the diode D2 (15)

The sum of the two voltages is the output voltage, V_{OUT}, of this voltage-doubler circuitry. Calculate the V_{OUT} using Equation 13, Equation 14, and Equation 15.

$$V_{OUT} = V_{C5} = V_{C3} + V_{C8} \quad (16)$$

$$V_{OUT} = \left(\frac{V_{IN}}{2 \times n} - V_{F\_D1}\right) + \left(\frac{V_{IN}}{2 \times n} - V_{F\_D2}\right)$$

resulting under the assumption of (17)

$$V_{F\_D1} = V_{F\_D2} = V_{F\_D}$$

where

- V_{F_D} is the forward voltage drop of one of the diodes D1 or D2 used in the voltage doubler circuit (18)

The equation simplifies to Equation 19.

$$V_{OUT} = \frac{V_{IN}}{n} - 2 \times V_{F\_D} \quad (19)$$

5.5.1 Selection of Diodes and Transformer

The voltage stress across each diode is basically the voltage on the secondary winding at the time interval during which the respective diode is in reverse condition, in addition to the voltage on the respective capacitor (C3 or C8) of the voltage doubler.

The following equations show the required reverse voltage of diode D1 exemplarily.

$$V_{R\_D1} > \left|V_{s@2}\right| + V_{C3} \tag{20}$$

Utilizing Equation 15, Equation 20, and assuming that:

$$V_{C3} = V_{C8} = \frac{V_{OUT}}{2}$$

leads to (21)

$$V_{R\_D1} > (V_{C8} + V_{F\_D2}) + \frac{V_{OUT}}{2} = (\frac{V_{OUT}}{2} + V_{F\_D2}) + \frac{V_{OUT}}{2} = V_{OUT} + V_{F\_D2}$$

where

- V_{R_D1} is the minimum required reverse voltage of the diode D1 (22)

The equation can be commonly stated as:

$$V_{R\_D} > V_{OUT} + V_{F\_D}$$

where

- V_{R_D} is the minimum required reverse voltage of each of the diodes D1 and D2 used in the voltage doubler circuit (23)

In each case, the reverse voltage capability of the diodes selected must have additional margin added to this calculated parameter value.

The average forward current of each of the diodes equals the output current of the converter, leading to:

$$I_{F(AV)\_D} > I_{OUT}$$

where

- $I_{F(AV)\_D}$ is the minimum required average forward current of each diodes D1 and D2 used in the voltage doubler circuit (24)

Because each diode conducts for half of the total period only, consider the required peak current through each of the diodes to be slightly higher than:

$$I_{FRM\_D} > 2 \times I_{OUT}$$

where

- I_{FRM} is the minimum required repetitive peak forward current of each of the diodes used in the voltage doubler circuit (25)

The I_{FRM} specification of the diodes is not usually a limiting factor, because diodes can withstand much higher peak currents compared to their maximum rated average current, as given in the datasheets for diodes.

Figure 14 shows the waveforms, which represent the voltages across and the currents through the diodes based on a simulation with the TINA-TI software [6].

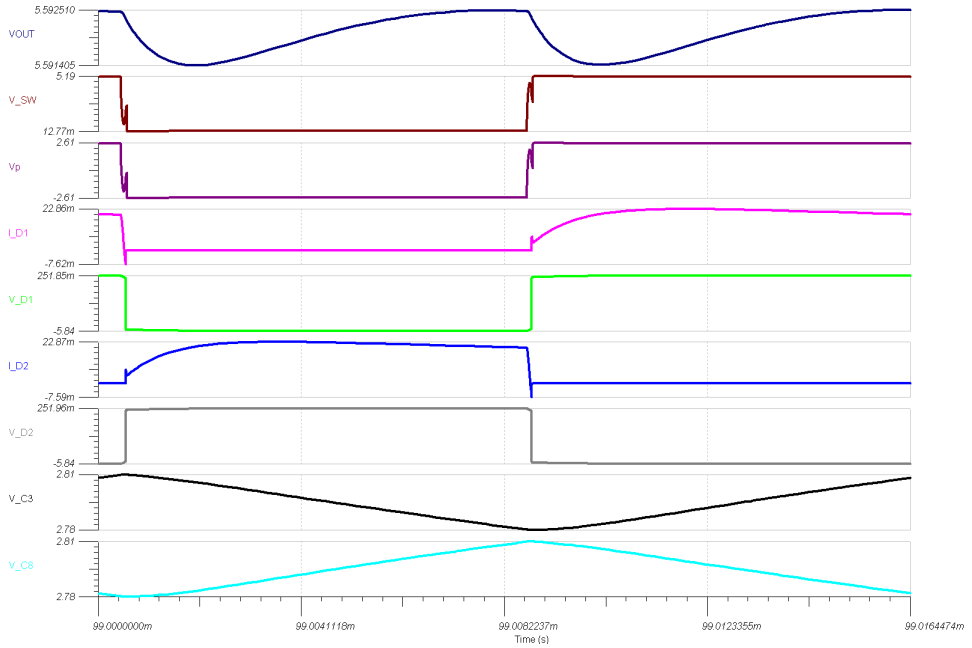


Figure 14. Waveforms of Diode Voltages and Diode Currents (D1 and D2) for V_{IN} = 5.2 V and I_{OUT} = 10 mA

Except for the very common selection parameters used in the previous Equation 23, Equation 24, Equation 25 using additional diode parameters must be taken into account during the complete diode selection process to maximize the efficiency of the isolated DC/DC converter.

These additional parameters are:

Forward voltage V_F at the respective forward current I_F

At the maximum load current the forward voltage drop of the diodes is the main loss contributor. Due to this fact, the forward voltage must be as low as possible at the respective forward current level. The peak forward current, which is slightly larger than twice the output current I_{OUT}, can be used for the purpose of simplicity (see Equation 25).

Silicon diodes generally do have a larger V_F (in the range of 750 mV at 25°C) compared to the forward voltage of Schottky diodes (about 350 mV at 25°C). Special considerations are required when operating at low temperatures; the V_F of both types of diodes has a negative temperature coefficient (TC), the V_F of silicon diodes increases roughly by 2 mV with each centigrade decrease in temperature (TC ≈ −2 mV/°C). Schottky diodes are given with roughly −1 mV/°C. These values are commonly known and used in the literature. Retrieve more accurate numbers out of the datasheets of specific diodes. The values of the temperature coefficient do not depend entirely on the type of diodes used, but also on the specific forward current at which the diodes are used.

There are two final important points to note related to this topic:

- Most of the parameters in the diode manufacturers' datasheets are specified at 25°C and are given as typical values only—the user must then approximate the specific values applicable for their respective application from the typical values given in the parametric tables and the different graphs provided. Gathering the specific values is especially important for the worst-case (min or max) values required to do a worst-case analysis for the design.
- Selecting diodes targeted for larger forward currents usually helps to reduce the forward voltage, but increases component size as well as diode capacitance and increases the reverse current.

Use Equation 26 for a rough estimation of the total conduction losses in both diodes.

$$P_{d\_Dconduction} \approx 2 \times V_{F\_D} \times I_{OUT} \quad (26)$$

where

- $P_{d\_D\ conduction}$ is the forward current based power dissipation in both diodes D1 and D2 together

For an assumed output current of 10 mA, assume a diode forward voltage of 430 mV (at −40°C, 20 mA), and the total resulting conduction losses of both diodes together is:

$$P_{d\_Dconduction} \approx 2 \times 430\ mV \times 10\ mA = 8.6\ mW \quad (27)$$

As Figure 4 shows, the approximated loss of almost 9 mW drives the ideal 100% efficiency of the isolated DC/DC converter down to 85%.

Reverse current I_R at the respective V_R

The I_R must be as small as possible at the reverse voltage, which is the sum of the DC/DC converter output voltage and the forward voltage (according to Equation 23). The reverse current is not a big concern for silicon diodes, but is a huge concern at high temperatures when using Schottky diodes. The reverse current of small Schottky diodes can easily go up to 100 µA at an applied reverse voltage of 5 V to 10 V and for temperatures in the range of 100°C, while silicon diodes can be in the range of 1 µA with the same conditions.

Equation 28 shows an approximation of the diode-based reverse current losses (Pd_D reverse) of the isolated DC/DC converter:

$$P_{d\_Dreverse} \approx (V_{OUT} + V_{F\_D}) \times I_{R\_D} \quad (28)$$

where

- $P_{d\_Dreverse}$ is the reverse current based power dissipation in both diodes D1 and D2 together
- I_{R_D} is the reverse current of the diodes D1 and D2 during the respective interval when the reverse voltage is applied to the diode. I_{R_D} does not show any output current dependency other than the dependency of V_{OUT} and the dependency of the forward voltage on the load current

For an assumed output voltage of 5 V and a diode forward voltage of 250 mV (at 100°C, 30 mA) the total resulting diode reverse current losses of both diodes together is based on an assumed 100 µA of reverse current at a reverse voltage of 5.25 V and at a temperature of 100°C. As Figure 4 shows, the approximate loss of 525 µW does not matter that much at an output power of 50 mW, but does significantly matter at a power level of 5 mW or lower.

$$P_{d\_Dreverse} \approx (5\ V + 250\ mV) \times 100\ \mu A = 525\ \mu W \quad (29)$$

Diode capacitance C_d and reverse recovery times t_{rr}

Both parameters influence the frequency-dependent switching losses. The lower the values of these parameters, the lower the respective losses. A direct comparison of the parameter values is difficult in most situations due to the different test conditions used for the specification, especially when comparing diodes from different manufacturers.

Considering all of the preceding points, a RB520S30 Schottky diode [10] has been selected for this design. Table 6 provides a comparison of that Schottky diode to a similar silicon diode. The PMLL4153 silicon diode is used in former designs (TIDA-00167 [7] and TIDA-00189 [8]) to sidestep the possible negative impact of an increased reverse current of Schottky diodes at elevated temperatures. Values for V_F, I_R, and C_d are estimations and approximations and are based on the typical curves of the manufacturers' datasheets

Table 6. Comparison of a Schottky Diode to a Silicon Diode

DIODE	V_R	$I_{F(AV)}$	V_F AT 20 mA	I_R AT 5 V	C_d AT 5 V	MANUFACTURER	PACKAGE TYP. DIMENSIONS
RB520S30	30 V	200 mA	425 mV at −40°C 340 mV at 25°C	400 nA at 25°C 13 µA at 85°C 130 µA at 125°C	8 pF	NXP Semiconductors	SOD523 (SC-79) 1.6 mm x 0.8 mm
PMLL4153	50 V	200 mA	760 mV at 25°C 880 mV at −40°C	30 nA at 25°C 200 nA at 85°C 2 µA at 125°C	8 pF	NXP Semiconductors	SOD80C 3.5 mm x 1.53 mm

5.5.2 Selection of Transformer

The selection or design requirements of the transformer must consider the following points:

- **V-t product (also called V-s or V-µs product)**: As described in the remarks and explanations which follow Figure 10, the goal is to operate the transformer in the linear region of the hysteresis curve, avoiding saturation at all operating conditions.
- **Turns ratio**: This parameter is mainly dependent on the output voltage, the input voltage, the diodes D1 and D2 forward voltage, and other operating conditions such as temperature and load current.
- **Isolation**: The class of isolation depends strongly on the isolation requirements of the system and end application.

5.5.2.1 Transformer Turns Ratio

The TIDA-00349 design uses an exemplary primary-to-secondary turns ratio n of 1:1.25. The same transformer is also used in two former designs TIDA-00167 [6] and TIDA-00189 [8].

For specific requirements of dedicated applications, the needed primary-to-secondary turns ration n can be derived by rearranging the given Equation 19.

$$n = \frac{V_{IN}}{V_{OUT} + 2 \times V_{F\_D}} \quad (30)$$

where

- V_{F_D} is the value of the forward voltage of each of the diodes D1 and D2 and—according to Equation 25—at twice the output current I_{OUT}

As Table 7 and Figure 15 show, Equation 30 already provides a good first approximation for the required turns ratio n compared with the real measurements at 25°C of the TIDA-00349 design using a transformer with a turns-ratio of 1:1.25 = 0.8. The calculated n in the example is based on the typical V_{F_D} of the RB520S30 Schottky diode [10] at 25°C and on the V_{IN}, V_{OUT}, and I_{OUT} measured on a real TIDA-00349 board. V_{F_D} is derived from the typical I_F versus V_F graph given in the datasheet of the diode.

Table 7. Comparison Between Calculated Turns Ratio and Results Based On Real Measurement

MEASURED ON TIDA-00349				EXTRACTED FROM RB520S30 DATASHEET I_F VERSUS V_F GRAPH	CALCULATED n TO MATCH THE MEASURED V_{IN} AND V_{OUT} AT GIVEN I_{OUT} ON TIDA-00349
V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	n OF TRANSFORMER USED	TYPICAL V_F AT 2 X I_{OUT} (mV)	
2.96	3.28	0.1	0.800	210	0.800
3	3.18	1	0.800	275	0.804
2.97	2.83	10	0.800	345	0.844
5.15	6.04	0.1	0.800	210	0.797
5.2	5.94	1	0.800	275	0.801
5.17	5.6	10	0.800	345	0.822

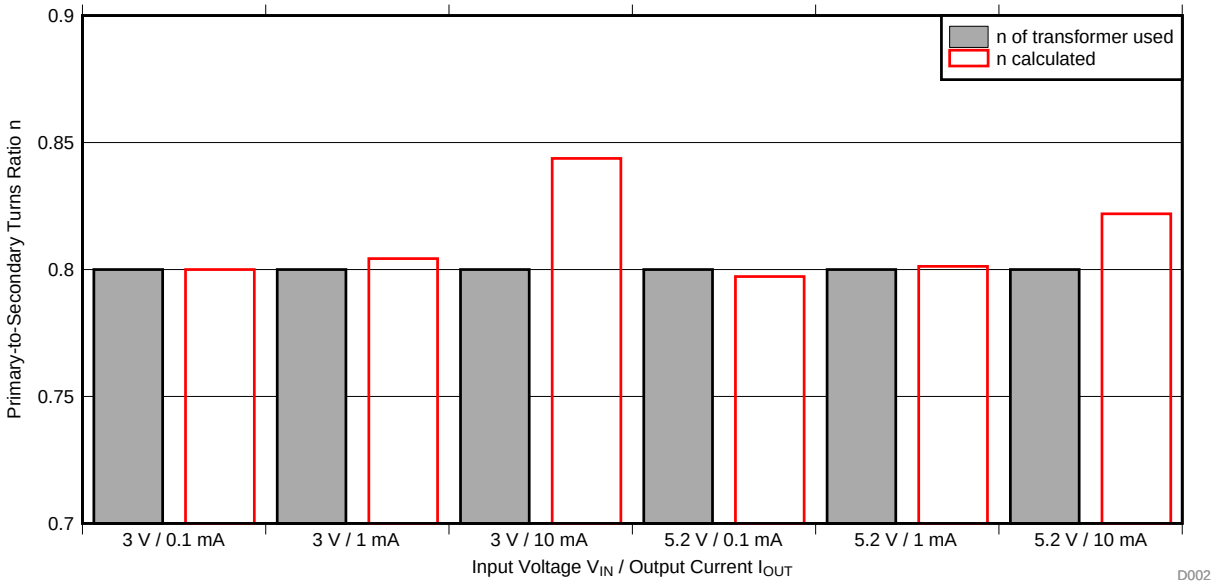


Figure 15. Comparison Between Calculated Turns Ratio and Results Based On Real Measurement

The good match of the calculated turns ratio with the measured results of TIDA-00349 using a transformer with a n = 0.8 holds especially true for low output current applications up to 1 mA. For larger currents it is obvious that the additional voltage drops caused by the R_DS_on of the TPS60402s internal FETs and the DC-resistance of the primary and secondary windings of the transformer cause a difference in the range of up to 5%, which may not be negligible.

In most of the cases, the goal is to ensure a minimum V_{OUT} even at the minimum V_{IN}. Consider also that the V_{F_D} has a negative temperature coefficient and that the forward voltage increases with the forward current through the diode; therefore, TI recommends to modify Equation 30 so that it addresses a worst-case scenario.

$$n = \frac{V_{IN\_min\_available}}{V_{OUT\_min\_needed} + 2 \times V_{F\_D\_max@Tmin}} \quad (31)$$

where

- $V_{IN\_min\_available}$ is the minimum voltage available at the DC/DC converter input
- $V_{OUT\_min\_needed}$ is the minimum voltage the DC/DC converter requires to provide on its output to power the isolated part of the system. This is especially important in cases where a post-regulator is used to finally provide a stable and accurate voltage rail. Such a post-regulator requires enough headroom voltage to properly work and to meet the specification as given in its datasheets. In the case of linear regulators, keep in mind that this headroom voltage is larger than the supposed dropout voltage V_{DO}.
- $V_{F\_Dmax@Tmin}$ is the maximum value of the forward voltage of each of the diodes D1 and D2 at the minimum temperature and—according to Equation 25—at twice the output current I_{OUT}.

For an even more accurate calculation at the level of output currents exceeding 1 mA, revisit the aforementioned parasitic resistances:

- R_DS_on of each of the FETs: Can be assumed to be in the range of 1 Ω
- DC resistance of the primary winding of the transformer: This is given with 1.2 Ω in the specification sheet of the transformer [9]
- DC resistance of the secondary winding of the transformer: This is given with 1.6 Ω in the specification sheet of the transformer [9]

These parasitic resistances must be factored in additionally to improve accuracy in the case of medium to higher output currents.

5.5.2.2 Transformer V-t Product (Also Called V-s or V-μs Product)

Exceeding the V-t product applied to the primary winding of the transformer drives the magnetic core into saturation, has a negative impact on efficiency, and can even lead to failures depending on how deeply the transformer is driven into saturation. To avoid saturation of the transformer core, the V-t product must be specified:

$$Vt_{\_min} \geq V_{p\_max} \times t_{ON\_max} = \frac{VIN_{\_max}}{2} \times \frac{T_{\_max}}{2} = \frac{VIN_{\_max}}{4 \times f_{\_min}}$$

where

- $Vt_{\_min}$ is the minimum required V-t product of the transformer to avoid saturation
- $V_{p\text{-}max}$ is the maximum voltage applied to the primary winding
- t_{ON_max} is the maximum time for which a switch (Q1 or Q2 in Figure 12) is ON
- V_{IN_max} is the maximum input voltage of the isolated DC/DC converter (in this case 5.2 V)
- $T_{\_max}$ is the maximum time of one period of the switching frequency
- $f_{\_min}$ is the minimum switching frequency; 30 kHz for TPS60402 (32)

Using the given numbers, calculate the minimum required V-t product to Equation 33:

$$Vt_{\_min} \geq \frac{5.2\ V}{4 \times 30\,kHz} = 43.3\ V\mu s \quad (33)$$

To ensure that the transformer stays far from saturation, TI recommends applying an additional margin. A slight reduction of the value of the magnetizing inductance can not be excluded, even if the V-s product is not (yet) violated. Transformers with V-s products larger than 50 V-μs must be used, assuming that this V-s product from the manufacturer is valid over the required operating temperature range.

Furthermore, the user must clarify with the transformer manufacturer as to whether the V-s products of a specific transformer are applicable for uni-directional or bi-directional magnetic excursion of the core. Because the transformer of this TIDA-00349 design is driven by a half-bridge (which belongs to the double-ended topologies), the magnetic excursion is bi-directional, ideally symmetrical, and DC-free. These qualities of the magnetic excursion result in a swing from A to A' and back to A during one full period of the switching frequency (see Figure 10 and Table 5). Consecutive full swings have the same absolute value as calculated in Equation 32, but opposite signs. As a result of this shared absolute value, the peak values of the V-s products under steady-state conditions at the end of each interval are therefore only on half of the calculated $Vt_{\_min}$ with both polarities (±21.7 V-μs) in the example of this design.

Under start-up conditions, the magnetic excursion with the same full swing starts from the origin of the hysteresis curve, but not from the point A', leading to a peak value for the first switching periods equal to the full swing value or $Vt_{\_min}$ as calculated in Equation 32.

5.5.2.3 Transformer Isolation

Due to the main objective of this design, which is the avoidance of ground loops in signal conditioning and data transmission applications, a transformer offering functional isolation is sufficient.

5.5.2.4 Transformer Specification

For the purpose of this design, an optimized transformer from WURTH ELEKTRONIK [9] that matches the listed requirements was used. Table 8 shows the short specifications for this transformer.

Table 8. Transformer Specifications

TURNS RATIO n (N_P:N_S)	MAGNETIZING INDUCTANCE L_m (mH)	V-t PRODUCT (V-µs)	ISOLATION (V_{AC}, 1 MINUTE)	DIMENSIONS (mm)	ORDER NO.	OPERATING TEMPERATURE RANGE (°C)	MANUFACTURER
1:1.25	> 3	100	1500	9.78 × 9.14 × 10.54	750314839	–40 to 100	WURTH ELEKTRONIK

5.6 Real Implementation of the Isolated DC/DC Converter

Figure 12 only shows a simplified schematic of the isolated DC/DC converter. The circuitry implemented on the board adds the following list of additional components and tweaks to ease the test and enable user-specific modifications:

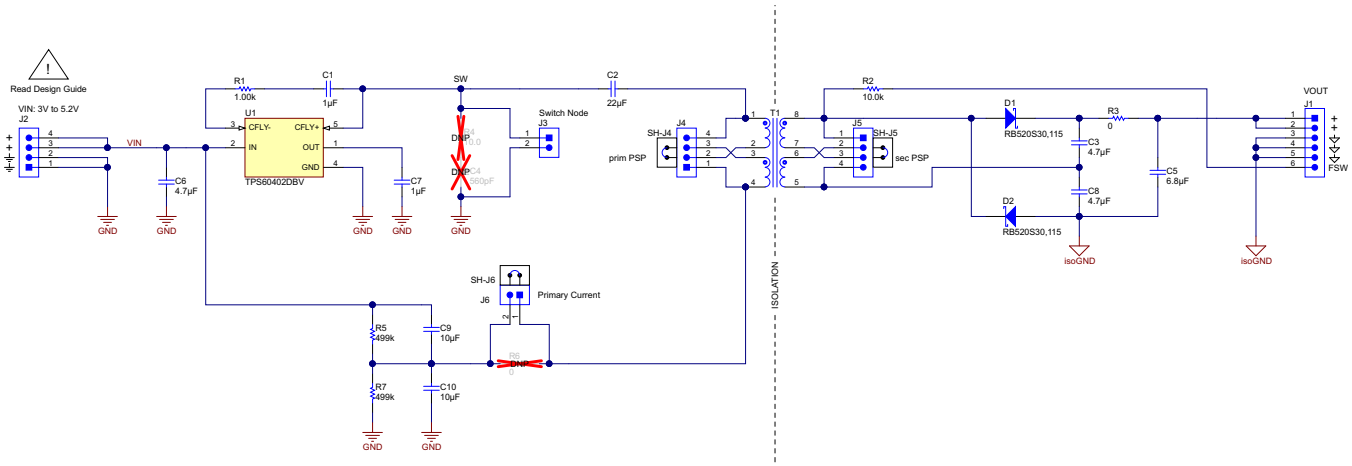


Figure 16. Isolated DC/DC—Real Implementation

- R4 and C4 are placeholders for a snubber circuitry, which is required in the case that the peaks and spikes of the voltage waveform on the switch node (SW) exceed the voltage rating of the TPS60402 CFLY+ pin. The snubber reduces the peaking, dampens a possible ringing, and reduces radiated noise on that node of the circuit at the expense of a reduced efficiency of the power conversion.

  The current design does not require these components. Therefore, these components have not been populated. If these components are needed, separate testing is required to evaluate the effectiveness of the snubber and its influence on the DC/DC converter efficiency. The values given are placeholder values and must be adapted according to the specific case. The value of the capacitor C4 is usually chosen so that the ringing frequency on the switch node is halved with C4 compared to the case without C4. R4 must be a short (or a 0-Ω resistor) for finding the right value for C4. If the best fitting capacitance value has been found and C4 has been populated with a capacitor with this optimal value, R4 can be varied to find the best compromise between ringing reduction and best efficiency. The test must be conducted by connecting the oscilloscope probe (high impedance, low capacitance) with the shortest possible grounding wire.

- The header pins of J3 can be used as a test point and GND connection for the modified use of the oscilloscope probe, similar to what Figure 17 shows with standard test points. Using the J3 header pins provides an easy way to connect the probe in a tip and barrel manner to the switch node. Connecting the probe in this manner avoids noise pickup, which otherwise occurs when the probe is used with a standard ground wire and alligator clip connected.

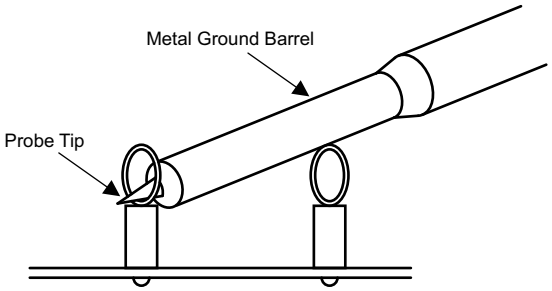


Figure 17. Tip and Barrel Method for Noise-Free Measurement

Figure 18 provides an example for a standard 10:1 oscilloscope probe, which comes with a probe tip cover, a long ground lead, and an alligator clip (on the left side of Figure 18). The use of such standard probes for measuring switching regulators is notorious for its noise pick-up. The right half of the picture shows the same probe but with a removed ground lead and probe tip cover. A self-made adapter based on a 2-pin socket, fitting on the board header J3, is used instead. One pin of this socket connects the probe tip to the switch node (to pin 1 of J3), the other pin connects the naked coaxial metal tube shield of the probe to ground (to GND, pin 2 of J3) as soon as the socket is plugged into the header J3.

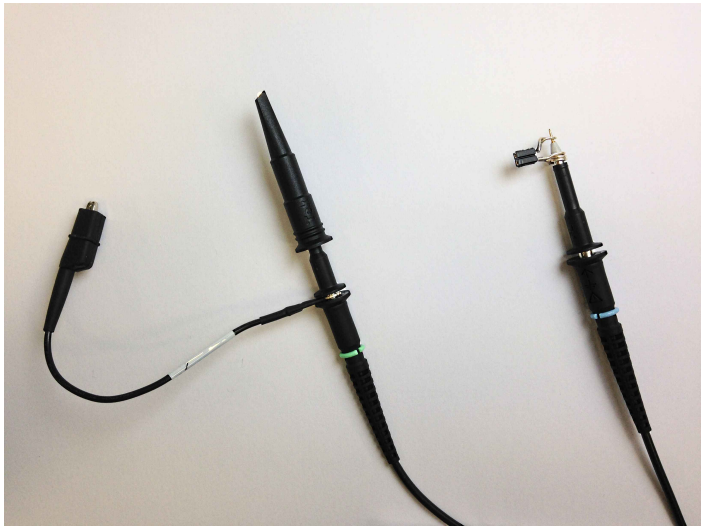


Figure 18. Standard Oscilloscope Probe (Left) With Long Ground Lead and Alligator Clip Versus Modified Oscilloscope Probe (Right) Using Self-Made Adapter

Figure 19 and Figure 20 show a comparison of the same switch-node signal on channel 2 (CH2) but measured with the standard probe configuration (Figure 19), or with the tip and barrel approach using the modified probe and adapter (Figure 20). The tip and barrel method provides a much cleaner waveform compared to the standard probe usage, which shows significant peaking and ringing (highlighted by the red circle in Figure 19).

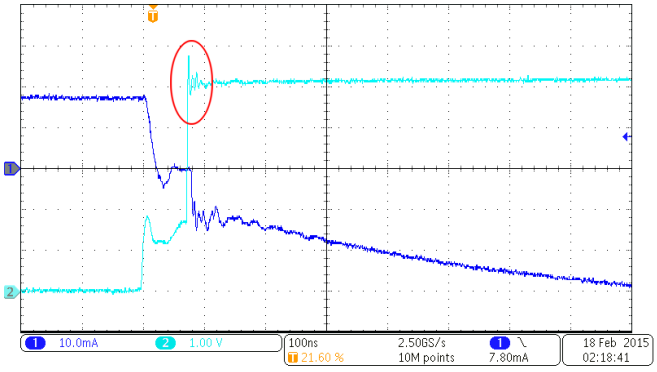


Figure 19. Switch-Node (CH2) Waveform Measured With Standard Probe Using Long Ground Lead With Alligator Clip

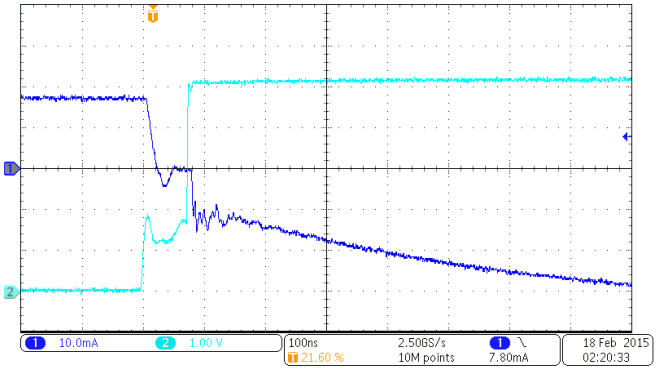


Figure 20. Switch-Node (CH2) Waveform Measured With Modified Probe Using Self-Made Adapter

- Header J6 provides an easy way of measuring the primary current of the transformer by combining a standard current probe with a self-made adapter (Figure 21). The self-made adapter must be plugged on header J6 instead of the respective jumper SH-J6.

Figure 21. Combination of Current Probe With Self-Made Adapter for Primary Side Current Measurement

- Headers J4, J5, and respective jumpers: In contrast to the statement that the half-bridge transformer does not require multiple or tapped windings on each side, the transformer T1 used in this design has two separate windings on the primary as well as on the secondary side. As can be seen in Figure 16, the windings on each side are connected in series; therefore, the windings are considered to be a single winding. The transformer provides an easy way to test other configurations with its dual-winding structure. These configurations include paralleling the windings or using only one of the separate windings on one side, but using both windings on the other side. This approach is supported by J4 and J5 and the respective jumpers, which are populated by default on the two inner pins of both headers, selecting the series connection mode of the two windings on each side. If required, a dedicated single winding transformer can be used in series manufacturing. The headers J4 and J5 can also be used to measure the voltages across the primary and secondary winding of T1.
  Carefully monitor component voltages and currents when the transformer configuration changes to avoid over-stressing the components or driving the transformer into saturation.

- R5 and R7 are used to keep the capacitive divider C9 and C10 balanced to cancel out their possible tolerances.
- R3 (0 Ω) can be replaced by a ferrite bead to form an output voltage filter. Due to the low switching frequency, this replacement does not help to filter out the switching frequency itself, but rather filters the spikes that are present on the output voltage. The tip and barrel method must be used for measuring the output voltage with an oscilloscope probe to avoid unwanted noise pick-up.
- The implementation of R2 and the FSW output provide an easy way of measuring the switching frequency by using an oscilloscope or multimeter. The FSW output (pin 6 of header J1) is decoupled by 10 kΩ (R2) from the secondary winding of the transformer T1. This decoupling reduces the influence of the frequency-measurement on the efficiency of the converter and waveforms.
  The FSW output can be further used to derive a synchronization signal for synchronizing the system powered by this isolated DC/DC converter to the switching frequency of the converter.

6 Test Results

6.1 Efficiency Measurements

The efficiency of the isolated DC/DC Converter has been evaluated in depth. A variable input voltage from 3 V to 5.2 V was applied through an ammeter on pin 3 of header J2, referenced to pin 2 (GND) of J2. Pins 1 and 4 were used as sense terminals for the input of a voltmeter. The voltmeter input was configured to operate in a high input impedance (High-Z) state, which prohibits the voltmeter from having any influence on the input current measurement. The output current and output voltage were controlled and measured by a source-measurement unit (SMU). The output of the DC/DC converter was loaded by a constant current ranging from 100 μA to 10 mA. The test was conducted at –40°C, 25°C, and 85°C.

Some tests were conducted with silicon diodes (PMLL4153) instead of Schottky diodes (RB520S30) to show the influence of the different types of diodes on the efficiency of the isolated DC/DC converter.

Figure 22, Figure 23, and Figure 24 show the efficiency versus output current graphs of the TIDA-00349 using Schottky Diodes RB520S30. The isolated DC/DC converter were evaluated at –40°C, 25°C, and 85°C and at different input voltages.

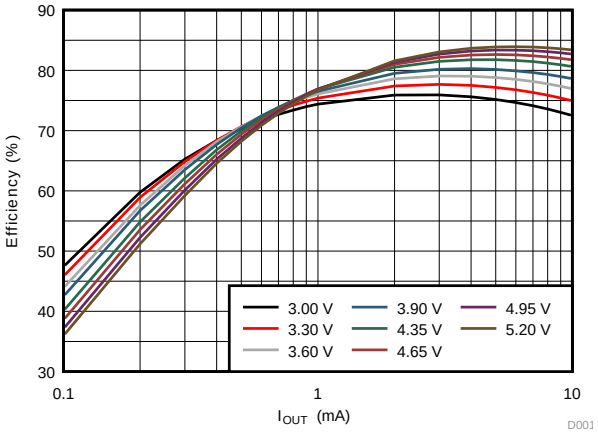


Figure 22. Efficiency Versus Output Current I_{OUT} With RB520S30 at TA = –40°C

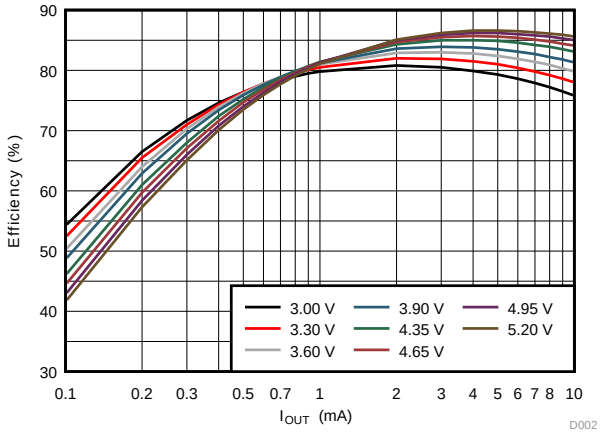


Figure 23. Efficiency Versus Output Current I_{OUT} With RB520S30 at TA = 25°C

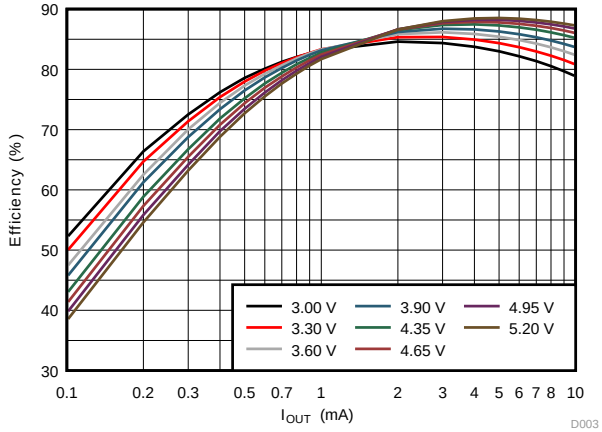


Figure 24. Efficiency Versus Output Current I_{OUT} With RB520S30 at TA = 85°C

Figure 25, Figure 26, Figure 27, Figure 28, Figure 29, and Figure 30 provide a comparison of the TIDA-00349 efficiency using the standard Schottky diodes as given in the Bill of Materials (BOM) or by alternatively replacing those diodes with silicon diodes PMLL4153. The test results show that the efficiency of a design based on Schottky diodes is much higher. This high efficiency is especially true for operation of the design at low input voltages (shown for V_{IN} = 3 V), at low ambient temperatures (–40°C), and at the full load current where the difference in efficiency is almost 24%. At those operating conditions, the influence of the lower V_F of the Schottky diodes compared to the V_F of silicon diodes has the largest impact.

From an alternate perspective, it is apparent that the advantage of the lower V_F diminishes when operating at the full input voltage, maximum temperature, and lowest current. Under such conditions the reverse current losses of the Schottky diodes exceed the losses of the silicon diode, leading to almost the same efficiency at a 100-µA load current, V_{IN} of 5.2 V, and an ambient temperature of 85°C.

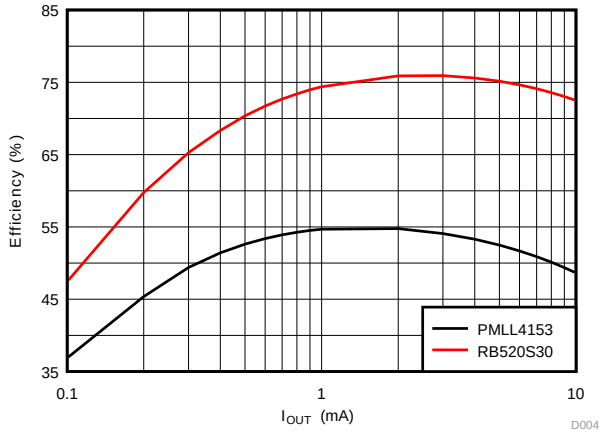


Figure 25. Efficiency Versus Output Current I_{OUT} of Two Different Diodes at V_{IN} = 3.0 V / TA = –40°C

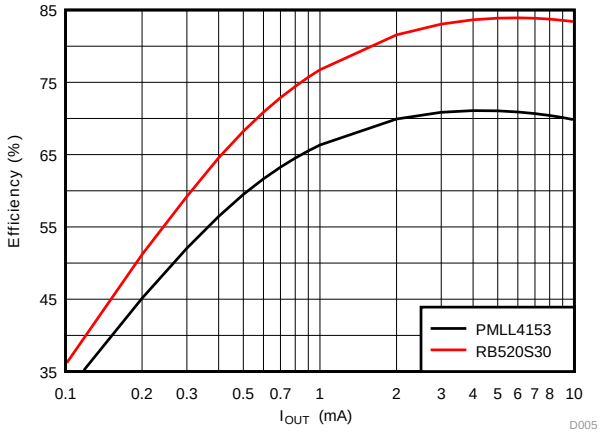


Figure 26. Efficiency Versus Output Current I_{OUT} of Two Different Diodes at V_{IN} = 5.2 V / TA = –40°C

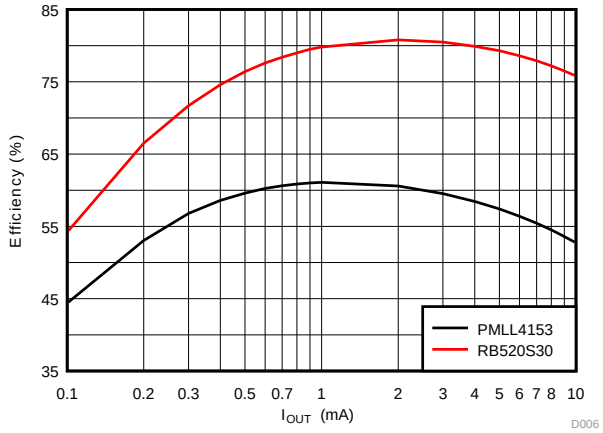


Figure 27. Efficiency Versus Output Current I_{OUT} of Two Different Diodes at V_{IN} = 3.0 V / TA = 25°C

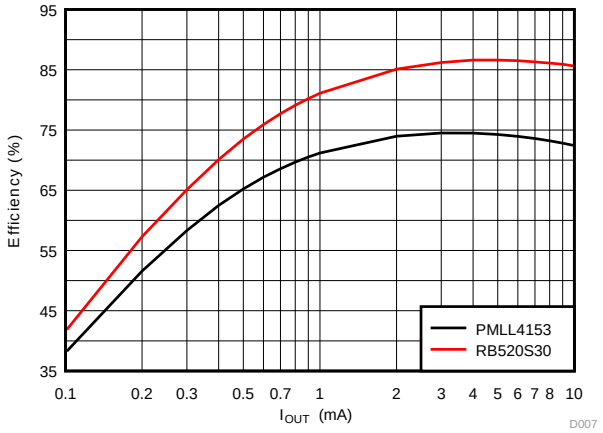


Figure 28. Efficiency Versus Output Current I_{OUT} of Two Different Diodes at V_{IN} = 5.2 V / TA = 25°C

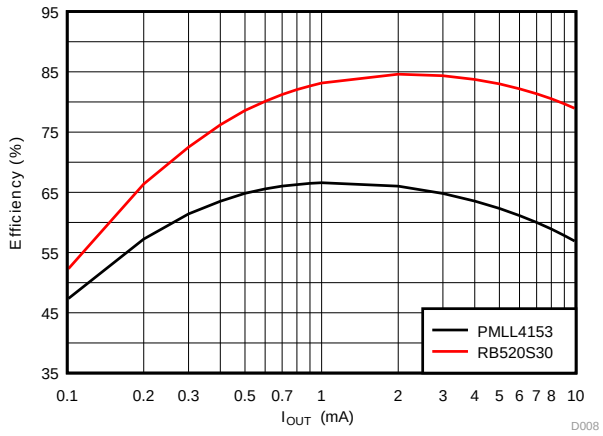


Figure 29. Efficiency Versus Output Current I_{OUT} of Two Different Diodes at V_{IN} = 3.0 V / TA = 85°C

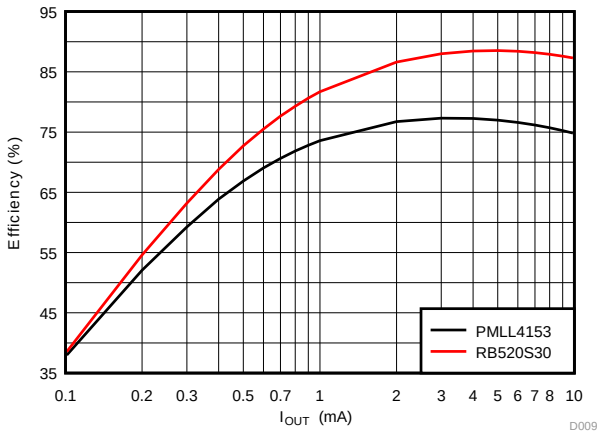


Figure 30. Efficiency Versus Output Current I_{OUT} of Two Different Diodes at V_{IN} = 5.2 V / TA = 85°C

Figure 31, Figure 32, Figure 33, and Figure 34 show that as the temperature increases under medium-to-full load current conditions, so does the efficiency of the converter. This correlation is again based on the negative temperature coefficient of V_F.

There is a point where the 85°C curve crosses the 25°C curve. This point can be found within the low-to-medium load current range, within which the reverse current-based losses of the diodes become dominant. Because of the fact that the reverse current of Schottky diodes is much larger than that of silicon diodes, the crossing happens for Schottky diodes at higher load currents than as compared to silicon diodes. Because the reverse current losses of the diodes also rise with increased voltage, the crossing point occurs at higher load currents the higher the input voltage of the converter is. The curves of the silicon diode PMLL4153 do not show a crossing of the curves at a 3-V input voltage over the full output current range.

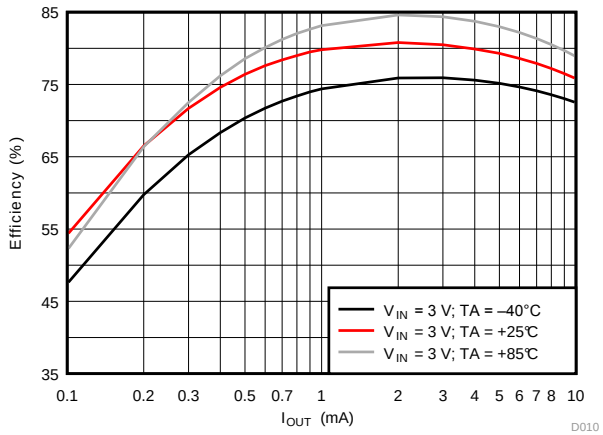


Figure 31. Efficiency Versus Output Current I_{OUT} of RB520S30 at V_{IN} = 3 V and at Different Temperatures

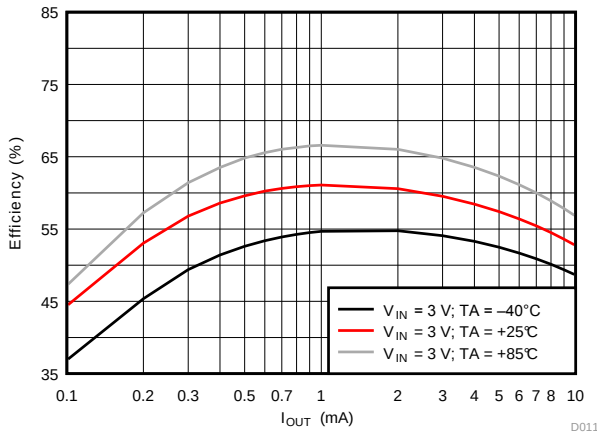


Figure 32. Efficiency Versus Output Current I_{OUT} of PMLL4153 at V_{IN} = 3 V and at Different Temperatures

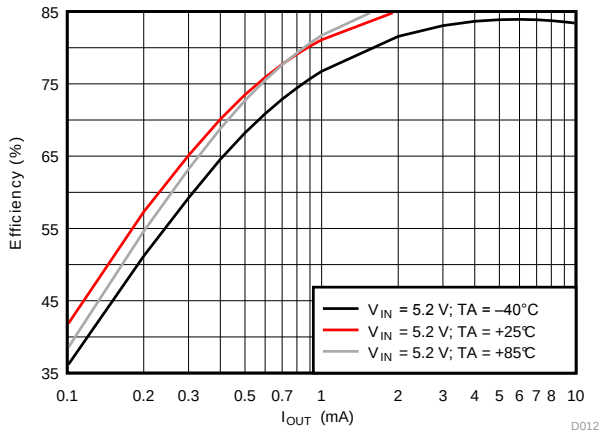


Figure 33. Efficiency Versus Output Current I_{OUT} of RB520S30 at V_{IN} = 5.2 V and at Different Temperatures

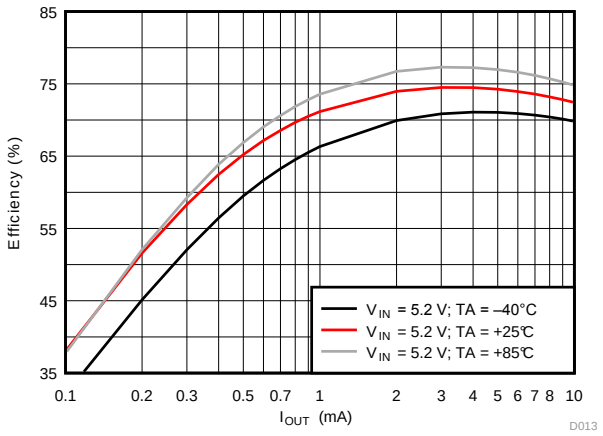


Figure 34. Efficiency Versus Output Current I_{OUT} of PMLL4153 at V_{IN} = 5.2 V and at Different Temperatures

6.2 Voltage and Current Waveforms

The majority of the voltage measurements were conducted with modified oscilloscope probes using the tip and barrel technique as outlined in Figure 17 and Figure 18. Similarly, the current probe adapter shown in Figure 21 was used for measuring the transformer currents.

6.2.1 Switch-Node Voltage and Transformer Windings Current Waveforms

The waveforms were measured at the minimum and the maximum V_{IN} and I_{OUT} as given in Table 1.

Figure 35 and Figure 36 show the primary current and switch node voltage for a load current of 100 µA. The primary current is the sum of the magnetizing current and the reflected load current. The magnetizing current is dominant.

Oscilloscope—channel assignment:

- CH1: Primary current measured on J6
- CH2: Switch-node voltage measured on J3

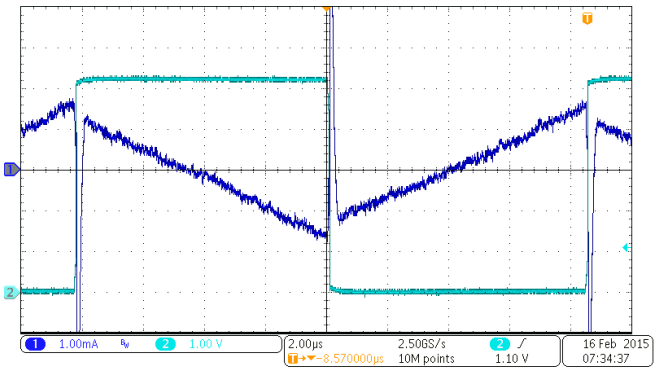


Figure 35. Switch Node Voltage and Primary Winding Current at V_{IN} = 5.2 V and I_{OUT} = 100 µA

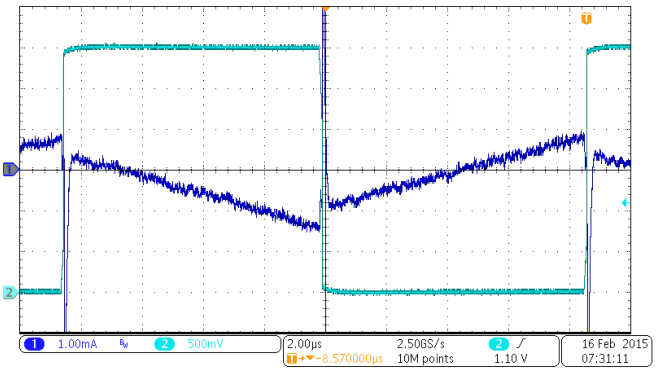


Figure 36. Switch Node Voltage and Primary Winding Current at V_{IN} = 3 V and I_{OUT} = 100 µA

Figure 37 and Figure 38 show the primary current and switch node voltage for a load current of 10 mA. The primary current is the sum of the magnetizing current and the reflected load current. The reflected load current is dominant.

Oscilloscope—channel assignment:

- CH1: Primary current measured on J6
- CH2: Switch-node voltage measured on J3

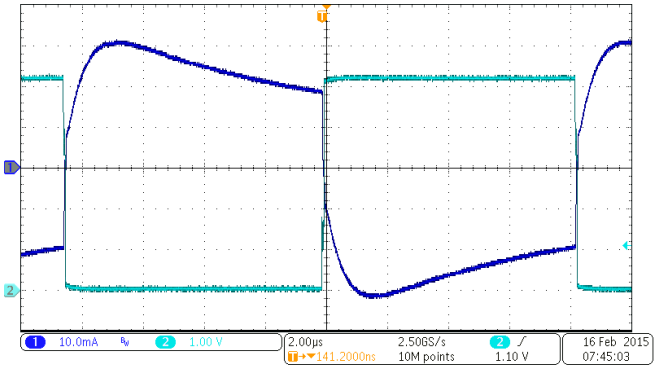


Figure 37. Switch Node Voltage and Primary Winding Current at V_{IN} = 5.2 V and I_{OUT} = 10 mA

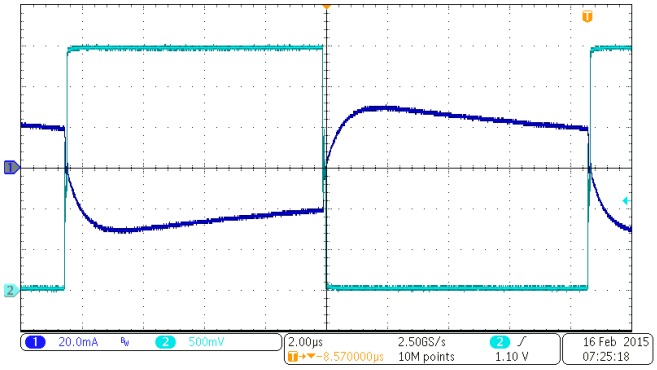


Figure 38. Switch Node Voltage and Primary Winding Current at V_{IN} = 3 V and I_{OUT} = 10 mA

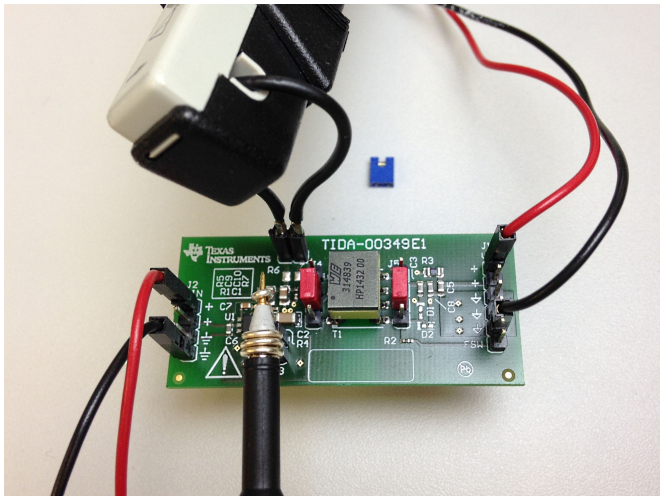


Figure 39. Test-Setup for Switch Node Voltage and Primary Winding Current Measurement

Figure 40 is an example of a measurement of the secondary winding current at the condition of a 10-mA load.

Oscilloscope—channel assignment:

- CH1: Secondary current measured on J5 (pin 2–pin 3)
- CH2: Switch-node voltage measured on J3

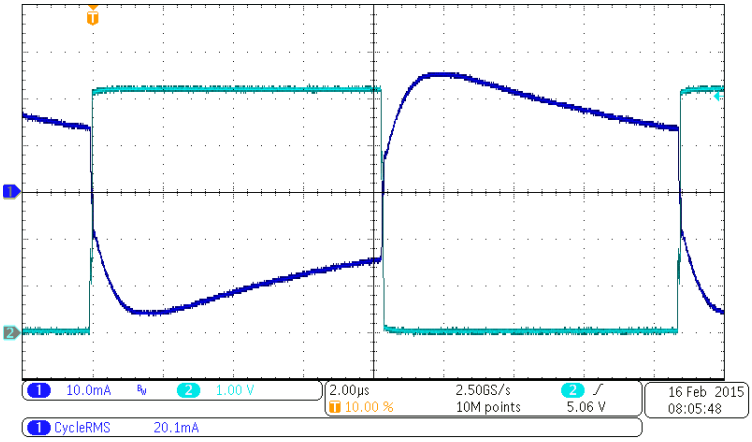


Figure 40. Switch Node Voltage and Secondary Winding Current at V_{IN} = 5.2 V and I_{OUT} = 10 mA

6.2.2 Primary and Secondary Winding Voltage and Primary Current Waveforms

Oscilloscope—channel assignment:

- CH1: Primary current measured on J6
- CH2: Primary winding voltage measured on J4 (pin 4–pin 1)
- CH3: Secondary winding voltage measured on J5 (pin 4–pin 1)

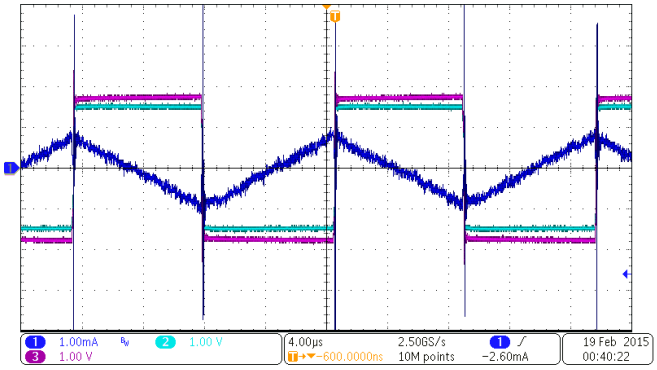


Figure 41. Primary and Secondary Winding Voltage and Primary Winding Current at V_{IN} = 3 V and I_{OUT} = 0 µA

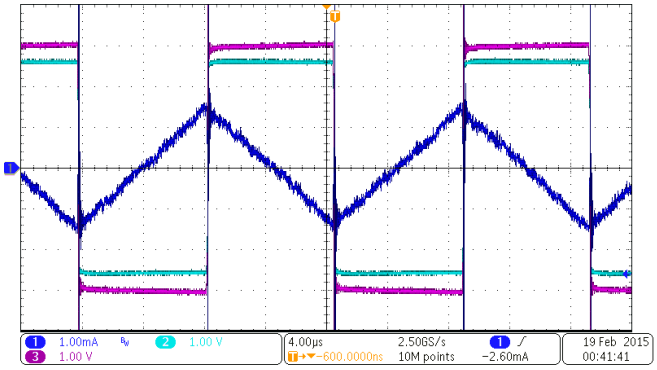


Figure 42. Primary and Secondary Winding Voltage and Primary Winding Current at V_{IN} = 5.2 V and I_{OUT} = 0 µA

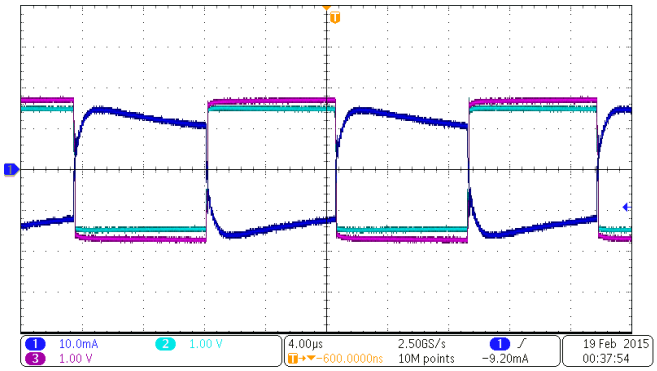


Figure 43. Primary and Secondary Winding Voltage and Primary Winding Current at V_{IN} = 3 V and I_{OUT} = 10 mA

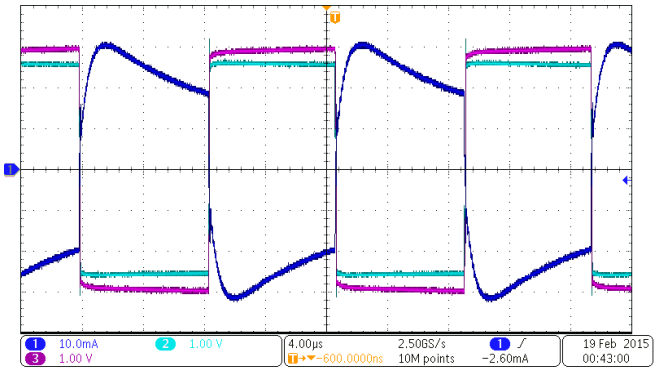


Figure 44. Primary and Secondary Winding Voltage and Primary Winding Current at V_{IN} = 5.2 V and I_{OUT} = 10 mA

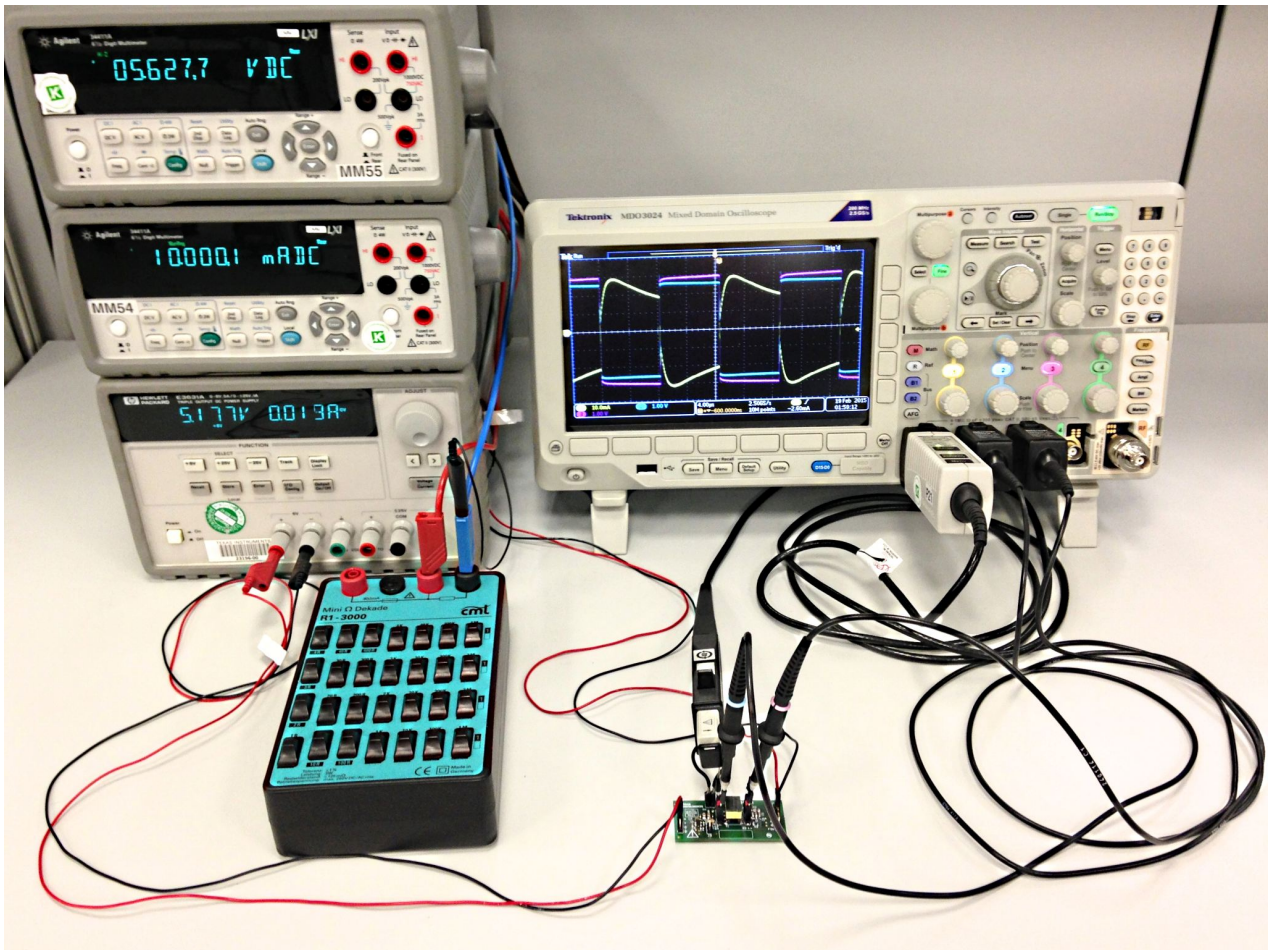


Figure 45. Test Setup for Primary and Secondary Winding Voltage and Primary Winding Current Measurement

6.2.3 FSW—Switching Frequency Output Waveforms

Oscilloscope—Channel Assignment:

- CH1: FSW—Output voltage waveform on J1 (pin 6 referred to pins 3–pin 5)

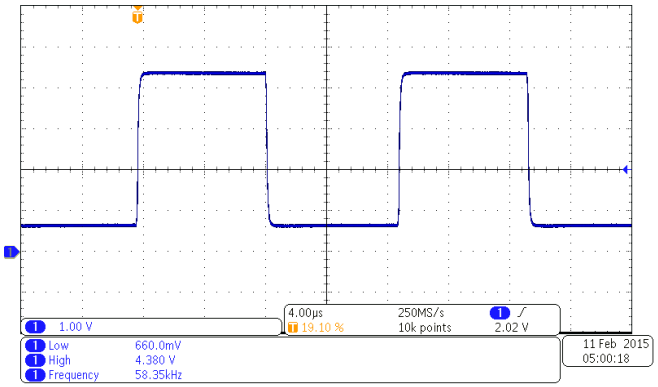


Figure 46. FSW Output Waveform at V_{IN} = 3 V and I_{OUT} = 0 A

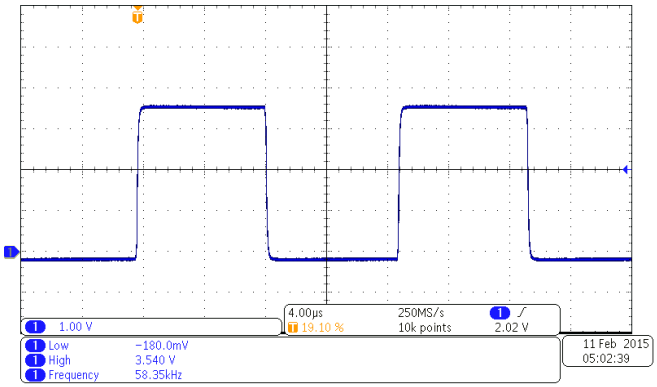


Figure 47. FSW Output Waveform at V_{IN} = 3 V and I_{OUT} = 100 µA

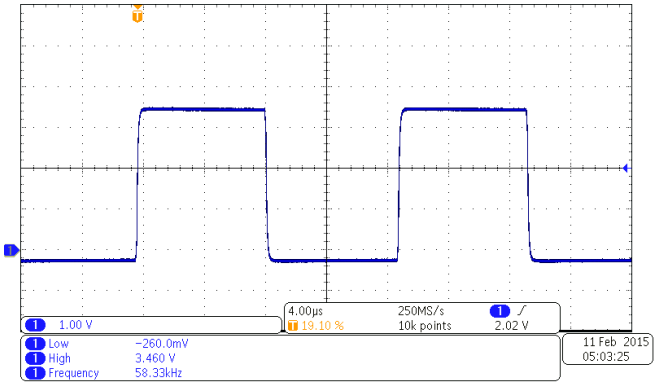


Figure 48. FSW Output Waveform at V_{IN} = 3 V and I_{OUT} = 1 mA

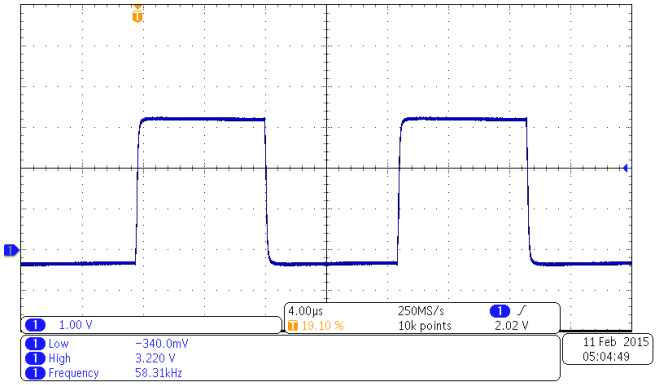


Figure 49. FSW Output Waveform at V_{IN} = 3 V and I_{OUT} = 10 mA

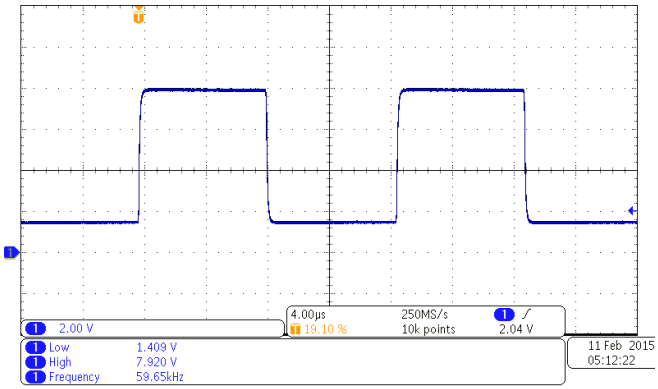


Figure 50. FSW Output Waveform at V_{IN} = 5.2 V and I_{OUT} = 0 A

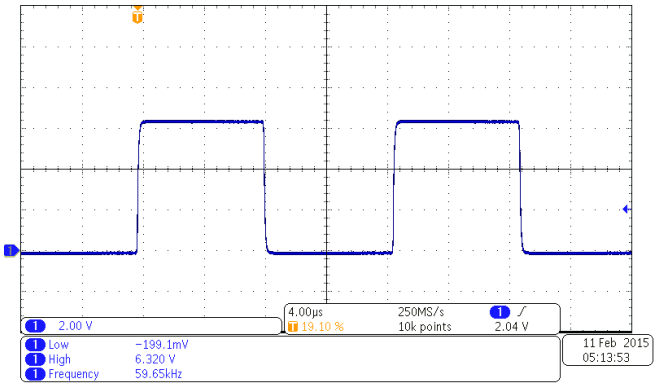


Figure 51. FSW Output Waveform at V_{IN} = 5.2 V and I_{OUT} = 100 µA

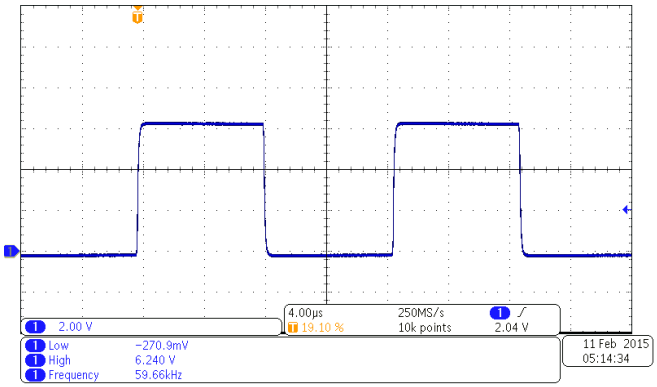


Figure 52. FSW Output Waveform at V_{IN} = 5.2 V and I_{OUT} = 1mA

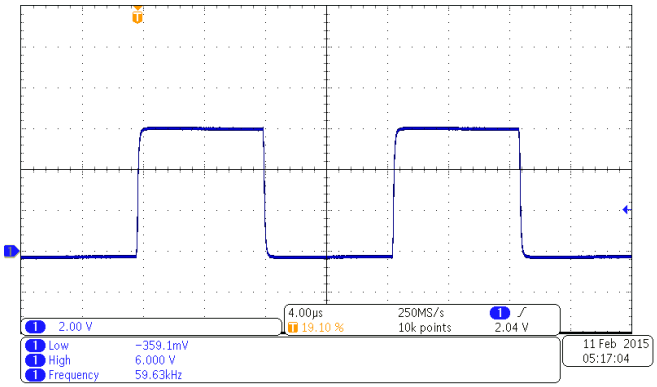


Figure 53. FSW Output Waveform at V_{IN} = 5.2 V and I_{OUT} = 10 mA

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00349

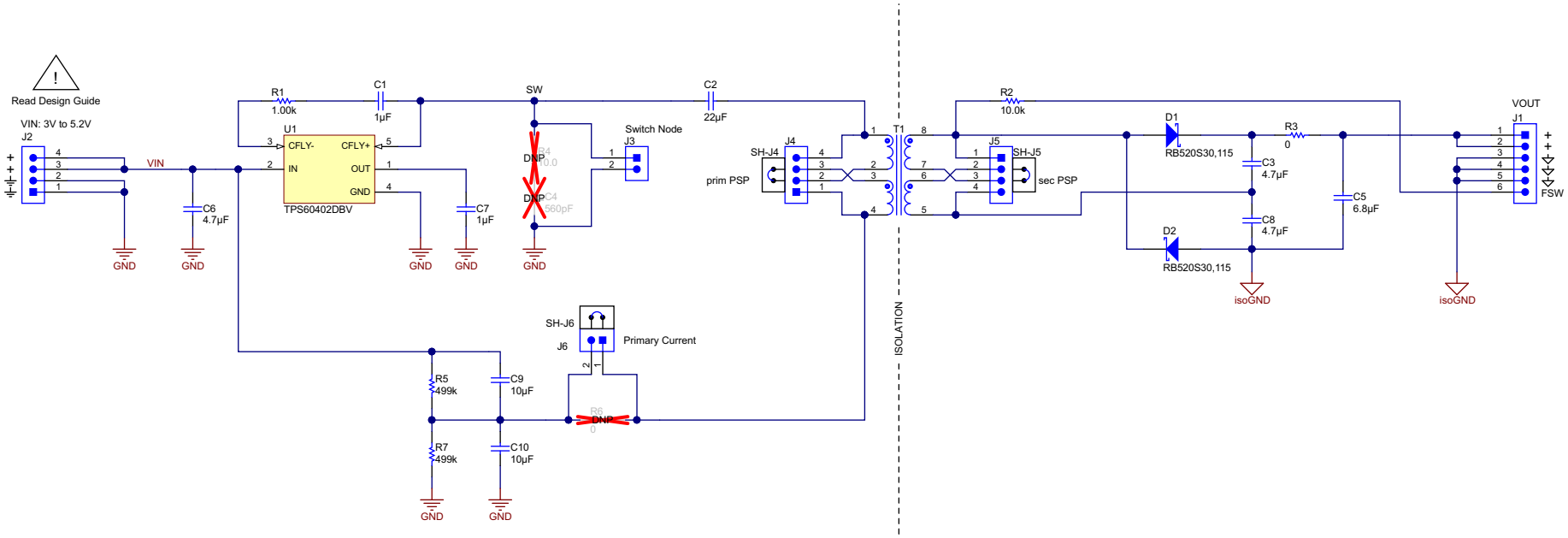


Figure 54. TIDA-00349 Schematic

7.2 Bill of Materials

To download the Bill of Materials (BOM), see the design files at TIDA-00349.

7.3 Layout Prints

To download the layer prints, see the design files at TIDA-00349.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00349.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00349.

7.6 Software Files

To download the software files, see the design files at TIDA-00349.

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8.1 Trademarks

9 About the Author

JÜRGEN SCHNEIDER is a systems engineer at Texas Instruments where he is responsible for developing TI-Designs for the industrial automation segment. He holds a Dipl.-Ing. (FH) degree in Industrial Electronics and has worked 13 years as a design engineer for semiconductor manufacturing equipment, telemetry systems, and electro-medical devices before joining TI in 1999. Jürgen has worked with TI as an analog field specialist, FAE, and systems engineer for power solutions. He presents at technical conferences and seminars and has been one of the presenters of the industry-wide known TI Power Supply Design Seminar for multiple years. Jürgen also has the distinguishment of being elected as a Member, Group Technical Staff.

Revision History A

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2015) to A Revision	Page
• Changed design from preview to full release	1

Revision History B

Changes from A Revision (March 2015) to B Revision	Page
• Changed efficiency versus I_{OUT} performance graph to updated legend	1

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