Simon Forstner

TI Designs: Verified Design

High Voltage 12 V – 400 V DC Current Sense Reference Design

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Circuit Description

This Verified Design shows a low cost circuit to measure currents with very high common mode of up to 400V using an INA138. A DDZ12CSF-7 Zener Diode and STR2550 Transistor were used to create a simple floating power supply and biasing the INA138 directly from the high voltage source. The 400V in this design is an example. With different components even higher common mode voltages can be achieved.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
INA138	Product Folder

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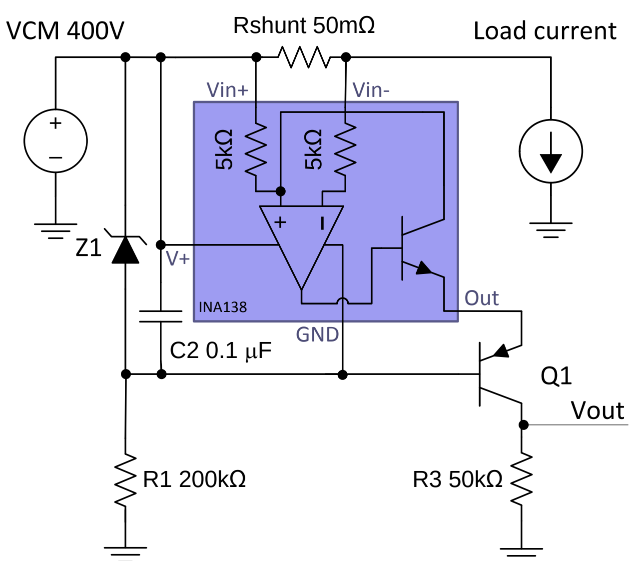

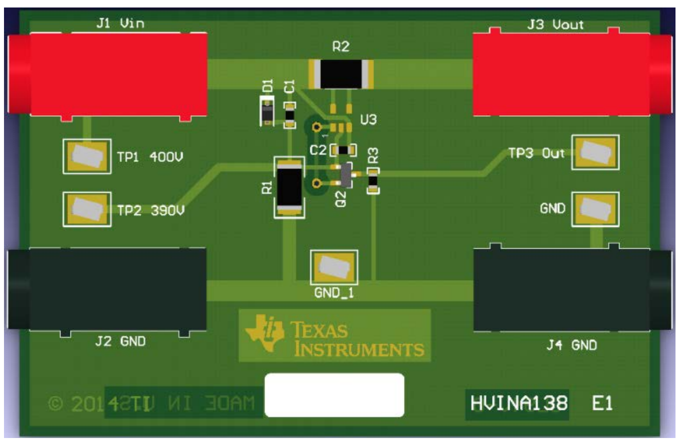

CAUTION: This equipment operates at high voltages and currents which can result in hazardous electrical shock. Please make sure you understand and follow all necessary safety precautions prior to purchasing and operating.

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1 Design Summary

The design requirements are as follows:

- Common Mode Voltage: 12 V to 400 V
- Input: 0.1 A – 6 A (50mΩ Shunt) or 1 A – 20 A (5mΩ Shunt)
- Output: 50 mV – 3 V

The design goals and performance are summarized in Table 1 Comparison of Design Goals, Simulation, and Measured Performance. Figure 1 depicts the measured relative output error of the design.

Table 1 Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Error (%FSR)	0.3%	0.012%	0.17%
Relative Error (Iload=200 mA)	10%	0.13%	5.03%

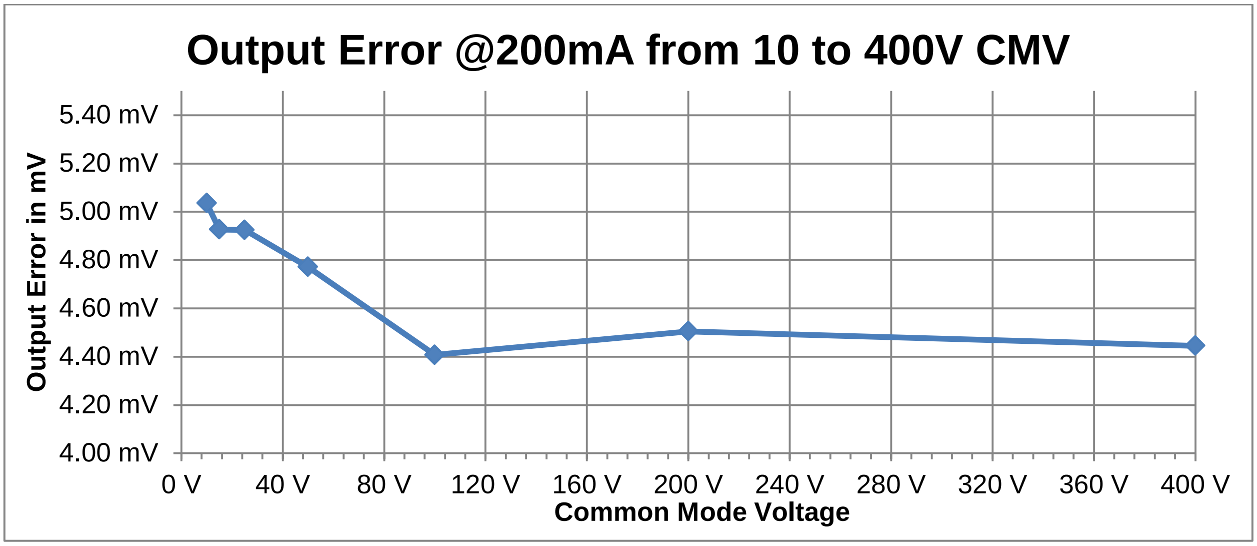

Figure 1: Output Error over Common Mode Voltage

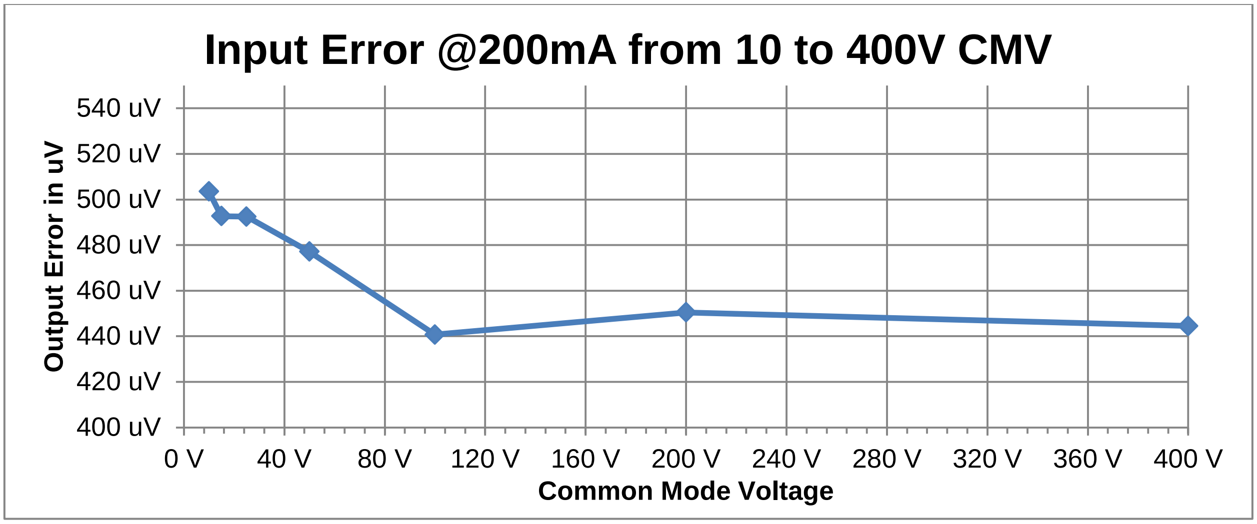

Figure 2: Input Error over Common Mode Voltage

2 Theory of Operation

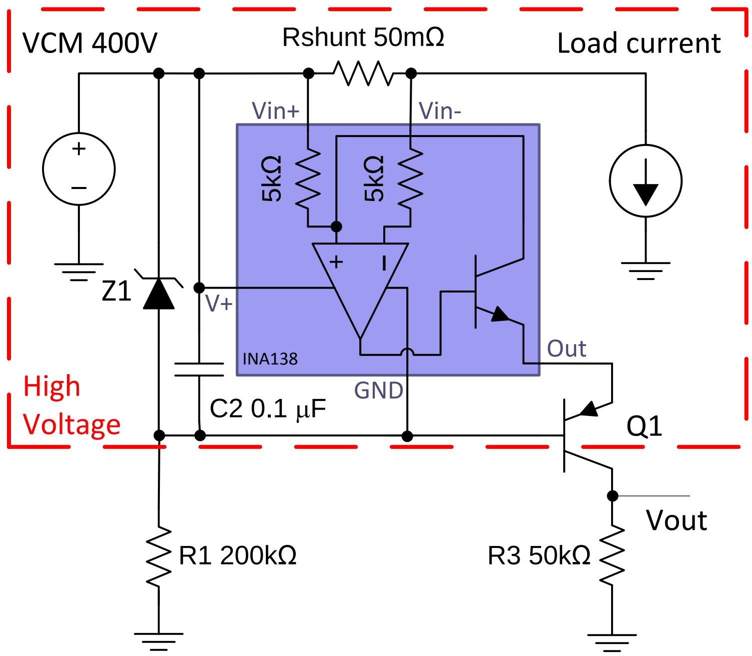

Figure 3 - Schematic

The INA138 only works up to a common mode voltage of 36V. To be able to measure currents at higher voltages we need the INA138 to “float” near the measurement voltage. This is achieved by using a 10V zener diode (Z1) to create a “virtual ground” which is always ~10V below the common mode voltage. Connecting the power supply and ground pins of the INA138 across the zener diode utilizes the zener as a floating power supply. The rest of the voltage, in our case up to 390V, will drop over the series resistance (R1) to ground. Power to the INA138 will be provided directly from the high voltage rail which eliminates the need for an extra LDO or something similar for voltage regulation.

INA138 is used in this design because of its ability to output a current as illustrated in Figure 3 - Schematic. The voltage drop over the shunt resistor generates a higher voltage on the plus input of the internal Opamp than on the minus input. The Opamp will then start to rise its output voltage and with that the base voltage of the internal NPN Transistor. Now the transistor will let some current flow through emitter and collector. This current has to come from the Vin+ input and therefore generates a voltage drop over the internal 5kΩ resistor. It will then regulate the output current to generate a voltage drop equal to the shunt resistor drop over the internal 5kΩ resistor at the Vin+ input. Now we have reached steady state and the INA138 generates an output current which is directly related to the voltage drop over the shunt resistor. The output current is calculated as:

$$I_{out} = \frac{I_{Load} \cdot R_{Shunt}}{5k\Omega} \quad (1)$$

With a load current equal to 200mA and a 50mΩ shunt the output current is calculated like as:

$$I_{out} = \frac{I_{Load} \cdot R_{Shunt}}{5k\Omega} = \frac{V_{Shunt}}{5k\Omega} = \frac{10mV}{5k\Omega} = 2\mu A \quad (2)$$

The output current of the INA138 will flow through the PNP Transistor (Q1) used to cascode the INA138 and create a voltage drop over resistor R3. The voltage over R3 is now referenced to the system ground and can be easily measured with an ADC or µController. The output voltage is calculated as illustrated below:

$$V_{out} = \frac{I_{Load} \cdot R_{Shunt} \cdot R_3}{5k\Omega} = \frac{V_{Shunt} \cdot R_3}{5k\Omega} = \frac{10mV \cdot 50k\Omega}{5k\Omega} = 100mV \quad (3)$$

3 Component Selection

3.1 Current Shunt Monitor

The INA138 was chosen because of its ability to output a current. This made it easy to get an output voltage referenced to ground with the use of a PNP transistor. For faster transient response devices with a wider gain bandwidth such as INA139 can be selected.

3.2 Zener Diode and Series Resistance

The input voltage of the INA138 can range from 2.7V to 36V. The Zener Diode voltage should be chosen somewhere in that range. Conveniently a 12V diode lies in the middle between those two voltages. Not only will the Zener diode regulate the maximum voltage applied across the INA138 and protect it from transient events it will also allow for a suitable margin to still reach the 2.7V needed to start up the device. Since datasheet parameters such as offset are defined for 12V Vin+ to GND using a 12V Zener diode makes it easy to predict the maximum output errors. Substituting a 10V Zener diode will have little impact on accuracy and is used throughout the following simulations and testing verification.

The series resistance (R1) has the most influence over the power consumption. The main voltage drop (up to 390V in this case) drops over this resistor. As calculated in equation **(4)** 0.76W is dissipated by the resistor.

$$P(R1) = \frac{(V_{CM} - V_{Diode})^2}{R1} = \frac{(400V - 10V)^2}{200k\Omega} = 0.76\,W \tag{4}$$

When selecting the value for resistor R1 it is important to consider several system requirements. Most important is maintaining enough current flow through the Zener diode at the lowest value of the common mode voltage required for system operation. For use at lower voltages a smaller resistor lets the Zener Diode run more safely further above its needed minimum current to maintain the voltage regulation but will also have an impact on the power dissipation at the higher common mode voltages.

3.3 PNP Transistor

The PNP transistor is used to stand off the high voltage while passing the current from the INA138 through to a ground referenced resistor. The most important requirement for the transistor is to be able to withstand the maximum voltage coming from the input. For the output accuracy it is also important to use a transistor with a high β_F (sometimes called h_{FE}, DC current Gain, current Gain) as this transistor parameter has an influence on the gain accuracy of the design.

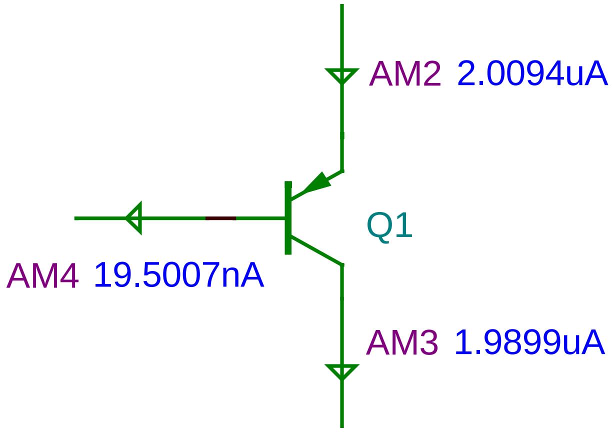

Figure 4 – Current through the PNP Transistor

Figure 4 – Current through the PNP Transistor shows the current running through a transistor with a β_F of roughly 100. A β_F of 100 means that approximately 1% of the current flowing through the emitter will not flow out the collector but instead will flow out of the base. This reduction in collector current due to the β_F adds a gain error of 1% to our whole system for a β_F equal to 100.

The PNP transistor can be exchanged by a P-Channel MOSFET. Replacing the bipolar transistor with a FET device will eliminate the gain error term due to the base current effects in the bipolar device. One downside is that V_{th} of high voltage FETs can be as high as 5V. This will require the output of INA138 to be 5V higher than the GND of the INA138. This can be a problem for lower common mode voltages and for Zener Diodes with low voltages.

4 Simulation

4.1 Steady State

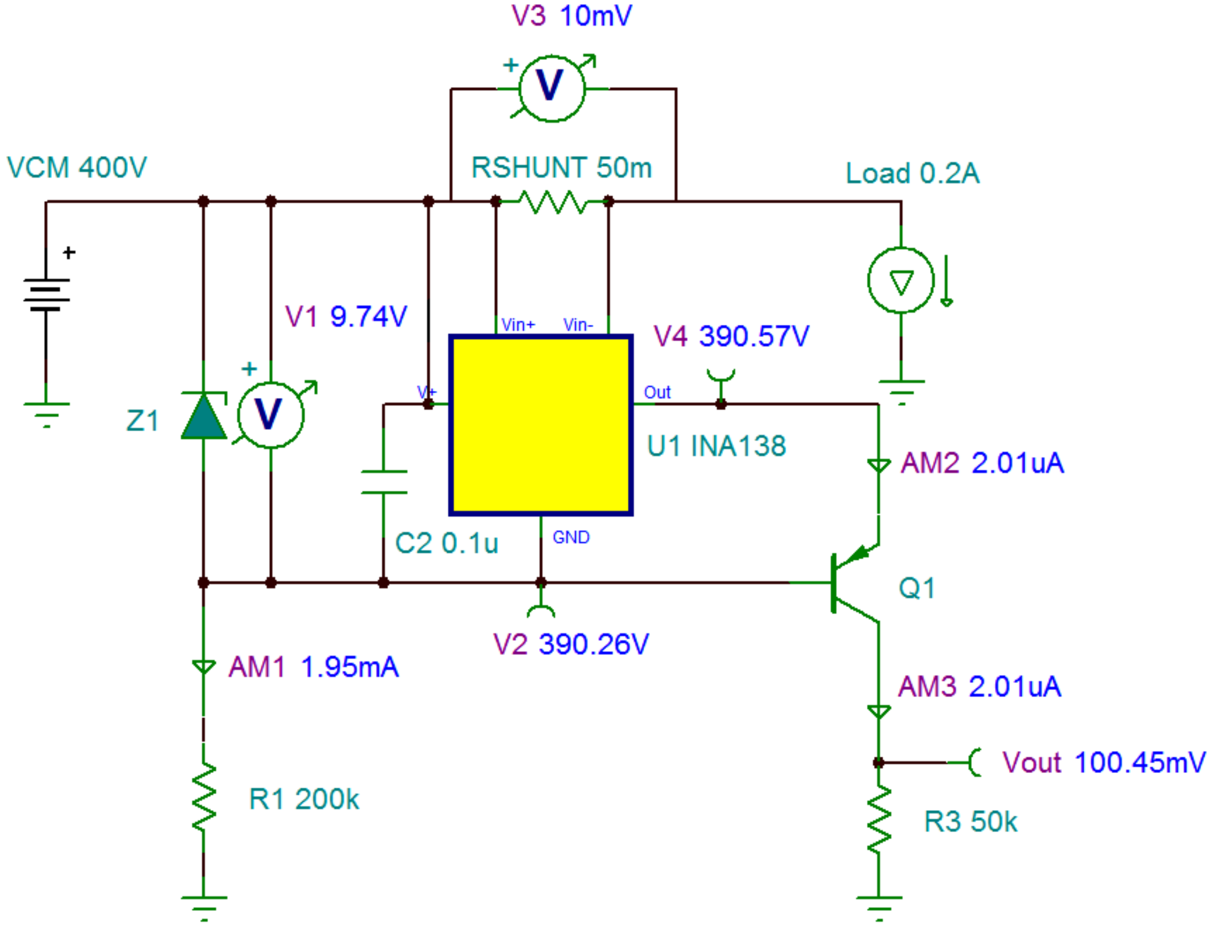

Figure 5 - DC Circuit Simulation

In Figure 5 - DC Circuit Simulation a steady state simulation of the circuit at 400V DC is illustrated. Note that with the component values illustrated the INA138 is biased from a floating 10V power supply created by the Zener diode. Approximately 2mA of current flows in R1. This current will vary according to the common mode voltage. The load current is set to 200mA and creates a voltage drop of 10mV across the shunt resistor. This input voltage is multiplied by the gain of the circuit, resulting in an output voltage of approximately 100mV.

4.2 Performance with different Common Mode Voltages

Table 2 - V_{out} over different Common Mode Voltages shows the common mode voltage (VCM), the voltage drop over the diode (V+ to INA-GND) which is also the INA138 supply voltage and the output voltage measured at R2 (V_{out}). In all simulations the load was set to 0.2A which generated a 10mV drop over the shunt resistor.

Table 2 - V_{out} over different Common Mode Voltages

VCM	V+ to INA_GND	V_{Out}	Relative Output Error
6.00 V	1.50 V	125.110 mV	25.11%
7.00 V	2.65 V	100.37 mV	0.37%
8.00 V	3.85 V	100.37 mV	0.37%
10.00 V	6.25 V	100.37 mV	0.37%
15.00 V	11.12 V	100.37 mV	0.37%
25.00 V	11.35 V	100.37 mV	0.37%
50.00 V	11.46 V	100.37 mV	0.37%
100.00 V	11.54 V	100.37 mV	0.37%
200.00 V	11.62 V	100.37 mV	0.37%
400.00 V	11.69 V	100.37 mV	0.37%

The simulation shows that for common mode voltages below 7V the supply voltage for the INA138 is too low. Since the INA138 model is not defined outside the datasheet specs the output shows strange behavior. But for all voltages above 7V the output behaves as it should and gives us 100.37mV. Because the common mode for the INA138 does not change significantly after 15V VCM the common mode rejection ratio of the whole system is very good and we get the same results over the full voltage range.

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

The PCB used in this design is 3” by 2”. Most of the space is used by the isolated banana jacks. The actual parts, excluding the shunt resistor, could be placed in a 0.5” by 0.5” area. The test pins are placed between the banana jacks so they are hard to touch by accident but still easy to reach with probes.

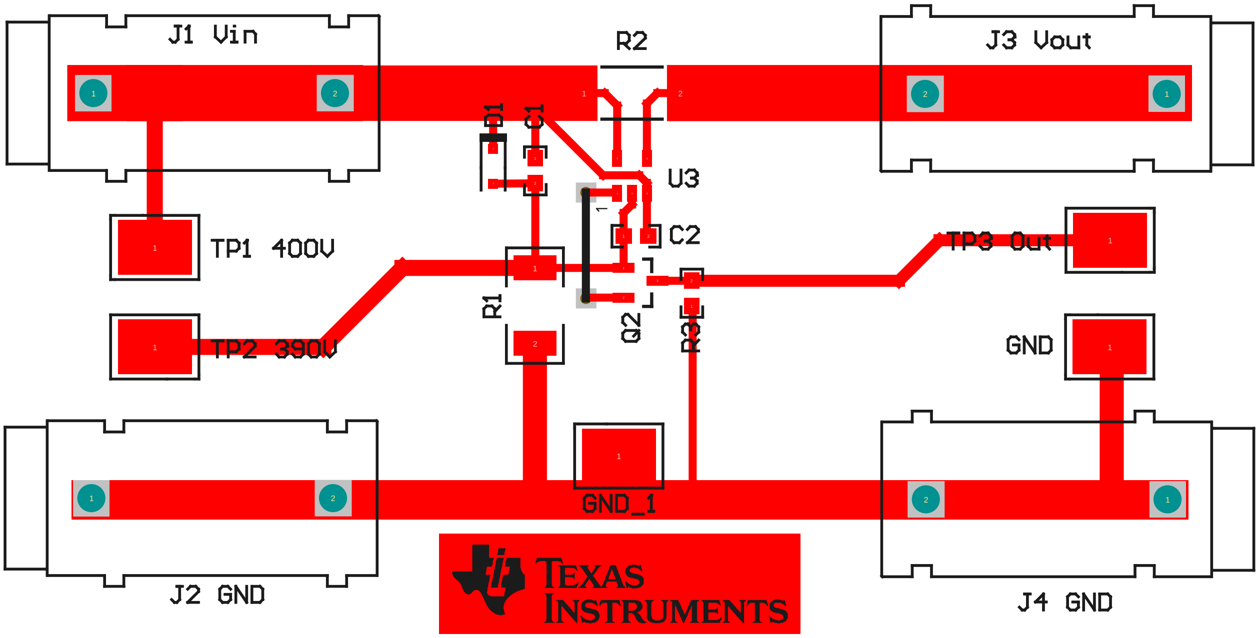

Figure 6 - PCB Layout

Also very important is to put a bypass cap (C2) close to the INA138. This makes the design a lot more stable and reduces the influence of noise which makes the results more accurate.

The layout for shunt voltage measurement is also important. The voltage sense lines should be connected to the inside of the shunt resistor pads as shown here. For shunt resistor values below 10mΩ a 4-wire force/sense pad layout is suggested. For more information refer to the Texas Instruments Application Note http://www.ti.com/lit/pdf/sboa137.

Due to the presence of high voltages, the spacing between high voltage pads and low voltage pads must to be considered. The PCB trace spacings used in this design meet the requirements specified in table 6-1 of the IPC-2221 standard for external conductors with conformal coating over assembly. The IPC-2221 “Generic Standard on Printed Board Design” specifies spacing requirements for various types of PCB construction, coating and applications.

6 Verification & Measured Performance

6.1 Performance with different Common Mode Voltages

Table 3 - Vout over different Common Mode Voltages shows the common mode voltage (VCM), the voltage drop over the diode (V+ to INA-GND) which is also the INA138 supply voltage and the output voltage measured at R2 (Vout). In all measurements the load was set to 0.2A which generated a 10mV drop over the shunt resistor.

Table 3 - V_{out} over different Common Mode Voltages

VCM	V+ to INA_GND	V_{Out}	Relative Output Error
6.00 V	1.45 V	0 mV	
7.00 V	1.75 V	96.29 mV	3.7%
8.00 V	2.35 V	95.79 mV	4.2%
10.00 V	4.58 V	94.97 mV	5.04%
15.00 V	10.62 V	95.07 mV	4.93%
25.00 V	11.95 V	95.08 mV	4.92%
50.00 V	11.95 V	95.23 mV	4.77%
100.00 V	11.99 V	95.59 mV	4.41%
200.00 V	12.00 V	95.50 mV	4.50%
400.00 V	12.01 V	95.55 mV	4.45%

The measurement shows that this particular device operates down to a common mode voltage of 7V resulting in a supply voltage for the INA138 of 1.75V. Since the INA138 is only specified down to a supply voltage of 2.7V it is not recommended to operate below a common mode voltage of 10V based on these results. The error of 5mV is mainly based on the input offset of maximum 1mV together with the amplification of 10V/V. From 10V to 400V the output only changes by 580µV indicating the superior common mode rejection ratio of this design over the full scale operating voltage range.

$$CMRR = 20 \cdot \log\left(\frac{\Delta V_{CMV}}{\Delta V_{Input}}\right) = 20 \cdot \log\left(\frac{390V}{58\mu V}\right) = 136dB \tag{5}$$

6.2 Maximum Relative Output Error

There are several main influences on the maximum output error

- The offset voltage of the INA138
- The initial CMRR of the INA138 and the system CMRR calculated in 6.1 with 58µV input related error
- The initial PSRR of the INA138
- The gain error due to β_F from the PNP transistor
- The shunt resistor accuracy
- The output resistor accuracy

6.2.1 Dominant Errors at Small Values of Load Current

When the load current is small there is a corresponding small input voltage to the INA138. Errors will be dominated primarily by the input offset related errors such as:

- The Input Offset Voltage (V_{OS})of the INA138
- The initial Common Mode Rejection (CMR) of the INA138
- The initial Power Supply Rejection (PSR) of the INA138

Because these errors are uncorrelated to one another they can be combined with a square root of the sum of the squares approach.

$$E_{Max} = \sqrt{\left(V_{OS}\right)^2 + \left(V_{CMR}\right)^2 + \left(V_{PSR}\right)^2} \quad (6)$$

Determining the errors associated with each of the three parameters is straightforward and described below.

Initial Offset Voltage Error

The maximum error due to input offset voltage can be taken directly from the INA138 device specification. The maximum input offset voltage is given as 1mV at 25˚C.

- V_{OS} = 1mV

Initial CMR Error

The maximum input offset error due to the common mode rejection of the INA138 (V_{CMR}) is calculated by determining the actual common mode voltage as applied to the INA138 with reference to the ground pin of the INA138. In this design this value is equal to the value of the zener voltage of approximately 10V. From the INA138 device specification the common mode rejection ratio minimum is given as 100dB (10µV/V), and since the test condition for the V+ input of the INA138 input offset voltage is with a 12V common mode voltage (CMV), the resulting common mode error is determined as:

$$V_{CMR} = \left|\left(CMV_{testcondition} - CMV_{actual}\right)\right| \times CMRR \quad (7)$$

$$V_{CMR} = \left|\left(12V - 10V\right)\right| \times 10\mu V / V = 20\mu V \quad (8)$$

This error term is described as “initial” as it is determined at a particular system common mode voltage that would result in a zener voltage equal to 10V. Any changes to the system common mode voltage will result in a very slight change in zener diode voltage, which in turn changes (albeit slightly) the common mode voltage applied to the INA138. In this case the results from section 5 can be used to estimate the common mode error if the common mode voltage is changing in the application.

Initial PSR Error

Similar to the initial common mode error, the initial error due to the power supply rejection of the INA138 can easily be determined. From the INA138 device specification the specified power supply voltage for the input offset voltage specification is given as 5V. Any deviation from 5V applied between the INA138 V+ pin and ground pin will result in an additional error, V_{PSR}. This error is determined as:

$$V_{PSR} = \left|\left(PSV_{testcondition} - PSV_{actual}\right)\right| \times PSRR \quad (9)$$

Where PSV is the power supply voltage applied between the V+ pin and ground pin of the INA138.

$$V_{PSR} = \left|\left(5V - 10V\right)\right| \times 10\mu V / V = 50\mu V \quad (10)$$

The total error at small load currents (input voltages) is calculated from equation **(**6**)** as:

$$E_{MAX} = \sqrt{1mV^2 + 20\mu V^2 + 50\mu V^2} = 1.001mV \quad (11)$$

6.2.2 Dominant Errors at Large Values of Load Current

At large load currents the input voltage developed across the shunt resistor will be at its maximum. This minimizes the percentage contribution of the errors from the initial error sources described above. The dominant errors sources for large inputs are:

- Gain error from the INA138
- Shunt resistor accuracy
- Output resistor accuracy

In this design it is assumed that the maximum INA138 gain error and resistor accuracy is 1%. Again because these error sources are uncorrelated to one another they can be combined with a square root of the sum of the squares approach.

$$E_{MAX} = \sqrt{INA138\_GAIN_{ERROR}{}^2 + SHUNT\_RESISTOR_{ERROR}{}^2 + OUTPUT\_RESISTOR_{ERROR}{}^2} \quad (12)$$

INA138 Gain Error

To determine the error due to the gain error of the INA138 we first determine the ideal maximum output voltage, V_{OUTMAX}. In this example it is assumed that the maximum load current is 6A resulting in a maximum output voltage of 3V. From the INA138 device specification the transconductance (gain) error is given as 1%. This in turn will result in an output referred error voltage of 30mV. Referring this output error back to the input it is required to divide by the gain of the circuit (10V/V). This results in an input referred gain error of 3mV.

Shunt Resistor Error

Similarly to the INA138 gain error the error contribution from the shunt resistor is determined in a similar fashion. In this example it is assumed that the maximum load current is 6A resulting in a maximum output voltage of 3V. It is also assumed that the shunt resistor tolerance is given as 1%. This in turn will result in an output referred error voltage of 30mV. Referring this output error back to the input it is required to divide by the gain of the circuit (10V/V). This results in an input referred error due to the tolerance of the shunt resistor of 3mV.

Output Resistor Error

Similarly to the INA138 gain error and the error due to the shunt resistor initial tolerance the error contribution from the output resistor is determined in a similar fashion. In this example it is assumed that the maximum load current is 6A resulting in a maximum output voltage of 3V. It is also assumed that the output resistor tolerance is given as 1%. This in turn will result in an output referred error voltage of 30mV. Referring this output error back to the input it is required to divide by the gain of the circuit (10V/V). This results in an input referred error due to the tolerance of the output resistor of 3mV.

Summing these errors results in:

$$E_{MAX} = \sqrt{3mV^2 + 3mV^2 + 3mV^2} = 5.2mV \tag{13}$$

The total error at the large load currents will also include the initial errors due to Vos, CMR and PSR resulting in a total error of:

$$TotalError_{RTI} = \sqrt{5.2mV^2 + 1.001mV^2} = 5.3mV \tag{14}$$

Total Error expressed as a percentage of the input voltage is given by:

$$TotalError\% = 100 \times \frac{InputErrorVoltage}{InputVoltage} \tag{15}$$

In general all errors can be combined statistically with the sum of the square roots.

$$E_{Max} = \sqrt{(V_{OS})^2 + (V_{CMRR})^2 + (V_{PSRR})^2 + (V_{Shunt} \cdot G_{Error})^2 + (V_{Shunt} \cdot G_{Shunt-Error})^2 + (V_{Shunt} \cdot G_{\mathrm{Re}s-Error})^2} \tag{16}$$

The maximum error over the shunt resistor drop voltage (blue curve) is plotted in Figure 7 – Maximum Relative Output Error The red curve shows the measured values which are a lot lower than the maximum possible values in our case.

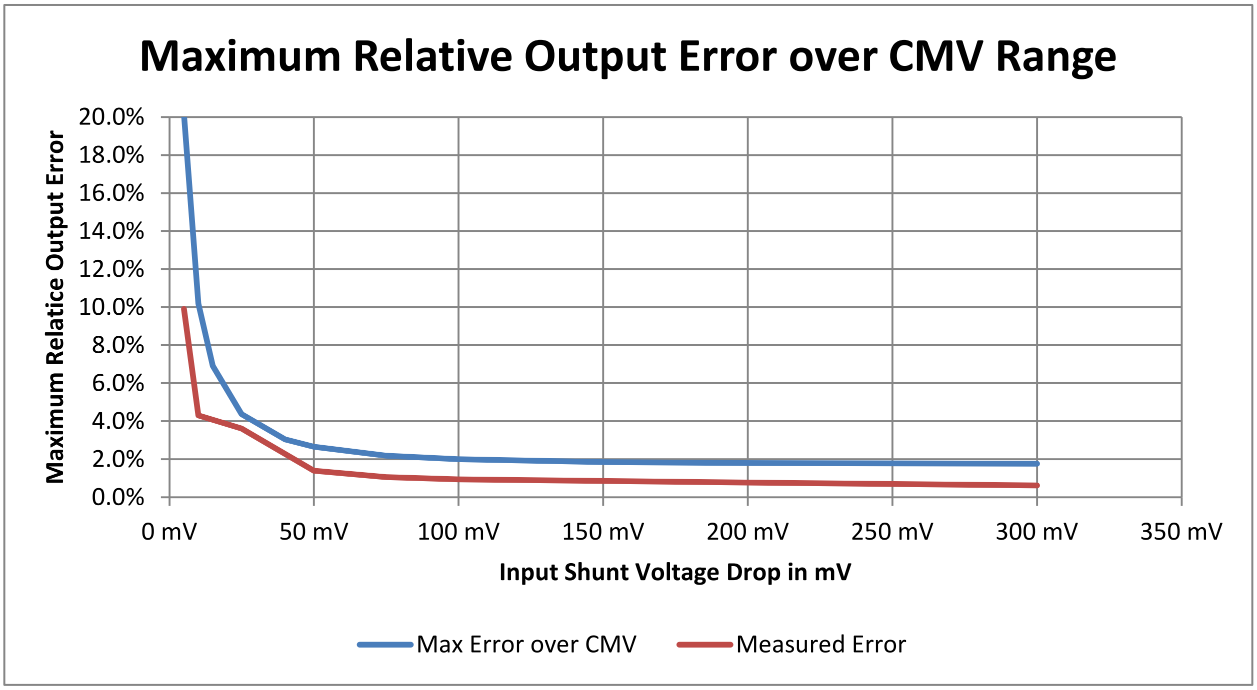

Figure 7 – Maximum Relative Output Error

7 About the Author

Simon Forstner is a field applications engineer at Texas Instruments. Simon graduated from the University of Applied Science in Munich where he earned a Bachelor of Electrical Engineering and a Master of Systems Engineering.

Appendix A.

A.1 Electrical Schematic

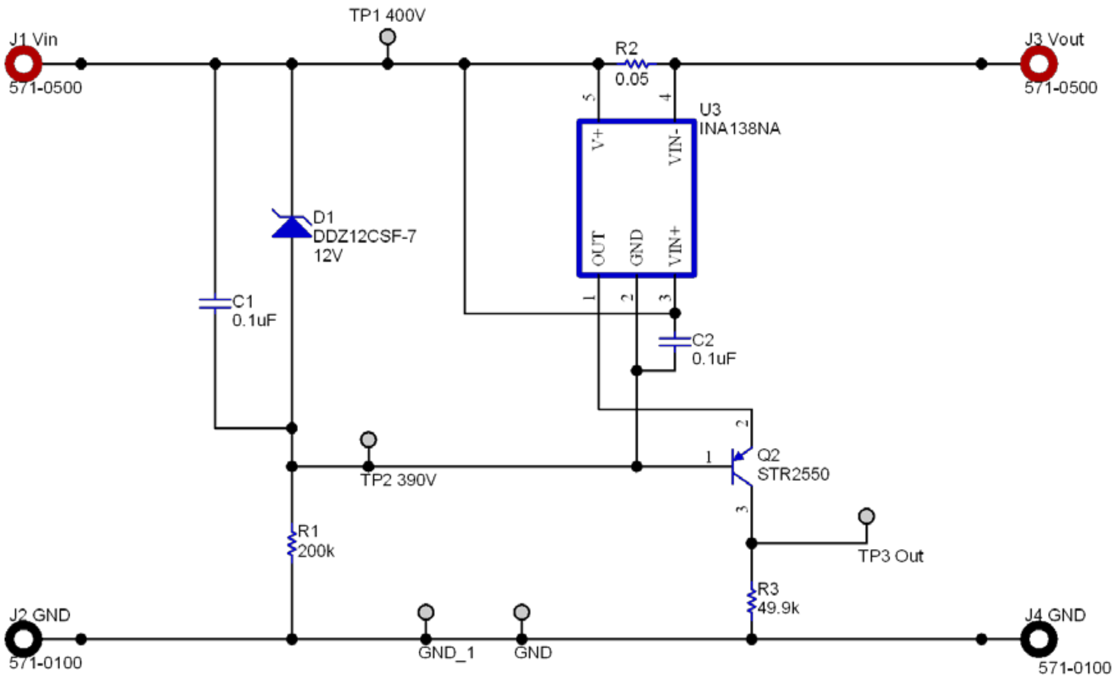

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item #	Quantity	Value	Designator	Description	Manufacturer	Manufacturer Part Number	Alternative Part Number
1	2	10pF	C1, C2	CAP, CERM, 10pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C100J5GACTU	CL10C100JB8NCNC
2	1	12V	D1	Diode, Zener, 12V, 500mW, SOD-323	Diodes Inc.	DDZ12CSF-7	MM3Z12VST1G
3	5	SMT	GND, GND_1, TP3 Out, TP1 400V, TP2 390V	Test Point, Compact, SMT	Keystone	5016	
4	2	10A	J1 Vin, J3 Vout	Standard Banana Jack, insulated, 10A, red	DEM Manufacturing	571-0500	
5	2	10A	J2 GND, J4 GND	Standard Banana Jack, insulated, 10A, black	DEM Manufacturing	571-0100	
6	1	500V	Q2	Transistor, PNP, 500V, 0.5A, SOT-23	ST	STR2550	PBHV9050T,215
7	1	200k	R1	RES, 200kohm, 1%, 1W, 2010	Vishay-Dale	CRCW20101R00JNEFHP	CRM2010-FX-2003ELF
8	1	0.05	R2	RES, 0.05 ohm, 1%, 2W, 2512	Stackpole Electronics Inc	CSRN2512FK50L0	PF2512FKF7W0R05L
9	1	49.9k	R3	RES, 49.9k ohm, 1%, 0.1W, 0603	Rohm Semiconductor	MCR03ERTF4992	RC1608F4992CS
10	1	INA138	U3	IC, High-Side Measurement Current Shunt Monitor	TI		

Figure A-2: Bill of Materials

Cautions and Warnings

WARNING:

Voltages of 400V can be possibly deadly. So please proceed with maximum caution and never handle the device alone.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

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