TI Designs
Piezo Speaker Strobe Notification Reference Design

![Texas Instruments logo]

TI Designs

This TI Design uses Texas Instruments' industrial piezo driver, flash LED driver, and the Ultra-Low-Power FRAM Microcontroller (MCU) to demonstrate implementation of both audible and visual notification subsystems, primarily intended for fire alert end-equipment systems.

Design Resources

TIDA-00376	Design Folder
DRV2700	Product Folder
LM3550	Product Folder
MSP430FR5969	Product Folder
LMR14030	Product Folder
LMV344	Product Folder
CSD15571Q2	Product Folder
TPD1E10B06	Product Folder
TPD6F003	Product Folder

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Design Features

- Meets NFPA 72 Code Requirements for Audible and Visual Notification Devices
- 86.5 dBA @ 3 m (520-Hz Square Wave)
- 80.5 dBA @ 3 m (2.84-kHz Sine Wave)
- 77.5 dBA @ 3 m (Pre-Recorded Speech)
- 300 candela @ 3 m (Flash Mode)
- 1.44-W Power Consumption (Audible and Visual Notification)
- 6.432-mW Power Consumption (Standby Mode)

Featured Applications

- Industrial
- Building Automation
- Fire Alarm
- Security Alarm
- Notification Appliance
- Sounder
- Speaker Strobe
- Horn Strobe
- Voice Evacuation

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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Input voltage	8-V to 28.8-V DC	Section 2.5
Regulated voltage rail	3.3 V ±10%, 3-A maximum output current	Section 2.5
Visual notification element	2 × Osram 2-W LED (4000K color temperature)	Section 2.3
Visual output options	Charge Mode, Torch Mode, Flash Mode	Section 4.3
Visual output level	300 Candela	Section 6.3.2
Visual output standard	NFPA 72, Section 18.5.3 NFPA 72, Section 18.5.5.6	Section 4.2.4
Audible notification element	PUI Audio Piezo Transducer	Section 4.1.1
Audible output options	520-Hz square wave, 2.84-kHz sine wave, pre-programmed speech file, white noise	Section 4.3
Audible output level	86.5 dBA @ 3 m (520-Hz square wave) 80.5 dBA @ 3 m (2.84-kHz sine wave) 77.5 dBA @ 3 m (pre-recorded speech)	Section 6.2.3
Audible output standard	NFPA 72, Section 18.4.1.5 NFPA 72, Section 18.4.3.1	Section 4.1.4
Operating temperature	–30°C to 70°C (limited by LM3550 and supercapacitor)	Section 3.1.2
Form factor	3.45×4.0-inch rectangular PCB	Section 5.1

2 System Description

Many industrial and building automation systems require visual and audible notification devices to alert those in close proximity to some sort of event. Many legacy notification devices use xenon flash bulbs for visual strobe notification and dynamic speakers for audible notification. However, industrial trends are shifting towards the use of light-emitting diodes (LEDs) and piezo transducers for notification devices to reduce both system size and power consumption.

Furthermore, there are code standards throughout the world that specify the performance requirements for visual and audible notification devices. In this TI Design, the United States-based National Fire Protection Association (NFPA) code governing fire alarm and signaling was used to guide design decisions.

Enabled by Texas Instruments' industrial piezo driver, flash LED driver, ultra-low power MCU, analog signal conditioning, and power management technologies, the Piezo Speaker Strobe Notification Reference Design TI Design demonstrates a method to produce visual and audible notifications that meet the requirements of the NFPA code for fire alarm notification devices.

At a high level, the Piezo Speaker Strobe Notification Reference Design system consists of a high-voltage piezo driver, piezo transducer, pulse-width modulation (PWM) signal conditioning, flash LED driver, high current LEDs, system MCU, and power management.

The system MCU controls both the visual and audible notification sub-systems using several push-buttons. Several audible modes are demonstrated, including a 520-Hz square wave, 2.84-kHz sine wave, pre-recorded speech file, and white noise. The flash LED driver operates in the normal, high-current flash mode as well as a lower current torch mode.

This design guide addresses component selection, design theory, and test results of the TI Design system. The scope of this design guide gives system designers a head-start in integrating TI's industrial piezo driver, flash LED driver, ultra-low-power MCU, analog signal conditioning, and power management technologies into their end-equipment systems.

The following sub-sections describe the various blocks within the TI Design system and what characteristics are most critical to best implement the corresponding function.

2.1 High Voltage Piezo Driver and Piezo Transducer

In the Piezo Speaker Strobe Notification Reference Design, a piezo transducer was chosen to be the primary method of audible notification. Piezo transducers generally have lower power consumption than dynamic speakers, particularly for narrow-bandwidth alarm signals that require a high sound pressure level (SPL) to meet regulatory requirements. To drive a piezo transducer, a high-voltage industrial piezo driver from Texas Instruments was selected. TI's industrial piezo driver technology is highly integrated, which minimizes end-equipment size, and it is capable of driving high voltages, which enables the use of less expensive, higher voltage piezo transducers.

With a direct-drive piezo voltage of 200 V_{PP}, the DRV2700 device from Texas Instruments is ideally suited to drive high-voltage piezo transducers. In addition, the short start-up time of 1.5 ms enables fast system response time to commands to begin producing an alert notification.

The AB5027B-3-LW100-R piezo bender from PUI Audio Inc. (www.PUIAudio.com) is ideally suited for audible notification end equipment systems, because it has been designed to provide resonant peaks at two common alert notification frequencies. In addition, this piezo transducer has low capacitance, which corresponds to its lower power consumption.

The relevant system theory and design details for the high voltage piezo driver and piezo transducer can be found in Section 4.1.1 and Section 4.1.2.

2.2 PWM Signal Conditioning

In the Piezo Speaker Strobe Notification Reference Design, the audible tones and notifications are produced by means of PWM signal generation. To prevent the PWM carrier frequency from entering the DRV2700 device, it is necessary to use analog signal conditioning. Furthermore, the DRV2700 has four fixed gain settings, which necessitates having a controlled maximum input voltage to prevent clipping of the output signal.

With TI's broad portfolio of general purpose amplifiers, this PWM signal conditioning is simple to implement. This design uses a three-stage approach: a voltage-divider followed by an op-amp buffer to control the amplitude of the input signal, and then two stages of low-pass filtering to eliminate the PWM carrier frequency. The LMV344 quad op-amp device is ideally suited to perform this PWM signal conditioning, while remaining extremely cost-sensitive.

The relevant system theory, design details, and simulation results for the PWM signal conditioning can be found in Section 4.1.3.

2.3 Flash LED Driver and High Current LEDs

The Piezo Speaker Strobe Notification Reference Design is able to draw a constant amount of current and still provide a high-intensity visual notification using high current LEDs by means of TI's flash LED driver technology. The selected driver uses a supercapacitor as the primary power source for the LEDs during a flash event. This enables a relatively low constant input current, which reduces voltage sag on the overall alert notification device power supply, while still allowing a very high current flash pulse.

The LM3550 flash LED driver was chosen to power and control the high current LEDs. This LED driver charges and controls a supercapacitor, as well as controlling an external NFET, which drives the high current LEDs.

Because of the high light output, the GW CSSRM1.PC-MTNP-5L7N-1 compact 2-W high power LED was chosen from Osram Opto Semiconductors (www.osram-os.com). With a maximum surge current of 2 A and a wide viewing angle of 120º, these LEDs are ideally suited for a visual strobe notification application.

The relevant system theory and design details for the flash LED driver and high current LEDs can be found in Section 4.2.

2.4 System MCU

The Piezo Speaker Strobe Notification Reference Design has several requirements for the system microcontroller. The LM3550 device communicates with the system MCU through I²C and also can use two general-purpose input output (GPIO) pins. The DRV2700 device is controlled by three GPIO pins, two for gain control, and one for overall device enable. The DRV2700 device is driven by a PWM-based audio source, which requires a Timer_B module for optimal performance. To achieve appropriate levels of audio fidelity, a minimum processor clock frequency of 8 MHz is required. There are three user push-buttons in this TI Design to cycle through the various operating modes, which use three GPIO pins.

Because this TI Design is meant to demonstrate TI technology, the MSP430FR5969 device was selected as the system MCU. This device fulfills all the requirements of this TI Design system, and features ultra-low power performance.

The relevant system theory, design details, and firmware description for the system MCU can be found in Section 4.3.

2.5   Power Management

The two most common power configurations for notification end-equipment systems is a line powered power source (100-V to 240-V AC, dependent on region) or a pre-regulated DC voltage, usually 24-V DC. The nominal power source for the Piezo Speaker Strobe Notification Reference Design is a 24-V DC voltage rail. This was specified to provide a universal platform for evaluation of the visual and audible notification implementation of TI technology.

It is common for end-equipment systems powered by a 24-V DC rail to have a wide specified voltage tolerance, as the 24-V DC power source is often powering many nodes connected together on a lengthy wire loop. Therefore, this TI Design was designed conservatively, with an input voltage range of 8 to 28.8 V.

All of the components in this TI Design can operate from 3.3 V; therefore, this was chosen as the primary regulated power rail. Because both the audible and visual notification subsystems potentially draw large amounts of current, a DC-DC buck converter was necessary to maintain efficient power conversion. A conservative maximum current of 3 A was defined to ensure enough point-of-load power was available to the TI Design system.

Using the WEBENCH Designer tool, the LMR14030 device was selected as an ideal compromise between efficiency and overall cost. However, integrating the technology demonstrated in this TI Design into an end-equipment system may necessitate a different power management configuration. WEBENCH Designer is an excellent tool to quickly and easily explore TI's broad power management portfolio to identify the ideal solution.

2.6   EMI Protection

The Piezo Speaker Strobe Notification Reference Design was designed to have robust protection against electromagnetic interference (EMI), particularly on the input power lines. Since every end-equipment system will have different power architectures, and thus, a different protection scheme against EMI, this TI Design demonstrates that a real system can be built to comply with the various EMI standards (IEC61000). The EMI test results give confidence that TI's technology can comply with EMI standards, given proper system design.

The primary EMI protection circuitry is located near the power input connectors as well as the JTAG programming connector. There is a protection network of discrete devices on the main power input net. This consists of a high-voltage (2 kV) shunt capacitor to ground, transient voltage suppression (TVS) device, common-mode choke, and fast bypass capacitor. This network protects against transient voltages and currents on the main power input as well as reduces differential-mode and common-mode RF transients.

The TPD1E10B06 single-channel ESD protection device was chosen to protect the JTAG programming interface. The TPD6F003 6-channel EMI filter with integrated ESD protection device was chosen to protect the data pins of the optional microSD card.

## 3   Block Diagram
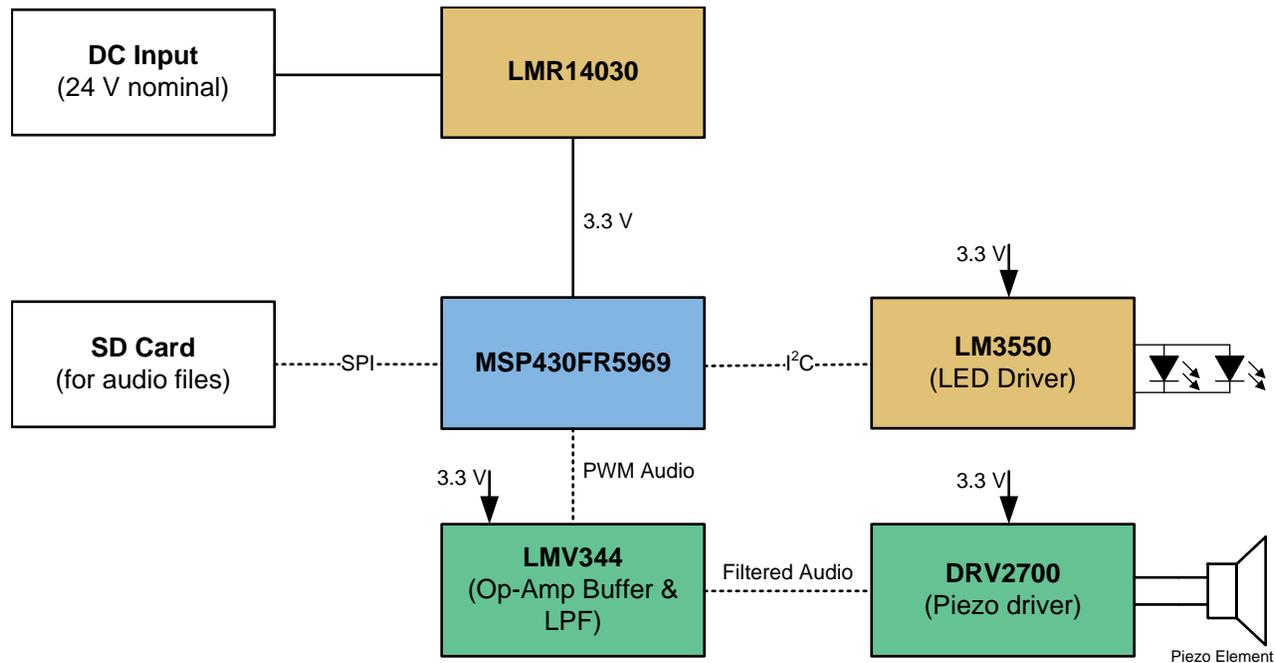
Figure 1. Piezo Speaker Strobe Notification Reference Design System Block Diagram

3.1   Highlighted Products

The Piezo Speaker Strobe Notification Reference Design Reference Design features the following devices:

*   DRV2700: Industrial Piezo Driver with Integrated Boost Converter
*   LM3550: Flash LED Driver with Automatic Vf and ESR Detection
*   MSP430FR5969: 16-MHz Ultra-Low-Power Microcontroller featuring 64 KB FRAM, 2 KB SRAM, 40 IO
*   LMR14030: Simple Switcher® 40-V, 3.5 A, 2.2 MHz Step-Down Converter with 40 µA I_Q
*   LMV344: Quad Rail-to-Rail Output CMOS Operational Amplifier with Shutdown
*   CSD15571Q2: 20-V N-Channel NexFET™ Power MOSFET
*   TPD1E10B06: Single-Channel ESD in a 0402 Package with 10-pF Capacitance and 6-V Breakdown
*   TPD6F003: 6-Channel EMI Filter with Integrated ESD Protection

For more information on each of these devices, see their respective product folders at www.ti.com.

3.1.1 DRV2700

The DRV2700 device is a single-chip piezo driver with an integrated 105-V boost switch, integrated power diode, and integrated fully-differential amplifier. This versatile device is capable of driving both high-voltage and low-voltage piezoelectric loads. The input signal can be either differential or single-ended and AC or DC coupled. The DRV2700 device supports four GPIO-controlled gains: 28.8 dB, 34.8 dB, 38.4 dB, and 40.7 dB.

The boost voltage is set using two external resistors. The boost current-limit is programmable through the $R_{(REXT)}$ resistor. The boost converter architecture does not allow the demand on the supply current to exceed the limit set by the $R_{(REXT)}$ resistor, which allows the user to optimize the DRV2700 circuit for a given inductor based on the desired performance requirements. Additionally, this boost converter is based on a hysteretic architecture to minimize switching losses and therefore increase efficiency.

A typical startup time of 1.5 ms makes the DRV2700 device an ideal piezo driver for coming out of sleep quickly. Thermal overload protection prevents the device from damage when overdriven.
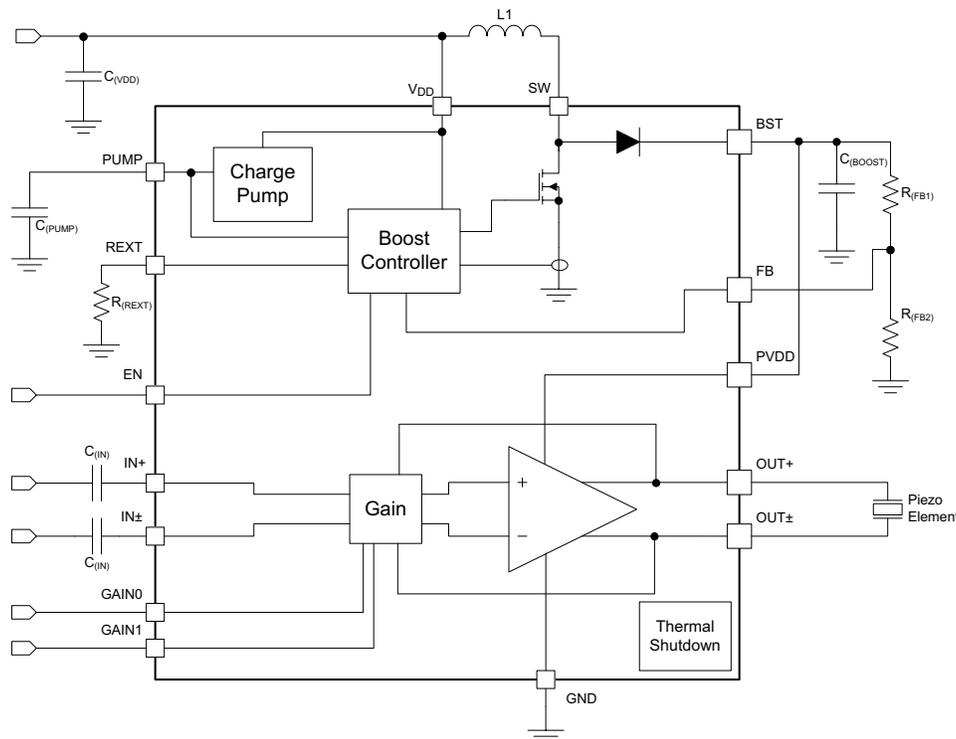
Figure 2. DRV2700 Functional Block Diagram

Features:
- 100-V boost or 1-kV flyback configuration
- ±100-V piezo driver in boost + amplifier configuration
  - 4 GPIO-adjustable gains
  - Differential or single-ended output
  - Low-voltage control
  - AC and DC output control
- 0- to 1-kV Piezo driver in flyback configuration
  - Low-voltage control
  - AC and DC output control
- Integrated boost or flyback converter
  - Adjustable current-limit
  - Integrated power FET and diode
- Fast startup time of 1.5 ms
- Wide supply-voltage range of 3 to 5.5 V
- 4×4×0.9-mm VQFN package
- 1.8-V compatible digital pins
- Thermal protection

3.1.2 LM3550

LM3550 is a low-noise, switched-capacitor DC-DC converter designed to operate as a current-limited and adjustable (up to 5.3 V) supercapacitor charger. LM3550 features user-selectable supercapacitor charge-termination voltages and an optimal charge-termination mode that maximizes flash-energy efficiency by accounting for flash element losses. Additionally, the device provides one adjustable constant current output (up to 200 mA) and one NFET controller ideal for driving one or more high-current LEDs either in a high-power flash mode or a low-power torch mode.
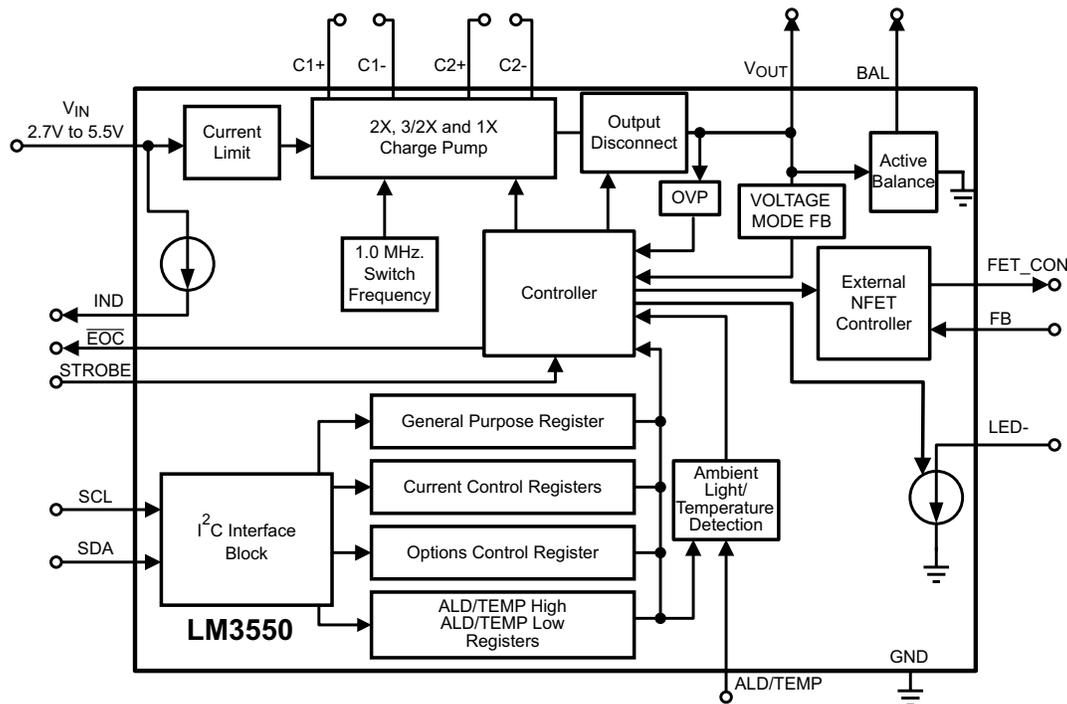
Figure 3. LM3550 Functional Block Diagram

Features:

- Up to 5-A flash current
- Four selectable supercapacitor charge voltage levels (4.5 V, 5.0 V, 5.3 V, optimized)
- Flash optimized charge mode for optimal efficiency
  - 33% faster charge time using optimal mode
  - 49% less power dissipated in current source using optimal charge mode
- Fast supercapacitor charger with 500-mA input current limit
- Adjustable torch current (60 to 200 mA)
- Ambient light or LED thermal sensing with current scaleback
- End-of-charge output ($\overline{EOC}$)
- Dedicated indicator LED current source
- No inductor required
- Manual flash enable through strobe pin input
- Programmable flash pulse duration, and torch and flash currents through I[2]C-compatible interface
- True shutdown (LED disconnect)
- Flash time-out protection
- LED temperature protection or ambient light sensing pin
- Low profile 20-Pin UQFN package (3.0 × 2.5 × 0.8 mm)

3.1.3 MSP430FR5969

The MSP430™ ultra-low-power FRAM platform combines uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing innovators to increase performance at lowered energy budgets. FRAM technology combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash at much lower power.

The MSP430 ultra-low-power FRAM portfolio consists of a diverse set of devices featuring FRAM, the ultra-low-power 16-bit MSP430 CPU, and intelligent peripherals targeted for various applications. The ultra-low-power architecture showcases seven low-power modes, optimized to achieve extended battery life in energy-challenged applications.
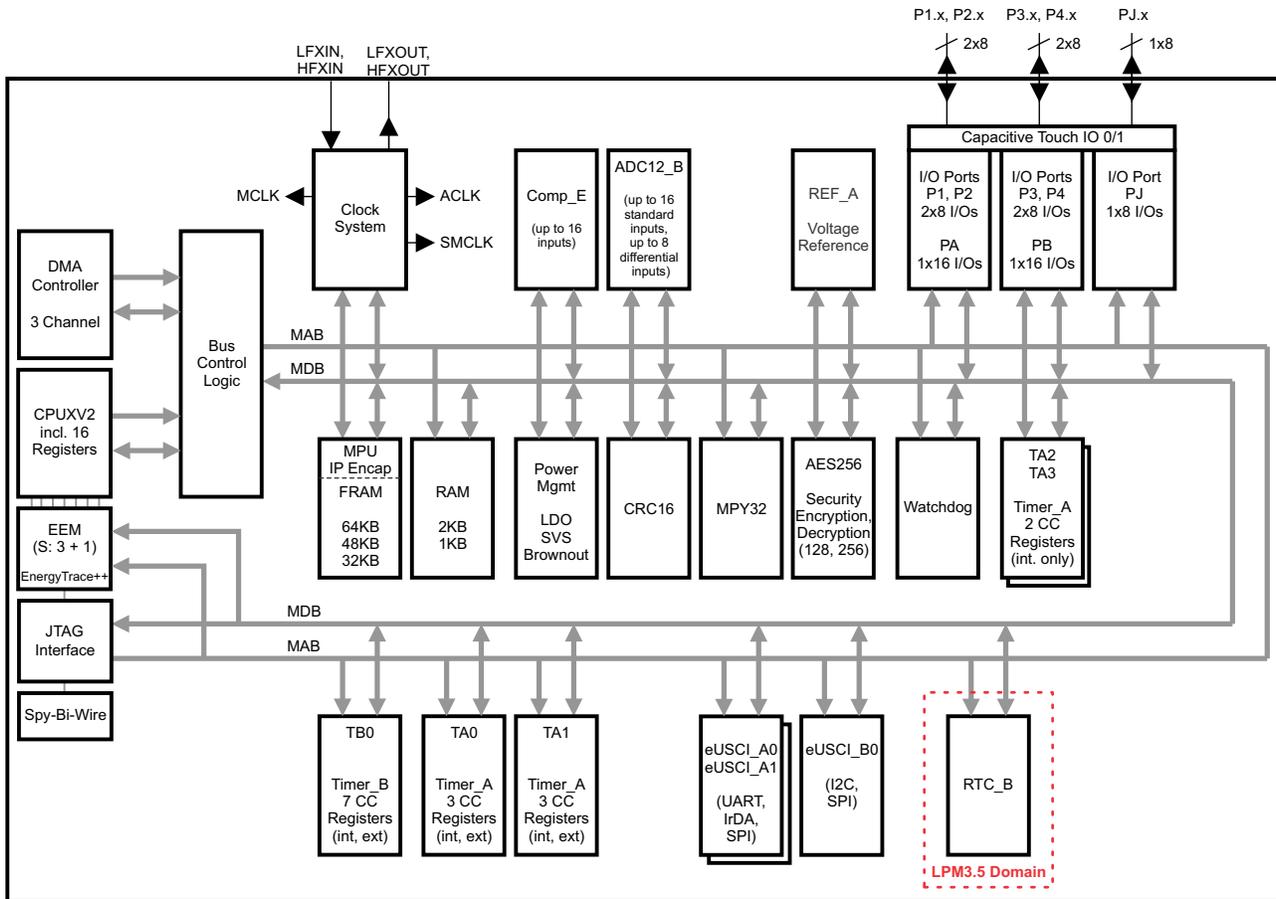
Figure 4. MSP430FR5969 Functional Block Diagram

Features:

- Embedded microcontroller
  - 16-bit RISC architecture up to 16-MHz clock
  - Wide supply voltage range (1.8 to 3.6 V) [1]
- Optimized ultra-low-power modes
  - Active mode: Approximately 100 µA/MHz
  - Standby (LPM3 with VLO): 0.4 µA (typical)
  - Real-time clock (RTC; LPM3.5): 0.25 µA (typical) [2]
  - Shutdown (LPM4.5): 0.02 µA (typical)

[1] Minimum supply voltage is restricted by SVS levels.
[2] RTC is clocked by a 3.7-pF crystal.

- Ultra-low-power Ferroelectric RAM (FRAM)
  - Up to 64 KB of nonvolatile memory
  - Ultra-low-power writes
  - Fast write at 125 ns per word (64 KB in 4 ms)
  - Unified memory = Program + Data + Storage in one single space
  - 10^{15} write cycle endurance
  - Radiation resistant and nonmagnetic
- Intelligent digital peripherals
  - 32-bit hardware multiplier (MPY)
  - Three-channel internal DMA
  - RTC with calendar and alarm functions
  - Five 16-bit timers with up to seven capture/compare registers each
  - 16-bit cyclic redundancy checker (CRC)
- High-performance analog
  - 16-channel analog comparator
  - 12-bit analog-to-digital converter (ADC) with internal reference and sample-and-hold and up to 16 external input channels
- Multifunction I/O ports
  - All pins support capacitive touch capability with no need for external components
  - Accessible bit-, byte-, and word-wise (in pairs)
  - Edge-selectable wake from LPM on all ports
  - Programmable pullup and pulldown on all ports
- Code security and encryption
  - 128-bit or 256-bit AES security encryption and decryption coprocessor
  - Random number seed for random number generation algorithms
- Enhanced serial communication
  - eUSCI_A0 and eUSCI_A1 support
    - UART with automatic baud-rate detection
    - IrDA encode and decode
    - SPI at rates up to 10 Mbps
  - eUSCI_B0 supports
    - I²C with multiple slave addressing
    - SPI at rates up to 8 Mbps
  - Hardware UART and I²C bootstrap loader (BSL)
- Flexible clock system
  - Fixed-frequency DCO with 10 selectable factory-trimmed frequencies
  - Low-power low-frequency internal clock source (VLO)
  - 32-kHz crystals (LFXT)
  - High-frequency crystals (HFXT)
- Development tools and software
  - Free professional development environments with EnergyTrace++™ technology
  - Development kit (MSP-TS430RGZ48C)
- Family members
- For complete module descriptions, see the *MSP430FR58xx, MSP430FR59xx MSP430FR68xx, and MSP430FR69xx Family User's Guide* (SLAU367).

3.1.4   LMR14030

The LMR14030 is a 40-V, 3.5-A step-down regulator with an integrated high-side MOSFET. With a wide input range from 4 to 40 V, it is suitable for various applications from industrial to automotive for power conditioning from unregulated sources. The regulator's quiescent current is 40 µA in Sleep Mode, which is suitable for battery powered systems. An ultra-low 1-µA current in shutdown mode can further prolong battery life. A wide adjustable switching frequency range allows either efficiency or external component size to be optimized. Internal loop compensation means that the user is free from the tedious task of loop compensation design. This also minimizes the external components of the device. A precision enable input allows simplification of regulator control and system power sequencing. The device also has built-in protection features such as cycle-by-cycle current limit, thermal sensing and shutdown due to excessive power dissipation, and output overvoltage protection.
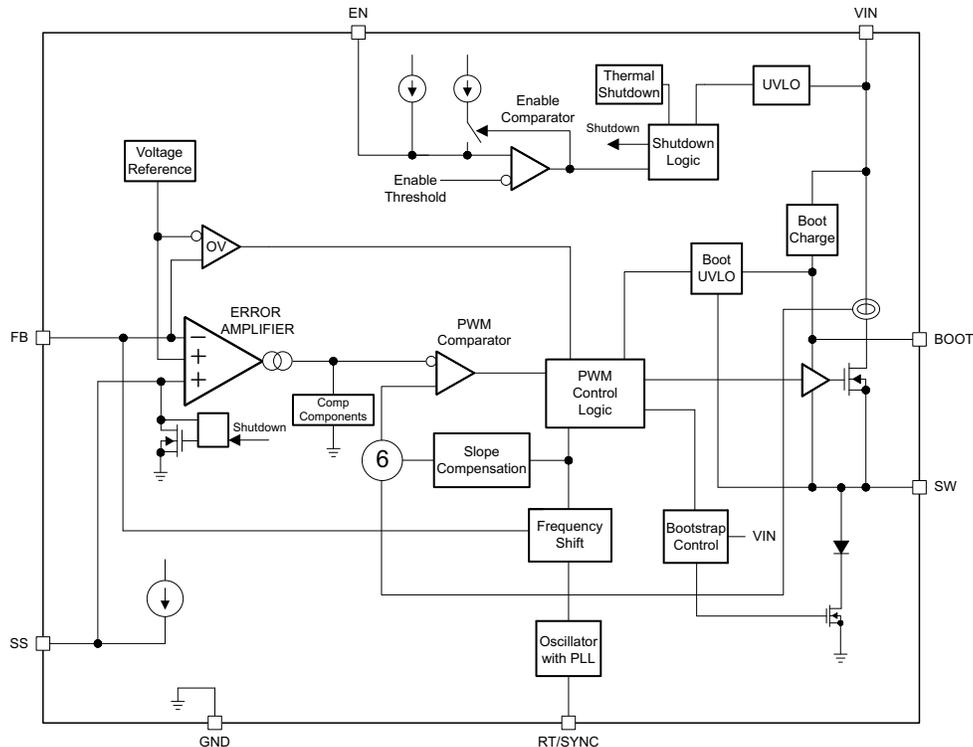
Figure 5. LMR14030 Functional Block Diagram

Features:

- 4- to 40-V input range
- 3.5-A continuous output current
- Ultra-low 40-µA operating quiescent current
- 90-mΩ high-side MOSFET
- Minimum switch-on time: 75 ns
- Current mode control
- Frequency synchronization to external clock

- Adjustable switching frequency from 200 kHz to 2.5 MHz
- Internal compensation for ease of use
- High duty cycle operation supported
- Precision enable input
- 1-µA shutdown current
- External soft-start
- Thermal, overvoltage, and short protection
- 8-pin HSOIC with PowerPAD™ package

3.1.5 LMV344

The LMV341, LMV342, LMV344 devices are single, dual, and quad CMOS operational amplifiers, respectively, with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1 pA (typ) and an offset voltage of 0.25 mV (typ). The single supply amplifier is designed specifically for low-voltage (2.7 to 5 V) operation, with a wide common-mode input voltage range that typically extends from –0.2 to 0.8 V from the positive supply rail. The LMV341 (single) also offers a shutdown ($\overline{SHDN}$) pin that can be used to disable the device. In shutdown mode, the supply current is reduced to 33 nA (typ). Additional features of the family are a 20-nV/$\sqrt{Hz}$ voltage noise at 10 kHz, 1-MHz unity-gain bandwidth, 1-V/µs slew rate, and 100-µA current consumption per channel.

Offered in both the SOT-23 and smaller SC-70 packages, the LMV341 is suitable for the most space-constraint applications. The LMV342 dual device is offered in the standard SOIC and MSOP packages. An extended industrial temperature range from –40°C to 125°C makes these devices suitable in a wide variety of commercial and industrial environments.

1OUT	1	14	4OUT
1IN−	2	13	4IN−
1IN+	3	12	4IN+
V+	4	11	GND
2IN+	5	10	3IN+
2IN−	6	9	3IN−
2OUT	7	8	3OUT
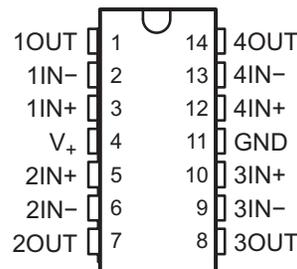
Figure 6. LMV344 Device Configuration

Features:
- 2.7-V and 5-V performance
- Rail-to-rail output swing
- Input bias current: 1 pA (typical)
- Input offset voltage: 0.25 mV (typical)
- Low supply current: 100 µA (typical)
- Low shutdown current: 45 pA (typical)
- Gain bandwidth: 1 MHz (typical)
- Slew rate: 1 V/µs (typical)
- Turn-on time from shutdown: 5 µs (typical)
- Input referred voltage noise (at 10 kHz): 20 nV/$\sqrt{Hz}$
- ESD protection exceeds JESD 22:
    – 2000-V human-body model (A114-A)
    – 200-V machine model (A115-A)

3.1.6   CSD15571Q2

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and load management applications. The SON 2×2 offers excellent thermal performance for the size of the package.
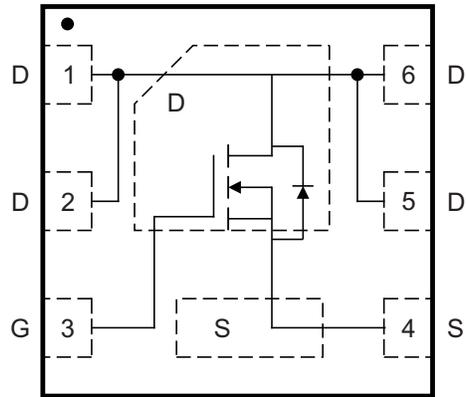
Figure 7. CSD15571Q2 Device Configuration

Features:
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb free terminal plating
- RoHS compliant
- Halogen free
- SON 2×2-mm plastic package

3.1.7 TPD1E10B06

The TPD1E10B06 device is a single-channel ESD TVS diode in a small 0402 package. This TVS protection product offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. The 12-pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps. The 0402 package is an industry standard and is convenient for component placement in space-saving applications.

Typical applications of this ESD protection product are circuit protection for audio lines (microphone, earphone, and speakerphone), SD interfacing, keypad or other buttons, VBUS pin and ID pin of USB ports, and general-purpose I/O ports. This ESD clamp is good for the protection of the end equipment like ebooks, tablets, remote controllers, wearables, set-top boxes, and electronic point of sale equipment.

Figure 8. TPD1E10B06 Functional Block Diagram

Features:

- Provides system-level ESD protection for low-voltage I/O interface
- IEC 61000-4-2 Level 4
  - >±30 kV (air-gap discharge)
  - >±30 kV (contact discharge)
- IEC 61000-4-5 (Surge): 6 A (8/20 µs)
- I/O capacitance: 12 pF (typical)
- R_{DYN}: 0.4 Ω (typical)
- DC breakdown voltage: ±6 V (minimum)
- Ultra-low leakage current: 100 nA (maximum)
- 10-V clamping voltage (max at I_{PP} = 1 A)
- Industrial temperature range: –40°C to 125°C
- Space-saving 0402 footprint (1 × 0.6 × 0.5 mm)

3.1.8   TPD6F003

The TPDxF003 family is a series of highly integrated devices designed to provide EMI filtering in all systems subjected to EMI. These filters also provide a TVS diode circuit for ESD protection, which prevents damage to the application when subjected to ESD stress far exceeding IEC 61000-4-2 (Level 4).

The TPDxF003 family is specified for –40°C to 85°C operation. These filters are also packaged in space-saving 0.4-mm pitch DQD packages.
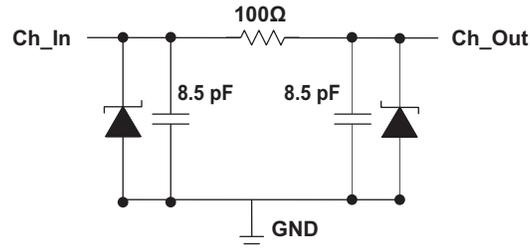
Figure 9. TPD6F003 Functional Block Diagram

Features:

- Four-, six-, and eight-channel EMI filtering for data ports
- –3-dB bandwidth of 200 MHz
- Greater than 25 dB attenuation at 1 GHz
- IEC 61000-4-2 Level 4 ESD protection:
    - ±12-kV contact discharge
    - ±20-kV air gap discharge
- Pi-Style (C-R-C) filter configuration
  (R = 100 Ω, C_{TOTAL} = 17 pF)
- Low 10-nA leakage current
- Easy flow-through routing

4   System Design Theory and Considerations

The Piezo Speaker Strobe Notification Reference Design TI Design demonstrates a low-power, integrated method to provide visual and audible notifications for alarm end-equipment systems. The DRV2700 industrial piezo driver is used to drive a piezo transducer that is optimized for audible alert notification systems. The LM3550 flash LED driver is used to drive high-current LEDs, while maintaining a constant input current during flash mode. The MSP430FR5969 ultra-low power MCU controls the system and enables demonstration of the visual and audible notification sub-systems.

4.1   Audible Notification Subsystem Design Theory

4.1.1   Piezo Transducer Design Theory

In order to meet the most up to date requirements for audible notification subsystems in a cost-efficient manner, the piezo transducer selection is critical.

For this TI Design, there are two main alert tones: a 520-Hz square wave and a 2.84-kHz sine wave. These signals are two common alert frequencies, particularly for fire alarm end-equipment systems. Therefore, the piezo transducer used must have resonant frequencies at these desired alert tones for best power efficiency and highest SPL output.

Through the use of a piezo bender that has a resonant peak at approximately 2.7 kHz in conjunction with a Helmholtz chamber that resonates at 520 Hz, the AB5027B-3-LW100-R piezo bender from PUI Audio Inc. meets the specifications for this TI Design.

In addition, the PUI Audio Inc. transducer has a low capacitance (~40 nF), which correlates to a lower power requirement for the piezo driver. The selected transducer also can operate at high peak-to-peak frequencies (120 V_{PP}), which enables output of multiple alert tones, as well as pre-recorded speech notifications.

4.1.2   High-Voltage Piezo Driver Design Theory

Based on the selection of the AB5027B-3-LW100-R piezo bender from PUI Audio Inc., the DRV2700 industrial piezo driver is an ideal product to amplify the filtered PWM signal from the MSP430FR5969 device. The DRV2700 can easily drive the selected transducer at 120 V_{PP} up to frequencies of 4 kHz while remaining within the specified operating range. The pairing of the DRV2700 device with the PUI Audio transducer enables the highest possible SPL output at the desired alert frequencies.

The DRV2700 device is a high-voltage amplifier with an integrated high-voltage boost converter. The boost converter supplies the high-voltage supply rail to the amplifier, which is configured to drive the piezo transducer differentially in this TI Design.

This TI Design is designed to set the boost voltage of the DRV2700 device to 65 V, which is the recommended setting for an output peak voltage of 60 V, or 120 V_{PP}. Since this TI Design is intended to drive the piezo transducer at a maximum voltage of 120 V_{PP}, and the maximum gain setting in the DRV2700 device is 40.7 dB or 108.4 V/V, the maximum allowable input voltage at the input terminals of the DRV2700 device is shown by Equation 1:

$$\text{Maximum Input Voltage} \; = \; \frac{120 \; V_{PP}}{108.4} \; = \; 1.107 \; V_{PP}$$

(1)

Therefore, the PWM signal conditioning circuit described in Section 4.1.3 must have a maximum output voltage of 1.107 V_{PP} in order to prevent clipping on the output of the DRV2700 device. Since end-equipment systems typically aren't concerned with audio fidelity, but rather with total SPL output, some clipping on the output signal may be acceptable.

All remaining component selection in the DRV2700 circuit was completed according to the design procedures described in that device's datasheet on www.ti.com (SLOS861).

4.1.3   PWM Signal Conditioning Design Theory

This TI Design produces audio signals using a pulse-width modulated (PWM) output from the MSP430FR5969 system MCU. There are several different signal types that are produced: a 520-Hz square wave, a 2.84-kHz sine wave, pre-recorded speech output, and white noise.

The 520-Hz square wave is produced by using the Timer_B module to directly output a 520-Hz PWM signal with 50% duty cycle. The 2.84-kHz sine wave, pre-recorded speech output, and white noise signals are all produced by using a 32-kHz PWM signal and altering the PWM duty cycle as needed. The pre-recorded speech file has a sampling rate of 8 ksps, which implies a maximum original signal bandwidth of 4 kHz.

To keep the DRV2700 device within specified operating limits for use with the selected piezo transducer, it is necessary to eliminate any frequency content above 4 kHz. Furthermore, to avoid clipping the output of the DRV2700 device, it is necessary to ensure a maximum input voltage to the DRV2700 of 1.107 V_{PP}.

A two-stage approach was implemented to ensure that both of these design requirements were met. The PWM output from the MSP430FR5969 has a peak-to-peak voltage of VDD – GND, and since VDD = 3.3 V in this TI Design, a voltage divider and op-amp buffer was used to decrease the PWM output to approximately 1.1 V_{PP}. To ensure that no frequency content above 4 kHz reaches the DRV2700 device, the divided PWM output is passed to a 3-pole, Butterworth low-pass filter (LPF) using two op-amps with a cutoff frequency of 4 kHz. This LPF was designed using WEBENCH Designer, and the entire PWM signal conditioning circuit was simulated using TINA-TI.

The TINA-TI circuit used to simulate the PWM signal conditioning circuit is shown in Figure 10.
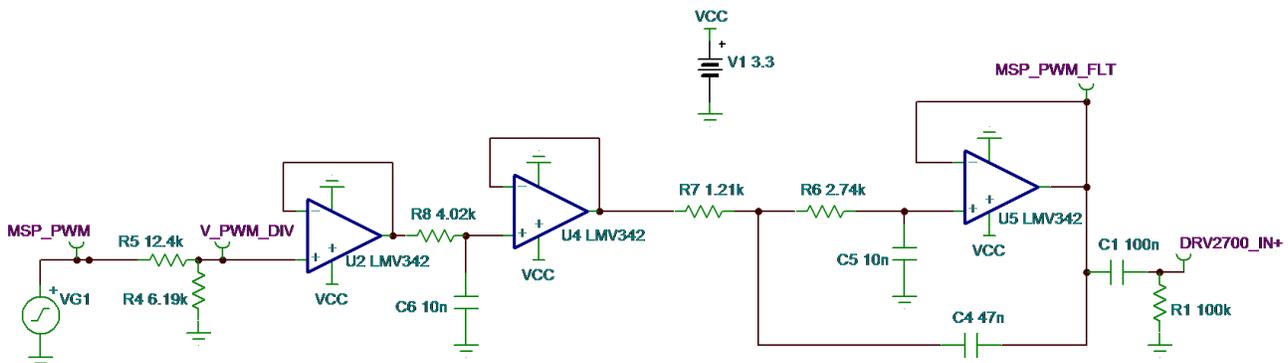
Figure 10. TINA-TI Simulation Circuit

To verify the frequency response of the PWM signal conditioning circuit, an AC transfer characteristic was generated. The simulation results are shown in Figure 11. The response has a slight roll-off at low frequencies; this is caused by the input capacitor on the IN+ pin of the DRV2700 device, in combination with the input impedance of that same device. The 3-dB frequency of the low-pass filter is at 4 kHz.
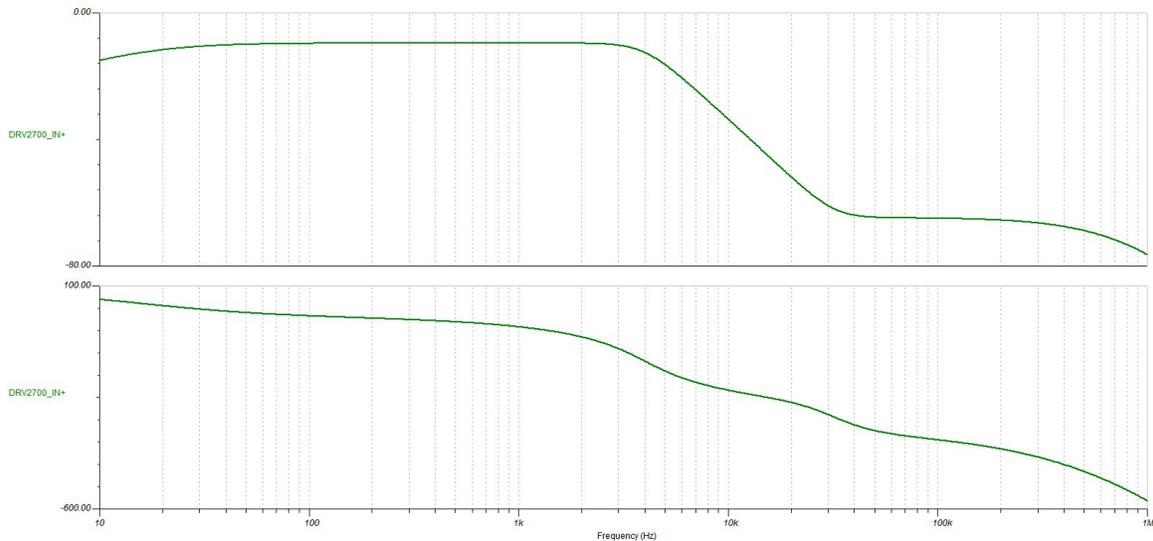
Figure 11. TINA-TI Simulation Results — AC Transfer Characteristic Simulation

The TINA-TI transient simulation results for both a 520-Hz PWM input and a 32-kHz PWM with superimposed 2.84-kHz sine wave are shown in Figure 12 and Figure 13. Both simulations results show the original input signal as well as the final output signal that would then be fed into the DRV2700 device's high-voltage amplifier.
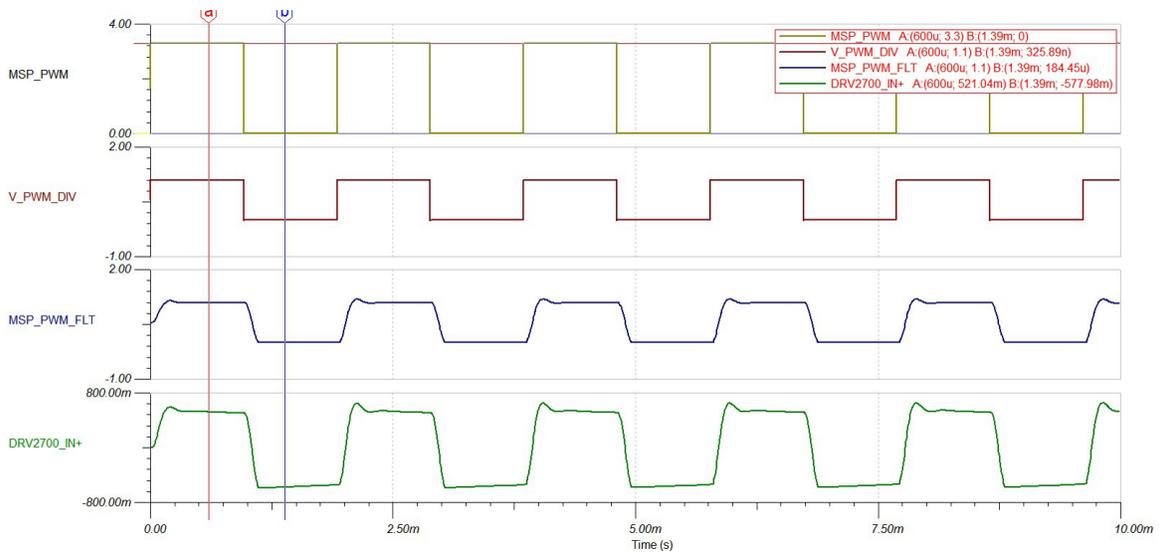
Figure 12. TINA-TI Simulation Results — Transient Simulation with 520-Hz Square Wave Input
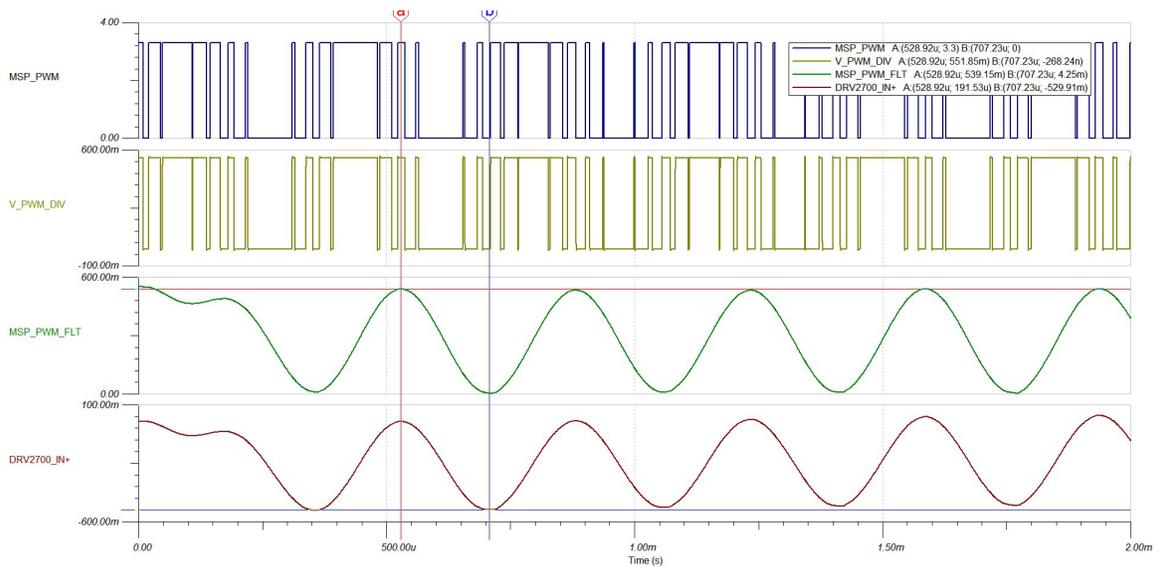
Figure 13. TINA-TI Simulation Results — Transient Simulation with 2.84-kHz Sine Wave Input

4.1.4 Applicable NFPA Code Requirements

The NFPA 72 National Fire Alarm and Signaling Code contains several sections pertinent to audible notification subsystems. Chapter 18, Section 4 contains all the requirements relating to audible notification devices for use in fire alarm applications.

The main engineering specifications from the NFPA 72 code that this TI Design is designed to meet can be summarized as follows:

- Maximum total SPL of 110 dBA at minimum hearing distance
- SPL at least 15 dBA above ambient, as measured 5 ft (1.5 m) above the floor
- Audible alarm signal in sleeping areas must be square wave with fundamental frequency of 520 Hz ±10%
- Pre-recorded messages should have voice intelligibility, but shall not be required to be determined through quantifiable measurements

Section 6.2 shows the audible notification subsystem test results that prove that this TI Design meets the minimum standards as listed in NFPA 72 code.

4.2 Visual Notification Subsystem Design Theory

In order to meet the requirements for visual notification devices, the selection of the high-current LEDs and the flash LED driver is critical.

4.2.1 LED Design Theory

The main selection parameter for the high-current LEDs in this application is the luminous intensity, which has units of candelas and is defined as the luminous power per unit solid angle.

To first get an estimate of the required number of LEDs and LED current magnitude, a look at the Relative Luminous Flux curve found in the LED manufacturer datasheet is needed. In the Osram datasheet for the LED used in this design, the luminous flux gain at 2 A is approximately 2.1 times that of the output at 700 mA. With this information, and using the Brightness Group information for the LED, it can be determined that the typical Luminous Intensity of the LED is 79 cd at 700 mA. Using the gain of 2.1 achieved at 2 A and applying it to the typical value at 700 mA leads to a luminous intensity of 158 cd for a single LED at 2 A. To ensure the NFPA 72 standard of a 185-cd light source was met with this TI Design, two LEDs driven in parallel at 2 A each were chosen. As this design relies on the radiation pattern of the LEDs themselves with no extra optics, a higher total luminous intensity value with a target typical of 320 cd helps ensure the NFPA code requirement would be met at the wider operating angles.

4.2.2 LED Driver Design Theory

To achieve a total LED current of 4 A, a storage and discharge approach must be used as most systems will not allow peak surge currents of this magnitude to pulled at any given time. To minimize the peak current draw, this TI Design uses a supercapacitor in conjunction with the LM3550 charger and flash controller. In the charging phase, the LM3550 uses a multi-gain input current limited switched capacitor boost converter to charge the supercapacitor to its target voltage. In this design, 5.3 V was chosen to maximize the available energy. Once charged, the current source controller of the LM3550 controls the current through the LEDs by adjusting the gate drive on an external N-FET and monitoring the voltage across a series current setting resistor. Pulse timing can either be controlled through an external strobe pin or through the setting of an internal I^{2}C register. To increase the accuracy of the current through two LEDs, duplicate sets of feedback resistors and current sink FETs are used, but only one of the feedback nodes connects back to the device. This approach evens out the LED current to an acceptable level and minimizes the power dissipated that would be present in a single discrete N-FET.

4.2.3 Supercapacitor and Driver Design Theory

To support a 4-A flash current and ensure that a proper recharging of the supercapacitor can occur during the one-second period of flash pulses, picking the correct capacitance value is crucial. If the capacitor has too low of a capacitance, it would recharge quickly but it might not be able to support the full LED current over the desired flash pulse duration. If the capacitor is too large, the physical size of the capacitor could be non-ideal and cost ineffective. In selecting a capacitor, parameters such as target current, pulse duration, available capacitance values, and the associated ESR of the capacitor should be known before sizing the capacitor.

At start-up, assuming the supercapacitor is fully discharged the LM3550 transition through multiple voltage gains to charge the capacitor to the target voltage. As the device transitions gains, the charging current will change based upon the voltage ratio. If the capacitance it larger, it will take longer to achieve the initial charge.
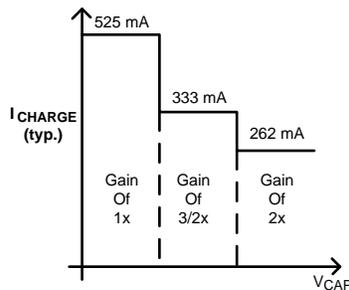
Figure 14. LM3550 Charging Current Profile

Once charged, the amount of tolerated capacitor droop during a flash must be calculated.
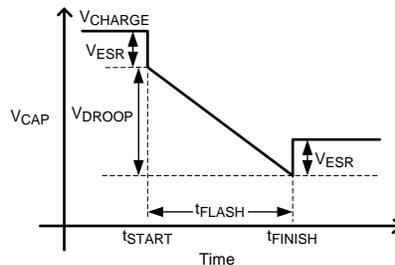
Figure 15. LM3550 Supercapacitor Voltage versus Time

When a constant load current is drawn from the charged supercapacitor, the voltage on the capacitor will change. The capacitor ESR and capacitance both affect the discharge profile. At the beginning of the flash (t_{START}), the supercapacitor voltage will drop due to the supercapacitor's ESR. The magnitude of the drop is equal to the flash current (I_{FLASH}) multiplied by the ESR (R_{ESR}).

$$V_{ESR} = I_{FLASH} \times R_{ESR} \tag{2}$$

Once the initial voltage drop occurs (V_{ESR}), the supercapacitor voltage will decay at a constant rate until the flash ends (t_{FINISH}). The voltage droop (V_{DROOP}) during the flash event is equal to flash current (I_{FLASH}) multiplied by the flash duration (t_{FLASH}) divided by the capacitance value of the supercapacitor (C_{SC}).

$$V_{DROOP} = \frac{\left(I_{FLASH} \times t_{FLASH}\right)}{C_{SC}} \tag{3}$$

After the flash event has finished, the voltage on the supercapacitor will increase due to the absence of current flowing through the ESR of the supercapacitor. This step-up is equal to $V_{ESR} = I_{FLASH} \times R_{ESR}$.

To maintain regulation across the external current source,

$$V_{DROOP} < V_{CHARGE} - V_{ESR} - V_{LED} - \left(I_{FLASH} \times R_{DSONNFET}\right) - V_{FB} \tag{4}$$

Substituting V_{DROOP} with the equation above and solving for C_{SC} yields Equation 5:

$$C_{SC} > \frac{\left(I_{FLASH} \times t_{FLASH}\right)}{\left(V_{CHARGE} - V_{LED} - \left(R_{ESR} \times I_{FLASH}\right) - V_{FB} - \left(\frac{\left(I_{FLASH} \times R_{DSON}\right)}{\text{Number LEDs}}\right)\right)} \tag{5}$$

In the case of this TI Design, I_{FLASH} = 4 A, t_{FLASH} = 16 ms, R_{SDON} = 16 mΩ, V_{LED} = 3.3 V, V_{CHARGE} = 5.3 V, and V_{FB} = 100 mV. When using the specification for the Murata supercapacitor used in this TI Design, R_{ESR} = 50 mΩ.

C_{SC} needs to be greater than 38 mF for a 16-ms flash. If t_{FLASH} was to increase to 100 ms, C_{SC} would need to equal 240 mF. Based on these findings, the Murata 470-mF (DMF3Z5R5H474M3DTA0, www.murata.com) supercapacitor was chosen to provide flash duration adjustability.

4.2.4 Applicable NFPA Code Requirements

The NFPA 72 National Fire Alarm and Signaling Code contains several sections pertinent to visual notification subsystems. Chapter 18, Section 5 contains all the requirements relating to visual notification devices for use in fire alarm applications.

The main engineering specifications from the NFPA 72 code that this TI Design is designed to meet can be summarized as follows:

- Flash rate between 1 and 2 Hz
- Maximum flash pulse duration of 200 milliseconds
- Maximum flash pulse duty cycle of 40%
- Flash color will be clear or nominally white, with maximum effective intensity of 1000 candelas
- When ceiling-mounted, the effective light intensity for a 70×70-ft (21.3×21.3-m) room must be at least 185 candelas
  - Alternatively, the light output must provide a minimum of 0.0375 lumens per ft^2 (0.4036 lumens per m^2)

Section 6.3 shows the visual notification subsystem test results that prove that this TI Design meets the minimum standards as listed in NFPA 72 code.

4.3 Firmware Control

The firmware for this TI Design is built on TI-RTOS, a real-time operating system for TI devices. The primary author of this TI Design chose TI-RTOS as the firmware platform to gain experience in the fundamentals of RTOS. The time for firmware development was reduced through the use of TI-RTOS.

The program is primarily designed for demonstration of the visual and audible notification subsystems. As such, the main interface consists of three user push-buttons.

BTN_LED controls the demo mode of the visual notification subsystem. On system power up, the visual notification mode is set to "Charge Mode". With each press of BTN_LED, the system cycles through the following modes:

- Charge Mode
- Torch Mode
- Flash Mode

Charge mode commands the LM3550 device to charge the supercapacitor to the pre-defined voltage of 5.3 V and maintain that charge.

Torch mode commands the LM3550 device to enter torch mode, which powers the two LEDs in a low-current mode, currently set to 100 mA. This mode bypasses the external FET and routes the LED current entirely through the LM3550 device.

Flash mode commands the LM3550 device to trigger a flash event at a frequency of 1 Hz. This mode is the primary mode of the LM3550 device, which controls the external FETs to send a high-current pulse from the supercapacitor through the two LEDs.

BTN_GAIN controls the volume of the audible notification subsystem. Pushing BTN_GAIN will cycle through the four gain settings on the DRV2700 device: 28.8 dB, 34.8 dB, 38.4 dB, and 40.7 dB. On system power up, the gain of the DRV2700 device is set to 28.8 dB, the lowest volume setting.

BTN_AUDIO controls the demo mode of the audible notification subsystem. Pushing BTN_AUDIO will cycle through the following modes:

- No audio output
- 520-Hz square wave output
- 2.84-kHz sine wave output
- Pre-recorded speech file output
- White noise output

The no audio output mode ensures that no PWM signal is being generated on the MSP_PWM pin and also ensures that the DRV2700 device is disabled for maximum power savings.

The 520-Hz square wave output mode sets MSP_PWM (connected to Timer_B0, CCR1) to generate a 520-Hz square wave. Once the Timer_B module is configured to generate the 520-Hz square wave, there is no further firmware intervention required to continue this mode.

The 2.84-kHz sine wave output mode sets MSP_PWM to generate a 2.84-kHz sine wave. The Timer_B module is configured to have a PWM frequency of 32 kHz, with a duty cycle that varies in a sinusoidal fashion.

The pre-recorded speech file output mode also sets the Timer_B module to have a PWM frequency of 32 kHz. However, instead of varying the duty cycle in a sinusoidal fashion, the duty cycle is varied by reading the hex values from a pre-recorded speech file that is pre-programmed on the non-volatile memory of the MSP430FR5969 device. The pre-recorded speech is the primary author saying "Hello, Texas Instruments." This mode will repeat the pre-recorded speech file continuously until another mode is selected.

The white noise output mode sets the Timer_B module to have a PWM frequency of 32 kHz. Using the Galois linear-feedback shift register algorithm, a pseudo-random duty cycle value is fed to the Timer_B module every PWM cycle. This results in an audio output of pseudo-white noise, which is used to generate the system-level audio frequency response test data.

The entire firmware uses the standard TI-RTOS objects of hardware interrupts (Hwis), tasks, semaphores, and clocks. Viewing the .cfg file of the TI Design firmware in Code Composer Studio™ (CCS) will enable easy evaluation of the system level firmware structure.

5   Getting Started

5.1   Hardware Overview

The Piezo Speaker Strobe Notification Reference Design TI Design hardware is shown in Figure 16. The PCB is in a 3.45×4.0-in rectangular form factor, and comes with 0.5-in nylon standoffs to ensure stability and ease of use while performing lab measurements.
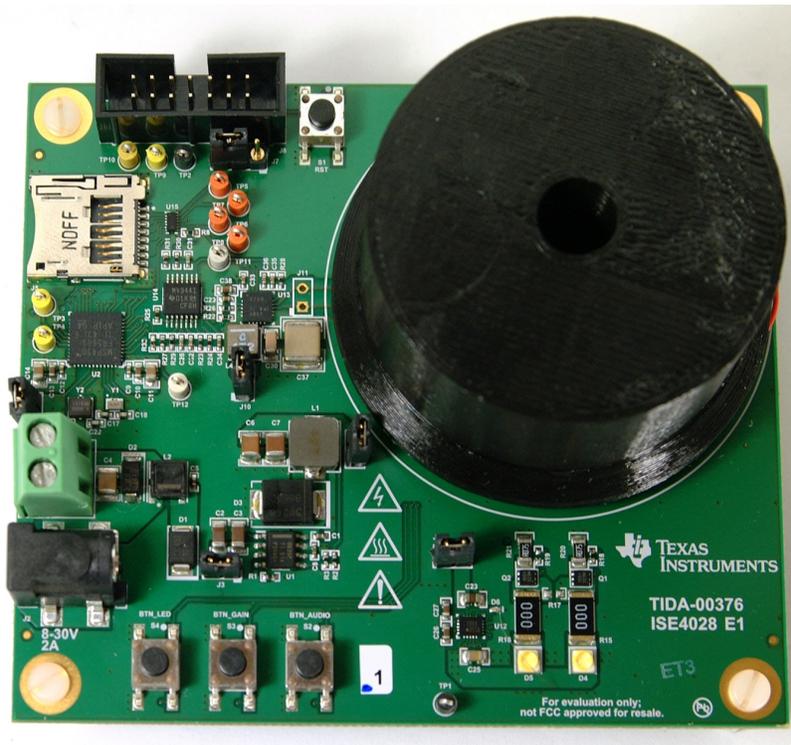
Figure 16. Piezo Speaker Strobe Notification Reference Design Reference Design Hardware

All of the main integrated circuits (DRV2700, LM3550, MSP430FR5969, LMV344, and LMR14030) are located on the top side of the PCB. The supercapacitor is soldered to the back side of the PCB along with a few passive components.

The three user push-buttons used to toggle through the various demonstration modes of the TI Design are located on the bottom-left edge of the PCB.

5.2 Loading the Firmware

The firmware used on this TI Design was developed using the CCS, version 6.1.0. The firmware was built on TI-RTOS, version 2.12.01.33.

To program or debug the TI Design hardware, close J7, pins 2-3 with a jumper shunt if powered externally. If running EnergyTrace™, or have other reason to power the MCU from the debugger, close J7, pins 1-2 with a jumper shunt, as well as open J6. All other 2-pin jumpers (J1, J3, J9, and J10) should be closed to ensure proper operation.

Power the board from 24 V, supplied at either J2 or J4, depending on connector availability.

> **NOTE:** See Figure 17 for a photo of the correct setup for programming or debugging the TI Designs hardware.
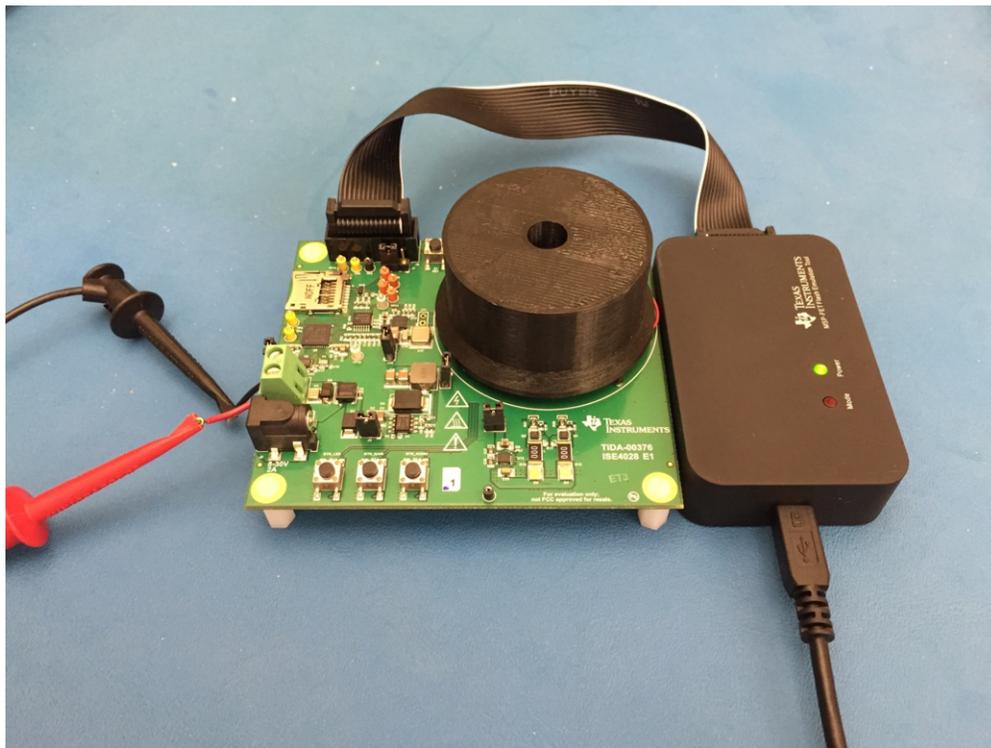
Figure 17. Configuration of Jumpers and Power for Programming and Debugging

The TI Design hardware is programmed by connecting the 14-pin JTAG ribbon cable from J8 to the MSP-FET MSP430 Flash Emulation Tool through CCS.

5.3 Demonstrating the TI Design Hardware

As described in Section 4.3, the TI Design hardware is demonstrated through the use of three user push-buttons. To enable demonstration of the TI Design, it is necessary to provide 24-V DC to either J2 or J4, depending on connector availability.

By default, the TI Design hardware starts up with the lowest audio volume setting, no audio playback, and no visual indications. Pressing BTN_LED, BTN_GAIN, and BTN_AUDIO will cycle through the various demonstration modes of the TI Design, as described in Section 4.3.

6   Test Data

> **NOTE:** Unless otherwise noted, the test data in the following sections was measured with the
> system at room temperature.

> **NOTE:** All of the measurements in this section were measured with calibrated lab equipment.

6.1   Overview

The Piezo Speaker Strobe Notification Reference Design TI Design has been characterized for functional usage including audible notification performance, visual notification performance, and power consumption.

The results of testing and characterization are shown in the following sections.

6.2   Audible Notification Performance

Because one of the two primary purposes of this TI Design is to showcase audible notification for alert end-equipment systems, the audible performance is critical to the design.

As described in Section 4.1, this TI Design is intended to produce the following audio output signals: 520-Hz square wave, 2.84-kHz sine wave, pre-recorded speech, and white noise. The 520-Hz square wave and 2.84-kHz sine wave are considered the alert tones and must achieve at least 15 dBA above the ambient SPL to comply with NFPA 72 code requirements. However, the ambient SPL depends on the environment in which the notification device is installed in, which can vary. Therefore, this TI Design is aiming to achieve as high a SPL as possible.

To fully characterize the audible notification performance, the following test data was gathered:

*   AC transfer characteristic of PWM signal conditioning circuit
*   Transient response of PWM signal conditioning circuit to both the 520-Hz square wave and 2.84-kHz sine wave
*   Overall audible frequency response using MCU-generated white noise as an audio source
*   Audible frequency response using MCU-generated alert tones (520-Hz square and 2.84-kHz sine)
*   Total SPL of both the 520-Hz square wave and 2.84-kHz sine wave alert tones
*   Evaluation of pre-recorded speech output voice intelligibility

6.2.1 PWM Signal Conditioning Performance

To verify that the PWM signal conditioning circuit operates as expected, several tests were performed. The first was the generation of an AC transfer characteristic from 10 Hz to 20 kHz. The 0-Ω jumper resistor between the MSP430FR5969 device and the MSP_PWM net was removed and a jumper wire was attached in its place. An Hewlett Packard (Keysight, http://www.keysight.com) 33120A Function and Arbitrary Waveform Generator was connected to the MSP_PWM net and configured to output a sine wave with a DC component of 1.65 V (3.3 V / 2) and peak-to-peak voltage of 3.3 V. The signal generator was then configured to a 10-Hz signal frequency. The peak-to-peak voltages at the MSP_PWM and MSP_PWM_FLT test points were recorded using a LeCroy (http://www.teledynelecroy.com) WaveJet 354A 500-MHz Oscilloscope. The frequency was then stepped up to 20 kHz, recording the input and output voltages at each step. The results of the AC transfer characteristic are shown in Figure 18. As predicted by simulations, the 3-dB cutoff frequency is at 4 kHz, and the AC transfer characteristic rolls off at 60 dB per decade.
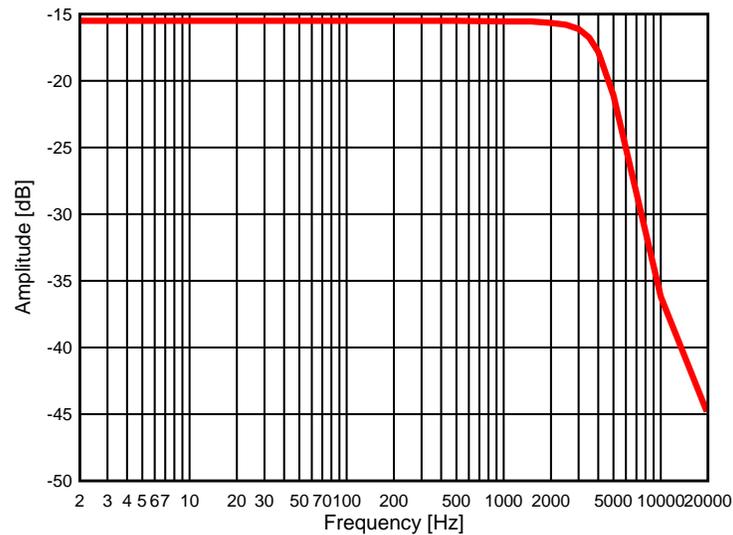
Figure 18. PWM Signal Conditioning Circuit AC Transfer Characteristic

The second test that was performed to verify proper operation is the transient response of the PWM signal conditioning circuit to both a 520-Hz square wave and 2.84-kHz sine wave input signal. The transient response of the circuit to a 520-Hz square wave is shown in Figure 19. There is some distortion on the output of the square wave. This is because the cutoff frequency of the LPF is 4 kHz, which means that the higher frequency harmonics of the square wave are much reduced in magnitude, leading to distortion. However, for audible notification applications, this distortion is acceptable since the primary goal is to provide a loud alert tone.
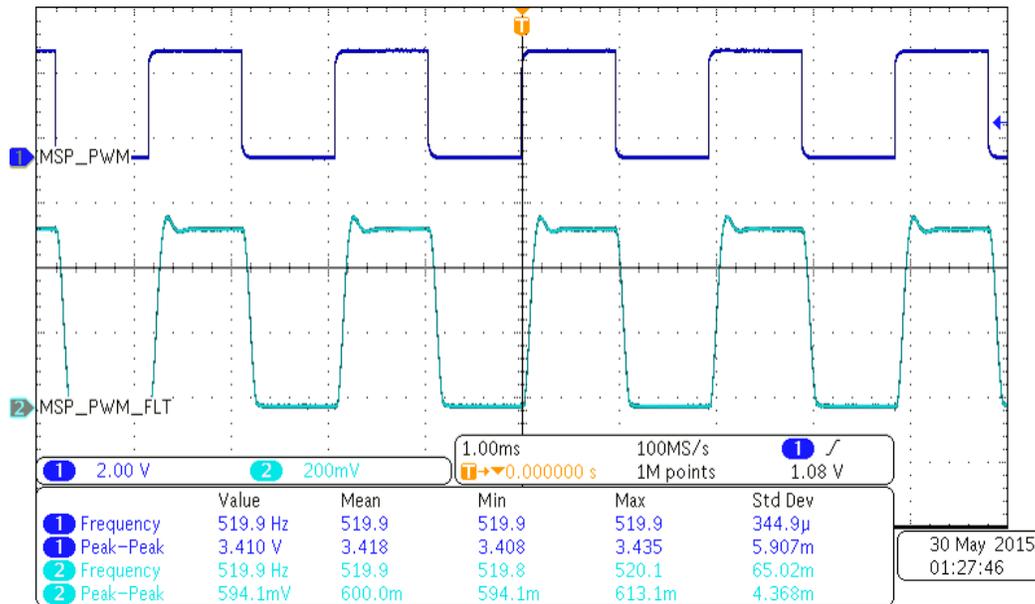
Figure 19. PWM Signal Conditioning Circuit Transient Response — 520-Hz Square Wave Input

The response of the circuit to a 2.84-kHz sine wave superimposed on a 32-kHz PWM signal is shown in Figure 20.
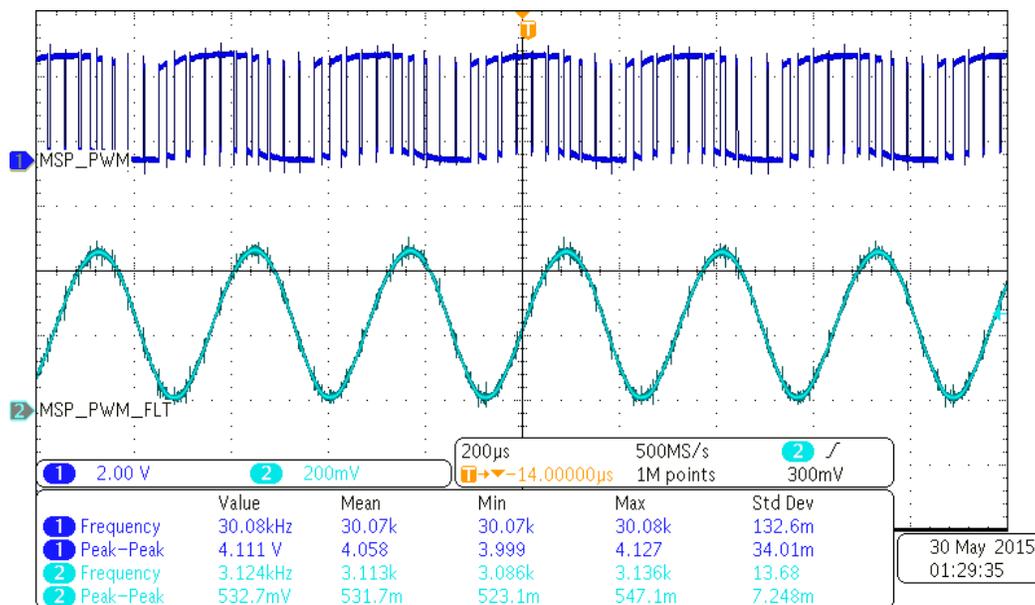
Figure 20. PWM Signal Conditioning Circuit Transient Response — 2.84-kHz Sine Wave input

6.2.2 Audible Frequency Response

To properly evaluate the audible performance of the entire TI Design system, the overall frequency response of the system to a white noise signal source was recorded. The purpose of this frequency response is to identify the resonant peaks present in the piezo transducer. Determining what frequencies the resonant peaks are at ensures that the alert tones are operating as efficiently as possible.

The white noise source was produced by pseudo-randomly varying the duty cycle of the 32-kHz PWM signal from the MSP430FR5969 device. More details can be found in Section 4.3. A Brüel and Kjær (http://www.bksv.com/) 4191 ½-inch free-field microphone was used in conjunction with the SoundCheck® System from Listen (https://www.listeninc.com) to measure the overall system frequency response of the TI Design, when placed within an audio test chamber.

The test setup for both audible frequency response and SPL measurements is shown in Figure 21.
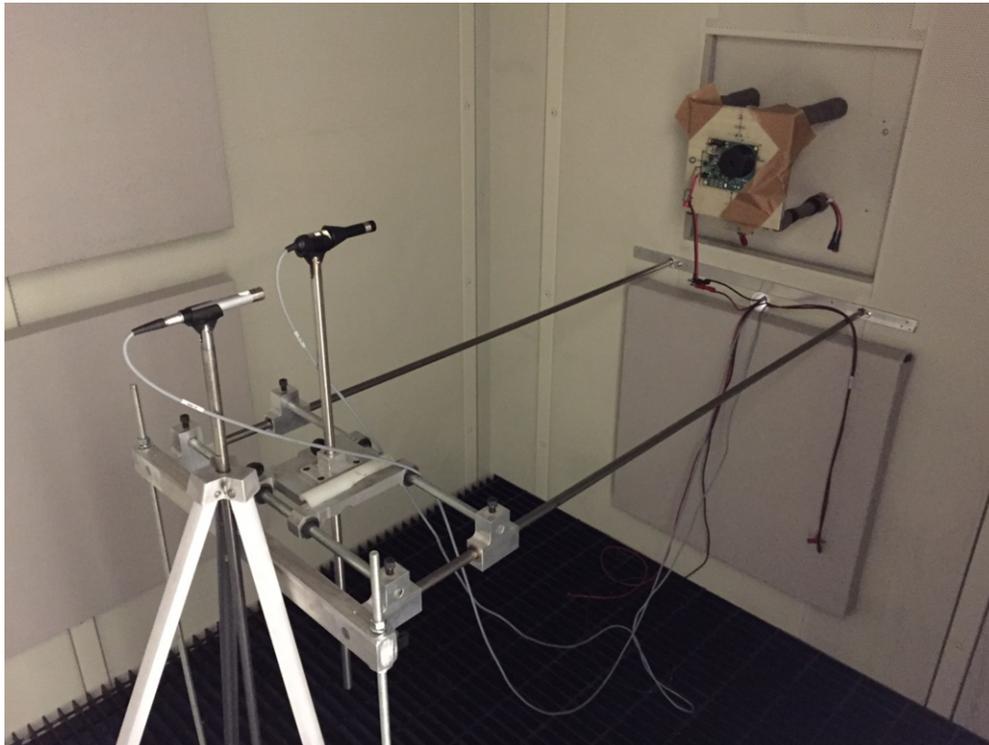
Figure 21. Overall Audible Frequency Response Test Setup

The overall system frequency response is shown in Figure 22. There is a pronounced resonant peak at approximately 520 Hz and 2.7 kHz. These resonant peaks ensure that the highest SPL level will be produced when the piezo transducer is fed with the 520-Hz square wave signal and the 2.84-kHz sine wave signal. The resonant peak at 520 Hz is due to the design of the Helmholtz chamber, while the 2.7-kHz resonant peak is due to the inherent resonance of the piezo bender at that frequency.
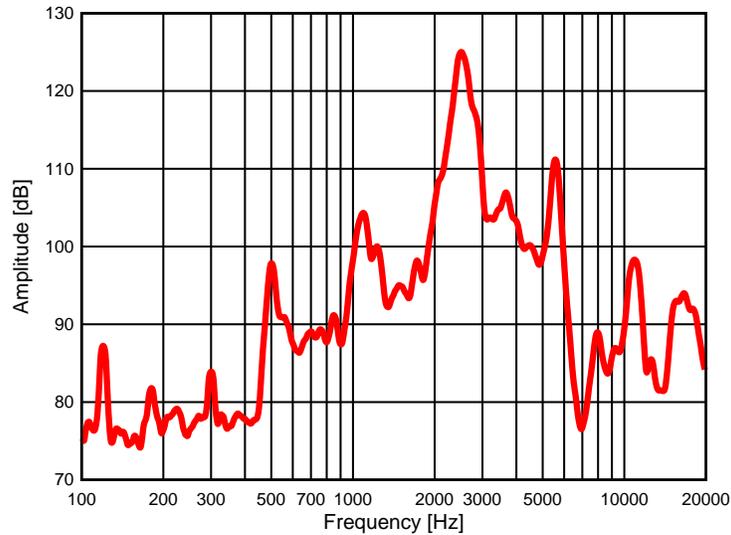
Figure 22. Overall Audible Frequency Response — White Noise Input

The overall system frequency response was also measured while both the 520-Hz square wave and 2.84-kHz sine wave alert tones were active. The test results are shown in Figure 23 and Figure 24. As expected, there are frequency peaks at the fundamental frequencies of the alert tones as well as at the appropriate harmonics.
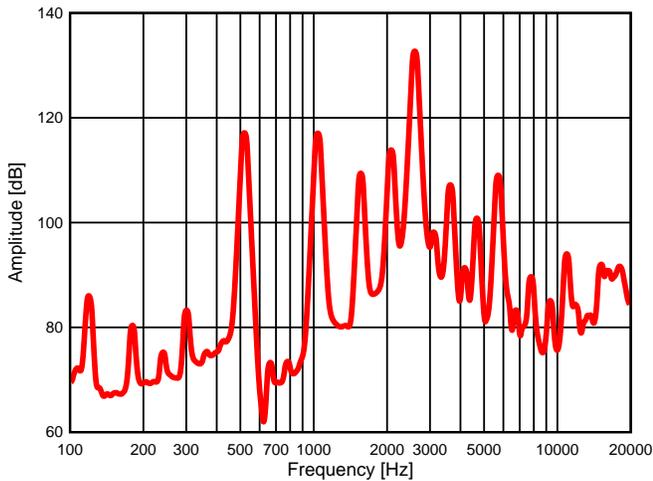
Figure 23. Overall Audible Frequency Response — 520-Hz Square Wave Input

Figure 24. Overall Audible Frequency Response — 2.84-kHz Sine Wave Input
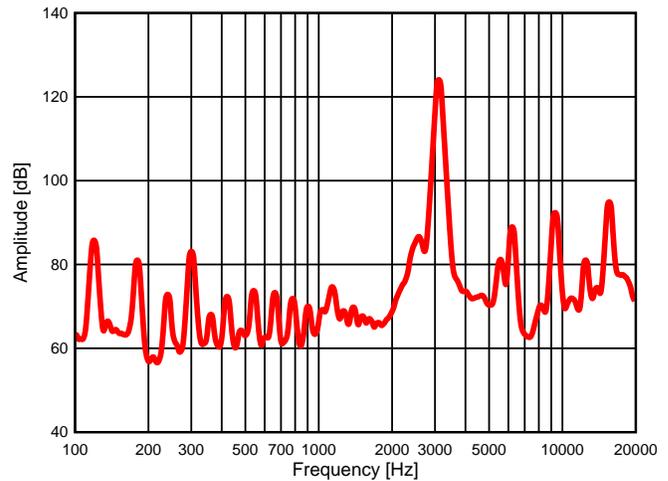
6.2.3 Sound Pressure Level (SPL) Characterization

Using a Brüel and Kjær 2237 Sound Level Meter and 4137 microphone within an audio test chamber, the total sound pressure level was measured for the 520-Hz square wave and 2.84-kHz sine wave alert tones as well as the pre-recorded speech output. The microphone was placed 10 cm from the TI Design hardware to reduce unwanted measurement error due to sound reflections.

The results of those measurements are shown in Table 2, Table 3, and Table 4. The SPL at a 3-m distance is calculated using the principal that SPL drops 6 dB when the listening distance has doubled. The equation to determine the SPL at 3 m is shown here:

$$\text{SPL @ 3 m} = \text{SPL @ 0.1 m} - \left| 20 \times \log_{10} \frac{0.1\,\text{m}}{3\,\text{m}} \right|$$

(6)

Table 2. SPL Test Results — 520-Hz Square Wave Signal

	SPL @ 10 cm (dBA)	Calculated SPL @ 3 m (dBA)
DRV2700 Gain = 28.8 dB	102.0	72.5
DRV2700 Gain = 34.8 dB	108.4	78.9
DRV2700 Gain = 38.4 dB	113.6	84.1
DRV2700 Gain = 40.7 dB	116.0	86.5

Table 3. SPL Test Results — 2.84-kHz Sine Wave Signal

	SPL @ 10 cm (dBA)	Calculated SPL @ 3 m (dBA)
DRV2700 Gain = 28.8 dB	100.5	71.0
DRV2700 Gain = 34.8 dB	106.3	76.8
DRV2700 Gain = 38.4 dB	107.9	78.4
DRV2700 Gain = 40.7 dB	110.0	80.5

Table 4. SPL Test Results — Pre-Recorded Speech Signal

	SPL @ 10 cm (dBA)	Calculated SPL @ 3 m (dBA)
DRV2700 Gain = 28.8 dB	94.0	64.5
DRV2700 Gain = 34.8 dB	100.0	70.5
DRV2700 Gain = 38.4 dB	104.0	74.5
DRV2700 Gain = 40.7 dB	107.0	77.5

6.2.4 Pre-Recorded Speech Playback Performance

The TI Design hardware comes pre-programmed with a speech file of the primary author saying "Hello, Texas Instruments." This speech file automatically repeats while in that audio output mode. There is no quantitative measurement for speech intelligibility; however, when listening to the speech output, the recorded message is clearly audible.

The filtered waveform of the speech output file is shown in Figure 25.
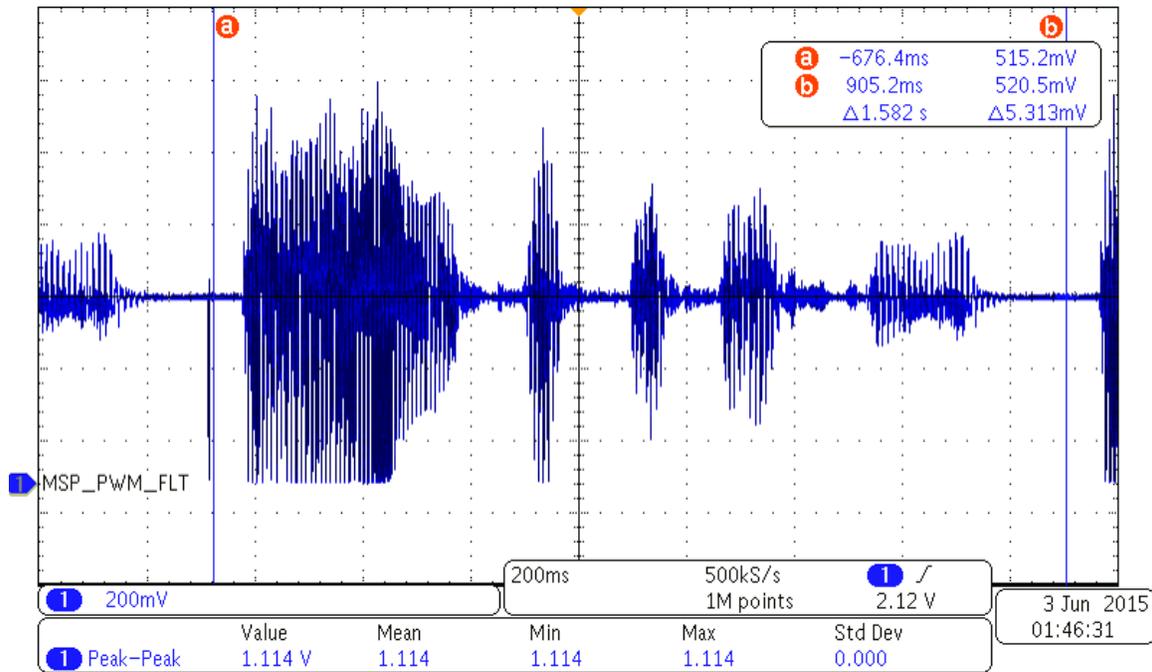
Figure 25. Pre-Recorded Speech Output Waveform

6.3 Visual Notification Performance

Because one of the two primary purposes of this TI Design is to showcase visual notification for alert end-equipment systems, the visible alert performance is critical to the design.

As described in Section 4.2, this TI Design is intended to operate in both a low-power torch mode as well as a high light output flash mode. The NFPA 72 code specifies a minimum light output level that visible notification devices must meet or exceed. The flash mode of operation is the mode characterized for compliance to NFPA 72 code requirements.

6.3.1 Visual Notification Duty Cycle and Pulse Width Characterization

NFPA 72, Chapter 18, Section 5.3 specifies that the flash rate must be between 1 and 2 Hz. The pulse duration must be no greater than 200 ms, and the flash pulse duty cycle must not exceed 40%.

The LM3550 device has a programmable time-out duration, which effectively controls the pulse width of the flash. The flash rate is controlled by the system MCU. To lower system power consumption, the shortest time-out duration of 16 ms was used along with a 1-Hz flash rate.

Figure 26 and Figure 27 show oscilloscope screen captures of both the flash pulse width and the flash frequency in the visual notification subsystem, respectively. The data was collected by probing at the LED pin of the LM3550 device. The figures clearly show a pulse width of 15.8 ms and a flash frequency of 1.051 Hz, both of which meet NFPA 72 code requirements.
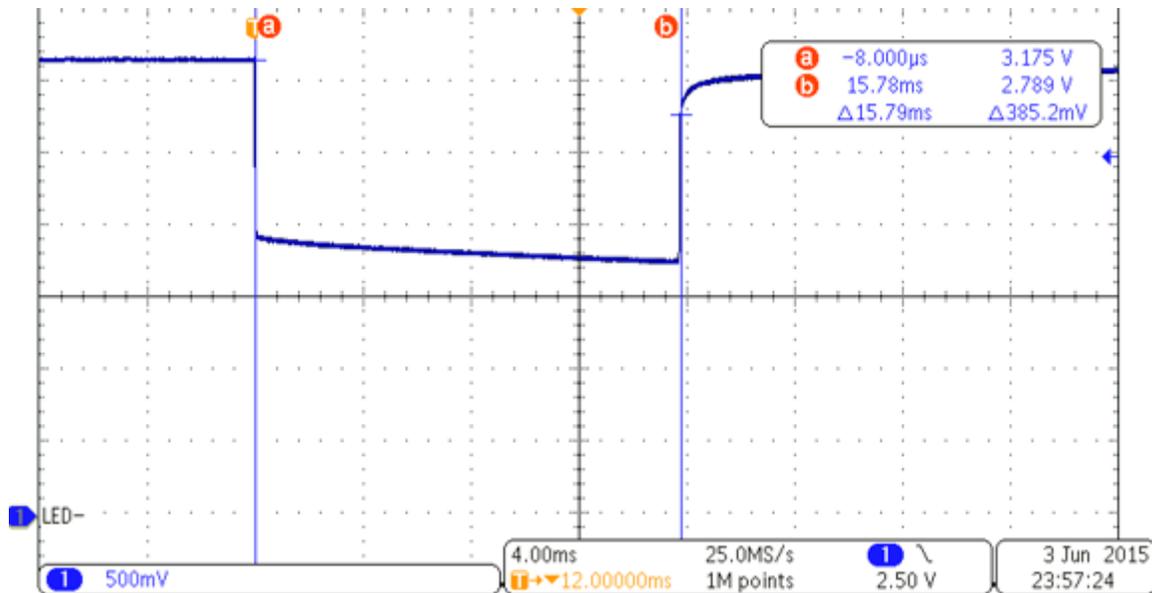
Figure 26. Flash Pulse Width
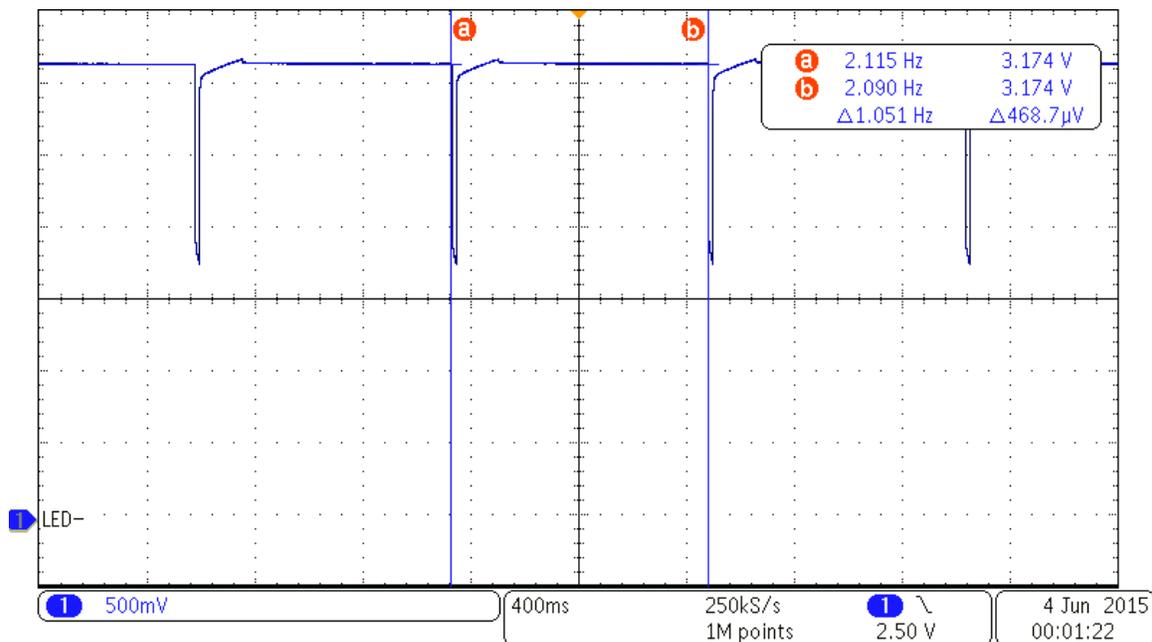
Figure 27. Flash Frequency

6.3.2 Total Light Output

Using an Extech (www.extech.com) 407026 light meter set to record the maximum lux value over a two-minute period, the total light output was measured and is shown in Table 5. As seen in the illuminance columns (lm/ft^2), this TI Design exceeds the NFPA 72 code requirements for light output by a wide margin.

Table 5. Visible Notification Subsystem Light Output

TEST CONDITIONS				DUAL-LED OUTPUT MEASUREMENTS			
DEPTH (ft)	WIDTH (ft)	ANGLE (°)	DISTANCE (ft)	MEASURED LUMINOUS EMITTANCE (lux)	CALCULATED ILLUMINANCE (lm/ft^2)	CALCULATED NFPA72 REQUIREMENT (lm/ft^2)	CALCULATED LUMINOUS INTENSITY (candela)
10	0	0.0	10.00	29	2.694	1.850	269.4
10	5	26.6	11.18	25	2.322	1.368	290.3
10	10	45.0	14.14	15	1.394	0.694	278.0
15	0	0.0	15.00	16	1.486	0.822	334.5
15	5	18.4	15.81	14	1.300	0.690	325.0
15	10	33.7	18.02	10	0.929	0.430	301.0
15	15	45.0	21.13	7	0.650	0.308	290.4

6.4 Power Characterization

One of the key design considerations for integrating the Piezo Speaker Strobe Notification Reference Design TI Design into end-user systems is the overall system current consumption. Because there are several modes of operation, test data has been collected showing the total system current consumption during each mode.

6.4.1 Audible Notification Subsystem Power Performance

As mentioned previously, there are several modes available in the audible notification subsystem. There are also four gain settings for the DRV2700 device. Total system power consumption has been recorded for all modes and the DRV2700 gain combinations of the audible notification subsystem. The input voltage rail was set at 24-V DC. The results are summarized in Table 6.

Table 6. Input Current — Audible Notification Subsystem

AUDIBLE NOTIFICATION SUBSYSTEM MODE	I_{INPUT} (mA)	P_{INPUT} (mW)
520-Hz Square wave, Gain = 28.8 dB	10.2	244.8
520-Hz Square wave, Gain = 34.8 dB	21.9	525.6
520-Hz Square wave, Gain = 38.4 dB	34.3	823.2
520-Hz Square wave, Gain = 40.7 dB	46.3	1111.2
2.84-kHz Square wave, Gain = 28.8 dB	22.4	537.6
2.84-kHz Square wave, Gain = 34.8 dB	45.7	1096.8
2.84-kHz Square wave, Gain = 38.4 dB	73.2	1756.8
2.84-kHz Square wave, Gain = 40.7 dB	104.3	2503.2
Pre-recorded speech output, Gain = 28.8 dB	1.5	36.0
Pre-recorded speech output, Gain = 34.8 dB	3.7	89.8
Pre-recorded speech output, Gain = 38.4 dB	5.4	128.6
Pre-recorded speech output, Gain = 40.7 dB	6.8	162.2
White noise, Gain = 28.8 dB	13.4	321.6
White noise, Gain = 34.8 dB	26.3	631.4
White noise, Gain = 38.4 dB	41.1	986.4
White noise, Gain = 40.7 dB	56.2	1348.8

As evident from the power data, increasing gain increases the system power consumption. Also, increasing the alert tone frequency increases the system power consumption. This is expected behavior, because the input power consumption of the audible notification subsystem is linearly dependent on the input signal frequency, piezo transducer capacitance, and the output voltage.

6.4.2 Visible Notification Subsystem Power Performance

As mentioned previously, there are two modes available in the visual notification subsystem: torch mode and flash mode. Total system power consumption has been recorded for all visible notification subsystem modes. The input voltage rail was set at 24-V DC. The results are summarized in Table 7. The flash mode consumes less overall power than the torch mode, even though total light output is much higher since the flash mode is a duty-cycled mode of operation.

Table 7. Input Current — Visible Notification Subsystem

VISIBLE NOTIFICATION SUBSYSTEM MODE	I_{INPUT_AVG} (mA)	P_{INPUT} (mW)
Torch Mode (I_{LED} = 100 mA)	38.9	933.6
Flash Mode (t_{FLASH} = 16 ms, f_{FLASH} = 1 Hz)	15.5	372.5

In Flash Mode, there is an input current pulse on the 24-V DC input terminal when each flash event occurs. With a 16-ms pulse duration, the LM3550 takes approximately 171 ms to recharge the supercapacitor, at which point the current drawn from the input drops very low, as shown in Figure 28. These current pulses occur during and after each flash event at a frequency of approximately 1 Hz, as shown in Figure 29.
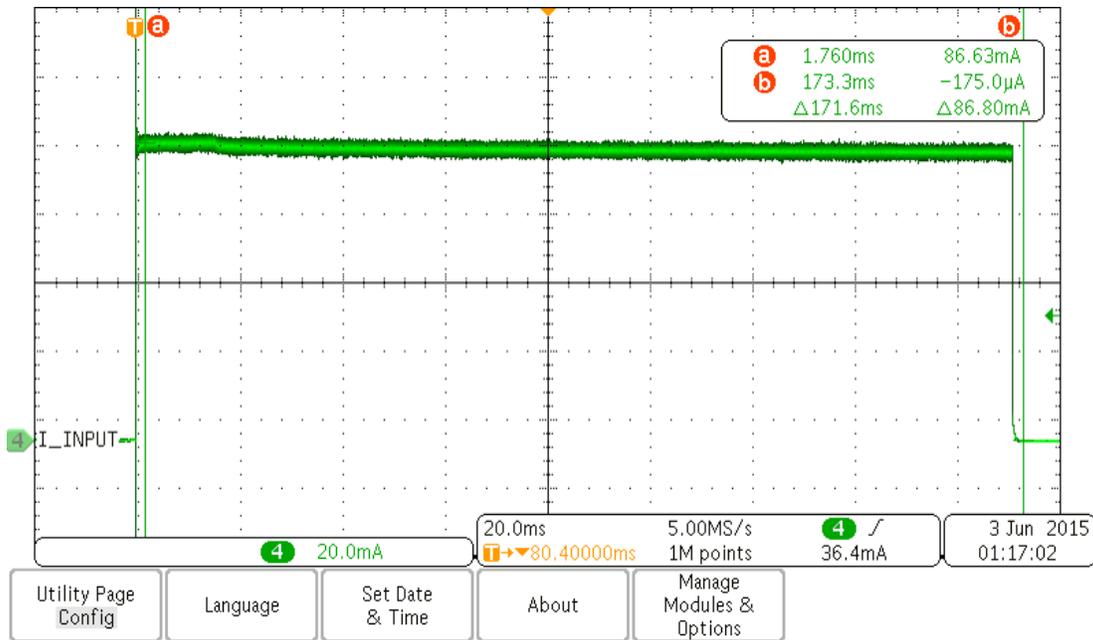
Figure 28. Input Current During Visual Notification Flash Mode — Showing Current Pulse Width
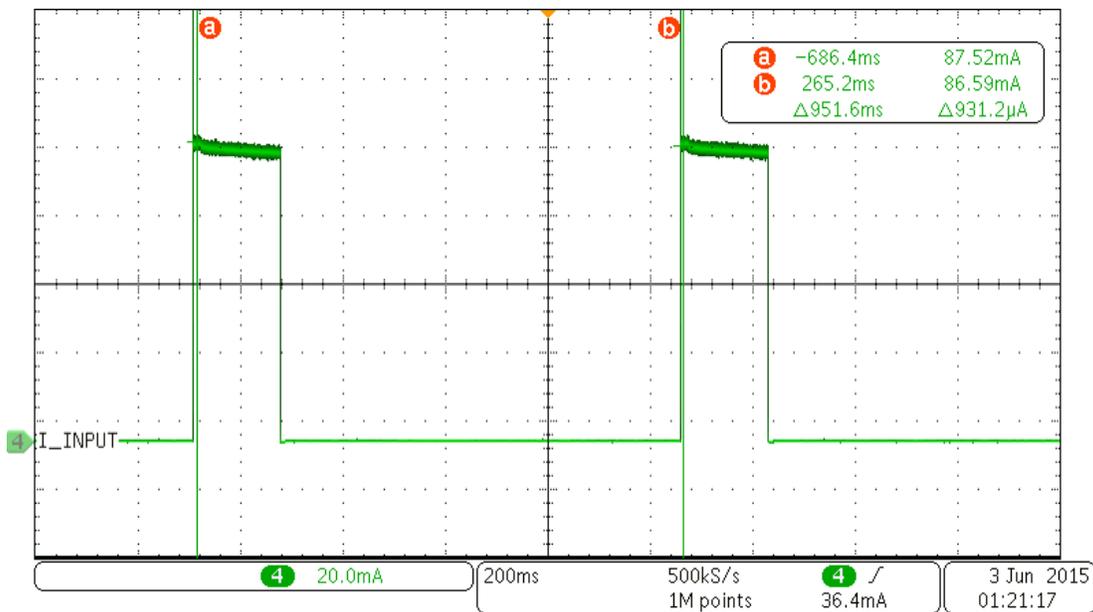
Figure 29. Input Current During Visual Notification Flash Mode — Showing 1-Hz Frequency

6.4.3   Total System Power

When the audible notification subsystem is operating in the 520-Hz square wave mode at full DRV2700 gain and the visual notification subsystem is operating in flash mode, the total power consumption at the input power supply averages 60.17 mA. There are some current pulses visible during each LED flash event, which are visible in Figure 30. With a 24-V DC input voltage, the total system power consumed is 1.44 W.
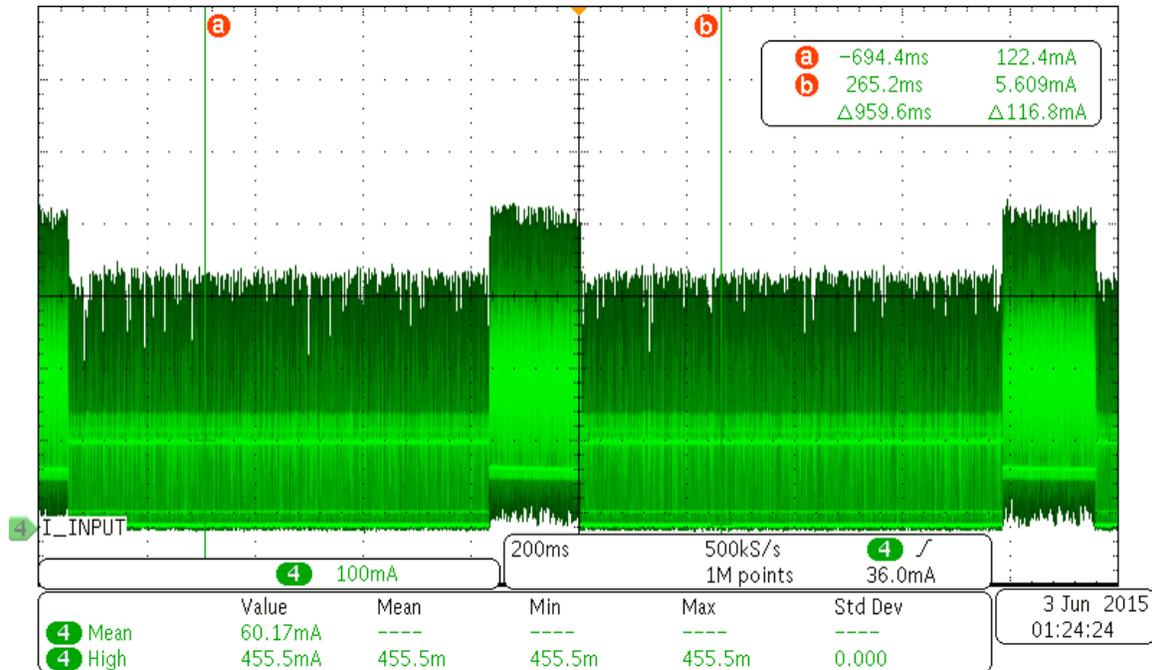
Figure 30. Input Current During Audible and Visible Notification Events

6.4.4   System Standby Power Performance

When the audible and visible notification subsystems are disabled, the system is considered to be in standby mode. During standby mode, the main sources of power consumption are the shutdown or standby currents of the various integrated circuits in the TI Design system (DRV2700, LM3550, MSP430FR5969, LMV344, and LMR14030).

The total standby current drawn from the TI Design subsystem in standby mode is 268 µA from the 24-V DC input supply. This current could be reduced by putting the LM3550 device in full shutdown mode, as opposed to standby mode; however, the loss of charge in the supercapacitor because of this shutdown mode may cause initial flash mode activation to be delayed.

7 Design Files

7.1 Schematics

To download the schematics, see the design files at [TIDA-00376 Schematics](#).
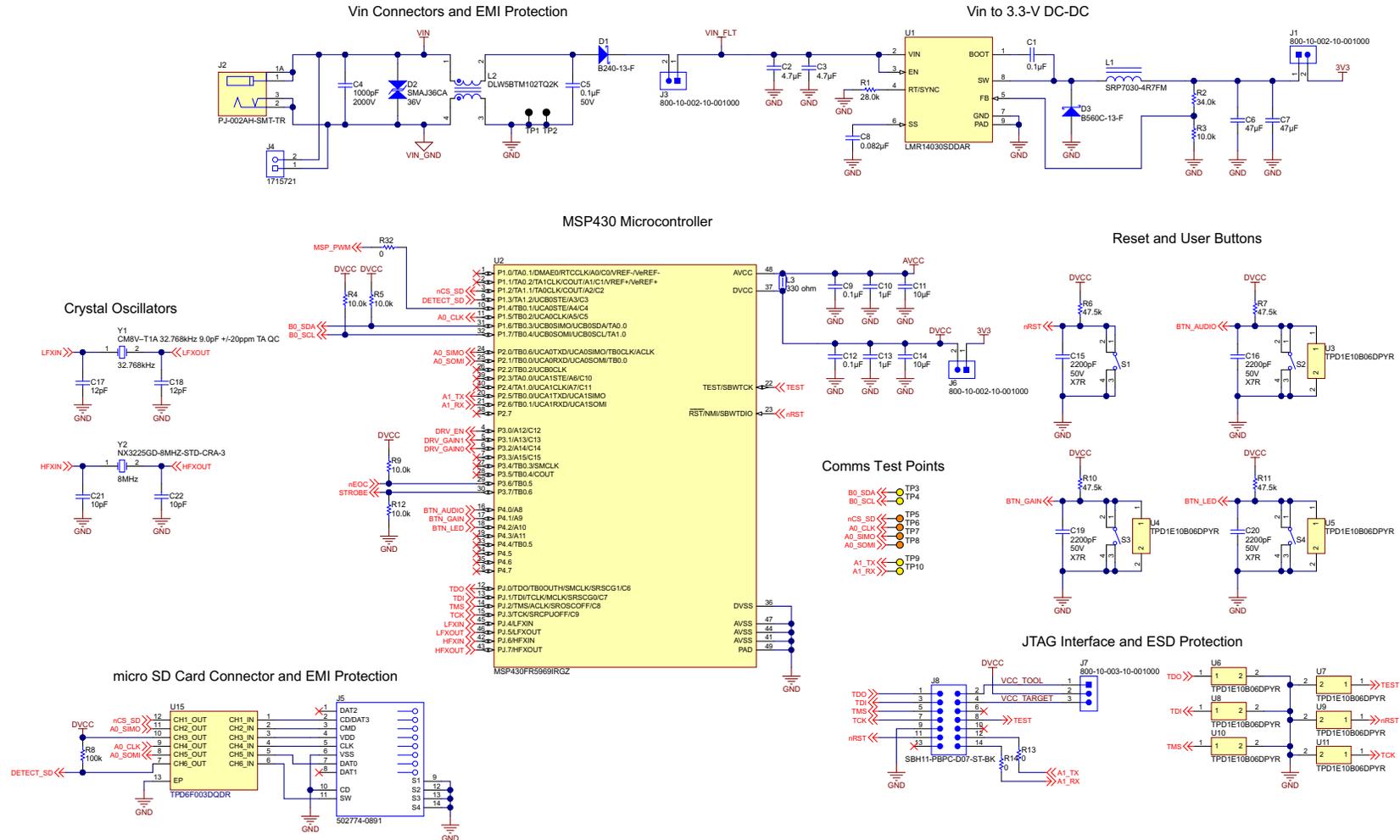
Figure 31. PWR MCU Schematic

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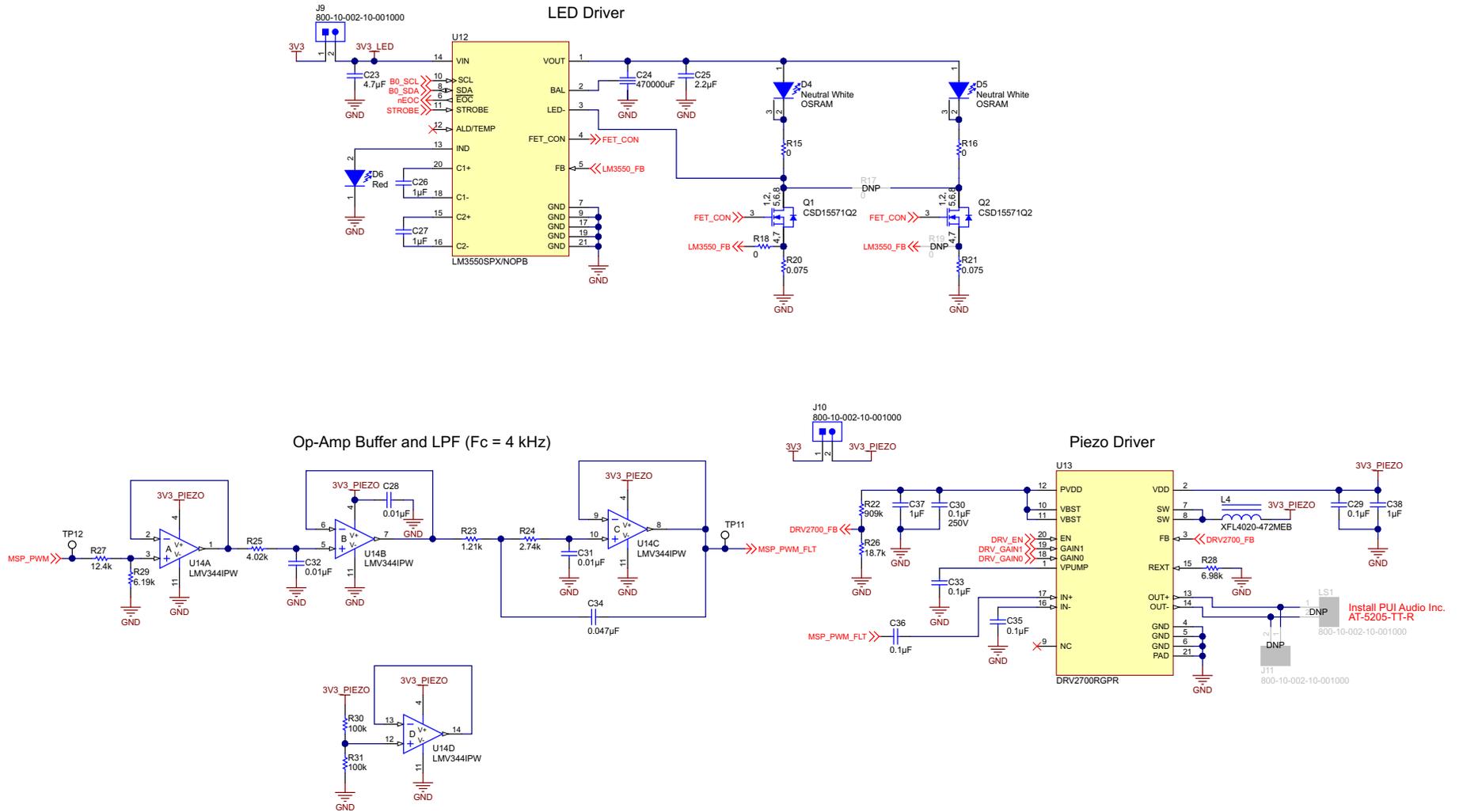
Figure 32. Piezo LED Schematic

7.2　Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00376 BOM.

7.3　Layer Plots

To download the layer plots, see the design files at TIDA-00376 Layer Plots.

7.4　Altium Project Files

To download the Altium project files, see the design files at TIDA-00376 Altium.

7.5　Layout Guidelines

To ensure a high performance, the Piezo Speaker Strobe Notification Reference Design TI Design was laid out using a four-layer PCB. The second layer is a solid GND pour, and the third layer is used for power rail routing with GND fills in unused areas. The top and bottom layers are used for general signal routing and also have GND fills in unused areas.

For all of the TI products used in this TI Design, follow the layout guidelines given in the respective datasheets.

7.6　Gerber Files

To download the Gerber files, see the design files at TIDA-00376 Gerber.

7.7　Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00376 Assembly Drawing.

7.8　Software Files

To download the software files, see the design files at TIDA-00376 Firmware.

8   References

For additional references, see the following:

1. Texas Instruments, *DRV2700 Industrial Piezo Driver With Integrated Boost Converter*, DRV2700 Datasheet ([SLOS861](#))
2. Texas Instruments, *LM3550 5-A Flash LED Driver With Automatic VLED and ESR Detection for Mobile Camera Systems*, LM3550 Datasheet ([SNVS569](#))
3. Texas Instruments, *MSP430FR59xx Mixed-Signal Microcontrollers*, MSP430FR5969 Datasheet ([SLAS704](#))
4. Texas Instruments, *LMR14030 Simple Switcher® 40 V 3.5 A, 2.2 MHz Step-Down Converter With 40 µA I_Q*, LMR14030 Datasheet ([SNVSA81](#))
5. Texas Instruments, *Rail-to-Rail Output CMOS Operational Amplifiers With Shutdown*, LMV344 Datasheet ([SLOS447](#))
6. Texas Instruments, *20-V N-Channel NexFET™ Power MOSFETs*, CSD15571Q2 Datasheet ([SLPS435](#))
7. Texas Instruments, *Single Channel ESD Protection Device in 0402 Package*, TPD1E10B06 Datasheet ([SLLSEB1](#))
8. Texas Instruments, *TPDxF003 Four-, Six-, and Eight-Channel EMI Filters With Integrated ESD Protection*, TPD6F003 Datasheet ([SLLS907](#))

9   About the Authors

EVAN D. CORNELL is a systems architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Evan brings to this role experience in system-level analog, mixed-signal, and power management design. Evan earned his Master of Electrical and Computer Engineering (M.Eng.) and Bachelor of Science (BS) in electrical engineering from the Rose-Hulman Institute of Technology in Terre Haute, IN. Evan is a member of the Institute of Electrical and Electronics Engineers (IEEE).

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Revision History

Changes from Original (June 2015) to A Revision **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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