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TI Designs – Precision: Verified Design
3-Terminal PLC Reference Design

TEXAS INSTRUMENTS

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Design Resources

TIPD195	All Design files
TINA-TI™	SPICE Simulator
INA188	Product Folder
REF3225	Product Folder

Circuit Description

This 3-terminal PLC reference design inputs ±10 V or ±20 mA and outputs a single-ended voltage of 2.5 V ± 2.3 V. It utilizes the INA188, which is a zero-drift instrumentation amplifier. The 2.5 V reference voltage is supplied with the REF3225.

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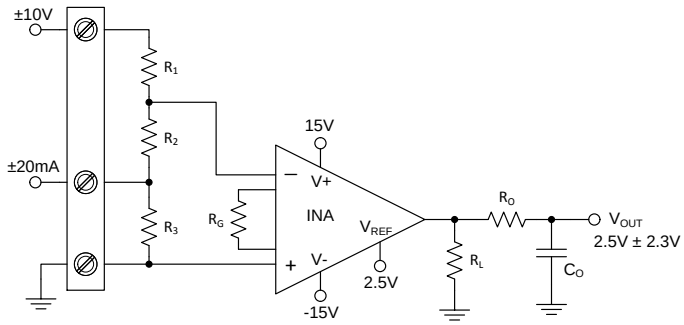

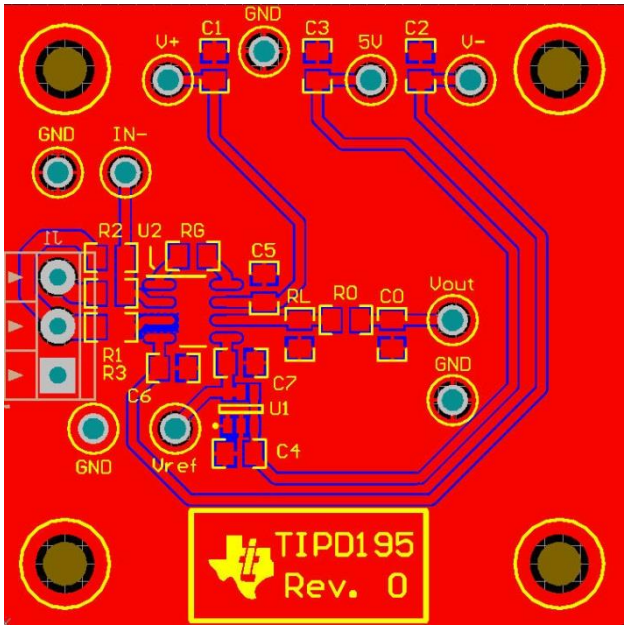

1 Design Summary

- Supply Voltage: ±15 V, +5 V
- Inputs: ±10 V, ±20 mA
- Output: 2.5 V ± 2.3 V

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Total Unadjusted Error (%)	0.2%	0.094%	0.153%

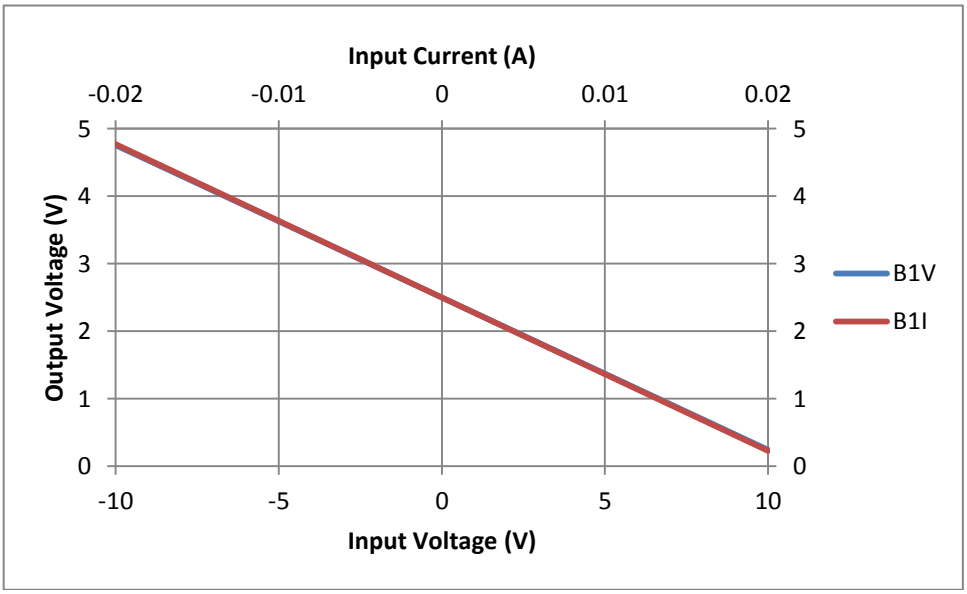

Figure 1: Measured Transfer Function

2 Theory of Operation

Figure 2 depicts a more detailed version of the schematic.

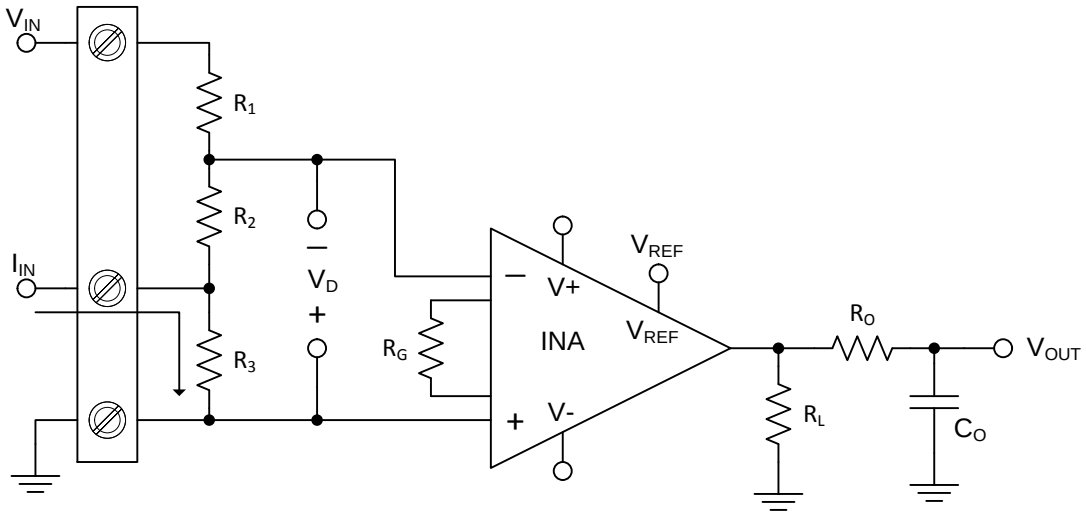

Figure 2: Detailed Schematic

This circuit has two modes of operation: current input and voltage input. This is contingent upon the relationship shown in Equation (**1**).

$$R_1 >> R_2 >> R_3 \quad (1)$$

Given this relationship, the transfer function for current input mode, V_{OUT-I}, is given in Equation (**2**). 'G' represents the gain of the instrumentation amplifier.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF} \quad (2)$$

Similarly, the transfer function for the voltage input mode, V_{OUT-V}, is given in Equation (**3**).

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2} \right) \times G + V_{REF} \quad (3)$$

3 Component Selection

3.1 R_1, R_2, R_3

The value of R_1 dominates the input impedance of the voltage input mode. The typical minimum input impedance is 100kΩ, which is the value selected for R_1 in this design. Note that increasing this value will introduce additional resistor noise.

The value of R_3 should be extremely small when compared to R_1 and R_2. This ensures that an insignificant amount of current is drawn by R_1 and R_2 when in current input mode. Therefore the value selected for R_3 is 20 Ω. Given an input current range of ±20 mA, the differential input, V_D, is ideally ±400 mV.

In voltage mode the differential voltage is given by Equation (4). Solving for R_2 and substituting for V_D (±400 mV), V_{IN} (±10 V), and R_1 (100 kΩ) yields the ideal value for the resistor.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167k\Omega \quad (4)$$

The nearest 0.1%, low drift resistor value is 4.12 kΩ. To minimize error, 0.1% low-drift resistors were also selected for R_1 and R_2.

3.2 Voltage Reference

A reference voltage must be applied to the instrumentation amplifier because the inputs are bipolar. This voltage should be at the middle of the desired output swing range. The REF3225 is a low-drift, high-accuracy precision voltage reference that outputs 2.5 V given a 5 V supply.

3.3 Instrumentation Amplifier

The primary specification of interest in this design is input offset voltage. The INA188 is a precision, zero-drift instrumentation amplifier. The typical offset voltage is ±25±(60/G) µV. In addition, the INA188 has excellent offset voltage drift (±0.15±0.85/G µV/°C).

3.4 Gain & R_G

The ideal gain of the instrumentation amplifier is calculated in Equation (5).

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8V - 2.5V}{400mV} = 5.75\frac{V}{V} \quad (5)$$

The gain-setting resistor for the INA188 is calculated in Equation (6).

$$G_{INA188} = 1 + \frac{50k\Omega}{R_G} \rightarrow R_G = \frac{50k\Omega}{G_{INA188} - 1} = \frac{50k\Omega}{5.75 - 1} = 10.53k\Omega \quad (6)$$

The nearest 0.1% precision resistor value greater than 10.53 kΩ is 10.7 kΩ. A larger value was selected due to the inverse relationship between gain and resistor value. This adds margin to the design.

3.5 Common-mode Range

It is important to ensure that the input common-mode range vs. output voltage swing is sufficient for this design. The INA-CMV-CALC tool can be downloaded and utilized to ensure linear operation. Figure 3 depicts the common-mode vs. output voltage swing plot given +/-15 V supplies, 2.5 V reference, and gain of 5.67 V/V for the INA188. Notice the operating region for this design (yellow box) is well within the linear operating region (red and white lines).

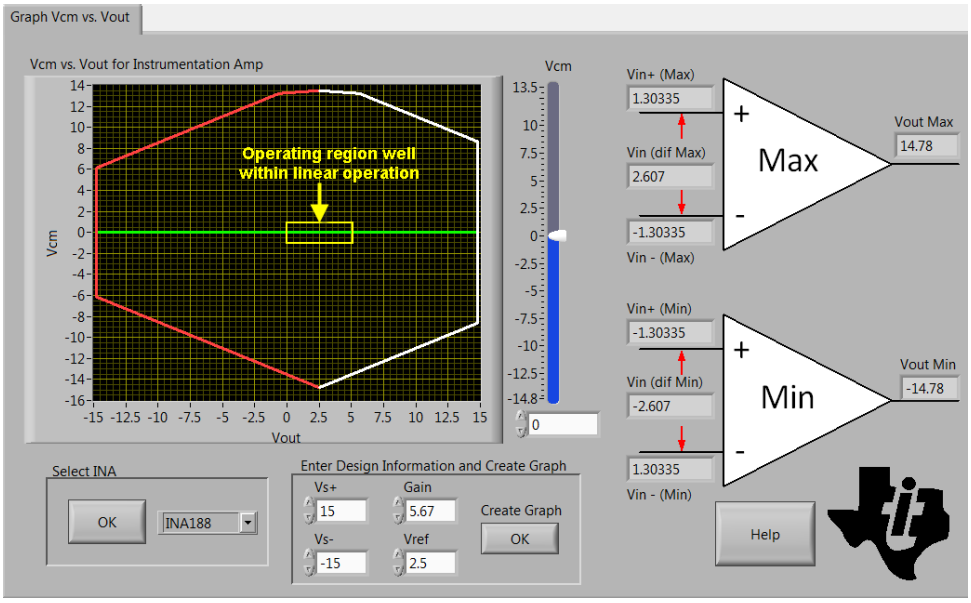

Figure 3: Vcm vs. Vout plot

4 Simulation

4.1 Transfer Function

Figure 4 depicts the TINA-TI schematic used to verify the transfer function of the design.

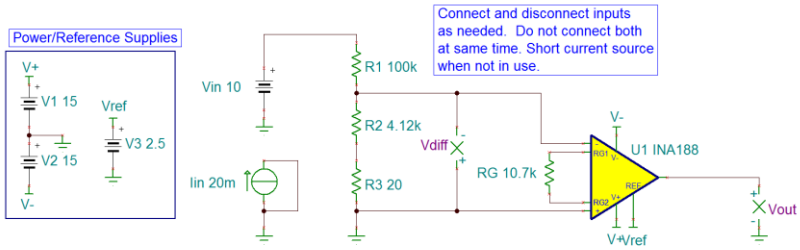

Figure 4: TINA-TI™ schematic for transfer function

Figure 5 depicts the transfer function in voltage mode. To prevent a simulation error, the current source must be shorted to ground as shown in Figure 4.

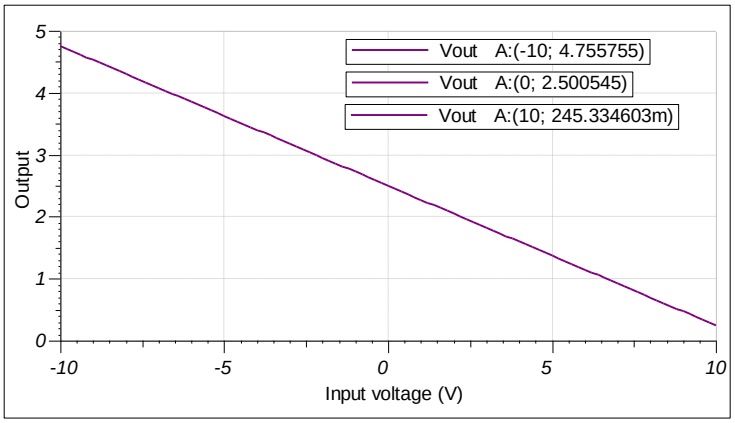

Figure 5: Voltage mode transfer function

Figure 6 depicts the transfer function in current mode. The voltage source should be completely disconnected from the circuit to simulate a real-world scenario.

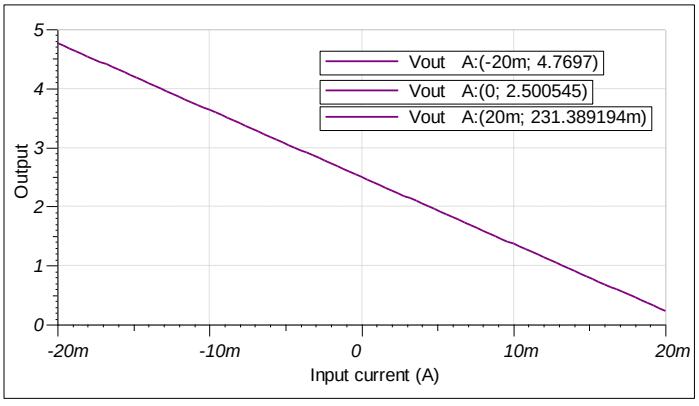

Figure 6: Current mode transfer function

4.2 Error Analysis

Parameter stepping of the circuit in Figure 4 was simulated by varying the resistors within their typical values (±1σ), which is 1/3 of their given tolerance. A spreadsheet in the design archive zip file was used to determine the corresponding resistor values. Given four resistors in the design, there are 16 combinations. Table 2 compares the simulation results for both current and voltage mode with the design goal.

Table 2. Design Goals vs. Simulated Performance

	Goal	Simulated (Current)	Simulated (Voltage)
Offset Error		0.022%	0.022%
Gain Error		0.0601%	0.092%
Total Error	0.2%	0.065% (RSS)	0.094% (RSS)

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The PCB layout is depicted in Figure 7. The traces for the inputs were kept as short and balanced as possible to minimize impedance. This was aided by placing the terminal block (J1) on the bottom of the PCB. All other standard PCB layout practices were observed, including local power supply decoupling and placing R_G close to the device.

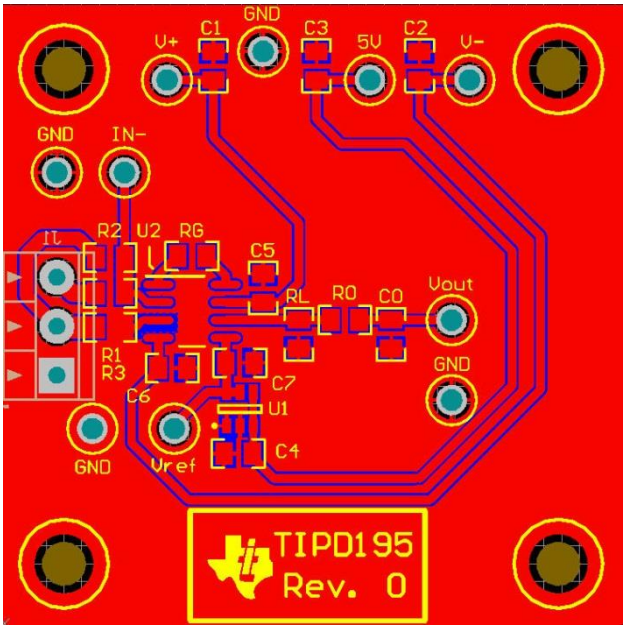

Figure 7: PCB Layout

6 Verification & Measured Performance

6.1 Transfer Function

The output voltage was measured while sweeping the input current from -20 mA to 20 mA and from -10 V to 10 V. Five boards were assembled and measured. The transfer function measurement for Board 1 is shown in Figure 8 while the remaining results can be found in the design archive zip file.

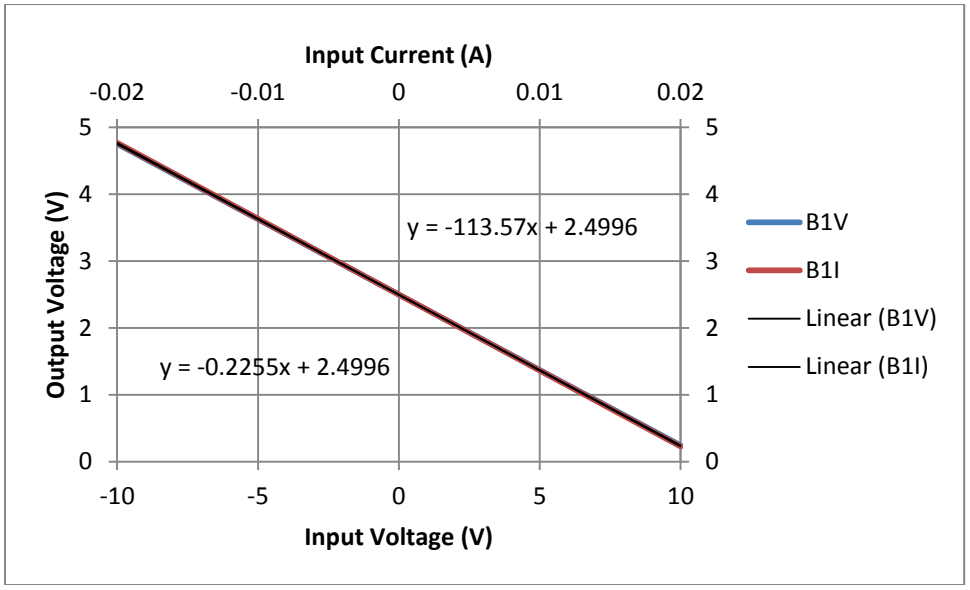

Figure 8: Board 1 Measured Data

The ideal offset voltage for both modes of operation is 2.5V. The ideal gain for the voltage mode is -0.225521486 V/V, which was obtained via simulation and given in the design archive zip file. Similarly, the ideal gain for the current mode is -113.458 V/A.

Table 3 compares the design goal with measured performance. Measurement results for all boards is contained in the design archive zip file.

Table 3. Design Goals vs. Measured Performance

	Goal	Measured (Current)	Measured (Voltage)
Offset Error		±0.031%	±0.032%
Gain Error		±0.139%	±0.15%
Total Error	0.2%	0.142% (RSS)	0.153% (RSS)

7 Modifications

Table 4 lists some key specifications of the INA188 used in this design.

Table 4. INA188 Specifications

	Typical	Maximum
Offset Voltage	35.58 µV (G=5.67V/V)	84.98 µV (G=5.67V/V)
Gain Error	±0.05% (G=10)	±0.2% (G=10)

Comparing the INA188 gain error to the measured results from Table 3 shows that the resistors are the primary source of error.

Given an ideal differential voltage of ±400 mV, the offset voltage of the INA188 contributes just 0.009% (typical) or 0.021% (max) error. Comparing the INA188 offset error to the measured results from Table 3 shows that the resistors are again the primary source of error. To improve the accuracy of this design, consider tightening the tolerance of the 0.1% resistors to 0.05% or better.

Typical laboratory bench power supplies were used to provide the ±15 V and +5 V rails. In an actual design it may be desirable to use the TPS65133 or the TPS65130. These devices output ±5 V or ±15 V given a single +5 V supply.

While this design utilizes dual supplies, sometimes it is desirable to use a single 5 V supply. The INA326 is a rail-to-rail input/output instrumentation amplifier that should be considered. For true zero output voltage, the LM7705 negative bias generator may be used as shown in TIPD129.

8 About the Author

Pete Semig is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He supports Texas Instruments' difference amplifiers & instrumentation amplifiers. Prior to joining Texas Instruments in 2007, he earned his B.S.E.E. and M.S.E.E. from Michigan State University in 1998 & 2001, respectively. From 2001-2007 he was a faculty member in Michigan State University's Department of Electrical & Computer Engineering where he taught a variety of courses and laboratories.

9 Acknowledgements & References

The author would like to acknowledge Collin Wells for his technical contributions to this design.

Appendix A.

A.1 Electrical Schematic

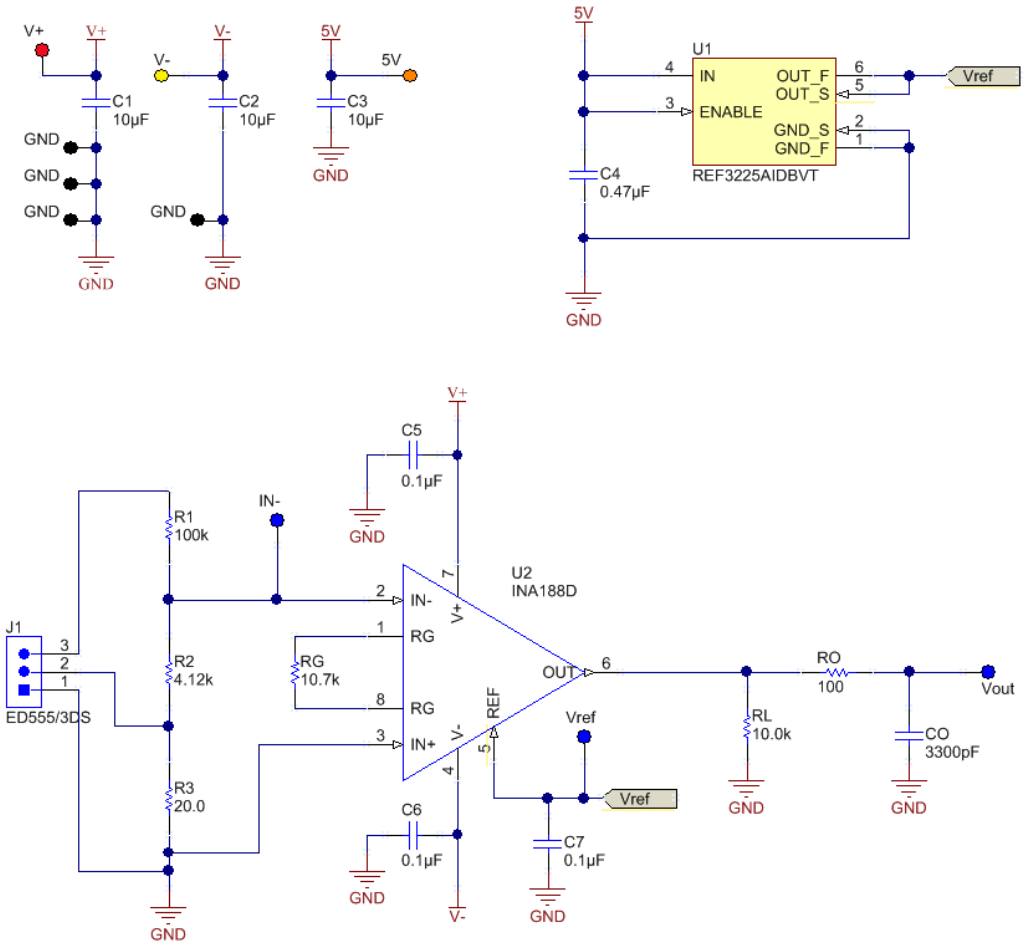

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Texas Instruments

Bill of Materials

TI DESIGNS

TIPD195: 3 Terminal PLC Reference Design

Quantity	Designator	Value	Description	Manufacturer	Manufacturer Part Number	DigiKeyPartNumber
3	C1, C2, C3	10uF	CAP CER 10UF 35V 10% X6S 0805	MuRata	GRM21BC8YA106KE11L	490-10504-1-ND
1	C4	0.47uF	CAP, CERM, 0.47 µF, 20 V, +/- 10%, X5R, 0805	Taiyo Yuden	TMK212BJ474KD-T	587-1290-1-ND
3	C5, C6, C7	0.1uF	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0805	AVX	08055C104KAT2A	478-1395-1-ND
1	CO	3300pF	CAP, CERM, 3300 pF, 50 V, +/- 10%, X7R, 0805	Yageo America	CC0805KRX7R9BB332	311-1131-1-ND
1	J1	N/A	Terminal Block, 6A, 3.5mm Pitch, 3-Pos, TH	On-Shore Technology	ED555/3DS	ED1515-ND
1	R1	100k	RES SMD 100K OHM 0.1% 1/10W 0805	TT Electronics/Welwyn	PCF0805-12-100KBT1	985-1404-1-ND
1	R2	4.12k	RES SMD 4.12K OHM 0.1% 1/8W 0805	Panasonic Electronic Components	ERA-6AEB4121V	P4.12KDACT-ND
1	R3	20	RES SMD 20 OHM 0.1% 1/10W 0805	TE Connectivity AMP Connectors	RN73C2A20RBTD	A119985CT-ND
1	RG	10.7k	RES SMD 10.7K OHM 0.1% 1/8W 0805	Yageo	RT0805BRD0710K7L	YAG1762CT-ND
1	RL	10.0k	RES, 10.0 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080510K0FKEA	541-10.0KCCT-ND
1	RO	100	RES, 100, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805100RFKEA	541-100CCT-ND
1	V+	Red	Test Point, TH, Compact, Red	Keystone	5005	5005K-ND
1	V-	Yellow	Test Point, Compact, Yellow, TH	Keystone	5009	5009K-ND
1	5V	Orange	Test Point, Compact, Orange, TH	Keystone	5008	5008K-ND
4	GND	Black	Test Point, TH, Compact, Black	Keystone	5006	5006K-ND
3	Vref, Vout, IN-	Blue	Test Point, Compact, Blue, TH	Keystone	5122	5122K-ND
1	U1	N/A	IC VREF SERIES 2.5V SOT23-6	Texas Instruments	REF3225AIDBVR	296-39162-1-ND
1	U2	N/A	INA188 Precision, Zero-Drift, Rail-to-Rail Out, High Voltage INA	Texas Instruments	INA188	INA188
4	N/A	N/A	STANDOFF HEX 4-40THR ALUM 1L"	Keystone	2205	2205K-ND
4	N/A	N/A	MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener Supply	PMSSS 440 0025 PH	H703-ND

Figure A-2: Bill of Materials

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