TI Designs
Noise-Tolerant Capacitive-Touch Human-Machine Interfaces Design Guide

TEXAS INSTRUMENTS

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Design Resources

TIDM-CAPTOUCHEMCREF	TI Design Files
MSP430FR2633	Product Folder
UCC28910	Product Folder
TPS7A4533	Product Folder
TCA9535	Product Folder
TPD1E10B06	Product Folder
ISO7221C	Product Folder
MSP-CAPT-FR2633	Tools Folder

TI E2E™ Community

ASK Our E2E Experts

Universal AC Input
↓
Input EMI Filter
↓
Flyback Switcher UCC28910
↓
Linear Regulator TPS7A4533
↓

IO Expander TCA9535 → LED Touch Status Indicators

Touch Sensing MCU

MSP430FR2633

→ LED System Status Indicators
← Capacitive Touch Buttons
← Capacitive Touch Slider

Isolated UART ISO7221C
↕
ESD Protection TPD1E10B06
↓
Isolated UART Interface

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Design Features

- MSP430™ CapTIvate™ MCU for Noise-Tolerant Capacitive-Touch Sensing
- IEC 61000-4-6 Conducted Noise Tolerance
- IEC 61000-4-4 Electrical Fast Transient/Burst Tolerance
- IEC 61000-4-2 Electrostatic Discharge Tolerance
- Mutual and Self Capacitance
- Universal AC and 12-VDC Power
- Isolated Communications Port for Debug and Test

Featured Applications

- Appliances and White Goods
- Industrial Control Panels
- TV, AV, and Set-Top Box Interfaces
- Building Automation User Interfaces
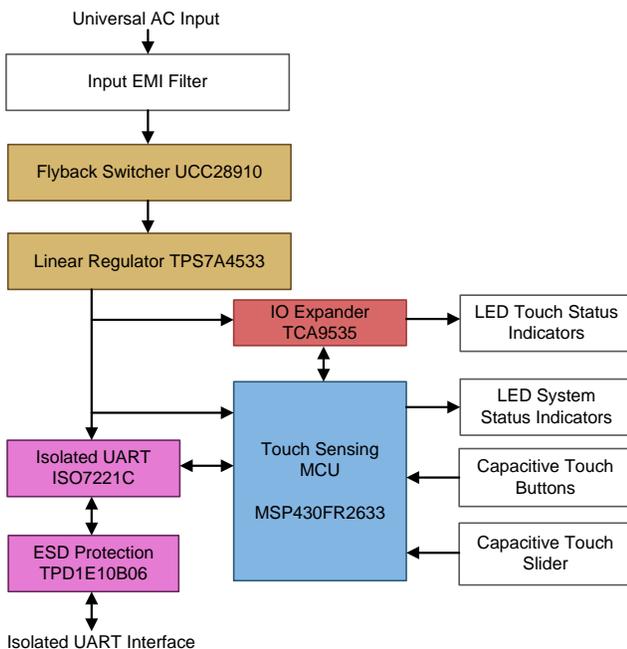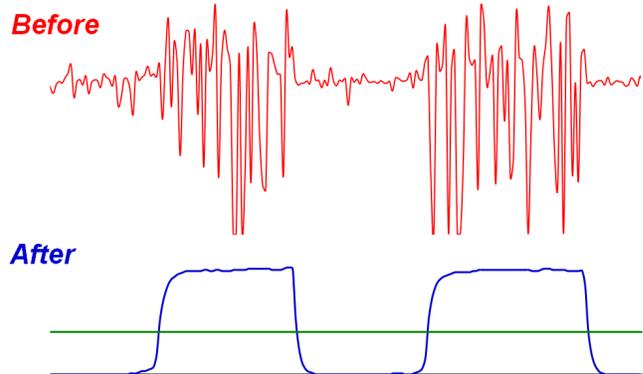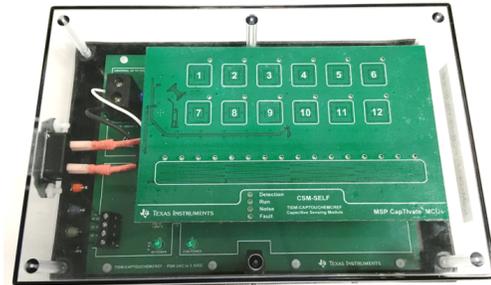
Before

After

An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

The TIDM-CAPTOUCHEMCREF is a reference design for implementing noise-tolerant capacitive-touch human-machine interfaces (HMIs). These interfaces are composed of modular subsystems connected to create several test configurations for evaluating immunity to conducted-RF noise, electrical fast transients, and electrostatic discharge (ESD) events in different power source and application scenarios.

A complete system assembly consists of one capacitive-sensing module (CSM), one power-supply module (PSM), one enclosure, and the associated wiring harnesses.

There are two CSMs:
- CSM-MUTUAL (A mutual-capacitance-based user interface module)
- CSM-SELF (A self-capacitance-based user interface module)

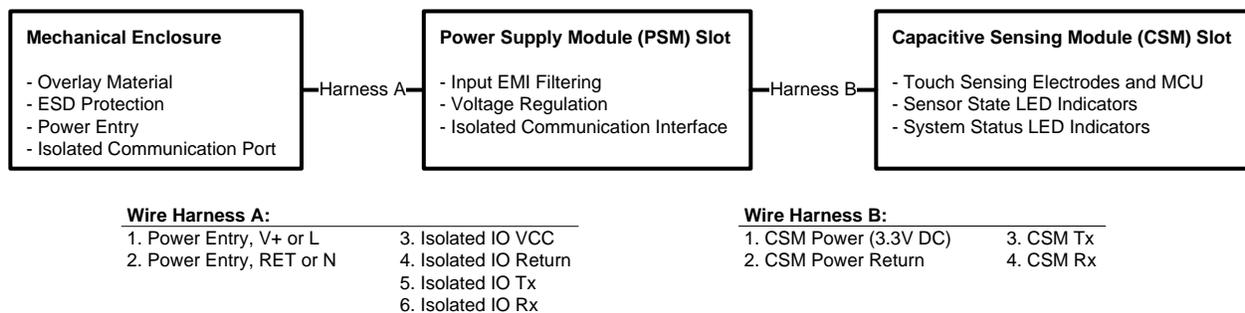There are two PSMs (one for AC-mains power and one for 12-VDC power):
- PSM-UACTO3.3VDC (A universal AC to 3.3-VDC power-supply module)
- PSM-12VDCTO3.3VDC (A 12- to 3.3-VDC power-supply module)

A CSM may be connected to either PSM for power, or powered directly, for a total of six testable combinations:
- CSM-MUTUAL with universal (90 to 265 VAC at 50 to 60 Hz) power entry
- CSM-MUTUAL with 12-VDC power entry
- CSM-MUTUAL with 3.3-VDC direct power
- CSM-SELF with universal (90 to 265 VAC at 50 to 60 Hz) power entry
- CSM-SELF with 12-VDC power entry
- CSM-SELF with 3.3-VDC direct power

In addition to the test configurations outlined previously, each PSM can be configured with or without a small form-factor, common-mode choke on the 12-VDC supply rail.

Figure 1 shows the enclosure, PSM, and CSM subsystems connected to form a complete functional unit.

Wire Harness A:
1. Power Entry, V+ or L	3. Isolated IO VCC
2. Power Entry, RET or N	4. Isolated IO Return
	5. Isolated IO Tx
	6. Isolated IO Rx

Wire Harness B:
1. CSM Power (3.3V DC)	3. CSM Tx
2. CSM Power Return	4. CSM Rx

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Figure 1. Top-Level Subsystem Diagram

1.1 Key System Specifications

Table 1. Capacitive-Sensing Module Specifications

PARAMETER	CSM-SELF	CSM-MUTUAL
Buttons	12 toggle buttons with state retention	32 toggle buttons with state retention
Sliders	Single 6-in [150 mm] slider: 8-bit (256 points) 0.023-in [0.6 mm] per point with state retention	None
Report rate	25 Hz	25 Hz
Response time (Typical)	90 ms	90 ms
Serial interface	250-kbps full-duplex isolated UART	
Input voltage	3.3 VDC	
Maximum-power consumption[1]	205 mW (62 mA)	234 mW (71 mA)
Typical-power consumption[2]	6.9 mW (2.1 mA)	12.6 mW (3.8 mA)
Minimum-power consumption	4.6 mW (1.4 mA)	10.6 mW (3.2 mA)
MSP430FR2633 FRAM code footprint	10630B (69% usage)	10696B (70% usage)
MSP430FR2633 FRAM data footprint	494B (96% usage)	494B (96% usage)
MSP430FR2633 RAM footprint	1868B (45% usage)	2687B (65% usage)

[1] Power consumed with all sensor status LEDs on and scan LED on.
[2] Power consumed with all sensor status LEDs off and scan LED on.

Table 2. Power-Supply Module Specifications

PARAMETER	PSM-UACTO3.3 VDC	PSM-12VDCTODC3.3 V
Supported-input voltage range	90 to 265 VAC	3.8 to 13 VDC
Power-supply output voltage	3.3-V nominal	3.3-V nominal
Power-supply output tolerance	±4 mV (25°C), ±100 mV (–40°C to +85°C)	±4 mV (25°C), ±100 mV (–40°C to +85°C)
Maximum load (12-V rail)	6 W	N/A
Maximum load (3.3-V rail)	330 mW	330 mW

2 System Block Diagram

Figure 2 is a block diagram of the superset system that includes the universal AC-mains supply.
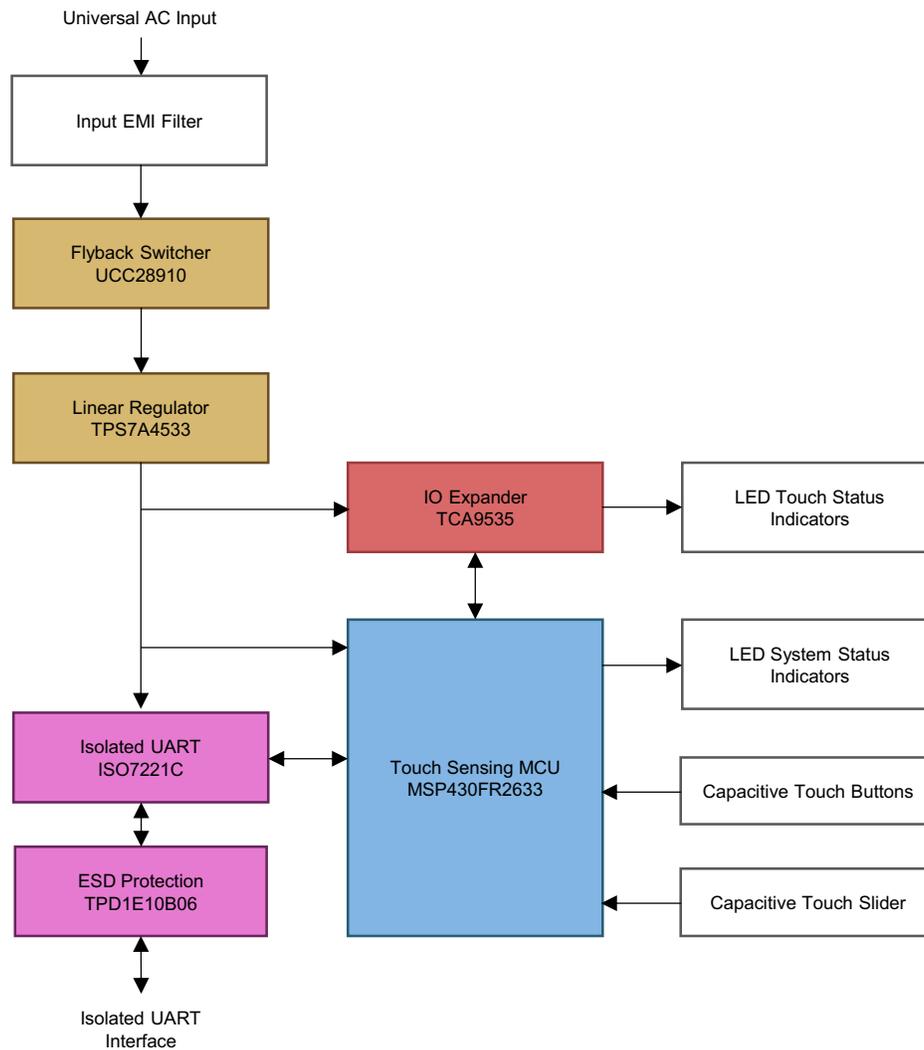
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Figure 2. System Block Diagram

2.1 MSP430FR2633

The MSP430FR2633 is a 16-bit microcontroller with programmable ferroelectric memory (FRAM) and CapTIvate capacitive-sensing technology. CapTIvate is a flexible and robust capacitive-sensing technology targeted at capacitive user interface applications such as buttons, sliders, wheels, and proximity sensors. The CapTIvate technology in the MSP430FR2633 has several key features designed to ensure accurate touch detection in noisy environments. Figure 3 shows the high-level block diagram of the CapTIvate peripheral architecture.
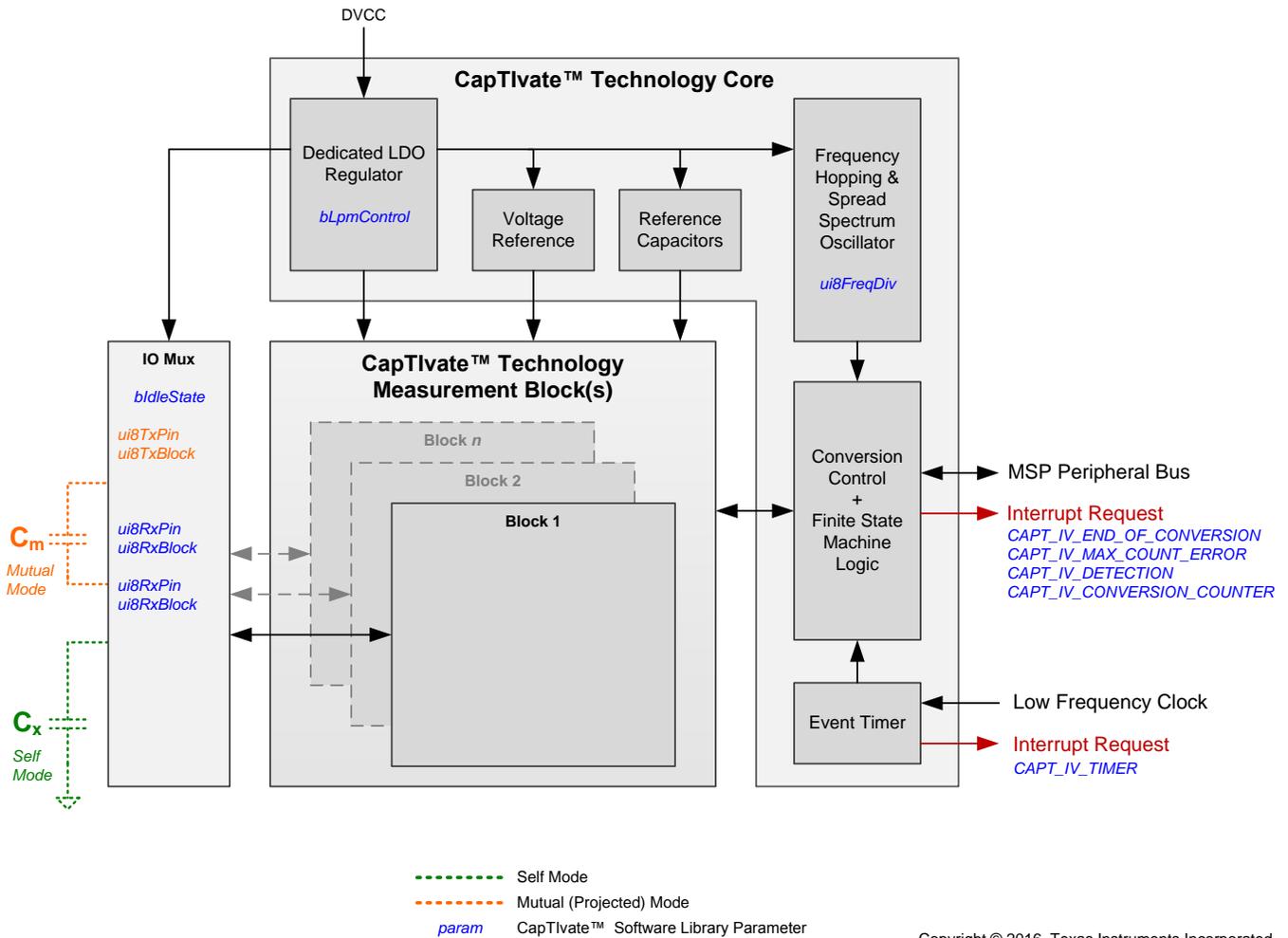

Figure 3. CapTIvate Peripheral Architecture

2.1.1 Dedicated Voltage Regulator

The CapTIvate peripheral contains a dedicated on-chip low-dropout (LDO) regulator that creates a low-noise, 1.5-V supply for the CapTIvate analog measurement blocks. This dedicated LDO provides several benefits. The sensitivity of the user interface does not vary with any changes in the DVCC-supply voltage. Solutions that are referenced directly to DVCC are negatively affected by variations in sensitivity when the DVCC changes because the E-field propagation from the electrode is reduced as voltage is reduced. The 1.5-V CapTIvate LDO is operational throughout the 1.8- to 3.6-V supply range of the MCU. The LDO also provides line regulation, limiting the effect of periodic and transient voltages on the DVCC supply rail in differential mode. The CapTIvate LDO is seperate from the LDO supplying the digital logic on the MCU, minimizing interference from switching digital logic on-chip.

2.1.2 Integrator-Based Charge Transfer Engine

The CapTIvate peripheral uses a highly flexible charge transfer-based measurement engine that acts as a charge integrator, with a low-impedance electrode drive. This method is more immune to conducted noise than are relaxation oscillator-based sensing methods with high-impedance drives.

2.1.3 Parasitic-Capacitance Offset Subtraction

The CapTIvate peripheral features parasitic-capacitance offset subtraction in the analog signal chain. This feature allows for the effects of large parasitic capacitances to be removed from the measurement, and therefore, increases sensitivity to touches. This feature benefits noise immunity because large, dense circuit-return structures can provide shielding. With many capacitive-sensing solutions, only limited circuit-return shielding can be used near the sensing electrodes. This lack of dense shielding structures negatively impacts tolerance of ESD, EFT, and RF interference. With CapTIvate, good EMC layout techniques can be used without compromising the capacitive-sensing performance. Figure 4 shows the CapTIvate measurement block signal chain.
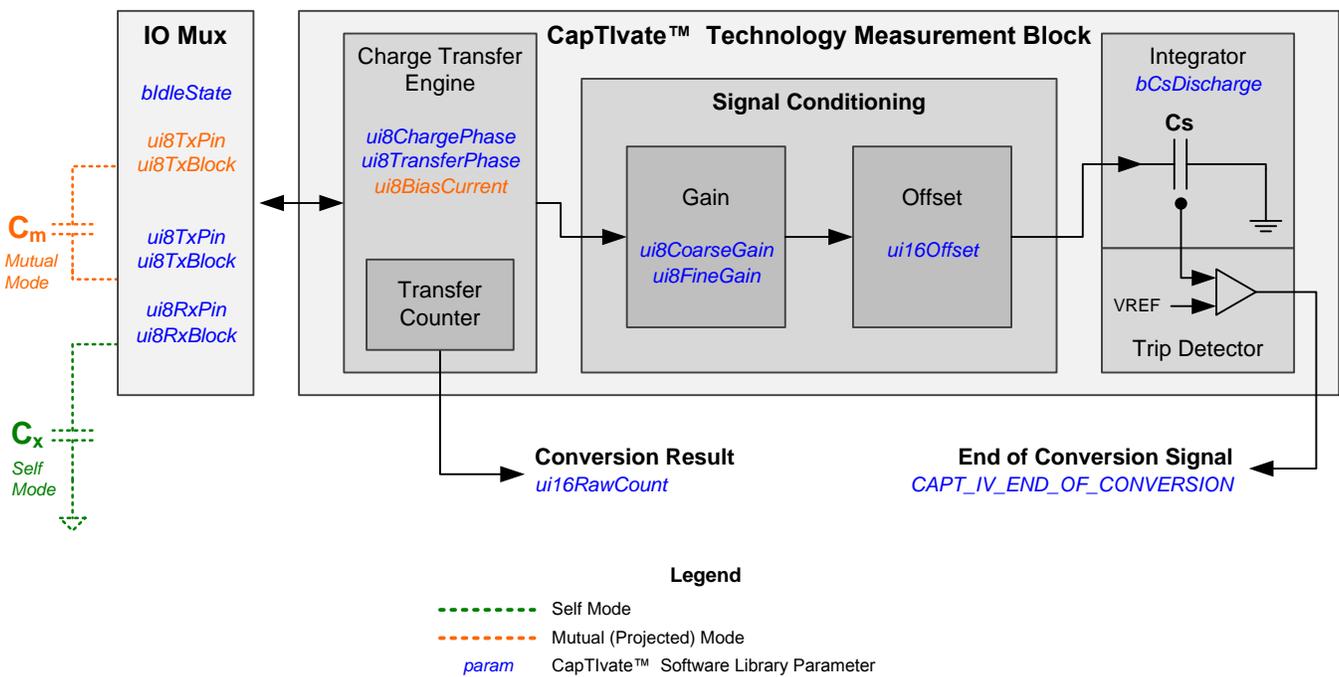

Figure 4. CapTIvate Measurement Block Signal Chain

2.1.4   Frequency-Hopping and Spread-Spectrum Oscillator

The CapTIvate peripheral contains a dedicated, on-chip oscillator for conversion clocking. This oscillator has a frequency-hopping capability. This ability lets the oscillator switch to one of four base conversion frequencies that are strategically selected to avoid harmonic overlap. If noise exists at a conversion frequency or its harmonic, switching the conversion frequency to one of the other options detects this noise so it can be eliminated. Figure 5 shows this concept.
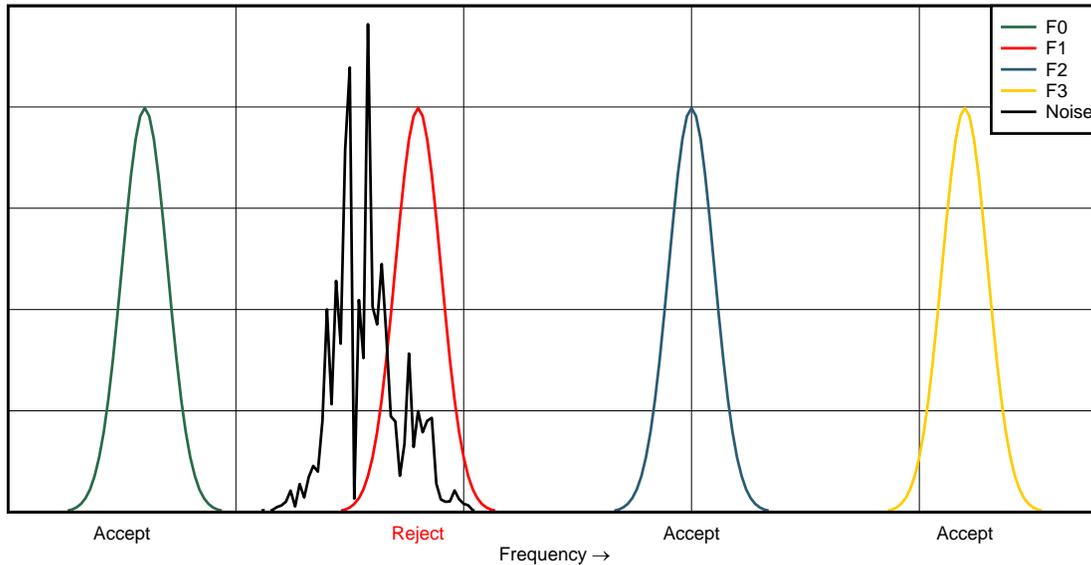

Figure 5. CapTIvate Frequency Hopping Oscillator

2.1.5   CapTIvate Design Ecosystem

The CapTIvate peripheral comes with a complete design ecosystem, including the full-feature CapTIvate software library and the CapTIvate design center development GUI. The software library provides algorithms for noise immunity that use the frequency-hopping capability of the oscillator.

2.2 *TCA9535*

The TCA9535 device is a 16-bit digital I/O expander with an I^{2}C host interface. The expander operates from 1.65 to 5 V with 5-V tolerant I/O ports and is ideal for large-scale I/O expansion when connected to microcontrollers with small pin counts. To support the connection of multiple expanders to the same I^{2}C bus, devices are address-selectable with up to eight addresses, because of three address selection pins. The expander may be used to provide additional I/O to read switches and sensors, or to drive LEDs, fans, and other devices. The TCA9535 device contains latched outputs with high-current drive capability and is suitable for driving LEDs directly. Figure 6 shows a functional block diagram.
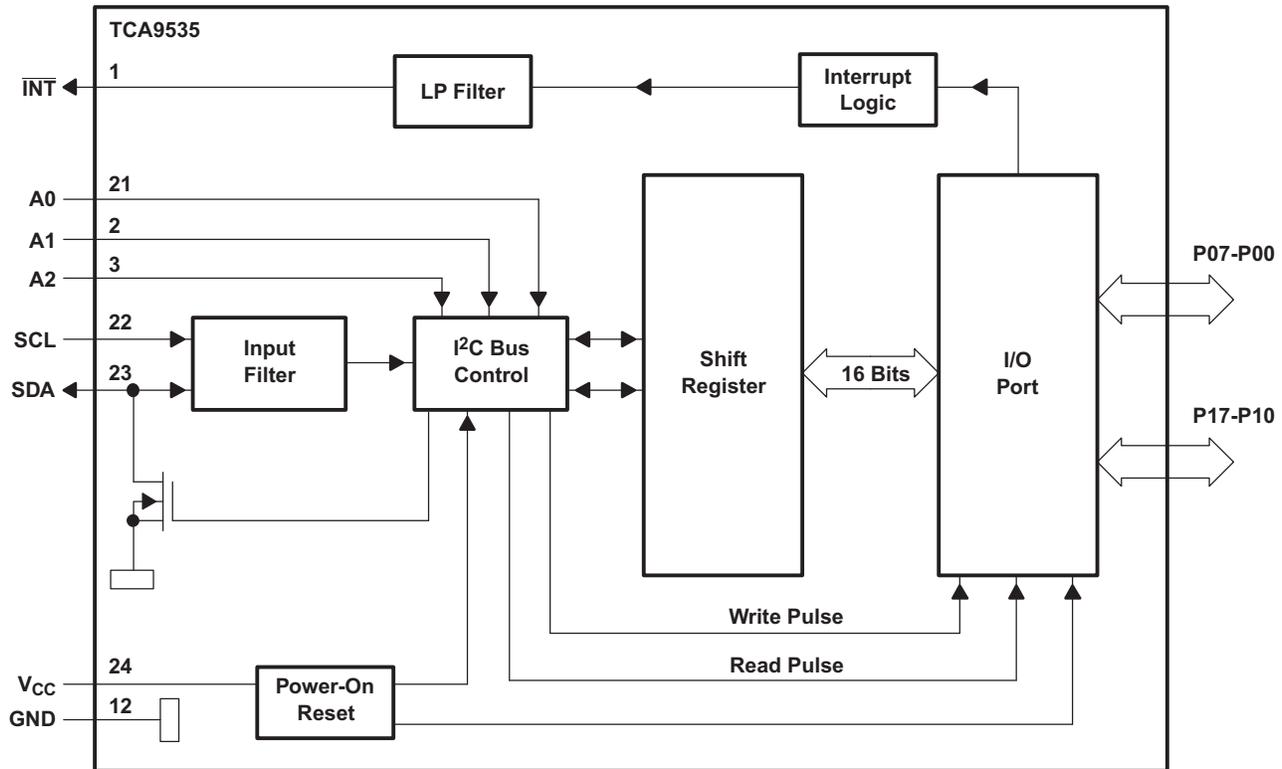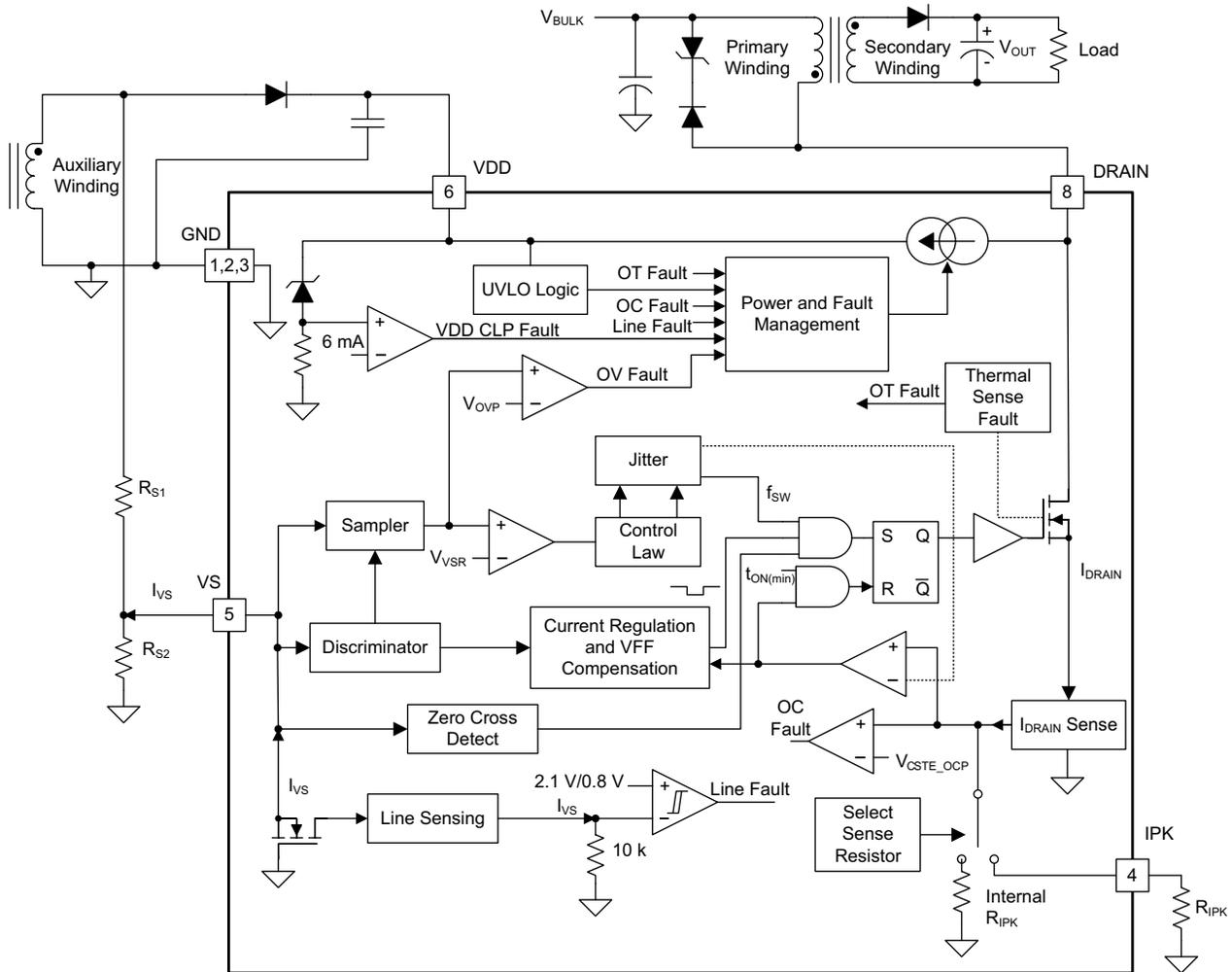

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Figure 6. TCA9535 Functional Block Diagram

2.3 UCC28910

The UCC28910 device is the switching IC in the isolated flyback converter used in the universal AC to 12-VDC power converter of this design. This converter contains an integrated, 700-V power FET with the control logic for the converter. The UCC28910 device provides output voltage and current regulation without an optical coupler and achieves this by monitoring operating information from an auxiliary flyback winding and from the power FET to provide the output voltage and current control. The UCC28910 control algorithms vary the switching frequency and peak-primary-current modulation to achieve high efficiency. Discontinuous conduction mode (DCM) with valley switching is used to reduce switching losses. Switching frequencies extend to 115 kHz. Frequency jittering combined with controlled-drain voltage slope during FET switch-on and switch-off reduce the cost of the input EMI filter required on the power supply. Figure 7 shows a functional block diagram of the switcher.

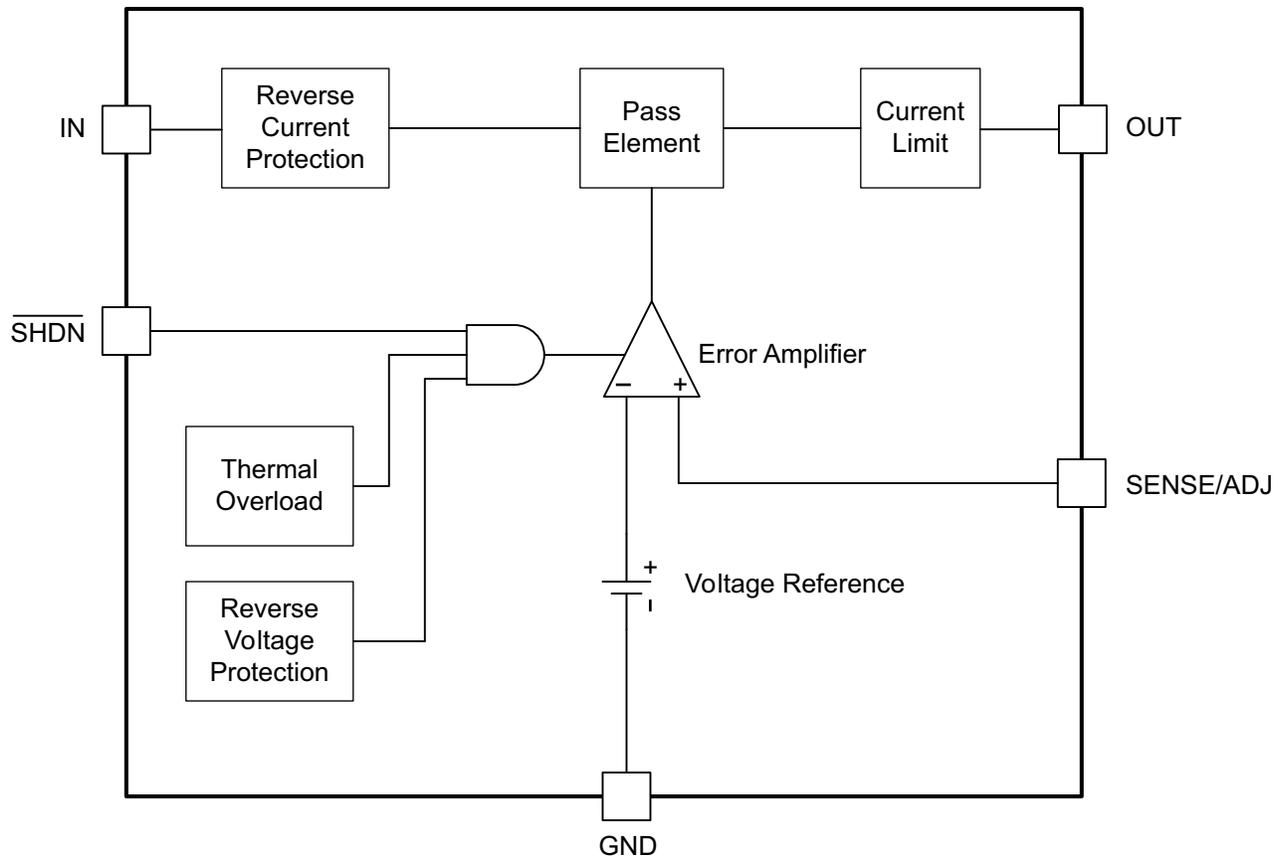Copyright © 2016, Texas Instruments Incorporated

Figure 7. UCC28910 Functional Diagram

The UCC28910 supports output power up to 6 W in an enclosed power adapter or up to 7.5-W open frame, assuming support for a wide input range of 90 to 265 VAC.

2.4 *TPS7A4533*

The TPS7A4533 is an LDO voltage regulator optimized to have a fast transient response. This voltage regulator has a fixed-output voltage of 3.3 V. Other members of the TPS7A45xx family are available in other output voltages or with an adjustable-output voltage. The regulator can supply up to 1.5 A of output current at a dropout of 300 mV. Quiescent current is 1 mA when enabled, and less than 1 µA in shutdown mode. Input voltages may be up to 20 VDC.

The regulator is stable with 10 µF of output capacitance, with relaxed ESR requirements. Small ceramic capacitors can be used for the bulk output capacitance. The regulator contains several internal protection circuits, such as current limiting, thermal limiting, reverse-current protection, and reverse-battery protection. No protection diodes are required. Figure 8 shows the functional diagram of TPS7A45xx.

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Figure 8. TPS7A45xx Functional Diagram

The TPS7A4533 also has a junction temperature rating of 125°C, allowing high-voltage drops at high current with fewer cooling constraints.

2.5 TPD1E10B06

The TPD1E10B06 is a transient-voltage suppressor (TVS) device for protecting downstream ICs against ESD events. Figure 9 shows the back-to-back diode array featured in this device. The 12-pF line capacitance is acceptable for the 250-kbps UART interface used in this design. If a TVS was required on capacitive-sensing lines, a device with a lower line capacitance must be used. Figure 9 shows a functional diagram of TPD1E10B06.
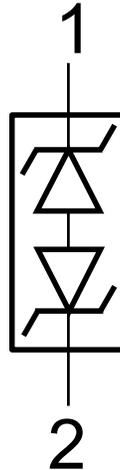

Figure 9. TPD1E10B06 Functional Diagram

The TPD1E10B06 device is rated for 30-kV contact and 30-kV air discharge per the IEC 61000-4-2 standard and has a 10-V clamping voltage at 1 A of current, and a breakdown voltage of 6 V, which is greater than the maximum 5-V VCC and logic level used in the isolated I/O interface of this design.

2.6 ISO7221C

The ISO7221C is a high-speed, dual-channel digital isolator with 40 kV/µs of common-mode transient immunity when supplied at 3.3 V and provides up to 2.5-kV$_{rms}$ continuous isolation. The isolator is ideally suited for computer peripheral interfaces and data acquisition, and provides power domain isolation in this TI Design so data can be sent from the system to a host PC during conducted-noise testing. The isolator uses TI's silicon dioxide isolation barrier that provides galvanic isolation of up to 4-kV peak. Figure 10 shows the simplified schematic of the ISO7221C.
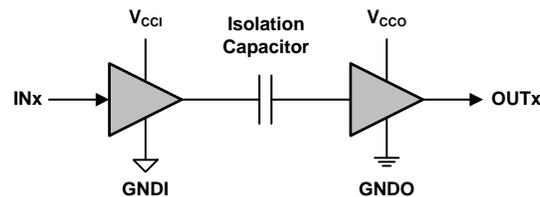
V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

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Figure 10. ISO7221C Simplified Schematic

Unlike optical couplers, the ISO7221C does not require external components to improve performance or provide biasing and current limiting. This device requires only two bypass capacitors, one for each power domain.

3 Capacitive-Sensing and Electromagnetic Compatibility (EMC) Theory

Capacitive-touch sensing is based on the precision measurement of small changes over time in the electric field that surrounds a conductive electrode. The field around the electrode changes when the user of the interface approaches and touches it. The change in the electric field results from a change in the overall dielectric between the sensing electrode, nearby conductive structures, and earth ground. This change is detected and interpreted by software running on a microprocessor that determines whether an interaction has occurred and flags to the application that the sensor has been touched. Because this change in an electric field over time is small, electromagnetic interference (EMI) (whether radiated or conducted into the measurement circuit) with significant amplitude can disturb the measurement if that EMI is at a frequency at which the measurement circuit is vulnerable. Because of this effect, electromagnetic compatibility is important when designing capacitive-touch user interfaces. This section provides an introduction to the ways in which EMI may disturb a capacitive-sensing circuit.

3.1 Types of EMI

Because capacitive-touch interface designers are focused primarily on the susceptibility of the capacitive-touch sensing circuit to unwanted EMI, the focus of this TI design is how to overcome susceptibility challenges rather than the challenges of emissions. The foundational test and measurement standards for the immunity of products to EMI are defined in the IEC 61000-4 series. Specific immunity requirements for a product vary by geographic region and by product type, but most product standards refer to the test and measurement techniques in the IEC 61000-4 series. This design addresses the three tests that most commonly create problems for capacitive-touch designers:

- Conducted-noise immunity (CNI)
- Electrical fast transients/burst immunity (EFT/B)
- Electrostatic Discharge Immunity (ESD)

3.1.1 Common-Mode Conducted Disturbances

Capacitive-touch circuits are inherently vulnerable to radio frequency (RF) interference. There are two types of RF interference: conducted and radiated. The distinction is arbitrary and is based on the frequency of the noise being tested. At lower frequencies (10s of kHz to 10s of MHz), the wavelengths are sufficiently long so that it is unlikely that products are efficient receiving antennas. Performing a radiated (far-field) test at these frequencies is also unrealistic, because the antennas required to generate disturbances must be either large or high power. For example, a 1-MHz noise signal has a wavelength of 300 m. Due to the large wavelengths of lower frequencies, immunity to RF disturbances in the range of 0 Hz to 80 MHz is tested by directly coupling the noise signal into the product under test through its power or signal cables. This coupling method is also indicative of real scenarios. The IEC 61000-4-6 standard specifies how to test a product for immunity to conducted disturbances in the frequency range of 150 kHz to 80 MHz. Higher-frequency disturbances are radiated disturbances, and are covered by IEC 61000-4-3. Because most capacitive-sensing circuits operate at less than 80 MHz, the IEC 61000-4-6 conducted noise immunity test is most relevant. Immunity to radiated disturbances is important, but the majority of immunity issues occur during conducted-noise testing.

While the IEC 61000-4-6 standard is intended to test the immunity of products as a whole, the standard is also useful for debugging the immunity of subsystems inside a product. This usefulness is most evident in products with low-cost, switching power supplies. Commonly employed in low cost, compact power supplies, the flyback converter topology often provides a noisy rail with significant common-mode noise to the downstream electronics. Depending on the switching frequency of the converter and the amplitude of the noise generated, this common-mode interference can affect capacitive-sensing circuits. The challenge is applications where the power source is unknown. For cellular phones, tablets, and wearables that use low-cost USB-style chargers, the source can be a personal computer, laptop, wall-wart supply, or a 12- to 5-V supply in a car charger.

The power-supply design and topology plays a significant role in how much common-mode conducted noise current can be conducted from the input side to the output side.Figure 11 shows two different switch-mode power supply (SMPS) topologies. The left circuit represents a fully-isolated, SMPS with independent high-voltage and low-voltage returns. The right circuit represents a SMPS with an HV capacitor connecting the high-voltage return with the low-voltage return.
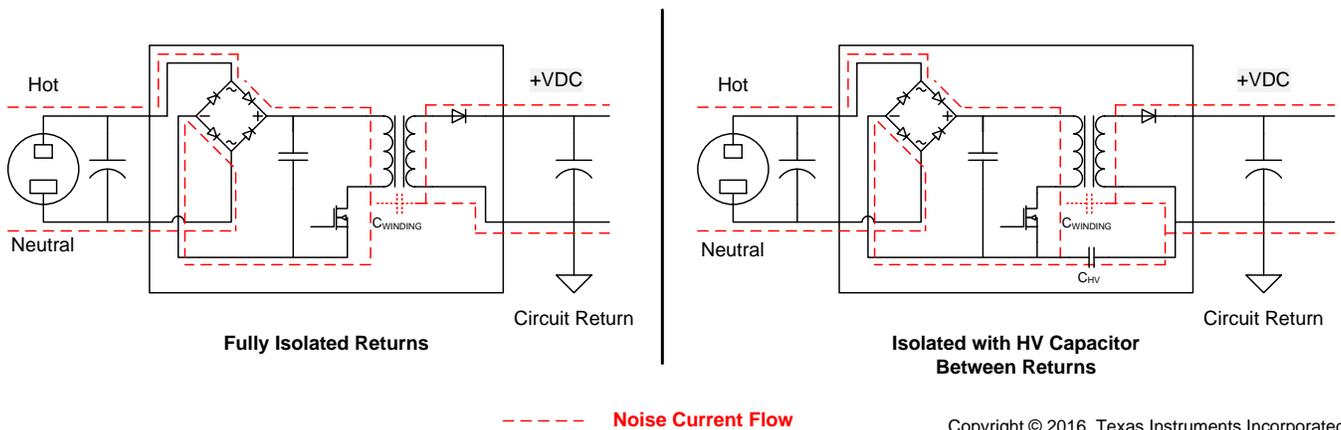
Figure 11. Common-Mode Conducted Noise Current Path through AC Supplies (SMPS)

In the fully-isolated case, there is no path for common-mode currents to flow. Ideal transformers only pass differential-mode AC because common-mode signals present no voltage across the transformer windings. There is no magnetic field generated from common-mode signals. While there is no magnetic coupling path, real transformers have some amount of non-negligible parasitic capacitance between the windings. The size of this undesired capacitance is a function of the physical construction of the transformer—the spacing between the windings and the dielectric material present between the windings. This parasitic capacitance becomes a common-mode coupling path between the high-voltage side and the output, low-voltage side, passing common-mode conducted noise to the low-voltage circuit.

The worst-case-scenario test for a capacitive-sensing interface is noise coupled directly onto the DC supply because there is no transformer to block the common-mode current.

In addition to any parasitic-winding capacitance, an SMPS may have a high-voltage capacitor between the high-voltage return and low-voltage return, as shown in the diagram on the right in Figure 11. The addition of this capacitor helps limit conducted emissions from the SMPS. While the addition of the high voltage capacitor limits noise generated by the power supply, the capacitor also has the unwanted side effect of providing a parallel pathway for noise currents entering the product from the AC mains supply. The SMPS used in this TI Design contains a provision for this HV capacitor to demonstrate this scenario.

3.1.1.1 *Effects of Common-Mode Conducted Noise on Capacitive-Sensing Measurements*

When the capacitive-sensing electrode becomes a part of the noise-current path, the capacitive measurement can be corrupted in several ways depending on the frequency, amplitude, and phase of the noise signal relative to the capacitive-sensing excitation signal.

Mutual capacitance and self-capacitance exhibit different phenomena.Figure 12 shows examples of unprocessed, raw data in response to two touches with and without conducted noise for mutual and self-capacitance. These examples were captured using the MSP430FR2633 capacitive-touch sensing MCU on board the CSM-SELF and CSM-MUTUAL capacitive-sensing modules.
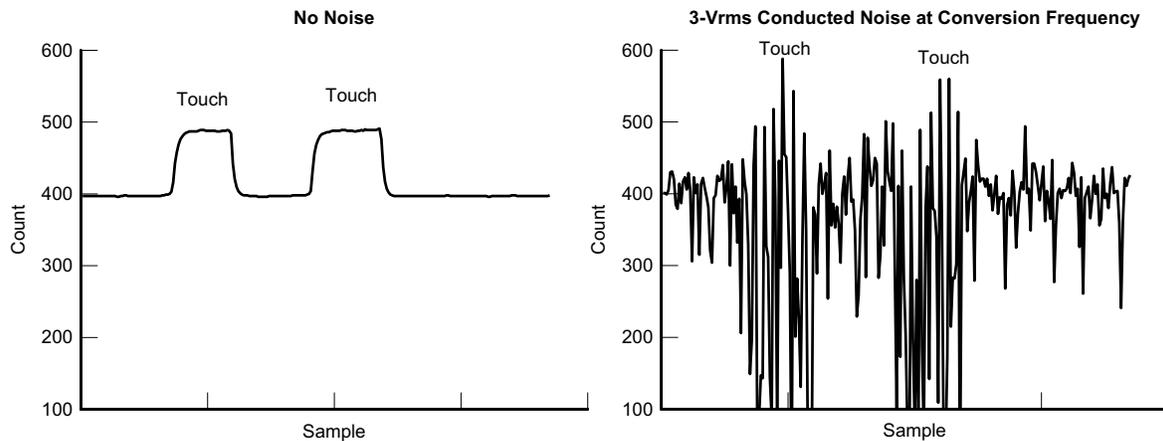
Figure 12. Mutual-Capacitance Conducted Noise Response (Unprocessed Data)

As shown in Figure 12, mutual-capacitance measurements are corrupted when subjected to common-mode conducted noise at or near their conversion frequency. The measurements vary unpredictably greater and less than the base count level of 400. When the buttons are touched, the magnitude of the noise increases but noise is present regardless of whether a touch is present.

Figure 13 shows that self-capacitance measurements exhibit an increase in sensitivity due to touch when subjected to common-mode conducted noise. Unlike the mutual-capacitance example shown in Figure 12, at this stress level the effects of the noise become visible only when a touch is present. The additional sensitivity results from the fact that the injected current into the MCU associated with the noise signal fills the integration capacitor quickly, thereby ending the conversion with a smaller number of change transfers than the no noise case.
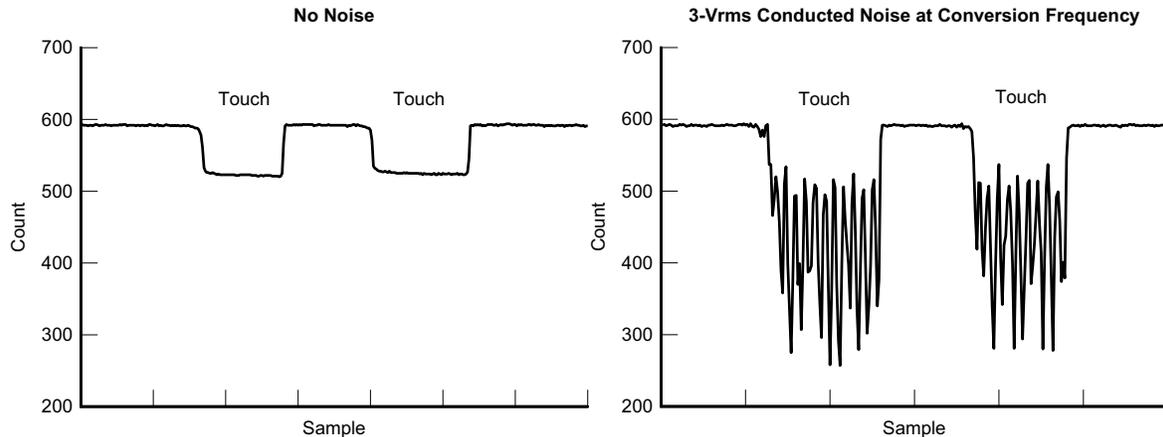
Figure 13. Self-Capacitance Conducted Noise Response (Unprocessed Data)

3.1.2 Electrical Fast Transients and Bursts

In addition to common-mode conducted noise, electrical fast transients frequently present problems for products of many types. Fast transient events are sudden, rapid spikes in voltage on power or signal lines entering a product. These events are generated by the switching of high-current inductive loads (such as motors or induction coils), as well as switch and relay contact bounce. Unlike conducted noise, electrical fast transients occur as one pulse or a burst of pulses, rather than a constant, periodic interference signal. Where conducted noise affects sensitive analog circuits, fast transients may disrupt a variety of circuit components. Failure modes include, but are not limited, to the following:

- Digital-signal corruption (incorrect digital I/O readings, particularly on open-drain style interfaces)
- Unintended digital IC device resets (through the RST line)
- Unintended IC brownout resets
- IC latch-up
- IC destruction
- Disruption of analog measurements, including capacitive sensing measurements
- Memory corruption

Consider a relay opening in a circuit path carrying a large current. When the relay opens, a significant voltage develops across the contacts of the relay. The size of that voltage is a function of the current flowing though the relay before the break, and the inductance of the current loop. If the voltage generated across the relay contacts becomes high enough to overcome the breakdown voltage of the air between the contacts, an air-gap discharge occurs (similar to an ESD event), and current flows between the contacts. This relatively low-impedance path leads to a lower voltage between the relay contacts, which quickly eliminates the air-gap arc that created the conducting path. This elimination causes the large current through the breakdown path to stop flowing, producing another high voltage across the contacts. This process occurs quickly as the relay contacts physically separate. Eventually, the contacts are physically far enough apart that the voltage across the contacts is no longer sufficient to trigger a breakdown of the air gap between them. When this occurs, the relay is effectively settled.

These transient bursts occur in many environments. Industrial and manufacturing environments with heavy-electrical equipment have higher-voltage transients than home and commercial environments that have lower-voltage transients from sources such as power tools and appliances.

The current path resulting from an EFT event is generally common mode and is capacitive, as shown in). EFT events can also be differential mode, where the current path is more obvious than in common-mode.

The IEC 61000-4-4 test specification describes how to test a product for immunity to electrical fast transients and bursts. Testing subjects the product under test to a burst of transients at a stress voltage, frequency, and repetition period. Transients are coupled into the product in differential and common mode. While most consumer products only require 500 V to 1 kV of immunity, many industrial and white goods products require immunity in the 2- to 4-kV range.

The primary defense against EFT is proper filtering and attenuation in the power supply of the product, typically at the power-entry point. Typical protection devices include transient-voltage suppression (TVS) devices, varistors, chokes, and inductors. Similarly to ESD, EFT transient voltages can produce large currents quickly. These large $\frac{dI}{dt}$ transitions generate significant magnetic fields that can induce unwanted currents on other circuits—even circuits behind the protection components of the power supply.

Electrical fast-transients may corrupt capacitive-sensing samples if a transient aligns in time with a measurement. In the event that a transient overlaps a sample, the effects are similar to those from common-mode conducted noise because fast transient voltages on the supply or I/O of a product can lead to large injected currents into a product, which lead to an incorrect integration during a charge transfer. Figure 14 shows the response of a self-capacitance button sensor to a 1.5-kV EFT test.
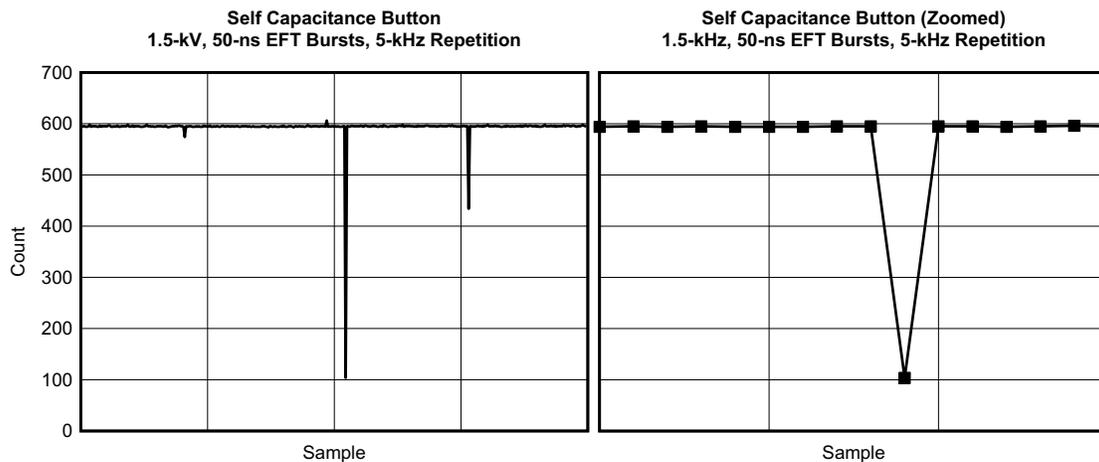
Self Capacitance Button
1.5-kV, 50-ns EFT Bursts, 5-kHz Repetition

Self Capacitance Button (Zoomed)
1.5-kHz, 50-ns EFT Bursts, 5-kHz Repetition

Figure 14. EFT Disruption of Self-Capacitance Button (Raw Data)

Note the asynchronous, aperiodic nature of the interference. During the test, a given EFT burst only affected one sample at a time in contrast to the conducted-noise interference previously discussed.

3.1.3   ESD Events

Many products require some level of ESD immunity analysis. If not properly handled during the design phase, ESD susceptibility can present as a problem during product qualification, becoming more expensive.

An ESD event is a sudden flow of current between two electrically-charged objects. The flow of current is usually caused by either direct contact between the two charged objects, or through the breakdown of a dielectric material. Discharge voltages may be several kilovolts or more. An ESD event applied directly to an integrated circuit pin can destroy the device if of sufficient current.

The ESD event may affect a product in several ways. The most obvious is a direct discharge to the product. This discharge typically occurs when an event happens on a power or interface connector into a product. A second and less obvious impact is the interference associated with an ESD event on a nearby conductive surface or product. ESD events are high-current events with a large time-varying current. This rapid change in current produces a significant magnetic field that can induce undesired current in a nearby circuit, even if there is no galvanic connection.

Consider ESD as a signal in a system, rather than just a static voltage. ESD discharges have outreaching effects beyond the discharge. ESD is effectively a wideband signal, varying from 1 MHz to 3 GHz that tries to penetrate a system.

3.1.3.1   Clarifying HBM, CDM, and IEC ESD Ratings

The IEC 61000-4-2 test standard is the industry-standard specification for system-level ESD testing. The standard specifies test methods for contact and air discharge to a product, and secondary effects resulting from nearby discharges. Semiconductor and integrated-circuit devices typically come with an ESD rating in the data sheet. Typically, a value is given based upon either the human-body model (HBM) or charged-device model (CDM). Distinguishing between HBM, CDM, and IEC 61000-4-2 is important. ESD ratings are incomparable between these different standards. HBM and CDM are ratings that intend to specify the immunity of the device to ESD events in an ESD-controlled environment, such as an electronics lab or an electronics assembly facility. These ratings have little or no meaning to system-level ESD immunity after a device is deployed in the field. Figure 15 shows the current waveforms of typical CDM, HBM, and IEC stresses.
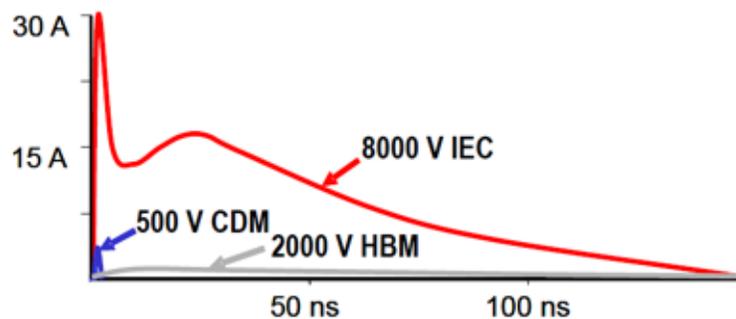

Figure 15. HBM Versus CDM Versus IEC ESD Waveforms

Consider the difference in peak current, pulse duration, and fall time. A typical IEC 61000-4-2 ESD pulse as a peak current of 3.75 A/kV with a rise time greater than 1-ns. Table 3 lists the differences between IEC and HBM/CDM ESD ratings.

Table 3. System-Level ESD Versus Component-Level ESD

Parameter	System-Level ESD	Component-Level ESD
Where is it commonly seen?	System or product EMC-requirement specifications	IC device data sheets
Event	Charged human discharging through a metallic tool to a system	Charged human discharging through the skin to a component
Model	IEC	HBM
Standard	IEC 61000-4-2	JEDEC/ESDA
Category	System EMC immunity	IC reliability
Applicable Environment	Normal operation of the product by a customer	Product assembly in an ESD-controlled facility
Power	Typically powered at most sensitive functional state	Unpowered
Typical Requirement	8-kV contact	1 kV or 2 kV
Peak Current	3.75 A/kV (30 A at 8 kV)	0.64 A/kV (1.3 A at 2 kV)
Rise Time	0.6 to 1.0 ns	2 to 10 ns
Failure Mode	Soft and hard failures	Hard failures
Application	PCs, cell phones, appliances, and so forth	IC

Figure 15 and Table 3 show that data sheet HBM values have only a minor impact on achievable system-level performance. HBM and CDM ratings exist only to specify the reliability of an integrated-circuit device during assembly, and do not cover soft failure use cases. Test data shows there is no strong correlation between HBM/CDM performance and IEC performance.

3.1.3.2 Mechanical Design Considerations for Direct ESD

Designing a product that is robust against ESD requires careful consideration of ESD in the mechanical design and the electrical design. For a capacitive-touch interface, the primary defense against ESD is the design of the overlay surrounding the sensing electrodes. The overlay dielectric material provides the primary electrical isolation between the conductive electrodes and any user or object that might interact with it. Insulating dielectric materials eventually break down and conduct when subjected to an electric field of sufficient strength. Different materials have different breakdown voltages at which they no longer perform as insulators. Typically, the breakdown voltage of a material is approximated in terms of volts per unit of thickness. This approximation is adequate for most product design work. A typical polycarbonate overlay material has a breakdown voltage rating of 15 kV per millimeter. Standard window glass has a breakdown voltage rating of about 10 kV per millimeter.

3.1.3.3 Electrical Design Considerations for Direct ESD

Electrical design for ESD involves developing a strategy for system-level protection. Categorize the signals on a PCB into two categories: internal and external. External signals are signals that are vulnerable to external ESD discharges. Examples of these signals include power cables or ports and I/O cables or ports. Internal signals only exist on a given PCB or subsystem of PCBs, and never leave the product or are exposed to an environment where they can be directly subjected to ESD stress.

Anything directly connected to an external signal must be protected. In addition, internal signals, traces, and other elements near external signals must also be protected because discharge currents in external signal traces and cables can generate strong EMI that induces currents in nearby internal conductors that can be unprotected. This issue can be addressed by suppressing and clamping high-transient voltages on external signals as soon as they enter the system to limit the amount of EMI inside the system near sensitive internal signals. This effect can be achieved through the use of transient voltage suppression (TVS) devices on external signals in the I/O section of the PCB. Off-board cables and wire harnesses, particularly those that exit a system as external signals, must be as short as possible. Cable harnesses can serve as antennas inside a product.

Transient voltage suppression devices work together with a series impedance and on-chip ESD clamps to protect the sensitive internal circuitry inside of an IC. Figure 16 shows a CMOS IC protected by an external TVS and a series resistance. If an ESD discharge occurs to this off-system connection, the primary clamp activates, absorbing a large amount of the current. Depending on the impedance of the primary clamp relative to the IC and resistor in series, a small current passes through the series resistance. If the voltage is higher than the trigger threshold of the on-chip clamp, the on-chip ESD clamps activates and clamps the voltage to protect the internal circuit. A small current flows into the internal circuit. Limiting the current as much as possible by clamping the voltage in two places is the goal. For the clamping to be effective, the impedance of the clamping paths must be low relative to the impedance of the internal circuit.
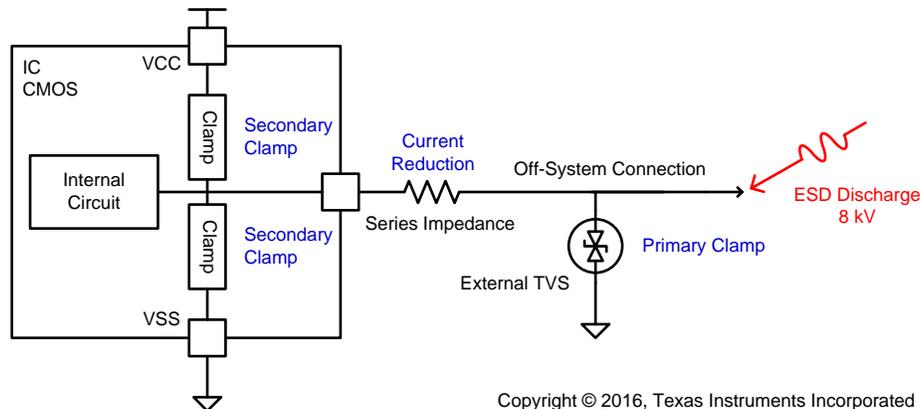
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Figure 16. ESD Protection Network for Off-System Connections

Three-Sided Approach to Noise Tolerance for Capacitive Touch

When designing a capacitive-touch interface that requires a certain level of noise tolerance, the path to a successful design must carefully apply a three-sided approach. The following are the three sides of the approach:

- Hardware design principles
  - Circuit-return, plane-shielding techniques
  - Filtering techniques
  - Protection devices
- CapTIvate™ peripheral EMC features
  - Integrator-based, charge-transfer engine
  - Offset-subtraction capability
  - Frequency-hopping and spread-spectrum oscillator
- Digital-signal processing tools
  - Multi-frequency processing (MFP) algorithm
  - Dynamic threshold adjustment (DTA) algorithm
  - Oversampling
  - IIR filtering
  - Debounce

All three sides are required to achieve immunity. Applying signal processing for an incorrectly-designed layout is often not feasible. This reference design provides an overview of the hardware and software design theory used to achieve designs with high noise tolerance.

4 Hardware Design Theory

This TI design contains four PCB designs: two capacitive-sensing modules and two power-supply modules. The design theory behind the schematic and layout of each PCB is discussed in this section. Successful capacitive touch-sensing designs begin with well-designed hardware. While software plays an important role in the success of the overall solution, the hardware design that enables the signal-processing algorithms and CapTIvate peripheral features to be effective. Poor schematic and layout practices lead to poor noise-immunity performance that cannot be overcome by signal-processing alone. To clarify these effects, this section introduces various design principles.

4.1 *Separation of Functions*

As introduced in Section 1, the power supply and capacitive-sensing functions are separated onto independent PCBs. This separation allows for the same power-supply hardware to be shared between the CSM-MUTUAL and CSM-SELF capacitive-sensing modules and also allows for different power supply scenarios to be tested. The functional divide from a schematic point of view is as follows:

- The PSM is responsible for power entry and input EMI filtering and contains the components required to protect all downstream circuits and devices from fast transient and ESD events on the power entry pins. The CSM expects transient voltages to be attenuated by the PSM, and it does not include its own protection devices.
- The PSM must contain a provision for a common-mode choke coil on the 12-V DC supply rail.
- The PSM must contain the digital isolator for the isolated communications interface, leaving management of different power domains to the PSM.
- The CSM must contain the capacitive-sensing MCU, all sensing electrodes, and state/status LED indicators.

4.2 *CSM*

The capacitive sensing module objectives, requirements, and design are discussed in this section.

4.2.1 Objectives

The CSM hardware was designed with the following objectives in mind:

- A high immunity to disturbances such as conducted noise, electrical fast transients, and electrostatic discharge
- Ability to demonstrate a touch-sensing panel with many sensors, as can be found in a large touch-sensing application such as an industrial control panel or home appliance
- Debug capability while installed in-system
- Ability to stream data through a common interface
- A low-cost module mentality (avoiding expensive PCB features such as micro traces, micro vias, and a high-layer count)

4.2.2 Requirements

The CSM hardware was designed with the following requirements:

- LED-state indicators for each sensor, to indicate the present state of the user interface visually
- LED system-status indicators for latched detect, run, noise detected, and system fault
- 3.3-V power input at greater than 100-mA maximum
- 250-kbps bidirectional UART interface for testing and debug purposes
- Ability to adhere the electrode side of the PCB directly to the overlay material

4.2.3 Layer Stack and Component Organization

The CSM-MUTUAL hardware consists of the following:

- A single, two-layer PCB with 32 mutual-capacitance touch buttons on the top layer and all components mounted on the bottom layer

The CSM-SELF hardware consists of the following:

- A single, two-layer PCB with 12 self-capacitance touch buttons
- A single, 4-element self capacitance touch slider on the top layer

All components are mounted on the bottom layer. While employing 4-layer PCBs to improve EMC is ideal, many touch-sensing applications are cost-constrained into 2-layer PCBs. For this reason, the reference designs PCBs are all two layer PCB designs.

4.2.4 Component Selection

The mutual- and self-capacitance modules use the same IC components. These components are introduced in the following subsections.

4.2.4.1 MSP430FR2633 Touch-Sensing Microcontroller

The MSP430FR2633 touch-sensing microcontroller (MCU) with CapTIvate technology was selected to be the touch-sensing device for both sensing modules. This MCU provides optimal flexibility in application configuration, is programmable, and has high-quality development tools. The CapTIvate technology on-chip has features targeted towards noise immunity. The 32-pin QFN package was selected for its 16 capacitive-sensing I/O pins and 15.5 KB of useable FRAM memory.

4.2.4.2 TCA9535 I^2C I/O Expander

Both the CSM-MUTUAL and CSM-SELF modules have more LEDs than the MSP430FR2633 has digital I/Os. An additional I/O expander device is required to control the onboard LEDs. The TCA9535 is a simple, easy-to-use digital I/O expander, controlled by the MSP430FR2633 through an I^2C interface.

The TCA9535 can source and sink more current per I/O when compared with the MSP device (10 and 25 mA, respectively). The TCA9535 is used in this design to actively drive the LED anode high (to VCC) and low (to circuit return). This is preferable to an open-drain or open-collector configuration, in which the anode or cathode of the LED floats when off. The floating of the anode or cathode may cause a capacitance shift that appears as noise on a capacitive sensing electrode.

Also, the TCA9535 can source current to each LED and the return current can go into the ground plane eliminating the requirement to source and return tracks. This benefit simplifies fitting the design into two layers. In addition, the IC has a low typical-quiescent current of 30 µA. Two expanders are used in each capacitive-sensing module.

4.2.4.3 Dialight Reverse-Mount LEDs

Backfiring, reverse-mount LEDs from Dialight were used for the state and status indicators. These LEDs are efficient (requiring only 2 mA of current for reasonable intensity). 620-Ω resistors set the LED current. With a typical forward voltage of 2.2 V, the LED current is approximately 1.8 mA per LED. The worst-case current with a forward voltage of 2.0 V is 2.1 mA per LED. The worst-case total LED current is 75.6 mA on the CSM-MUTUAL module, which has 36 LEDs. 25 mA is left in the power budget for the ICs.

4.2.4.4 Board-to-Board Connectors

Two 4-pin, 0.1-in. pitch surface mount headers are used for board-to-board interfacing. Surface-mount connectors are required so that the top layer of the PCB is free from components, letting it be flush mounted to the overlay material without air gaps.

4.2.5 Form Factor

The CSM-MUTUAL and CSM-SELF PCBs are designed to fit into the polycarbonate enclosure so that they can be mated to the top half of the enclosure directly. The CSM-MUTUAL measures 5.5 in. × 4 in., and the CSM-SELF measures 6.4 in. × 4 in. For more information, see Figure 17.
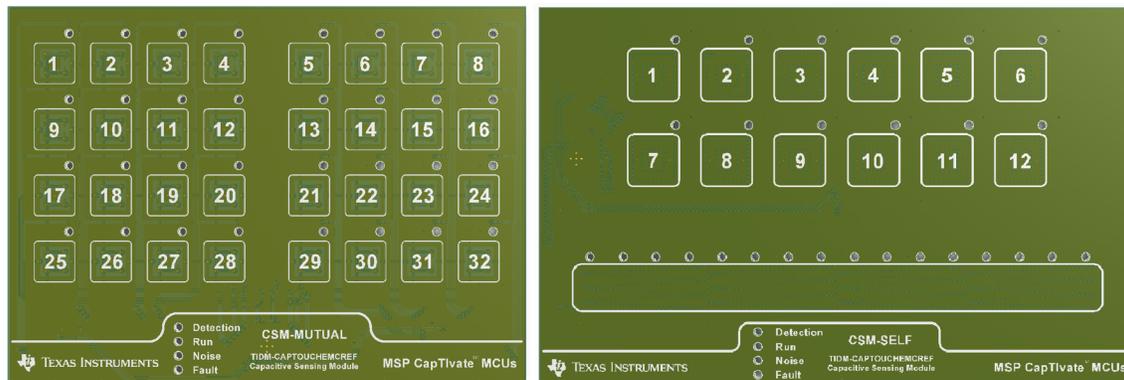

Figure 17. CSM-MUTUAL and CSM-SELF PCBs (Top View)

4.2.5.1 Air Gaps

Air gaps between the sensing electrodes and the overlay material reduce sensitivity and noise immunity, and introduce the potential for moisture to enter between the electrodes and the overlay, affecting sensitivity. Designs that require noise immunity must eliminate air gaps in the stackup. Mutual capacitance is particularly sensitive to air gaps, because the overlay helps form the starting E-field between the Rx and Tx with which the user destructively interferes.

4.2.5.2 Overlay Thickness

The TIDM-CAPTOUCHEMCREF enclosure is 2.5 mm thick, which is a common thickness in industry. Many white goods and appliance applications have overlays of 2 to 4 mm. Thicker overlays improve ESD performance at the expense of sensitivity.

4.2.6 Electrode Design

Designing electrodes for noise immunity involves balancing trade-offs. The primary trade-off is the balance between sensitivity and noise immunity. Section 3 introduced the current paths in a capacitive-sensing circuit. Proper electrode design for noise immunity is an expansion of that analysis to include the behavior of E-fields. To improve the sensitivity of a sensing electrode, the touch capacitance must be increased while minimizing the parasitic self capacitance to circuit return and earth ground. To achieve this improvement, electrodes must be enlarged and the size and spacing of nearby planes (usually power and return planes) must be limited. Implementing these changes to improve sensitivity has a direct negative impact on the noise immunity of the electrode.

As Figure 11 shows, the coupling path for noise from the perspective of the electrode is the free-space coupling to earth ground and any touch capacitance. Limiting the noise current injected into the receive electrodes in both the self- and mutual-capacitance sensing topologies reduces the effects of noise. If the noise current is conducted into the product through the power-supply cables, the power supply can help limit this current. If the noise is radiated into the product, the power supply can have little effect on the noise current. Electrode design does have a significant impact on both conducted- and radiated-noise immunity and fast transient and ESD immunity. Limiting the free-space coupling capacitance between the sensing electrode and earth ground and limiting any touch capacitance can also limit the injected noise current. The art of capacitive touch is careful balance between achieving the required sensitivity and the required noise immunity.

4.2.6.1 Self-Capacitance Electrode Design

Self-capacitance electrode design for noise immunity is straightforward because there are relatively few variables available for the designer to control. The goal is to reduce the fringing E-field out of the electrode as much as possible while obtaining the required sensitivity to accurately detect touches. The variables available include the following:
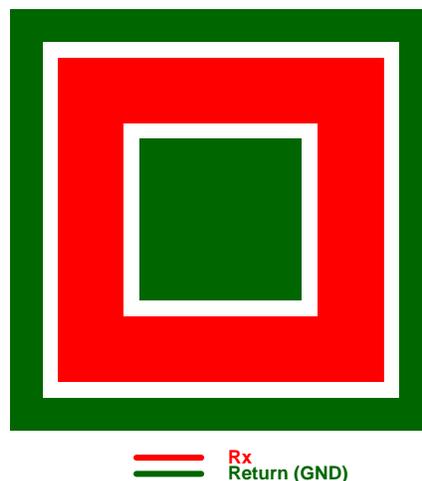
- Overall geometry size
- Overall shape
- Clearance to power planes

Self-capacitance button sensors are typically designed as either circular- or square-solid electrodes, sized in the range of 8 mm to 15 mm. Reducing the size of the electrode to less than that of a finger reduces the sensitivity. Increasing the size of the electrode to greater than that of a finger does not greatly increase the sensitivity but increases the susceptibility to noise. The increase in susceptibility to noise results from the increased free-space coupling associated with the increase in electrode surface area. With regard to sensitivity and noise immunity, there is no significant difference between circular and square electrodes. If crosstalk between buttons is an issue, circular electrodes might provide better isolation between buttons. Preventing crosstalk can be important in designs that have a thick overlay stack and densely-packed buttons.

Limiting the E-field projection of the electrode reduces the free-space coupling to earth ground. Reducing free-space coupling to earth ground limits the ability of conducted or radiated noise to affect the electrode, especially when no users are interacting with it. This practice stabilizes the electrode from false detect scenarios. Limiting the E-field projection can be achieved through the following two methods:

- Reducing the overall size of the electrode
- Reducing the clearance to nearby power planes

The CSM-SELF electrode geometry applies these methods by tightly closing the return-plane clearance to the outside the electrode and by introducing a return plane inside the electrode, turning the electrode geometry into a ring that is surrounded by circuit return. With many touch-sensing solutions, this much parasitic loading and E-field reduction makes touch detection difficult. The parasitic-offset subtraction capability of the MSP430FR2633 CapTIvate™ MCU allows enough sensitivity to be regained, enabling aggressive circuit return ground structures inside and around the electrode, improving noise immunity. Figure 18 shows the Rx geometry used for the CSM-SELF panel


Rx
Return (GND)

Figure 18. Self-Capacitance Electrode Geometry (Top View)

Table 4 defines the electrode parameters for the CSM-SELF module.

Table 4. Self-Capacitance Electrode Geometry

Geometry	Style	Size (mm)	Size (mil)
Overall geometry	Square ring	11 × 11	430
Plane keepout	Flood on bottom layer, space × distance from overall geometry on top layer	0.5	20
Rx thickness	Top layer	2.5	100
Rx to return fill spacing	Void area	0.5	20
Inner return (ground) fill	Top layer	5 × 5	200 × 200

The CSM-SELF module also contains a slider sensor made up of four electrodes. Slider sensors pose additional challenges because they typically have more surface area than buttons. Slider sensors must always be connected to the MSP430FR2633 MCU so all elements can be scanned in parallel. Parallel scanning all the electrodes in a slider allows for common-mode rejection of noise and other disturbances between the elements of the slider. If a transient event occurs during the measurement of a slider, it affects all elements proportionally because they were scanned at the same time. The MSP430FR2633 supports up to four parallel scans. For this reason, four electrodes are used in the 6-in. slider sensor of the CSM-SELF panel. The electrode layout for the slider is shown in Figure 19.
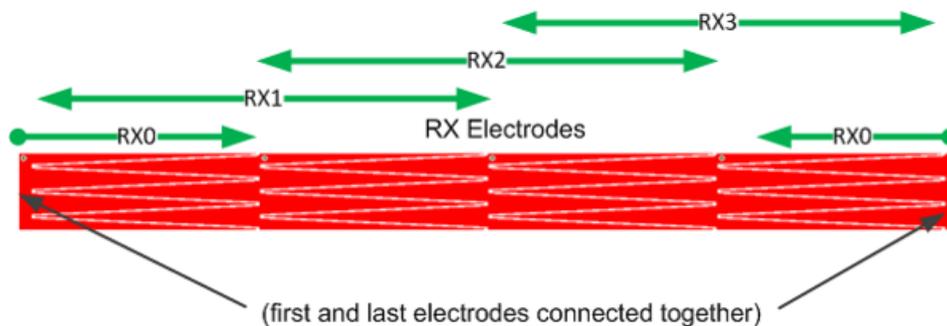
Figure 19. Self-Capacitance Slider Implementation

Electrode RX0 of the slider is broken in half and connected to either end of the slider. This slider behaves as a wheel that is disconnected at one point and allows for linear-position tracking using the CapTIvate software library. The electrodes are designed to have a linear change in surface area from one electrode to the next as a user moves the touch point across the slider.
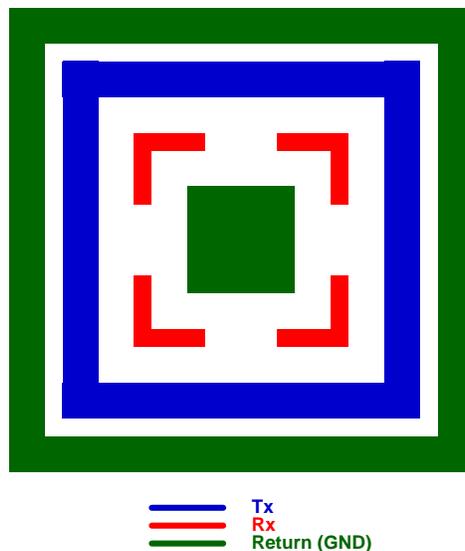
4.2.6.2   Mutual-Capacitance Electrode Design

Mutual capacitance differs from self capacitance in that the desginer can control the electric field of interest (that between the transmitter and the receiver). The quantity of interest in the measurement is the change in the field between the Tx and the Rx. Improving the sensitivity involves constructing the Tx and Rx to maximize the E-field between the two in the desired area of interaction (above the overlay material) and minimizing the E-field between them everywhere else on the PCB (to limit the parasitic-mutual capacitance). Another fact is that in mutual-capacitance sensing, the user disturbs an existing E-field (reducing the mutual coupling). For the reduction in mutual capacitance to occur when the electrode is touched, some base mutual coupling must exist. The goal is to create a large E-field, but only in an area where the user can easily interact with it. This additional control helps create a noise-immune design and introduces additional complexity when compared to the self-capacitance electrode.

Unlike in the self-capacitance electrode design, there are many variables available for the electrode designer to adjust. These variables follow:

- Overall geometry size
- Overall Tx-Rx geometry (shape)
- Tx thickness
- Rx thickness
- Tx–Rx spacing

Experimentation and E-field analysis shows that large E-field lines tend to concentrate near right angles in the electrode geometry in mutual-capacitance sensors. Designing square or rectangular electrodes tends to improve sensitivity (most of the sensitivity occurs at the corners of the nested-electrode components). By reducing the Rx area that is parallel to the Tx, the sensitivity of a rectangular or square geometry can be further improved. Figure 20 shows geometry that demonstrates this concept. The Rx square is only in the four corners (where mutual E-field concentration is the highest), limiting some of the parasitic-mutual capacitance between the Rx and Tx that only propagates between the two inside the PCB substrate and overlay.


```
━━━   Tx
━━━   Rx
━━━   Return (GND)
```

Figure 20. Mutual-Capacitance Electrode Geometry (Top View)

Figure 21 is a cross section of the electrode geometry shown in Figure 20. The image shown in Figure 20 also illustrates the PCB substrate, overlay material, and approximate E-field lines. Considering Figure 21, the user may visualize another important factor that affects mutual-capacitance sensitivity: the spacing between the Rx and Tx in the electrode design. If the Rx is further from the Tx, the E-field between the two projects higher through the overlay. The implication is that designs with large overlay thicknesses (greater than 2.5 mm) must have greater spacing between the Rx and Tx to ensure enough E-field penetration above the overlay. Designs with small overlays (less than 1 mm) can have light Rx to Tx spacing.
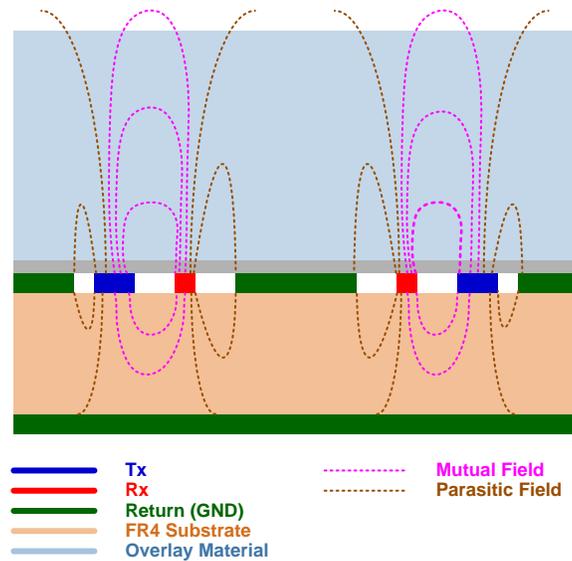
Figure 21. Mutual-Capacitance Electrode Geometry (Cross Section with Approximate E-Field Lines Shown)

In addition to Rx-Tx spacing, Rx must be sized appropriately for the best noise immunity. Because noise currents flowing into the Rx can corrupt measurement results, minimize the size of the Rx as much as possible while achieving the required sensitivity. Because noise coupling into the Rx is primarily a function of Rx surface area and parasitic loading, reduce the available surface area to which noise can couple to improve immunity.

To aid in noise immunity, a circuit return plane is placed inside the Rx ring in the electrode. When a user touches a button, the circuit return plane provides a low-impedance path for noise current rather than the Rx electrode and limits the fringing E-field out of the Rx into the overlay. Fringe-field lines inside of the Rx ring do not significantly contribute to overall sensitivity but they do contribute to the ability of noise to couple into the Rx. By placing the return plane inside of the Rx ring, the E-field out of the Rx is limited and the noise immunity is improved.

The Rx ring is placed inside of the Tx ring. The Tx provides some shielding in a mutual-capacitance design, contributing to a self-shielding electrode. This configuration works well for designs where power-plane shielding is not feasible. An example is a space-constrained form factor, where power planes cannot be used for shielding because the electrodes are at the edge of the PCB. The Rx must be contained in the Tx because it limits stray fringing E-field lines out of the Rx to earth ground through free-space coupling. Table 5 defines the mutual-capacitance geometry of the CSM-MUTUAL panel.

Table 5. Mutual-Capacitance Electrode Geometry

Geometry	Style	Size (mm)	Size (mil)
Overall geometry	Square-in-square	10 × 10	400
Plane keepout	Flood on bottom layer, space x distance from overall geometry on top layer	0.5	20
Tx thickness	Top layer	1	40
Rx thickness	Top layer	0.5	20
Inner return (ground) fill	Top layer	3 × 3	120
Tx to Rx spacing	Void area	1	40
Rx wing length	Not a critical dimension, but using 4 Rx *wings* instead of one continuous Rx ring slightly improves sensitivity, at the expense of additional vias and tracks	2	80

4.2.7   Electrode Connections

For both self- and mutual-capacitance designs, connections between the electrodes and the touch sensing MCU must follow the following guidelines:

- Critical traces must be as short as possible, including all self-capacitance Rx traces and all mutual-capacitance Rx traces. Limiting trace length limits the ability of the electrodes to act as antennas to radiated noise and the overall surface area of the electrodes, which improves immunity to conducted disturbances such as conducted RF noise and EFT. Designs with large boards and spread electrode patterns must place the MCU at the center of the design.

- Traces widths must be small. The ideal size is in the range of 200 µm to 250 µm or 6 to 10 mil. This size reduces the overall surface area of the trace and improves immunity to conducted RF noise and EFT. Thinner traces also present high impedance to transient currents such as those resulting from an ESD event. The exception to this rule is designs with highly-resistive traces, such as indium-tin-oxide (ITO).

- Mutual-capacitance designs must make the total Tx's per Rx as small as possible. The CSM-MUTUAL panel has 32 buttons, which can be achieved through the use of a 4 Rx × 8 Tx matrix, or even a 8 Rx × 4 Tx matrix. Because the MSP430FR2633 MCU was used for the design, there are 16 sensing I/O pins available. The 32 buttons are realized through two separate 4 Rx × 4 Tx matrices. This requirement limited the total Tx's per Rx to 4. This configuration provides better immunity to conducted noise than a 4 Rx × 8 Tx configuration because the overall Rx surface area is reduced by a factor of 2 and the Rx trace lengths are also significantly reduced. A user can touch the same Rx in multiple places. If a user touches an Rx in multiple places, an increased level of noise is coupled into the Rx, which reduces the immunity of the solution.

- The spacing between traces and nearby power planes must be closed and tight. This spacing increases parasitic loading, but provides significant noise-immunity benefits by limiting fringing E-field lines from electrode-connection traces.

- Mutual-capacitance designs must have as much space as possible between Rx traces and Tx traces to reduce parasitic mutual capacitance. If an Rx trace runs parallel to a Tx trace for any significant length, a *hot spot* forms on the PCB in that area. A false-touch detection can occur in this area, reducing the sensitivity of that Tx/Rx combination in the desired area of interaction.

- Avoid routing sensing lines through connectors. The touch-sensing MCU must be located on the same circuit board as the electrodes themselves. Cable harnesses with large connecters are the most troublesome due to the relatively large free-space couplings to earth ground that result from the connectors themselves and any unshielded cabling. Flex tails are more forgiving as the connectors are smaller and the flex cable can be designed with similar techniques to those mentioned previously, such as small trace widths.

- Route all critical electrodes (Rx's) on the bottom layer of the PCB if possible. This routing prevents traces from becoming touch sensitive and limits the ability of noise to couple to traces from the top side.

4.2.8   Series and Shunt Components

Series and shunt filter elements must be used on Rx and Tx I/Os to improve electromagnetic compatibility.

4.2.8.1   Self-Capacitance Mode

In self-capacitance mode, TI recommends a series resistor between the electrode and the MCU I/O pin. This impedance works with the electrode and I/O capacitance to form a low-pass filter, limiting the effect of high-frequency noise on the electrode. A 470-Ω series resistance with just a typical 5-pF I/O capacitance has a 3-dB cutoff frequency of 67.7 MHz. This pole is high enough to allow undisturbed charge transfers between the sensing MCU and the electrode but it helps roll off high-frequency disturbances greater than the cutoff frequency. Figure 22 shows a typical implementation.
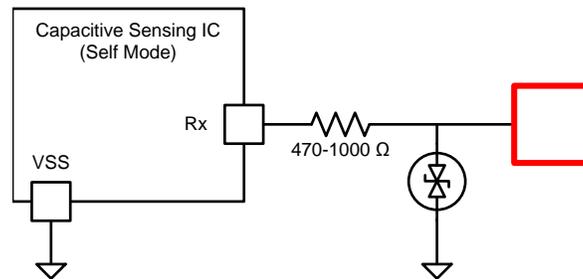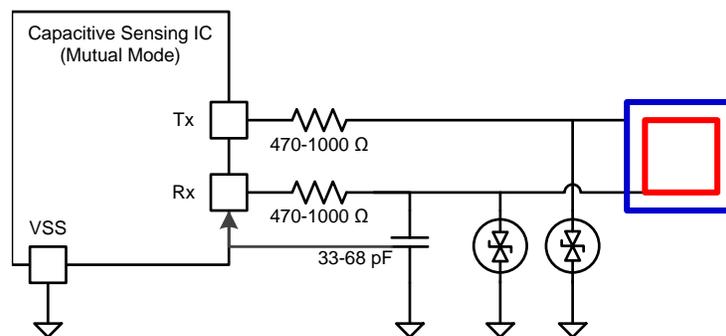
Figure 22. Self-Capacitance Series and Shunt Components

The series resistor must be placed as close to the sensing MCU pin as possible to provide the most benefit. TI recommends small surface-mount resistors. In addition to the series resistance, populating a transient voltage suppression (TVS) device in a shunt configuration on the sensing line improves the robustness of the system to ESD events that occur at the electrode. The TVS device works with the series resistance and the internal ESD protection clamps of the sensing MCU to protect the sensitive integrated-analog circuitry onboard the MCU from a high-voltage transient.

As discussed in Section 4.4, the primary defense against ESD is the overlay material. The CSM-SELF and CSM-MUTUAL modules did not require TVS devices to pass system level ESD testing, because the overlay material provided the necessary protection. TVS diodes are usually required in designs with either thin overlays or overlays with low-electrical breakdown voltages.

4.2.8.2 Mutual-Capacitance Mode

In mutual-capacitance mode, all of the principles discussed previously for self-capacitance directly apply. In addition to those principles, a shunt capacitance is required on the Rx sensing line and must be placed as close to the MCU as possible and on the electrode side of the series resistance. For more information, see Figure 23.

Figure 23. Mutual-Capacitance Series and Shunt Components

This shunt capacitance provides a path for noise currents and stabilizes the sensitive receive electrode to circuit return. The shunt capacitance effectively reduces the susceptibility band around the conversion frequency and its harmonics in mutual mode. TI recommends a value of 33 to 68 pF for best performance. The CSM-MUTUAL panel uses 68-pF ceramic surface mount capacitors. An exact value is not critical; ±20% tolerances are usually acceptable. The capacitor must be placed as close to the MCU as possible. Figure 24 shows the CSM-MUTUAL layout. The shunt capacitance is directly connected to the solid ground plane (outer ring), and the series resistance is right before the MCU I/O pin. The CSM-MUTUAL design includes a provision for shunt capacitance on the Tx I/O pins as well, if required during testing.
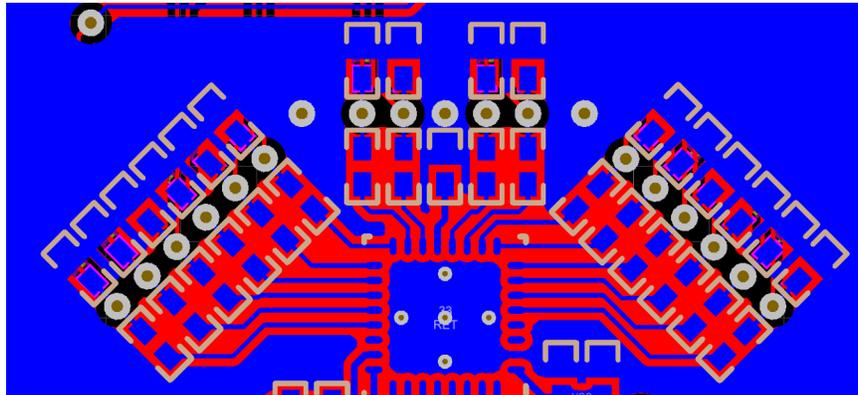
Figure 24. CSM-MUTUAL Series Resistance and Shunt-Capacitance Layout

4.2.9   Power Planes

As introduced in Section 4.2.6, power planes drastically improves immunity to radiated and conducted RF, fast transients, and ESD. While capacitive-sensing design recommendations often promote limited and/or hatched power-plane structures near the capacitive-sensing area of a PCB, designs that require high noise immunity must trade off some sensitivity for the immunity benefits of dense power planes.

4.2.9.1   Self Capacitance

Self-capacitance designs must have solid power planes (usually a circuit-return plane) on the top layer of the PCB, surrounding the sensing electrodes. The bottom layer must also have a dense circuit return plane but this plane must be a dense hatch, rather than a solid plane. A solid plane underneath a sensing electrode limits sensitivity to an extent greater than the noise immunity benefits it provides. A compromise is to put a dense hatch underneath the electrode. The CSM-SELF panel has a hatched-return plane across the entire bottom layer. The hatch consists of 8-mil traces spaced at 32-mil intervals. Use a 45 degree hatch pattern if traces are routed horizontally and vertically, as this ensures more even parasitic capacitance between traces and the ground hatch in designs that have traces on a layer opposite of the hatch.

4.2.9.2   Mutual Capacitance

Mutual capacitance designs must have solid power planes on the top and the bottom layer of the PCB. Mutual-capacitance sensors are more tolerant of parasitic capacitance to ground than self-capacitance sensors and using solid planes provides better shielding of sensing lines and sensing electrodes. The CSM-MUTUAL panel uses solid-circuit return planes on the top and bottom layers of the PCB.

4.2.10   Other Circuit Components

In addition to the capacitive-sensing components, there are several important design considerations for the CSMs.

4.2.10.1 *MCU DVCC Decoupling*

The MCU DVCC supply rail must be properly decoupled from the 3.3-V supply. The CSM-SELF and CSM-MUTUAL both employ the combination of a 4.7-µF bulk capacitor and a 100-nF decoupling capacitor on the DVCC pin. Figure 25 shows the layout for the CSM-MUTUAL panel.
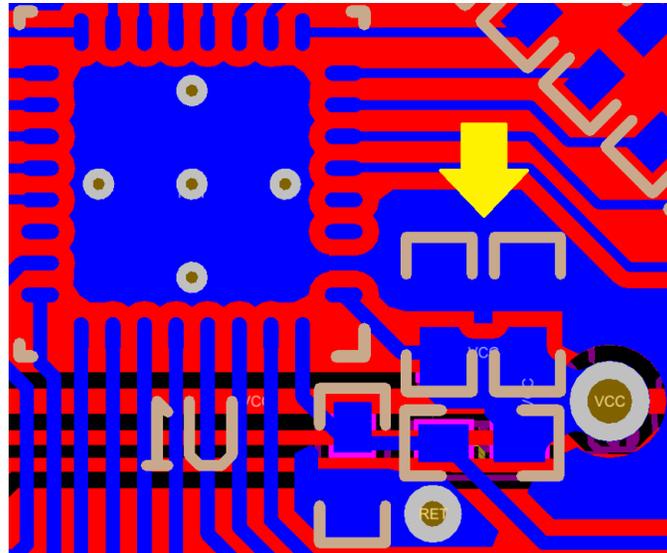

Figure 25. CSM-MUTUAL DVCC Decoupling and Bulk Capacitance

The two capacitors must be placed as close as possible to the DVCC rail to minimize EMI. The closeness of the capacitors correlates to the shortness the current loop is formed between the DVCC and DVSS pins and the capacitor terminals. Avoid vias between the DVCC and DVSS pins and the decoupling capacitance. The 100-nF capacitor must be placed closest to the MCU, followed by the 4.7-µF capacitor. While the CSM-SELF and CSM-MUTUAL capacitors to not have vias, having some bulk decoupling at the power entry point to the board to suppress high-frequency $\frac{dI}{dt}$ across the cable harness sourcing power to the CSM is also ideal. The DVCC and DVSS rails are typically sensitive pins for digital ICs. Fast transient and ESD events that present to these pins can cause undesired brownout reset conditions, which is unacceptable in many applications. Proper decoupling of the DVCC rail helps stabilize the DVCC and DVSS voltage. In this design, the power supply module (PSM) also handles transient voltage protection for the power supply. If the CSM-SELF or CSM-MUTUAL panels were tested for transient immunity on the supply rail, TI recommends a ferrite on the DVCC rail before the decoupling capacitance. This ferrite attenuates high-frequency transients while passing DC current. Transient voltage suppression devices can also be used on the DVCC rail with a ferrite to clamp transient voltages.

4.2.10.2 *MCU Reset and Spy-Bi-Wire I/O*

The MCU reset and Spy-Bi-Wire IO (SBWTDIO) pin on the MSP430FR2633 is another sensitive bidirectional pin. This pin is weakly pulled up to DVCC by a 47-kΩ resistor per standard MSP recommendations for Spy-Bi-Wire programming. This weak pullup makes the line prone to glitches during fast transient and ESD events. To counteract the weak pullup, a 510-pF capacitor is placed between the pin and circuit return. Spy-Bi-Wire communication can tolerate up to about 2.2 nF of total capacitance on the RST and SWBTDIO pin. Using a 510-pF resistor allows headroom for parasitic capacitance and cable capacitance. Longer SBW programming harnesses have a higher capacitance, and can cause programming errors if the RST and SBWTDIO capacitance is too high.

4.2.10.3   I²C Bus SDA and SCL

Because of their open-drain nature, I²C bus nets are prone to digital glitches. Fast transient and ESD events can cause digital glitches on these pins, because the net is floating on the bus side of the pullup when the line is not pulled low by a device. Further complicating I²C communication is the ease with which I²C state machines may be locked up due to glitches on the bus. TI recommends using relatively strong pullup resistors to reduce the possibility of I²C bus glitches. The CSM-SELF and CSM-MUTUAL panels use 2.2-kΩ pullup resistors. Decreasing the resistance increases the power consumption of the interface. Check the current-sink capability of all devices on the bus when selecting pullup resistors for an application.

4.3   Power-Supply Modules

This section discusses the two power supply modules. The TIDM-CAPTOUCHEMCREF was designed to analyze the noise performance of capacitive-sensing user interfaces in various power-supply scenarios. Products in the market with capacitive touch have a variety of power sources, including AC-mains power, power-over-Ethernet (PoE), 4- to 20-mA loop power, and 24-VAC power. For each of those sources, there is a variety of different power-supply topologies that can be used to derive the operating-supply rails in a product. Each source and topology has its own unique noise characteristics. Some supplies filter line noise better than others, and some supplies generate more noise from their own operation than others. These differences lead to a lot of unpredictable variables that can be encountered in the field. Testing an AC and a DC configuration provides multiple data points for testing. Noise in a product can come from other components inside a product other than the input supply line or the power supply, such as a switching relay or a switching-inductive load such as a motor. For this reason, provide a DC supply for testing to simulate the effects of common-mode noise and transient voltages present after the AC supply inside of a product. Home appliances and white goods commonly have these operating conditions. TI decided to include a universal AC to 3.3-VDC power-supply module and a 12- to 3.3-VDC power-supply module.

The PSM-12VDCTO3.3VDC is a single-stage power supply of a 12- to 3.3-VDC linear regulator stage. The PSM-UACTO3.3VDC is a two-stage power supply consisting of a universal (90 to 265 VAC) to 12-VDC flyback-switcher stage and a 12- to 3.3-VDC linear-regulator stage. The 12- to 3.3-VDC second-stage circuit is identical to that used in the PSM-12VDCTO3.3VDC.

4.3.1   Requirements

The PSM hardware was designed with the following requirements:
- Provide an AC mains to DC 3.3-V power supply, to simulate being attached to a noisy mains power supply
- Provide a DC 12-V to DC 3.3-V power supply, to simulate being attached to a noisy 12-V rail inside a product
- Provide an isolated CMOS communication interface to stream data to and from the CSM
- Provide up to 330 mW (100 mA at 3.3 V) of output power to the downstream CSM

4.3.2 Form Factor

The PCBs used for both PSMs were shaped to integrate with the polycarbonate enclosure used in the design. Figure 26 shows the top view of the PSM form factor. The top half of the PCB is used for the UAC to DC 12-V stage. On the bottom half of the PCB, the bottom right corner contains the DC 12-V to DC 3.3-V stage while the bottom left corner contains the isolated I/O domain.
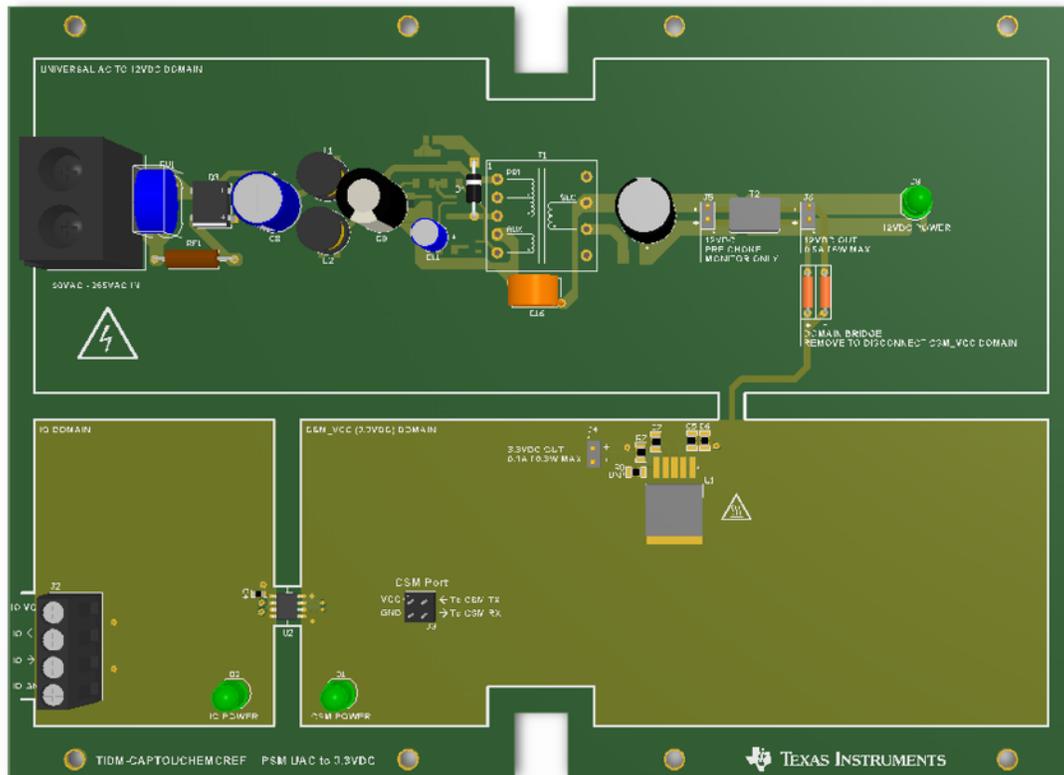

Figure 26. PSM UAC to 3.3-V DC PCB Top View

In the case of the DC 12-V supply, the universal AC to DC 12-V stage is empty with the exception of input filtering components. Both modules have the I/O connections and board-to-board headers in the same places. Because the two PSMs share common circuits (the DC 12-V to DC 3.3-V stage and isolated I/O domain are identical), the following sections break down each stage, rather than each PSM specifically.

4.3.3 Universal AC to 12-V DC Stage

Because of their smallness and efficiency, there has been a proliferation in the use of low-cost, flyback-switching power supplies in the market, particularly for mobile device chargers. Because of this trend and the limited power requirements of the reference design, a flyback converter topology was selected for the universal AC to DC 12-V stage. This stage is based upon the UCC28910 flyback switcher, which integrates a 700-V switching FET with control logic designed to operate in a primary-side-regulated configuration, where the output voltage is monitored through an auxiliary winding in the flyback transformer. The flyback transformer is a custom design for this application, and construction was provided by Wurth Electronics®. Discontinuous-conduction mode (DCM) with valley switching is used to minimize switching losses. The UCC28910 contains many integrated protection features that allow for a cost-effective, power-converter solution.

4.3.3.1   Power-Entry Terminal

Figure 27 shows the schematic for the power-entry terminal.
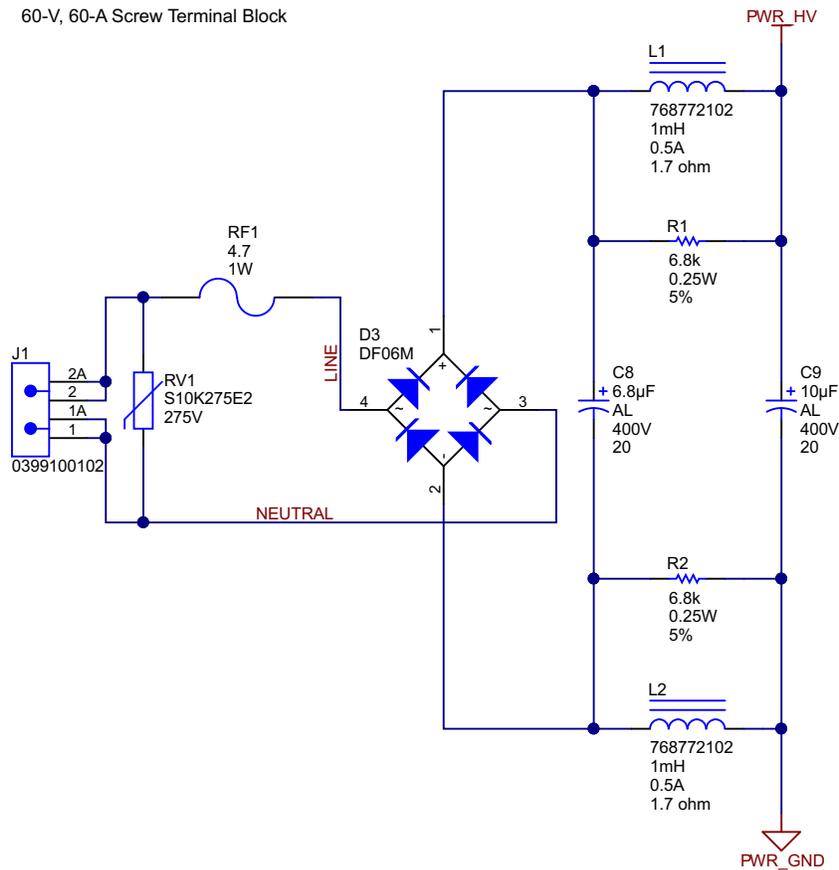
Figure 27. UAC Power-Entry Terminal Schematic

Power entry is provided by a screw terminal off-board connector rated for 600 V. RF1 is a wire-wound fusible resistor that protects the system in the event of an overcurrent. RF1 is rated for 1 W. The fusing characteristics provide fusing within 60 seconds when the power through the resistor is 25 times that of the rated power. In this case, 25 times the rated 1-W power is 25 W. A short between line and neutral causes this rating to be exceeded based on the 4.7-Ω resistance. When fused, the residual resistance is at least 100 times the rated resistance of 4.7 Ω. RV1 is a metal-oxide varistor that provides input-overvoltage protection and is rated for up to 275 VAC during operation. In the event of a transient voltage, RV1 transitions from high impedance to low impedance, clamping the voltage seen at RF1 and at the bridge rectifier D3. D3 is an integrated-diode bridge rectifier that produces the PWR_HV input-power rail, which is filtered by the input EMI filter and is rated for up to 1 A.

Capacitors C8 and C9 and differential mode inductors L1 and L2 are the input EMI filter. R1 and R2 dampen input-filter oscillations and prevent buildup of high voltages across L1 and L2. C8 and C9 must be high-voltage capacitors. The highest-peak voltage across C8 and C9 in normal operation is two diode drops less than 187 V, based on a 265 V_{rms} (374 V_p) input that has been bridge rectified. 400-V aluminum electrolytic capacitors are used in this design. For more information, see Figure 28.
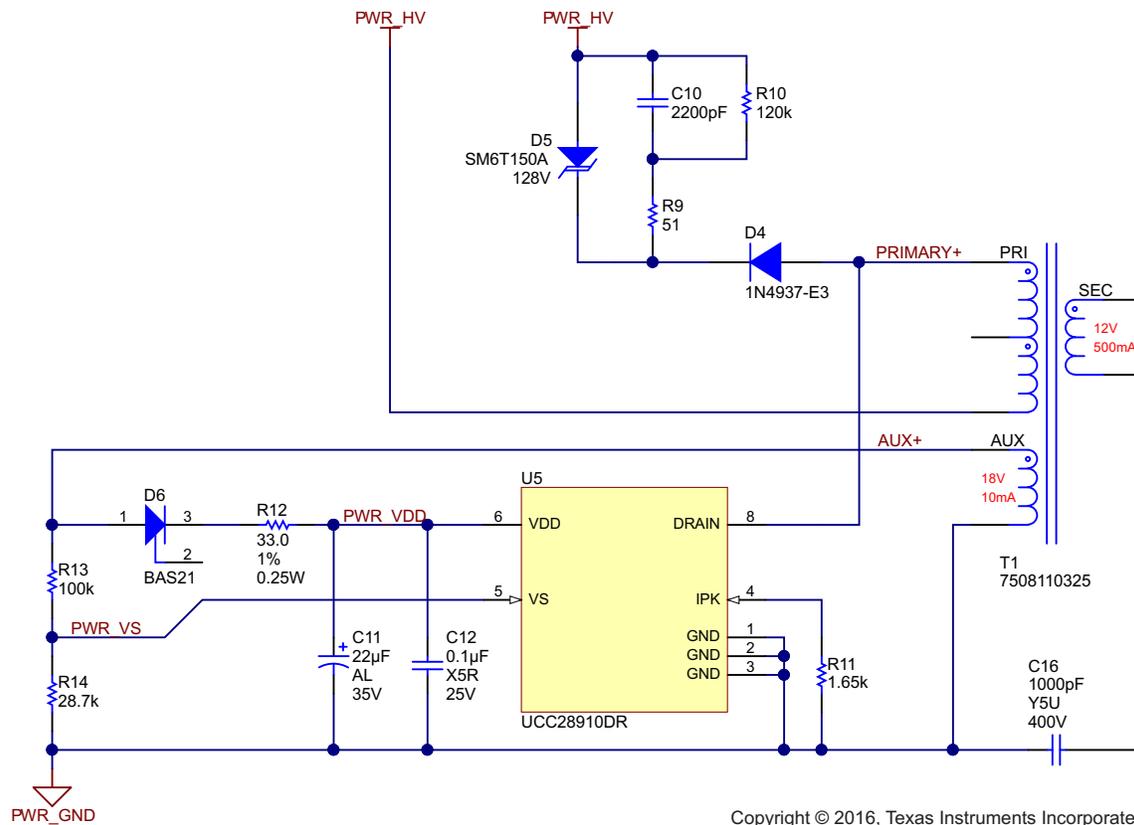
Figure 28. UAC High-Side Schematic

Resistors R9 and R10, capacitor C10, and diodes D5 and D4 are the high-side voltage clamp. This clamp prevents the switching FET drain voltage (pin 8 of U5) from exceeding the maximum rating of 700 V, when the FET breaks down and can destroy itself. The voltage rise on this node occurs at the FET turn-off point. In addition to clamping the voltage, the circuit provides a clean input to the VS node by damping any oscillation that is present on the drain voltage as a result of the transformer-leakage inductance on the primary winding.

Diode D6 is a rectification diode that provides the VDD supply for the switcher off the auxiliary winding in the flyback transformer. D6 works in conjunction with R12, C11, and C12 to stabilize VDD. C11 is the bulk capacitor (aluminum electrolytic), and C12 acts as a decoupling capacitor (low-ESR ceramic).

Resistors R13 and R14 form the resistor divider for the voltage sense (VS) terminal of the switcher. R13 is R_{S1} in terms of the UCC28910 design model, and R14 is R_{S2}. R_{S1} is selected first and it sets the enable and start-up voltage for the switcher. R_{S2} sets the desired output voltage and is calculated based on RS1 and the transformer turns ratios. For more information, see Equation 1.

$$R_{S1} = \frac{v_{RMS\_EN} \times \sqrt{2}}{N_{PA} \times I_{VSLRUN}}$$

$$R_{S2} = \frac{V_{VSR} \times R_{S1} \times N_{PA}}{\left(V_{OUT} + V_F\right) \times N_{PS} - \left(V_{VSR} \times N_{PA}\right)}$$

(1)

Table 6 shows the calculations for R_{S1} and R_{S2}.

Table 6. UAC RS1 and RS2 Calculations (VS Resistance Divider)

Parameter	Value	Conditions
V_{OUT}	12.00 V	Target
N_{PS}	7.82 :1	P:S
N_{PA}	5.38 :1	P:A
V_{RMS_EN}	80 V	
I_{VSLRUN}	0.000210 A	Typical
V_{VSR}	4.05 V	Typical
V_F	0.4 V	At Low Current
R_{S1}	100.1 kΩ	
R_{S2}	29.0 kΩ	

R11 sets the maximum-drain current peak. C16 is a provision for a high-voltage capacitor between the high-voltage return and the output, low-voltage return. Populating this capacitor improves the conducted-emissions performance of the power supply. For more information, see Figure 29.

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Figure 29. UAC Low-Side Schematic

The low side of the UAC to DC 12-V stage is primarily made up of power-rectifier diode D7 and bulk capacitor C13. The bulk output-capacitance size determines the transient-load regulation performance of the converter, as well as the ripple voltage. Equation 2 shows the maximum-voltage drop on the output when switching from no load to 500 mA of load can be calculated based on the output capacitance and minimum-switching frequency.

$$V_{DROP} = \frac{I_{TRANSIENT}}{C_{OUTPUT} \times F_{SW}}$$

<div align="right">(2)</div>

Assuming a minimum-switching frequency of 360 Hz and worst-case load transient of 500 mA, a voltage drop of 0.93 V occurs on the output (approximately 7%) as shown in Table 7. This performance is tolerable for the application because the 12-V rail is conditioned further by the 12-V to 3.3-V linear-regulator stage, and because large load transients are not occurring during operation of the reference design.

Table 7. UAC Output Bulk Capacitance and Transient Load Worst-Case Response

Parameter	Value	Conditions
$I_{TRANSIENT}$	0.50 A	Worst case
F_{SW}	360 Hz	Minimum
C_{OUTPUT}	0.0015 F	Bulk only
V_{DROP}	0.93 V	Worst case

Resistors R15, R18, and power-good diode D8 establish the minimum-output current of the converter stage. The R18/D8 diode circuit draws 9.9 mA at 12 V, and R15 draws less than 1 mA. The common-mode choke provision consists of R16, R17, and T2. If no common-mode choke is used on the output, R16 and R17 must be populated with zero-Ω resistors. If a common-mode choke is populated, R16 and R17 must be DNP. The common-mode choke coil T2 is placed after the SMPS so it can block common-mode current generated by the SMPS. A common-mode choke coil is placed before the SMPS as a part of the power entry and EMI circuit.

4.3.3.2 *Layout Considerations*

The UCC28910 switcher layout is as small as possible and on a single layer where possible. R13 and R14 must be as close to the switching IC (U5) as possible (these set the output voltage and turn-on voltage). R11 must also be as close to the switcher as possible. R11 sets the peak-current limit for the drain of the U5. Increasing the copper area connected to the ground pins improves heat extraction from the U5. For more information, see Figure 30.
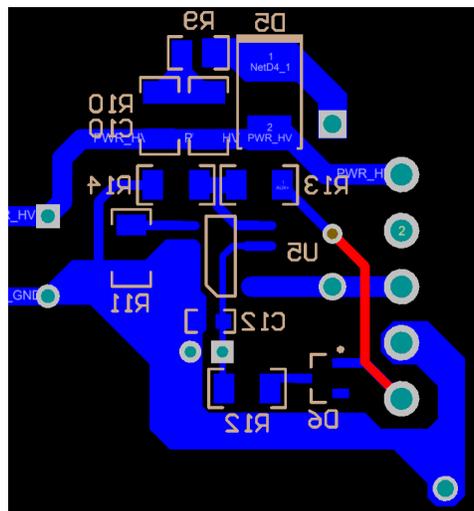
Figure 30. UCC28910 Layout

Minimizing the length and overall size of the drain trace improves radiated emissions.

4.3.4 12-VDC to 3.3-VDC Stage

[Figure 31](#) shows the 12-VDC to 3.3-VDC stage is based on the TPS7A4533 linear LDO regulator.
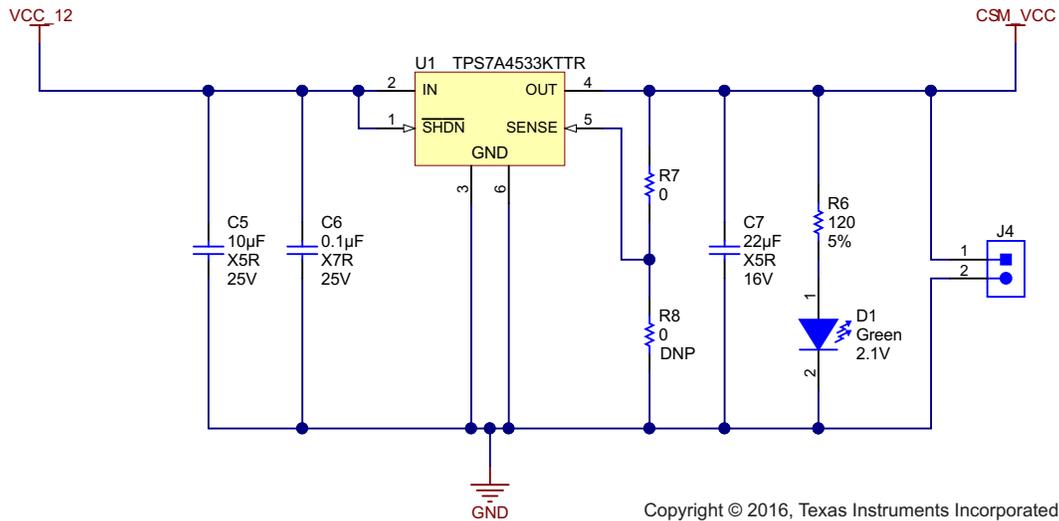

Figure 31. 12-VDC to 3.3-VDC Linear Regulator Schematic

4.3.4.1 Linear-Regulator Schematic

Capacitor C5 provides bulk input capacitance, and capacitor C6 provides decoupling for the linear regulator U1. C7 provides the output capacitance. The TPS7A4533 is a unique regulator in that it is stable with just 10 µF of output capacitance, and there are no significant ESR requirements to maintain stability. Because a fixed-output regulator is used, the output is connected directly to the sense input through zero-Ω resistor R7. Resistors R8 and R9 may be modified to allow the use of a variable output voltage linear regulator from the same device family, such as the TPS7A4501. When a fixed-output voltage IC is used, R8 is a DNP. Resistor R6 and diode D1 set the minimum-output load current of 10 mA.

4.3.4.2 Thermal Considerations

Linear regulator U1 drops from 12 to 3.3 V at up to the 100-mA specification. Because of the large-voltage drop across the regulator, a significant amount of heat is generated in U1 when the load is maximum. To dissipate this heat, a PCB heatsink is used instead of a discrete heatsink. To enable this, the TO-263 package is used that has a small junction-to-case thermal coefficient of 0.3 °C/W.

Assuming a worst-case input voltage of 13 VDC (8% greater than nominal) and an output-voltage regulating at 3.2 V (3% less than nominal), the worst-case voltage drop across the pass transistor is 9.80 V. At the maximum-specified operating load of 100 mA + 10-mA base current (from R6 and D1), the maximum-pass transistor power dissipation is 1.08 W (see [Equation 3](#)).

$$P_{reg(max)} = \left(V_{in(max)} - V_{out(min)}\right) \times \left(I_{out(max)} + I_{pre(max)}\right) + \left(V_{in(max)}\right) \times \left(I_{q(max)}\right) = 1.08 \text{ W} \tag{3}$$

The worst-case efficiency based on this dissipation is 22.2% (see [Equation 4](#)).

$$\eta \approx \frac{P_{out}}{P_{out} + P_{reg(max)}} = \frac{0.32 \text{ W}}{0.32 \text{ W} + 1.12 \text{ W}} = 22.2\% \tag{4}$$

The TI WEBENCH Design Center PCB Thermal Calculator can be used to estimate the case to ambient thermal coefficient for a given package and PCB layout. The large return plane in the layout for the 12- to 3.3-VDC stage provides a decent case-to-ambient thermal coefficient of 40 °C/W assuming natural convection (no fans). The maximum-junction temperature can then be calculated as in [Equation 5](#) based on a maximum 60°C ambient temperature (140°F).

$$T_{junction} = T_{ambient} + \left[P_{diss}\left(\theta_{jcb} + \theta_{ca}\right)\right] = 60 \text{ °C} + \left[1.12 \text{ W} \times \left(0.3 \frac{°C}{W} + 40 \frac{°C}{W}\right)\right] = 105 \text{ °C} \tag{5}$$

This result is 20°C less than the maximum-junction temperature of the device. In Figure 32, note the size of the plane to achieve the necessary dissipation without a heatsink.
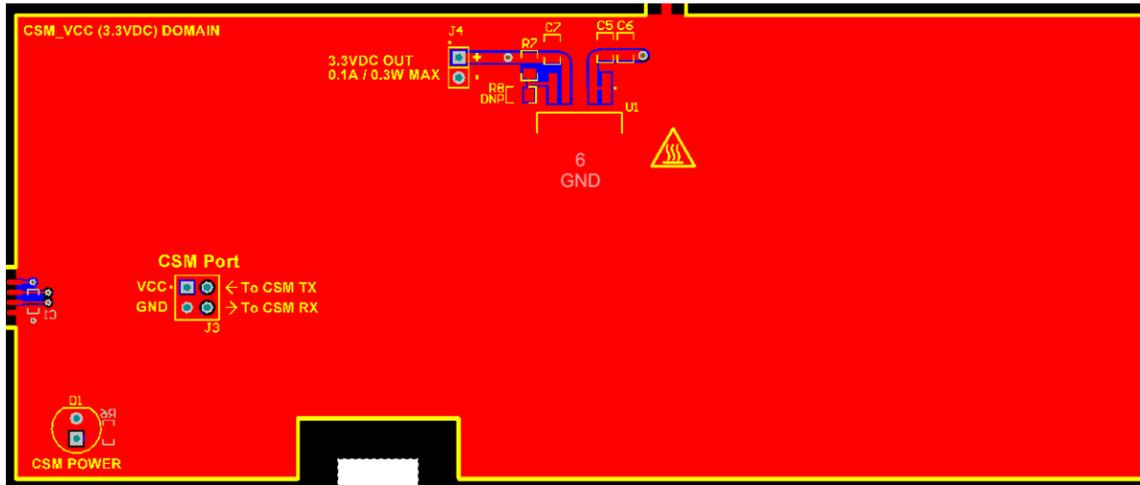

Figure 32. 12- to 3.3-VDC Linear Regulator Layout

Capacitors C5, C6, and C7 must be as close to regulator U1 as possible. A solid return plane (top layer) and solid VCC plane (bottom layer) are used for the 3.3-V domain. The 4-pin CSM port header in the layout connects to the CSM and provides power and serial communication connections.

4.3.5 Isolated I/O Domain

The isolated I/O domain contains a separate, isolated VCC and return plane that can be powered externally by a CAPTIVATE-PGMR module to communicate with the MSP430FR2633 MCU onboard the CSM. Figure 33 shows the top and bottom layers of the I/O domain on the PSM. The ESD protection clamps (TPD1E10B06 TVS devices) are close to the connector on the IO_VCC, IO_TXD, and IO_RXD connections.
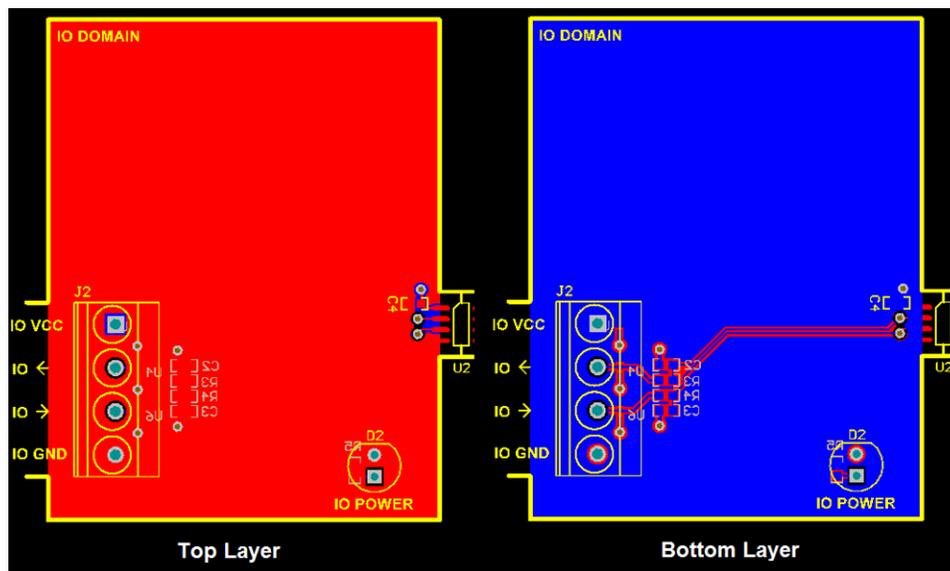
Figure 33. Isolated I/O Layout (Top and Bottom Layers)

Figure 34 shows a close-up of the ESD protection layout. The TVS devices are placed as close to the connector as possible, with vias to the ground plane on the opposite layer. Keeping the protection close to the connector serves two purposes. Through the diode, the size of the current loop from the pin to the I/O return pin in the connector is minimized, reducing the impedance of the path through the TVS device. This low impedance path encourages ESD current to flow through encourages ESD current to flow though the TVS rather than through the protected circuit.

The limited current loop-size limits the EMI generated by that loop as a result of the large $\frac{dI}{dt}$ flowing through it. If the TVS devices are far from the I/O connector, they are less effective at reducing current into the protected circuit and the large ESD current flowing through a larger loop area generates significantly more EMI that can then couple into and disturb neighboring circuits.
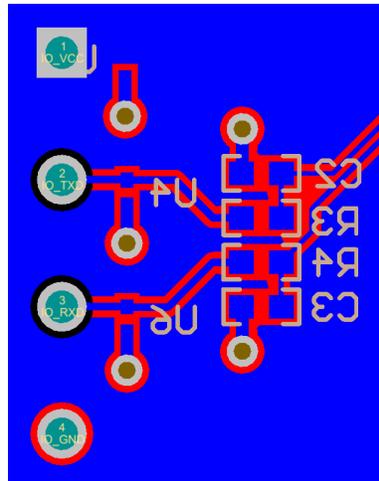
Figure 34. Isolated I/O ESD Protection (Bottom Layer)

4.4 Mechanical Design

The mechanical design of the TIDM-CAPTOUCHEMCREF includes the enclosure, the power entry, and I/O ports, and the wiring harnesses.

4.4.1 Enclosure Design

The enclosure is a two-piece, commercially-available polycarbonate (PC) box. Polycarbonate is an ideal material because it has a high-dielectric breakdown voltage (typically 15 kV/mm), a reasonable dielectric constant (typically 3 to 4), and it is easy to machine and less brittle when compared with other plastics such as acrylic. The high-dielectric breakdown voltage improves immunity to ESD events. Having a high-dielectric constant improves the sensitivity of the capacitive-sensing solution for a given thickness. The breakdown voltage and dielectric constant are related inversely in capacitive-sensing materials. For example, glass (another common overlay material) has a lower breakdown voltage, but a higher dielectric constant. The SERPEC 193C enclosure is used for this design, with the PS19 water-proofing gasket to seal the top and bottom of the enclosure (shown in Figure 35).
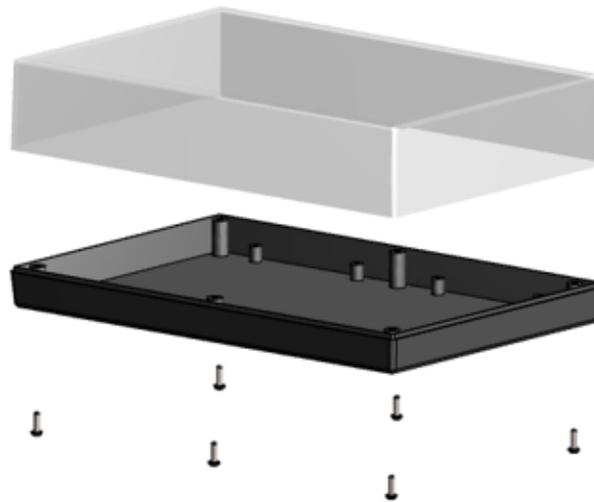
Figure 35. Enclosure

The enclosure measures 9.50 in. × 6.34 in. × 2.5 in. The power-supply module is fastened to the black bottom half of the enclosure through plastic machine screws. The capacitive-sensing module is adhered directly to the inside of the clear top half of the enclosure, with the top half of the enclosure as the touch surface. A two-sided adhesive from 3M is used to mate the CSM PCB with the enclosure. Their 468MP adhesive is ideal for capacitive sensing because of its strength and electrical properties.

4.4.2 Power Entry

The power-entry terminal is a standard, two-wire (no safety ground) IEC 320-C18 power inlet. The terminal has a male (receptacle) inlet, to accept a standard IEC power cable with or without the earth-ground conductor. For more information, see Figure 36.

Figure 36. IEC 320-C18 Power Inlet

The wire harness from the power-entry terminal to the PSM is as short and as tight as possible to limit EMI effects out of the cable, particularly during EFT testing. When the wire harness is longer, the risk of an EMI problem with the rest of the system becomes higher. This risk results from the cables between the power-entry terminal and the PSM that carry the input-power signal before any conditioning has occurred. Because the input EMI filtering occurs on board the PSM, the power-entry cables are the main point from which EMI can couple into other sensitive circuits. During early EFT testing of the reference design, the wire harness between the power entry terminal and the PSM was long and traversed the enclosure. This length of unprotected and unfiltered cable contributed to massive EMI coupling between the power wires and the CSM, leading to system-level problems such as IC brownout resets and digital logic glitches. The simple rerouting of the power entry wire harness so that the wires were as short as possible and far from any other sensitive signal harnesses improved the immunity of the solution to EFT.

Most products address these issues through integrating an input EMI filter into the power-entry terminal or through integrating ferrite cores into the power cord. These methods reduce the risk of EMI coupling from the power-entry cables into sensitive circuits inside the product. Products commonly include multiple ferrite cores on wire harnesses between subsystems inside a product (for example, between a processor module and a motor-drive module, or between a processor module and a power supply). When a cable inside the product is longer, potential for it to create problems becomes higher. A longer cable responds better to lower-frequency noise content (both as a receptor and a transmitter) than a shorter cable.

4.4.3   Isolated I/O Connection

The isolated I/O terminals let the CAPTIVATE-PGMR module connect in a bidirectional UART communication capacity. The CAPTIVATE-PGMR module may be used to stream data from the target MCU on the CSM to the CapTIvate design center running on a host PC. The isolated I/O connection consists of four miniature banana jacks for to help connect. The isolation provided is adequate for conducted RF noise-immunity testing but must not be used for EFT or ESD testing.

5   Signal-Processing Design Theory

The TIDM-CAPTOUCHEMCREF uses the CapTIvate software library to process raw capacitive measurements from the CapTIvate peripheral on the MSP430FR2633. The CapTIvate software library contains many signal-processing features designed to improve the robustness and reliability of capacitive-touch solutions in noisy environments. This section introduces the signal-processing features used in this TI Design to process raw capacitive measurements into touch status reports.

To select signal-processing components to implement, revisit the effects of different types of noise on capacitive-touch measurements. As introduced in Section 3.1, disturbances such as conducted noise, fast transients, and ESD can corrupt measurement results in different ways. Figure 12 and Figure 13 show the standard effects for self- and mutual-capacitance sensors, respectively. Figure 14 shows the effects of EFT on a self-capacitance sensor. The digital-signal processing chain must handle the following main issues:

- Continuous corruption of measurement values when conducted noise exists at the conversion frequency (applies to self and mutual capacitance)
- Addition of unwanted sensitivity to touch due to current injection into the receive electrodes from conducted noise (self-capacitance mode only)
- Corruption of single-measurement results in a non-periodic way due to transient disturbances from EFT and ESD events (see Figure 37)
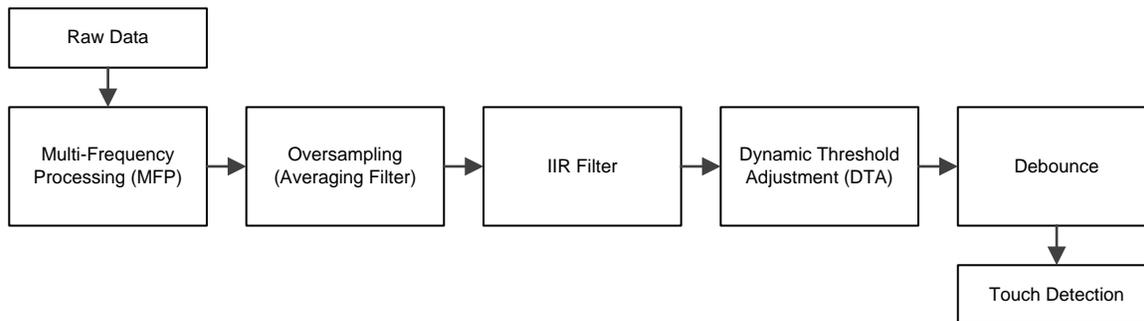
Figure 37. Signal-Processing Diagram

Figure 37 shows the signal-processing chain used to handle these issues. Processing begins after raw data is captured sequentially for each frequency tap (there are four). The raw conversion results from each frequency are combined into a single, composite result by the multi-frequency processing algorithm. The multi-frequency processing algorithm removes corrupted measurements in the event that conducted noise exists at one of the conversion frequencies. That process (measuring at four frequencies and resolving down to one result) is then repeated *n* times based on the oversampling level that is set (4× for the CSM-SELF, 2× for the CSM-MUTUAL). The oversampled results are then averaged to produce a new composite value. This oversampling process aids in reducing the effects of short, non-periodic transient disturbances, such as those due to an EFT or ESD burst. An IIR filter is then applied. The IIR filter acts as a low-pass filter, passing DC-state changes—touch and no touch states—and attenuating periodic noise, such as 50-Hz to 60-Hz interference. For the CSM-SELF, a dynamic threshold adjustment algorithm is applied to stabilize the sensitivity of each sensor in the event that there is strong conducted noise present in the system. Recall from Figure 13 that self-capacitance sensors exhibit increased, unwanted sensitivity to touch when subjected to strong common-mode noise. The DTA algorithm looks at the noise in historical measurements and computes a threshold adjustment to counteract the additional sensitivity associated with the noise. Basic debounce-in and debounce-out logic is used to qualify a state change into or out of touch detection. The debounce logic aids in preserving the correct state even if short transient events such as EFT or ESD disturb the sample stream.

IIR filtering and debounce are always available in the CapTIvate software library and they are adjustable through the CapTIvate design center. Enabling conducted noise immunity in the CapTIvate design center makes the MFP, oversampling, and DTA algorithms available. These algorithms are configured through a configuration structure in firmware.

5.1 Multi-Frequency Processing (MFP) Algorithm

The CapTIvate peripheral operates on a charge transfer measurement principle in which an internal clock, called the conversion clock, drives the conversion process of repeated charge transfer cycles.

There is a fundamental frequency called the conversion frequency involved. The conversion frequency is the rate at which charge transfers are driven on the sensing electrode. The period is defined as the charge phase plus the transfer phase plus any associated dead time between the two phases. The conversion frequency is a critical frequency in the sense that the measurement is the most vulnerable to noise at the fundamental-conversion frequency, and to a lesser extent at the harmonics of that frequency.

The CapTIvate oscillator has a base-trimmed frequency of 16 MHz. To provide immunity to RF noise at the conversion frequency, the oscillator can hop to three alternate sub-frequencies to move the conversion away from the noise source in the frequency domain, as shown in Figure 5. Table 8 lists the available frequency taps on the MSP430FR2633. The oscillator supports up to a 30% shift away from the base conversion frequency.

Table 8. MSP430FR2633 CapTIvate Oscillator Frequency Taps

Frequency Tap	Clock Frequency
Base [0]	16.00 MHz
Hop 1 [1]	14.70 MHz (–8%)
Hop 2 [2]	13.10 MHz (–18%)
Hop 3 [3]	11.20 MHz (–30%)

Table 9 lists the effective conversion frequencies for the CSM-SELF and CSM-MUTUAL panels. Both configurations use one divided-oscillator period for the charge and transfer phase, and that the mutual-capacitance module (CSM-MUTUAL) is configured to run at 2× the speed of the self-capacitance module (CSM-SELF). Mutual-capacitance electrodes can be driven faster than self-capacitance electrodes before the measurement results are affected. When selecting the base-conversion frequency for a sensor, ensure that the conversion frequency is appropriate for the size of the capacitance. Larger load capacitances require slower conversion frequencies to ensure complete charge transfers. Connect an oscilloscope to the sensing electrode to view the quality of the charge transfer waveform.

Table 9. CSM-SELF and CSM-MUTUAL Conversion Frequencies

Parameter	CSM-SELF	CSM-MUTUAL
Oscillator-frequency divider	÷4	÷2
Divided-oscillator frequency	4.00 MHz	8.00 MHz
Charge-phase length (divided oscillator cycles)	1	1
Transfer-phase length (divided oscillator cycles)	1	1
Conversion frequency (base)	2.00 MHz	4.00 MHz
Conversion frequency (hop 1)	1.84 MHz	3.68 MHz
Conversion frequency (hop 2)	1.64 MHz	3.28 MHz
Conversion frequency (hop 3)	1.40 MHz	2.80 MHz

There are four different frequency taps available at the oscillator, rather than the frequency divider and phase-length controls. These taps are beneficial because the location of the fundamental and associated harmonics can be shifted. The four frequency taps were selected to limit harmonic overlap.

The multi-frequency processing (MFP) algorithm in the CapTIvate software library resolves raw measurement data taken at multiple conversion frequencies into one composite measurement result that can be then passed on to the high-level processing algorithms as if only one conversion frequency was used. Do as follows:

1. Measure each time cycle at all four conversion frequencies (base, first hop, second hop, and third hop).
2. Apply the MFP algorithm to generate a composite result based on the four raw inputs and a value that

represents the noise observed in the raw measurement by comparing the four base-conversion frequencies.

3. Continue with higher-level processing using the composite result generated by the MFP algorithm.

There is no tuning required for the multi-frequency processing algorithm. The only controls that affect performance of the algorithm are the conversion control settings that determine the base conversion frequency, and the spread-spectrum modulation setting. The base conversion frequency must be high enough for a sufficient spread between the four frequencies. Conversion frequencies between 2 MHz and 4 MHz are appropriate for mutual-capacitance sensors. Conversion frequencies between 1 MHz and 2 MHz are appropriate for self-capacitance sensors. Spread-spectrum modulation spreads out the conversion frequency during the conversion. The modulation steps the conversion frequency up and down to ± 16% of the nominal conversion frequency, reducing the effects of noise at the base-conversion frequency and slightly increasing it at surrounding frequencies. Test data shows that the modulation feature must be disabled for mutual-capacitance sensors and enabled for self-capacitance sensors. Disabling it for mutual-capacitance sensors improves the performance of the MFP algorithm by providing better isolation between frequency taps. Enabling it for self-capacitance sensors improves the performance of the DTA algorithm by providing cleaner measurement of noise in the system across the noise-frequency spectrum.

5.2 Oversampling

Oversampling is a technique to reduce transient glitches in samples without negatively impacting the infinite-impulse response (IIR) filter down the signal stream. The CapTIvate software library allows measurement oversampling to be configured in binary increments (2×, 4×, 8×, 16×, and 32×). The oversampling algorithm is an averaging filter that captures the specified number of conversions and performs an average to generate a composite result. If multi-frequency conversions are configured, each sample in the oversampling set is composed of four conversions (1 at each frequency tap) that have been resolved through the multi-frequency processing algorithm. The CSM-MUTUAL software uses a 2× oversampling setting, while the CSM-SELF software uses a 4x oversampling setting. When one CSM-SELF sample passes the oversampling phase, it is composed of 16 separate raw measurements.

For a new design, set the largest oversampling possible while providing the required report rate for best performance. Every time the oversampling level increases one notch, the measurement time doubles from the current setting. Large sensing-panel configurations with lots of electrodes to scan are often limited in the total oversampling that can be applied for this reason.

The main benefit of oversampling versus IIR filtering is the way it handles transient disturbances. The following is an example of a CSM-SELF panel with a 4× oversampling setting. If one of the four samples is affected by some transient-noise source but the other three samples are correct, the bad sample has a one-time weight of 25%. After this sample is processed, that bad sample no longer affects any future samples. In the case of IIR filtering, the bad sample continues to affect the output for several samples because of the infinite-impulse response.
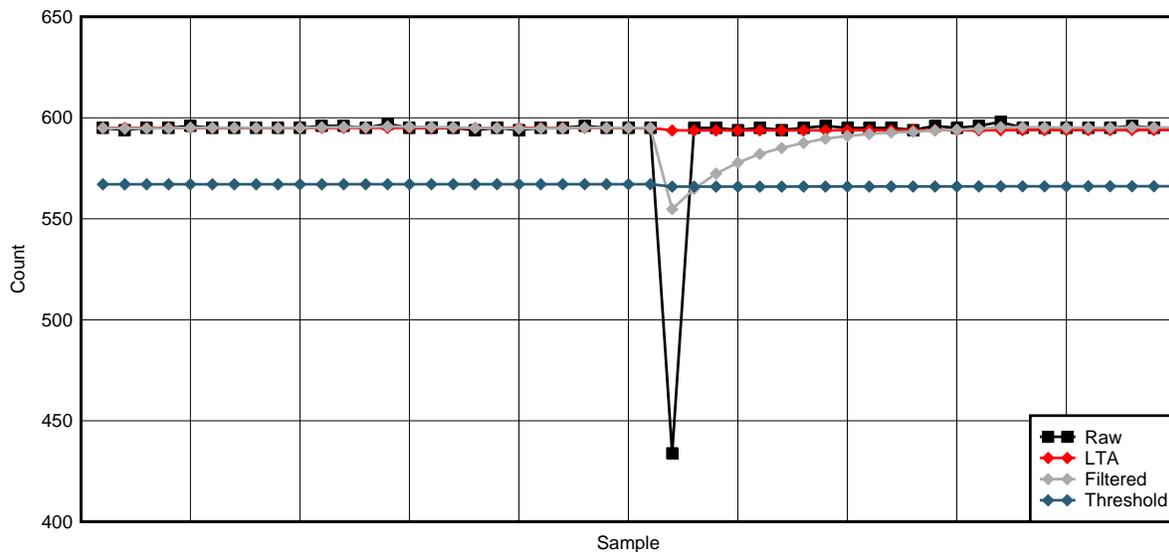
5.3 IIR Filtering

IIR filtering is an effective method of attenuating periodic low-frequency noise in a measurement, such as 50- to 60-Hz noise, with little memory overhead. The CapTIvate software library contains an IIR filter enabled by default for all sensors. See Figure 38 for an example. Acting as a low-pass filter, the IIR filter can remove a large portion of the periodic noise from the raw-input signal.
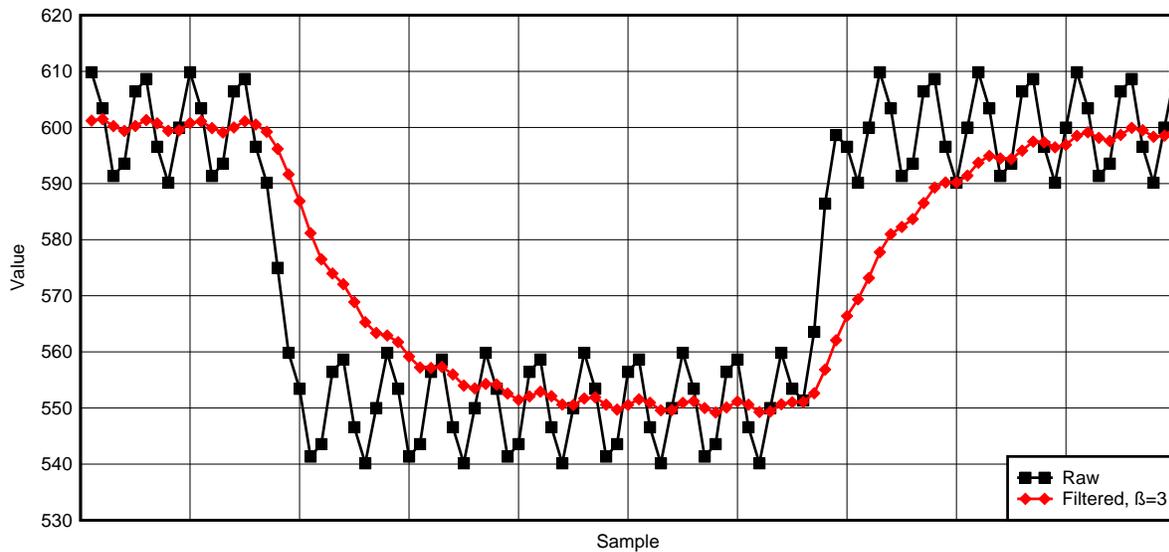
D002

Figure 38. IIR Filtering Periodic-Noise Response Example

There are a few tradeoffs to consider when using the IIR filter. Some positive phase shift introduced and transitioning between a touch states requires more samples because of the characteristic RC waveform. Transient noise spikes due to EFT or ESD lasting only for 1 sample can affect multiple samples (see Figure 39).

D003

Figure 39. IIR Filtering Transient-Noise Response Example

Figure 38 shows the response of a system to a single glitch (in this case, due to an EFT event). The glitch is only present in the raw data for one sample and that sample error can be handled with one count of debounce. The IIR filter output shows evidence of the glitch for several samples because of the infinite-response characteristic of the filter. The magnitude of the glitch is decreased but effects many samples. Two of those samples are actually lower than the threshold (a debounce setting of 1 cannot prevent a false detection).These scenarios show why it is good to use a combination of oversampling, IIR filtering, and debounce to ensure a system is reliable.

The IIR filter has a configurable strength, defined as the β value of the filter. A β = 0 system has no filtering and a 50/50 weighting between the historic sample and a new sample. A β = 2 system has a 75/25 weighting between the historic sample and a new sample. The response of the system slows down rapidly as the β value increases.

5.4 Debounce

The debounce feature of the CapTIvate software library allows the user to reject short variations in the data stream that are too short to be representative of a valid state transition (no touch to touched, or touched to no touch). The feature is configured in a samples-in and samples-out format. A *debounce-in* setting of 2 requires that after the touch threshold is crossed in the data stream, it must remain crossed for at least two additional samples before a touch is reported to the application. Figure 40 shows how debounce passes the steady-state touch condition, but rejects the short pulse which is a glitch. The touch threshold is crossed in both cases, but a touch is only reported to the application when the debounce criteria is met.
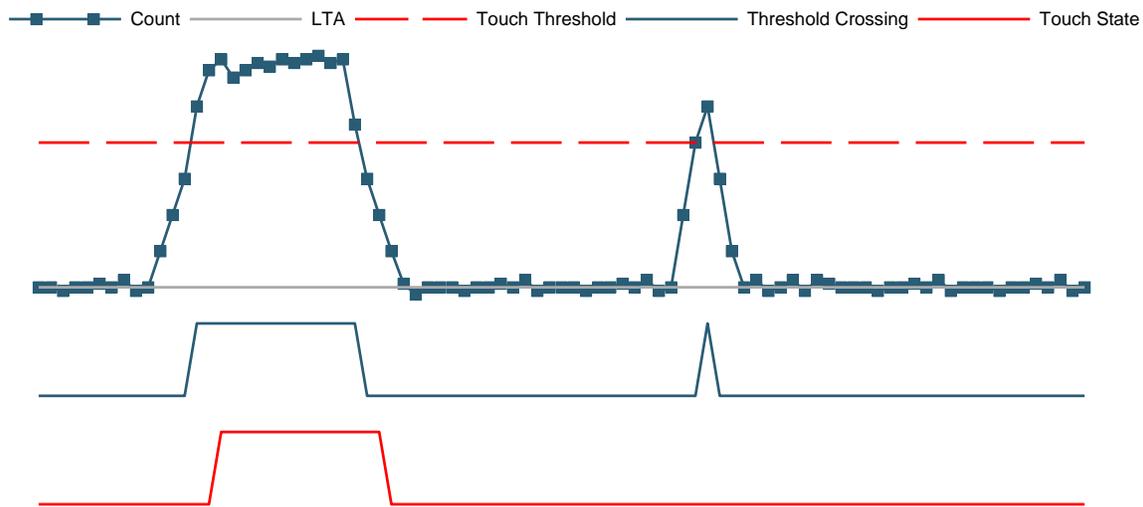
Figure 40. Debounce Example

As debounce levels increase, the response time to a touch increases.

5.5 Dynamic Threshold Adjustment Algorithm

In the presence of strong conducted noise, self-capacitance sensors exhibit extra sensitivity to touch as a result of unwanted injected noise current. Figure 13 introduced this effect and Figure 41 shows it in the test data section.
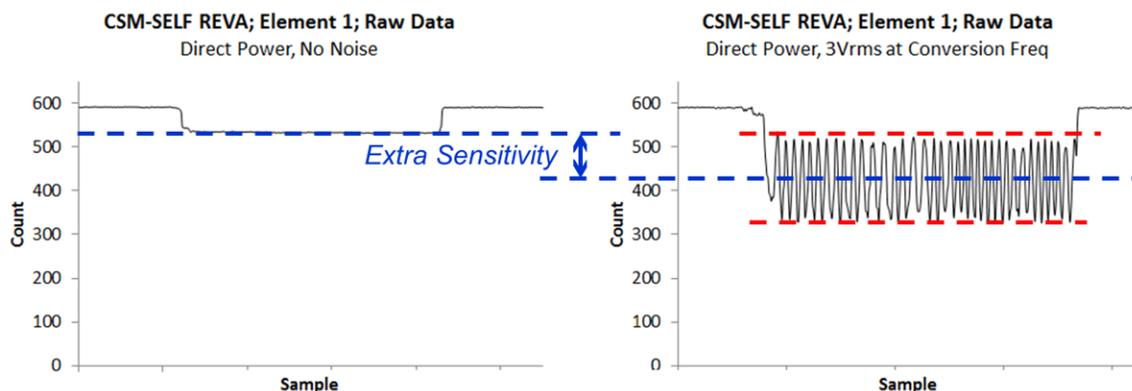
Figure 41. Extra Sensitivity in Self-Capacitance Mode Due to Conducted Noise

Figure 41 shows the extra sensitivity that results from noise. The periodic noise signal in the right plot can be removed with a combination of oversampling and IIR filtering but the DC offset between the blue dashed lines is not compensated for by these methods. This extra sensitivity can result in a proximity effect, where a capacitive button goes into detect early as the user approaches the sensor instead of when they touch the sensor. This behavior is undesirable in an application and poses the most challenge in designs where sensors are closely packed or used with thick overlay stackups.

The dynamic threshold adjustment (DTA) algorithm is a feature of the CapTIvate software library applied only in self-capacitance mode and is designed to counteract these effects to maintain the desired level of sensitivity. This feature is applicable only to the CSM-SELF-sensing panel in this design. The dynamic threshold-adjustment algorithm actively observes the noise in multi-frequency measurements and generates one relative global noise level based on the elements in the user interface. That global noise level is used to calculate a threshold-adjustment factor to compensate for the increased sensitivity because noise is in the system. The goal is to preserve the correct sensitivity as much as possible while preventing any false touch detections.

The DTA algorithm uses a global, relative noise value as an input that represents the highest noise value on any element in the application, expressed as a fraction of the long-term average (LTA) so that it can be applied to sensors with different conversion count settings. When conducted-noise immunity is enabled in the CapTIvate design center and multi-frequency conversions are configured, the EMC module of the CapTIvate software library computes the current global noise value based on the self-capacitance elements in the user interface. This value can be used to derive a threshold-adjustment factor.

The variation in sensitivity due to noise varies in a non-linear way with the noise measured in the system. Rather than varying in a linear way, the additional sensitivity increases slightly faster than the noise level increases. For this reason, a second order polynomial relationship computes the correct threshold adjustment based on the noise-level input. The following equations show this relationship. The relative adjustment value is computed on a simple $ax^2 + bx$ form, where the input x is the relative global noise level and the output is the relative global threshold-adjustment factor.

$$adj_{rel} = A \times noise_{rel}^2 + B \times noise_{rel} \tag{6}$$

$$touch\_thresh_{new} = touch\_thresh_{tuned} + adj_{rel} \tag{7}$$

$$prox\_thresh_{new} = prox\_thresh_{tuned} + \frac{adj_{rel} \times LTA}{128} \tag{8}$$

Coefficients A and B in the polynomial are tunable values in the CapTIvate software library and they are represented by IQ31 fixed-point decimal values. The library provides default values of 0.006 and 0.01 for A and B, respectively. Figure 42 shows the resulting compensation curve with the curve selected for the CSM-SELF (0.004 and 0.1 for A and B, respectively). Variations in electrode size, overlay thickness, and nearby ground structures can affect the performance of a given set of coefficients. Coefficient A must be between 0.003 and 0.008. Increasing it beyond 0.008 creates an aggressive ramp that can mask true touches. For most designs, achieving tolerance of 3-V_{rms} conducted noise with good layout techniques is straightforward. Pushing beyond 3 V_{rms} to 10 V_{rms} requires significantly greater attention to detail and careful testing.
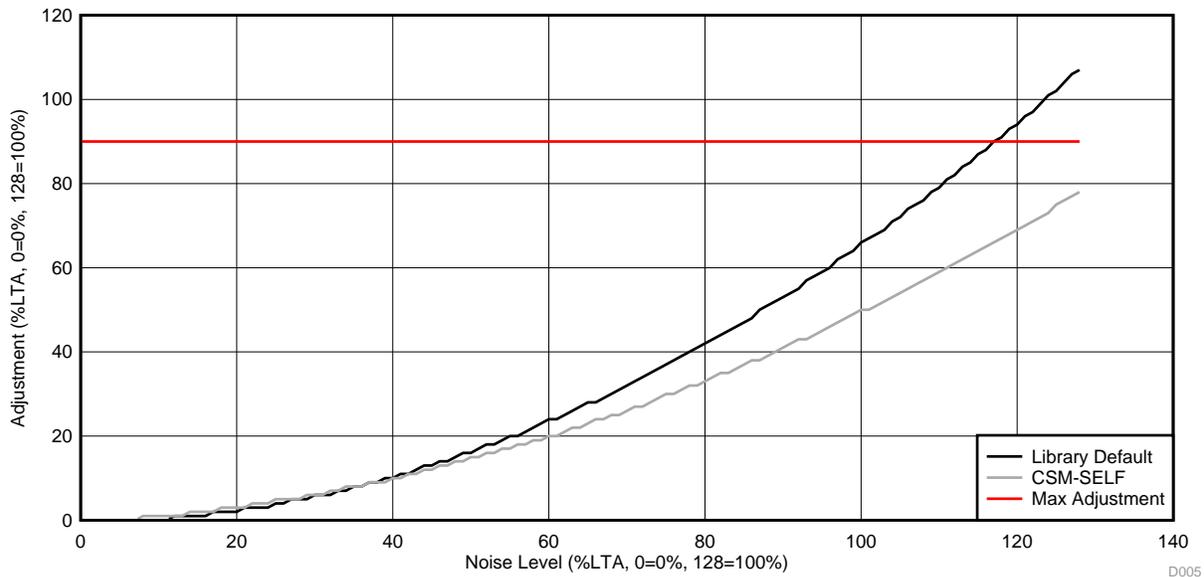
Figure 42. DTA Tuning Curves

Applying the DTA algorithm with the other processing to the case in Figure 41 produces the results shown in Figure 43. The threshold adjusts with the increase in sensitivity and the IIR filtering and oversampling has removed the sinusoidal-noise component from the measurement.
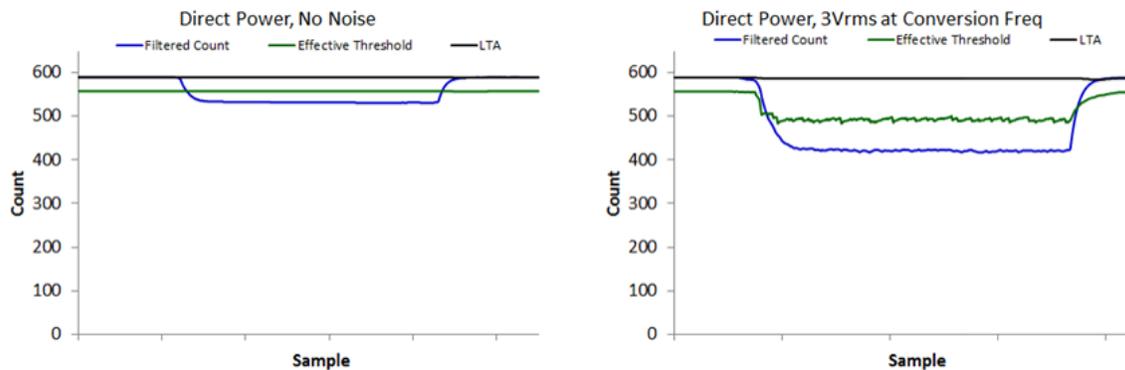

Figure 43. DTA Compensation Applied

The DTA algorithm acts as a peak detector. The algorithm locates the highest noise value in the system and holds that value through a mechanism similar to an IIR filter, where negative-going changes have strong filtering (to create the peak-detect function) and positive-going changes have weak filtering (to allow quick adjustment when a touch approaches). These settings are also adjustable.

6   Firmware Design

The firmware architecture for the MSP430FR2633 MCU on the CSM-SELF and CSM-MUTUAL was designed to meet the following requirements:

- The design must provide mutual-capacitance and self-capacitance implementations with a common firmware base for share components.
- The design must provide error and fault detection, logging, and reporting to aid in IEC testing and diagnostics.
- The design must be able to report the status of the UI visually (through LED indicators) as well as digitally through a serial interface.
- The design must use Driver Library API calls where possible.
- The design must use FRAM for sensor-state retention through power loss.

Figure 44 shows a block diagram of the firmware architecture. Common application code shared between the CSM-SELF and CSM-MUTUAL modules is blue. Code that is CSM specific is orange. Common libraries that are not application specific are white.
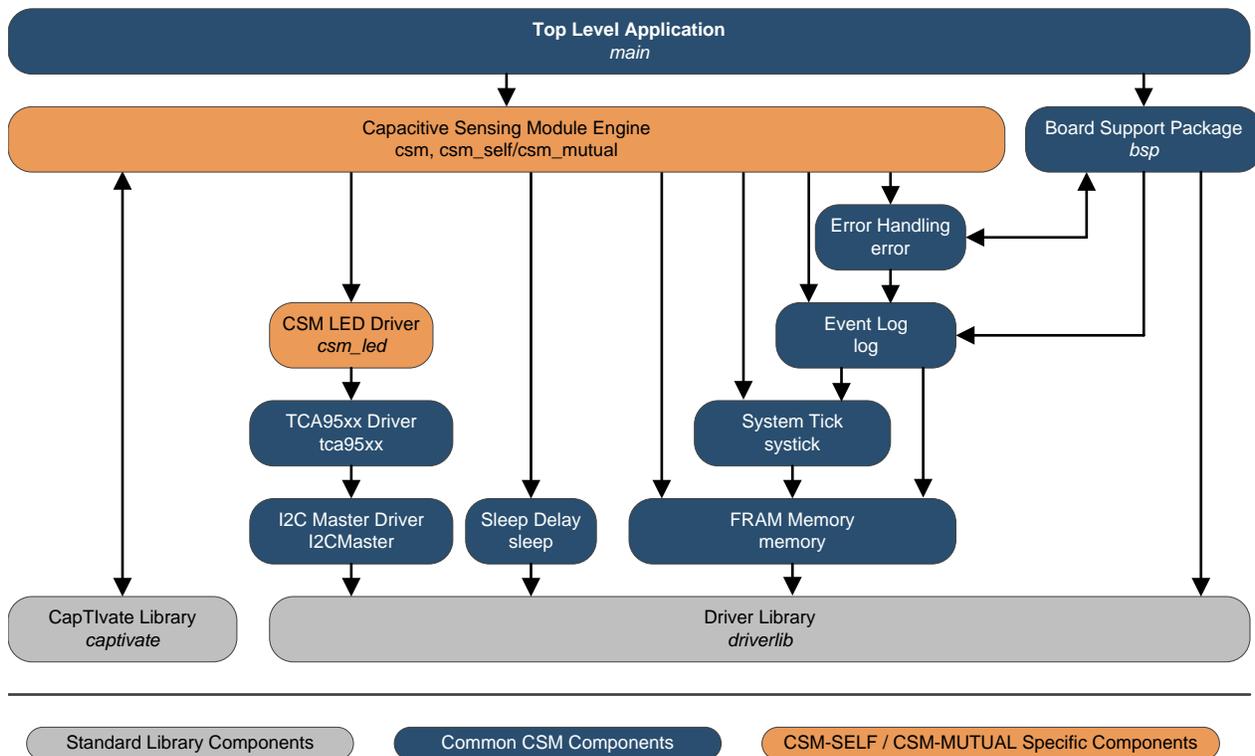
Copyright © 2016, Texas Instruments Incorporated

Figure 44. Firmware Architecture Block Diagram

Section 6.1 explains the firmware modules.

6.1   *Board Support Package*

The board support package (BSP) handles configuration of the microcontroller and its responsibilities follow:

- Port mux configuration
    - All unused ports are active low.
    - The BSP controls the system status LEDs for latched detect, run, noise, and fault.
- Clock system configuration
    - 16-MHz MCLK sourced from the DCO

– 2-MHz SMCLK sourced from the DCO
– 32-kHz ACLK internally sourced from the REFO
– 32-kHz FLLREF internally sourced from the REFO
- FRAM controller configuration
  – One dwell state
  – All FRAM error interrupts enabled
- Watchdog timer configuration
  – Watchdog mode, with a 16-s timeout
- NMI interrupt handler configuration
  – Vacant memory access interrupt (fatal error)
- Managing the fatal error handler
  – Lock the application and set the fault status LED
- Capture of the SYSRSTIV (reset source) during boot
  – Log the cause of all resets for testing

The 16-MHz MCLK (CPU clock) allows for fast execution of algorithms, improving the response time of the system. FRAM accesses are limited to 8 MHz (one dwell state); ROM, RAM, and cache accesses occur at 16 MHz.

6.2 CapTIvate Software Library

TI is releasing this TI Design with version 1.03.02.00 of the CapTIvate software library. The CapTIvate design center generated the user configuration files for the CSM-MUTUAL and CSM-SELF modules.

6.2.1 CSM-SELF Configuration

The CSM-SELF panel contains 12 buttons and one slider. The CapTIvate design center organizes these sensors into three time cycles (for the buttons) and one time cycle (for the slider). A conversion-count value of 600 was used with a conversion gain value of 100 to achieve the required sensitivity to overcome the strong-return plane parasitic loading on the buttons. The strong-return plane loading was added in the layout process to enhance noise immunity. In addition to these parameters, spread spectrum modulation is enabled, and a maximum count is set at 625 to limit spikes due to noise and prevent conversion time from increasing. The automatic power-down control is selected, which prevents the CapTIvate LDO from powering down after each time cycle. reducing wake-up times and improving the scanning efficiency. Debounce values of 2 are used for entering and exiting a touch or proximity state.

A conversion count of 650 and conversion gain of 100 are used to provide some additional sensitivity for the slider. The slider requires more sensitivity than the buttons because a position is computed from the measurements, rather than just a touch status. Similar settings are used otherwise. The slider has 8 bits of resolution (256 points).

While full multi-touch status is reported for each button and each element of the slider, this reference design allows only one button to be touched at a time. The first button touched has its state updated; additional buttons do not change state until all buttons are released and the other buttons are touched again. This feature improves immunity to crosstalk between buttons, particularly in high-noise environments. The buttons and slider operate independently; either one can be touched concurrently.

6.2.2 CSM-MUTUAL Configuration

The CSM-MUTUAL panel has 32 buttons arranged as two 4 × 4 matrices. The CapTIvate design center organizes the two matrices into eight total time cycles of four elements each. A conversion count of 400 is used with a conversion gain of 150 to provide an appropriate sensitivity to detect touches reliably. Spread-spectrum modulation is disabled to improve the effectiveness of the frequency-hopping algorithm. A maximum-count error threshold of 600 is set to limit errant samples due to noise to 600. 600 is 200 counts greater than the baseline of 400, allowing for a touch delta of up to 200. Most touch deltas are in the range of 75 to 100 for this design. Debounce values of 2 are used for entering and exiting of a touch or proximity state. The maximum bias current drive (20 µA) is applied to help drive the large load capacitance on the Rx lines.

While full multi-touch status is reported for each button, this reference design only lets one button from each matrix be touched concurrently. The first button touched has its state updated; additional buttons do not change state until all buttons are released and the other buttons are touched again. This improves immunity to crosstalk between buttons.

6.3 Capacitive-Sensing Module

The capacitive-sensing module (CSM) firmware block provides the top level control of the capacitive-touch interface, including its initialization, calibration, and its periodic updates. The module also provides board-specific (self and mutual) submodules with the appropriate CapTIvate event callback handlers for touch events. Sensor-state LEDs and the latched detection status LED are controlled by the module's event callback handlers. Touch events are also logged through the logging module.

Button and slider states are preserved in FRAM on the MSP430FR2633 through any power losses. When the CSM powers up, a power-on self-test (POST) runs to test all of the LEDs. After the POST, the state indicators shows the panel in the state that the module was when last powered down.

6.4 Sensor-State LED Control

Sensor states are shown on both CSMs through LEDs. These LEDs are controlled through TCA9535 I^{2}C I/O expanders. The CSM layer calls the TCA95xx firmware driver to control the LEDs. The TCA95xx driver calls the I^{2}C master driver to communicate with the expanders. All I^{2}C and TCA95xx errors are reported to the CSM layer, where they can be logged for review.

6.5 Event Logging

The log module uses a subset of the data section of FRAM on the MSP430FR2633 to store event information that can be read from the device through a serial interface and decoded on a host PC. The log buffer is designed as a low resource substitute. for a ring buffer; when the log is full, the least recent log messages are overwritten.

The system tick module provides two time stamps used for stamping log messages: seconds since last reset (PUC) and seconds since birth (programming). These time stamps enable log messages to be used to detect undesired resets during EMC testing.

The memory module abstracts locking and unlocking of the data memory section for simplicity and safety. All FRAM writes go through the memory module. Log messages have the following format: TIMESTAMP, SYSID, MSGID, and MSG.

6.6 Error Handling

The error-handling system runs above the logging system and allows for two types of runtime errors to be thrown by the application: fatal errors and nonfatal errors.

- Fatal errors
  - Halt the application from running and show that a fatal error has occurred
  - Log as an event

    Example: FRAM corruption detected, vacant memory access, invalid I^{2}C read back detected
- Nonfatal errors
  - Do not halt the application

– Log as an event

Example: I^{2}C slave nack, I^{2}C bus time-out, I^{2}C bus unavailable

7 Getting Started Hardware

The TIDM-CAPTOUCHEMCREF hardware can be configured in several ways. This section introduces how to wire in each board for demonstration, testing, programming, and debug.

7.1 Enclosure and Safety

When used with the PSM-UACTO3.3VDC power supply, this is a high-voltage reference design. Take standard safety precautions when evaluating a configuration that uses this power-supply module.

During EFT or ESD testing, dangerous voltages can present themselves in the circuit. Do not touch any circuit boards while conducting any EFT or ESD testing and follow good safety practices when running these tests.

Test the TIDM-CAPTOUCHEMCREF when fully assembled, with the PSM, CSM, and wiring harnesses safely inside of the polycarbonate enclosure. The isolated I/O interface can be used for extracting data without opening the enclosure.

7.2 Connecting to the CSM-SELF and CSM-MUTUAL Directly for Programming and Tuning

A CAPTIVATE-PGMR module can be directly connected to the CSM-SELF and CSM-MUTUAL PCBs to program and can debug the MSP430FR2633 target. Capacitive-sensing data can be sent and received with the CapTIvate Design Center in this configuration. As shown in Figure 45, jumper wires can be used to connect a given CSM to the CAPTIVATE-PGMR.
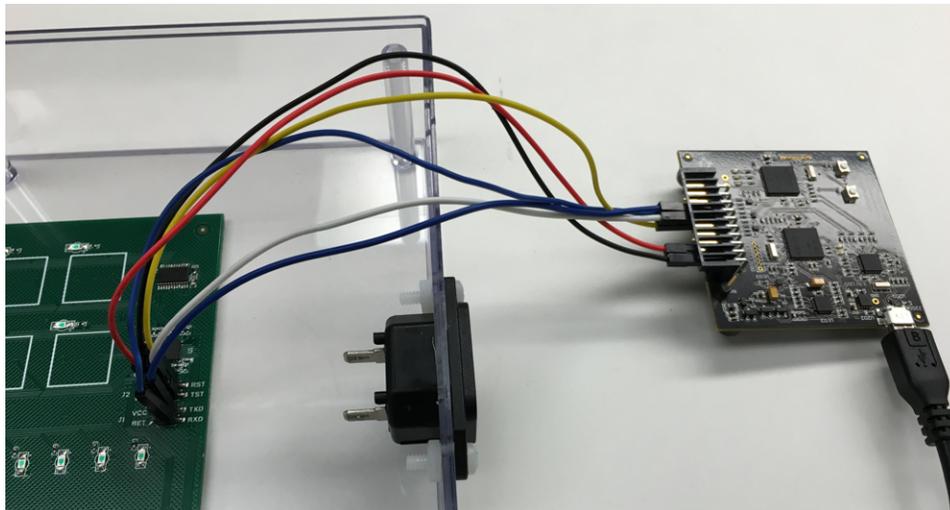
Figure 45. CAPTIVATE-PGMR Direct Attachment for SBW and Real-Time Tuning

The CSM can be powered directly from the CAPTIVATE-PGMR off of its 3.3-V rail. Figure 46 represents the primary, 20-pin header of the CAPTIVATE-PGMR. Table 10 shows the pin mapping between the CAPTIVATE-PGMR and the CSM headers.
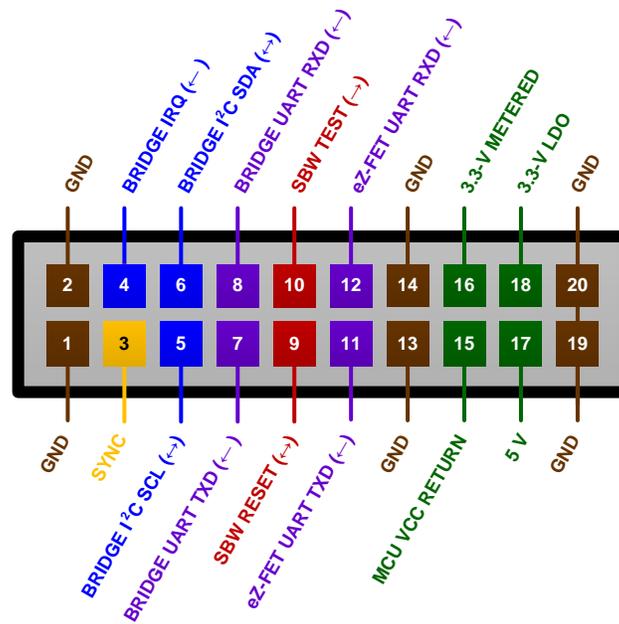
Figure 46. CAPTIVATE-PGMR Connector

**Table 10. Programming Wiring Connections**

CSM Header Label	CAPTIVATE-PGMR
VCC	3.3-V LDO [Pin 18]
RET	GND [Pin 20]
TST	SBW TEST [Pin 10]
RST	SBW RESET [Pin 9]
TXD	BRIDGE UART RXD [Pin 8]
RXD	BRIDGE UART TXD [Pin 7]

7.3 Wiring the PSM, CSM and Enclosure

The PSM is mounted directly into the bottom half of the enclosure with screws and has three wire harnesses.

7.3.1 Power-Entry Harness

Power entry is wired in through a 14 to 16 gauge wire rated for household voltage. Female spade crimp connectors are attached for connecting to the power-entry connector, as shown in Figure 47. The wire harness must be as short as possible.
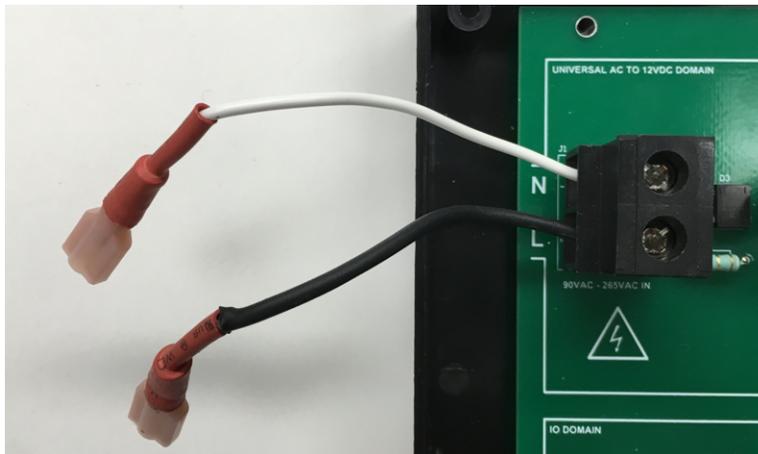
Figure 47. Power-Entry Wire Harness

7.3.2 Isolated I/O Harness

Small, short 18 gauge or less unshielded wires connect the isolated I/O section of the PSM to four mini-banana jacks that are screw-mounted into the bottom half of the enclosure near the isolated I/O section, as shown in Figure 48.
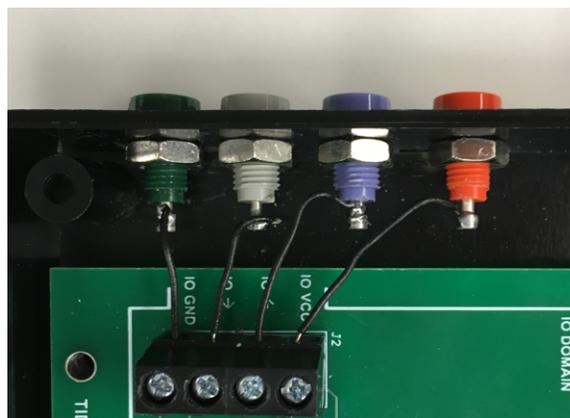
Figure 48. Isolated I/O Wire Harness

7.3.3 PSM-to-CSM Wire Harness

The PSM is connected to the CSM with a 4-wire harness. The wires must be no longer than require to make the connection. For more information, see Figure 49.
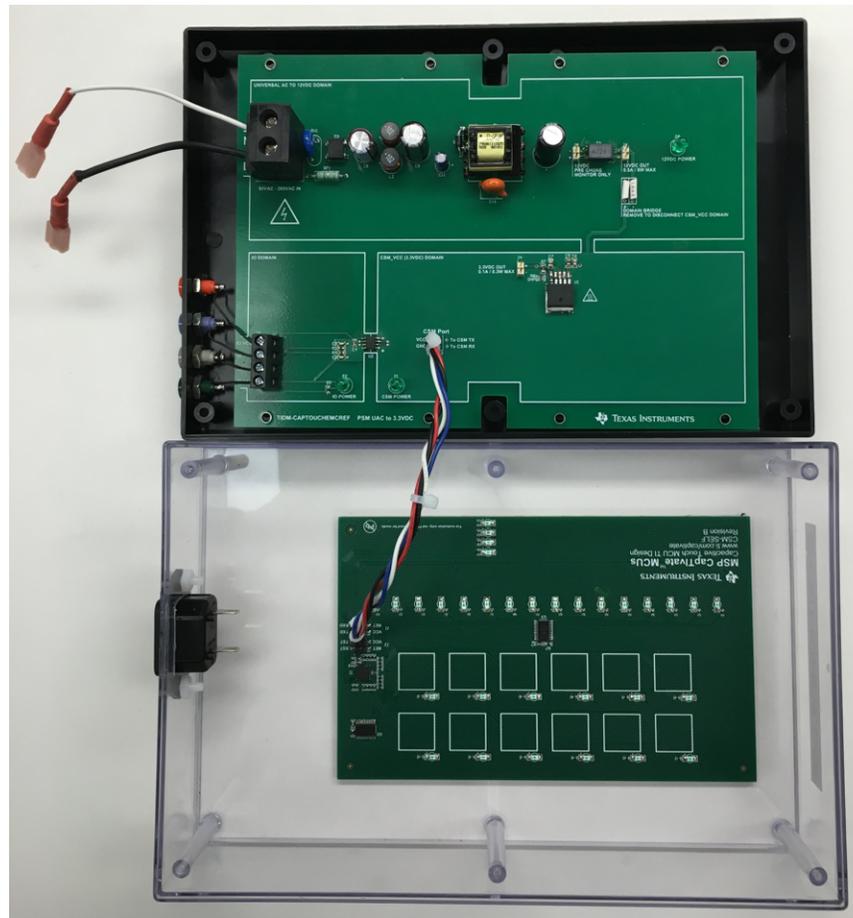
Figure 49. PSM-to-CSM Wire Harness

Figure 49 shows the CSM-SELF wired to the PSM-UACTO3.3VDC with a short, color-coded harness. To complete the assembly, the power entry connectors must be connected to the power-entry wire harness. The entire assembly can be connected with screws.

7.4 *Connecting an Assembled Unit to the CAPTIVATE-PGMR through the Isolated I/O*

An assembled TIDM-CAPTOUCHEMCREF unit can be connected to the CAPTIVATE-PGMR for bidirectional communication with the CapTIvate design center for performance evaluation. The isolated I/O interface provides the connection. A custom wire harness allows the CAPTIVATE-PGMR to connect to the four mini-banana jacks on the reference design, as shown in Figure 50.
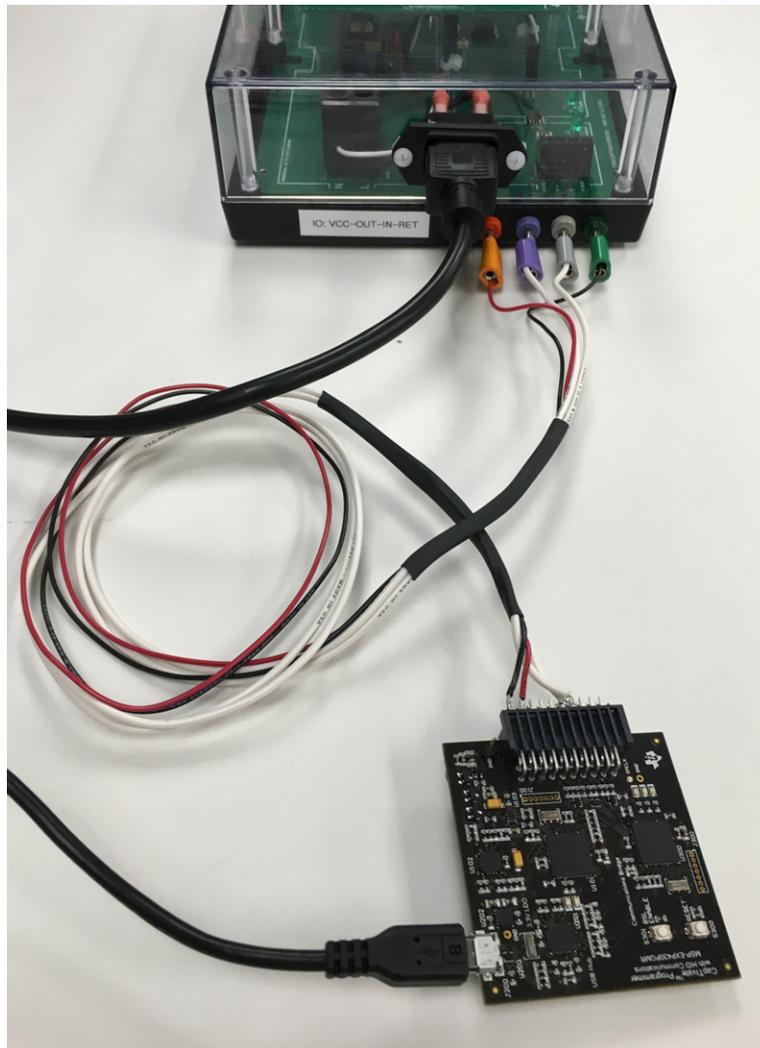
Figure 50. Reference Design Unit with CAPTIVATE-PGMR

7.5 *Overview of the LED-Status Indicators*

As shown in Figure 51, four status LEDs at the bottom of each CSM provide insight into how the CSM is operating.

Figure 51. CSM-Status LEDs

The first LED (amber) is a latched detect LED. When the CSM powers up, this LED is cleared. When any touch is detected, the LED lights and remains lit for the duration of the runtime session. This LED provides a visual indicator if any false detects occur during an EFT or ESD test because ia button-state LED can toggle and remain unseen.

The second LED (green) indicates that the interface is running and toggles when the user interface is refreshed. The third LED (yellow) indicates that noise is detected in the system by the CapTIvate software library EMC module. This LED reflects a logical OR of the noise status flag of every sensor. The fourth LED (red) is the fault detection LED. This LED is illuminated if a system fault is detected and is the result of a fatal error. If there is a calibration error, the fault LED also lights. In addition to the four status LEDs, each sensor has amber state LEDs that indicate the current state of that sensor. When a CSM powers up, it runs a POST of all LEDs in the system to ensure that they are working.

7.6   PSM-UACTO3.3VDC Configuration

The PSM-UACTO3.3VDC contains two power monitoring posts; one is on each side of the common-mode choke provision (J5 and J6). These allow voltages to be monitored on both sides of the choke, if populated. To use the common-mode choke, populate T2 on the top layer and depopulate R16 and R17 on the bottom layer. To use the supply without a common-mode choke, follow the previous procedure in reverse. For more information, see Figure 52.

Figure 52. PSM-UACTO3.3VDC Monitor Posts and Domain Bridge

Diode D8 indicates that the 12-V rail is live. The 12-V rail is connected to the 3.3-V domain by the two domain bridge jumpers, shown in Figure 52. During normal use, these jumpers are always populated. They can be removed to isolate the 3.3-V LDO from the 12-V rail.

7.7   PSM-12VDCTO3.3VDC Configuration

After the common-mode choke provision, the PSM-12VDCTO3.3VDC contains one 12-VDC power-monitoring post (J5). To use the common-mode choke, populate T1 and depopulate R9 and R10. To use the supply without the common-mode choke, follow this procedure in revers. LED D4 indicates when the 12-V input is live. For more information, see Figure 53.
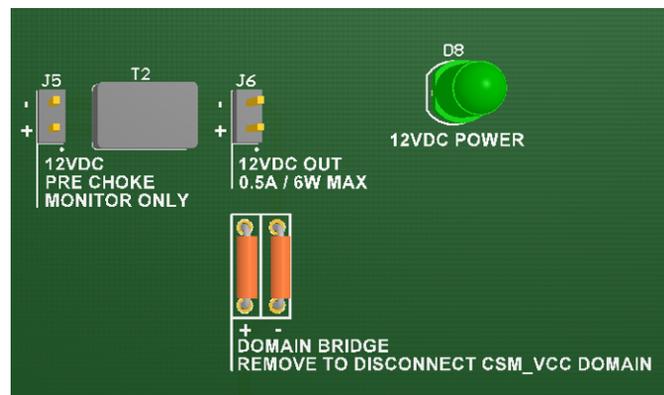

Figure 53. PSM-12VDCTO3.3VDC Monitor Posts

8   Getting Started Firmware and Software

This TI design contains target device firmware for the MSP430FR2633 MCUs used in this design and the host software components. The software download is organized into the following directories:

- Firmware
- DesignCenterWorkspace
- LogDecoder

To program and communicate with the MSP430FR2633 on the CSM-MUTUAL and CSM-SELF panels, a CAPTIVATE-PGMR module is required. The CAPTIVATE-PGMR module can be obtained as a part of the CapTIvate MCU development kit, at http://www.ti.com/tool/msp-capt-fr2633. The kit provides spy-bi-wire programming and energy monitoring through an onboard eZ-FET and high-speed serial communications through the on-board HID Bridge.

8.1   Firmware

The firmware directory contains the project source code, pre-compiled TI-TXT images, and *.projectspec project definition files for importing the CSM-SELF and CSM-MUTUAL projects into Code Composer Studio™ (CCS). Each capacitive-sensing module (CSM) has its own CCS .projectspec and output TI-TXT binary image. The common source code elements are shared between the two modules, while the source code elements that differ are stored individually for each module. The CCS .projectspec pulls in the correct files for the project of each module and sets the compiler and linker. The TI-TXT images can be used to program a CSM using the MSP430 flasher utility.

8.1.1   Evaluating the Firmware With CCS

To evaluate the firmware projects for the CSM-MUTUAL or CSM-SELF module, download the latest version of CCS at http://www.ti.com/tool/ccstudio. Import the CCS .projectspec corresponding to the module of interest from the /firmware/CCS directory in the software download. For instructions on how to wire the CAPTIVATE-PGMR to the CSM-MUTUAL or CSM-SELF modules for programming, see the Section 7.

8.1.2   Programming Images With MSP430 Flasher

The pre-compiled images for the CSM-MUTUAL and CSM-SELF modules are in the /firmware/img directory of the software download. The MSP430 flasher tool is available at http://www.ti.com/tool/msp430-flasher. Using this tool is the easiest way to program a module and requires no compiler, linker, or debug application.

For instructions on how to wire the CAPTIVATE-PGMR to the CSM-MUTUAL or CSM-SELF modules for programming, see the Section 7.

8.1.3   Selecting What Data to Output on the Serial Interface

There are several configuration options available in firmware to control the data that is sent over the serial interface from the MSP430FR2633 to the CapTIvate design center.

There are three data packets that can be enabled:

- Sensor data packets (disabled by default for efficiency)
- Element data packets (disabled by default for efficiency)
- General purpose data packets (disabled by default for efficiency),

The general purpose data packets may be configured to send one of the following:

- Full data set for one element (raw count at all four frequency taps, filtered count, LTA, and threshold)
- Log data (periodic streaming of the device log contained in FRAM, with information about errors and touch events)

Sensor and element data packets may be enabled in the CapTIvate design center under the controller customizer. Enabling these packets can increase the response time, as additional time is required for transmitting the data from each element back to the host.

General-purpose data packets are compile-time controlled in the csm.h header file. To disable any general purpose communications, set the CSM_GPDATA_MODE definition to CSM_GPDATA_IS_OFF (this is the default configuration). To configure general purpose communications for streaming detailed data for a single element, set the CSM_GPDATA_MODE definition to CSM_GPDATA_IS_NOISE_TEST_DATA. To configure it for periodically transmitting the device log, set it to CSM_GPDATA_IS_LOG. The CapTIvate design center and log decoder can then be used capture the log and decode it.

8.2 CapTIvate Design Center Workspace and Projects

The CapTIvate design center is a graphical configuration and realtime-tuning application for developing with the CapTIvate software library. It allows for easy adjustment of the tuning parameters associated with each capacitive sensing module. It also allows for visualization and logging of sensor data. The DesignCenterWorkspace directory is a CapTIvate design center workspace that contains two projects, one for each CSM:

- TIDM-CAPTOUCHEMCREF-CSMMUTUAL for the CSM-MUTUAL module
- TIDM-CAPTOUCHEMCREF-CSMSELF for the CSM-SELF module

To open a project, perform the following steps:

1. Download the latest CapTIvate design center by going to http://www.ti.com/tool/mspcaptdsnctr. The projects created for this TI Design used version 1.10.00.00 of the CapTIvate design center.
2. Run the CapTIvate design center.
3. Change the workspace to the DesignCenterWorkspace directory in the software download for this TI design.
4. Open the project of interest (TIDM-CAPTOUCHEMCREF-CSMMUTUAL or TIDM-CAPTOUCHEMCREF-CSMSELF).

8.3 Log Decoder

The /LogDecoder directory in the software download contains a python script for decoding log messages from either CSM into a plaintext comma-separated-value (CSV) file. Log messages provide detailed information about events that occurred on a CSM during runtime. They can be streamed from the CSM, captured to a file by the CapTIvate design center, and decoded by the log decoder.

The log feature is useful when performing intense transient testing (such as EFT and ESD). In these tests, having auxiliary equipment connected to the device under test is often not ideal because it can affect the test results. The log decoder uses the on-chip FRAM memory on the MSP430FR2633 to store event data, such as when a touch is detected, if a device reset occurs, or if a device error occurs (such as a memory error or I^2C bus error). The log is always running whenever the CSM is powered. After running an EFT or ESD test, the log can be read from the device with the CapTIvate design center, and decoded using the log decoder to determine whether any false detects, undesired resets, or other errors occurred during the test. All log messages are timestamped with a lifetime and a runtime mark.

8.3.1 Log Messages

Table 11 lists the messages captured by the log module.

Table 11. Log Messages

| System ID	Msg ID	Msg
Log_mainSys	Log_resetTrigger	Device reset trigger
Log_mainSys	Log_bootComplete	None
Log_errorSys	Error_vacantMemoryAccess	None
Log_errorSys	Error_TCA95xxReadbackError	None
Log_errorSys	Error_I2CBusUnavailableError	None
Log_errorSys	Error_I2CBusSlaveNackError	None
Log_errorSys	Error_I2CBusTimeoutError	None
Log_errorSys	Error_FRAMAccessTimeError	None
Log_errorSys	Error_FRAMBitErrorDetection	None

Table 11. Log Messages (continued)

Log_errorSys	Error_FRAMUncorrectableBitError	None
Log_errorSys	Error_invalidMemoryWriteAddress	None
Log_csmSys	Log_press	Sensor, Element
Log_csmSys	Log_release	Sensor, Element

8.3.2 How to Capture and Decode Log Messages

To capture and decode log messages, do as follows:

1. Program the MSP430FR2633 with the general purpose data mode set to log (see Section 8.1.3).
2. Connect power and communications connections to the reference design and allow it to run.
3. Open the general purpose user data window in the CapTIvate design center (the icon is shown in Figure 54).
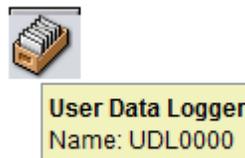
Figure 54. General Purpose User Data Log Icon in CapTIvate Design Center

4. Select Communications → Connect to enable communications.
5. Check the Log Data box.
6. dwell until data streams into the plot on the user data log (this can take up to 20 seconds, as the data log streams periodically several times per minute).
7. Uncheck the Log Data box.

   The data streamed into the user data log is captured by a file on the PC (userDataLog.csv). That log file is in the CapTIvate design center project directory.

8. Navigate to the /LogDecoder directory.
9. Run the batch file for the sensing module.

   The batch file reads the userDataLog.csv file and generates a user-readable file named eventLog.csv. All logged events appear in this CSV file in an easy-to-read format.

9 Test Method

The TIDM-CAPTOUCHEMCREF was tested to the relevant IEC 61000-4-x standards for conducted immunity (–6), fast transient/burst immunity (–4), and electrostatic discharge immunity (–2). Tests were performed internally for development and characterization, and verified at Northwest EMC.

9.1 Pass/Fail Criteria

Based on the IEC 61000-4 standard, the following capacitive-touch specific pass/fail criteria must be applied.

9.1.1 Class A

The equipment under test (EUT) operates as intended with no degradation of performance during the test or after the test. In the context of a capacitive-sensing interface, Class A requires the following:

REQ 10.1.1.1:

The EUT must not exhibit any false touch detections during or after the test.

REQ 10.1.1.2:

The EUT must always detect valid touches during and after the test.

REQ 10.1.1.3:

If the EUT contains slider or wheel sensors, the position must be reported accurately to within an acceptable limit during and after the test.

REQ 10.1.1.4:

The EUT capacitive-sensing module (CSM) must not experience a processor reset during the test. Internal non-volatile memory is used to determine if a reset occurs during a test.

9.1.2 Class B

The equipment under test (EUT) experiences a temporary loss of function or degradation of performance during the test. This degradation of performance ceases after the test, and from which the EUT recovers on its own without operator intervention. In the context of a capacitive-sensing interface, Class B requires the following:

REQ 10.1.2.1:

The EUT must not exhibit any false touch detections during or after the test.

REQ 10.1.2.2:

The EUT can miss (not detect and report) a valid touch during the test, if it recovers on its own to full functionality after the test is complete.

REQ 10.1.2.3:

The EUT capacitive-sensing module (CSM) must not experience a processor reset during the test. Internal non-volatile memory is used to determine if a reset occurs during a test.

9.1.3 Class C

The EUT experiences a loss of function or degradation of performance during the test which it does not recover from after the test stimulus is removed. The full functionality can be recovered by disconnecting and reconnecting power to the EUT. In the context of a capacitive-sensing interface, Class C requires the following:

REQ 10.1.3.1:

The EUT must not exhibit any false touch detections during or after the test.

REQ 10.1.3.2:

The EUT can miss (not detect and report) a valid touch during or after the test, if it recovers on its own to full functionality after a complete power cycle is performed by the test operator.

9.2 Test Method: Conducted Noise Immunity

Conducted RF noise immunity (CNI) is evaluated per the IEC 61000-4-6 standard. The test setup shall be compliant to the guidelines provided in the standard.

Three separate tests must be performed for conducted immunity:

- Class B verification with the standard frequency sweep as specified to ensure that no false detects occur for any sensor due to the noise
- Class A verification for a single button (a finger probe must be attached to the button before the test and the button must remain in detect for the test to ensure that valid touches can be detected in the presence of noise throughout the frequency range. If the button exits detect, the test is a failure.)
- Class A verification of the functionality (all sensors) of the entire panel while at specific frequencies that are most susceptible to conducted noise (At each frequency, a finger probe must be used to contact each button and the slider to verify that the sensor responds as expected.)

Table 12 details common test stress levels. TI must indicate the desired stress level for a test to the test facility.

Table 12. Common Test Stress Levels

IEC 61000-4-6 Test Level	RMS Open Circuit Test Voltage (V)	RMS Open Circuit Test Voltage (dBμV)	P-P Open Circuit Test Voltage (V)	P-P Open Circuit Test Voltage [AM] (V)	Calibration Level (dBμV)
1	1	120	2.82	5.08	104.4
2	3	129.5	8.46	15.24	113.9
X[6]	6	135.6	16.9	30.5	120
3	10	140	28.2	50.8	124.4
X[15]	15	143.5	42.3	76.2	127.9
X[20]	20	146	56.4	101.6	120.4

For conducted-immunity tests 1 and 2, a frequency sweep must be performed across the range requested by the IEC standard: 150-kHz to 80-MHz amplitude modulated at 80% depth on a 1-kHz carrier. The IEC specification calls for 1% steps across this range, with a dwell time of 1 second at each frequency.

9.3 Test Method: Electrical Fast Transient and Burst

Electrical fast transient and burst (EFT/B) immunity is evaluated per the IEC 61000-4-4 standard. The test setup must be compliant to the guidelines provided in the standard. The EUT must pass EFT/B testing with Class B performance. Table 13 details common stress levels tested.

Table 13. Common Stress Methods

IEC 61000-4-4 Test Level	Power Port Peak Voltage (V)	Repetition Frequency
1	500	5 kHz/100 kHz
2	1000	5 kHz/100 kHz
3	2000	5 kHz/100 kHz
4	4000	5 kHz/100 kHz

L, N, and L+N coupling modes must be tested, with + and – transients applied to each coupling at the specified stress level.

The status LEDs of the EUT must be used in combination with the internal event log to determine whether the EUT passed or failed the test. Because this is a Class-B test, the detection latch LED (amber) and the fault LED (red) must never illuminate during the test. In addition, the test event log must be read out of the EUT. The log must indicate that no undesired errors occurred, such as an IC reset or a false detection.

9.4   Test Method: Electrostatic Discharge

Electrostatic discharge (ESD) immunity is evaluated per the IEC 61000-4-2 standard. The test setup must be compliant to the guidelines provided in the standard. The EUT must pass ESD testing with Class B performance.

The status LEDs of the EUT must be used in combination with the internal event log to determine whether the EUT passed or failed the test. Because this is a Class-B test, the detection latch LED (amber) and the fault LED (red) must never light during the test. In addition, the test event log must be read from the EUT and it must indicate that no undesired errors occurred, such as an IC reset or a false detection.

9.5   Artificial Finger

An artificial finger was used to simulate touches during testing. The use of an artificial finger probe improves repeatability and safety during testing. The finger probe use was constructed to the CISPR standards: terminated to the reference ground using a 220-pF ±20% capacitor in series with a resistor of 510 Ω ±10%. The finger element consists of copper tape mounted to polycarbonate. For more information, see Figure 55.

Figure 55. Artificial Finger Probe

10   Test Data

The test data section contains characterization and test results. Power-supply characteristics are discussed and IEC 61000-4-x test results are shown with data captures where appropriate. Table 14 summarizes the IEC 61000-4-x performance of various combinations.

Table 14. IEC 61000-4-x Performance Summary

Configuration	IEC61000-4-6 Conducted Noise Immunity, Class A	IEC61000-4-6 Conducted Noise Immunity, Class B	IEC61000-4-4 EFT/B Immunity, Class B	IEC61000-4-2 ESD Immunity, Class B
Direct Power; CSM-MUTUAL	3 V_{rms}	10 V_{rms}	Not Tested	Not Tested
PSM-12VDCTO3.3VDC; CSM-MUTUAL	3 V_{rms}	10 V_{rms}	±4 kV	Not Tested
PSM-12VDCTO3.3VDC; CSM-MUTUAL; CMC	6 V_{rms}	10 V_{rms}	Not Tested	Not Tested
PSM-UACTO3.3VDC; CSM-MUTUAL	6 V_{rms}	10 V_{rms}	±4 kV	±8-kV contact; ±15-kV air
PSM-UACTO3.3VDC; CSM-MUTUAL; CMC	10 V_{rms}	20 V_{rms}	Not Tested	Not Tested
PSM-12VDCTO3.3VDC; CSM-SELF	3 V_{rms}	10 V_{rms}	±4 kV	Not Tested
PSM-12VDCTO3.3VDC; CSM- SELF; CMC	10 V_{rms}	10 V_{rms}	Not Tested	Not Tested
PSM-UACTO3.3VDC; CSM- SELF	10 V_{rms}	10 V_{rms}	±4 kV	±8-kV contact; ±15-kV air
PSM-UACTO3.3VDC; CSM- SELF; CMC	10 V_{rms}	20 V_{rms}	Not Tested	Not Tested

10.1 *PSM-UACTO3.3VDC Power Ramp*

Figure 56 shows a typical power ramp of the PSM-UACTO3.3VDC power supply. The dark-blue trace (1) is the 12-VDC rail, and the light-blue trace (2) is the 3.3-VDC rail. It takes about 11.2 ms for the 3.3-V rail to stabilize. The 3.3-V rail is available before the 12-V rail finishes ramping. Full ramp of the 12-V rail takes 40 to 50 ms during a cold start.
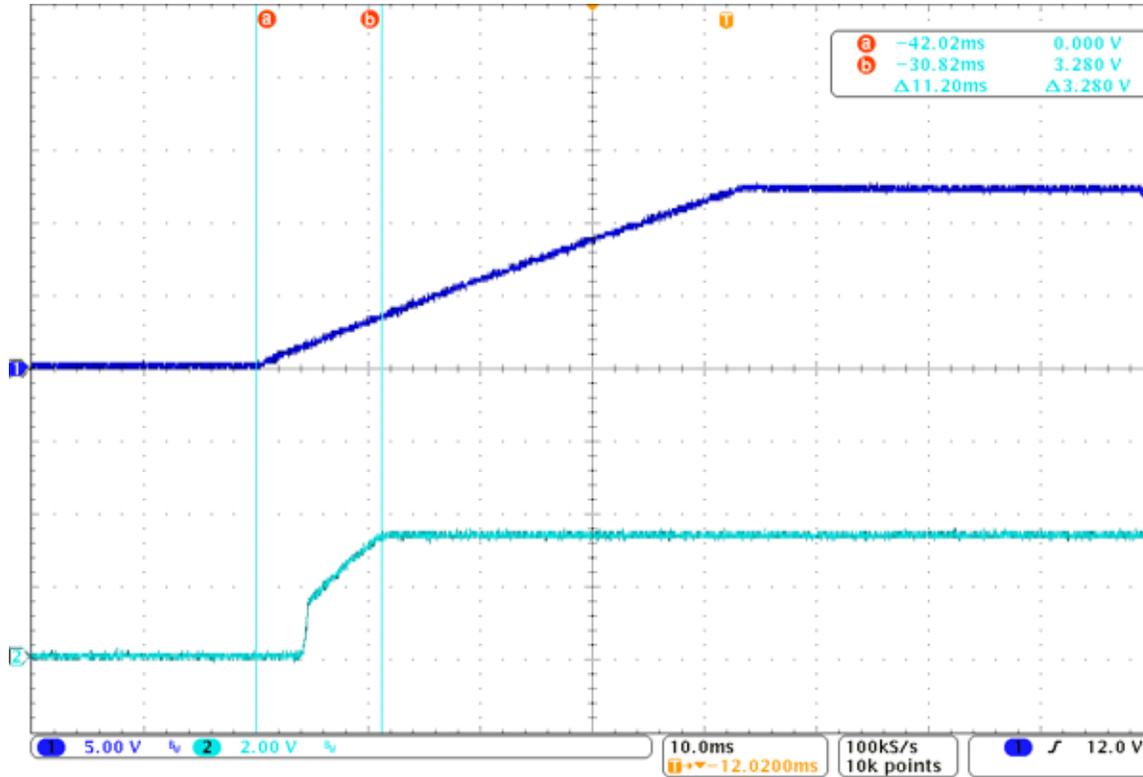
Figure 56. UAC Power Ramp

10.2 *Conducted-Noise Immunity (IEC 61000-4-6)*

The IEC 61000-4-6 test specification was used to evaluate immunity to conducted disturbances. Two types of test data are shown: frequency sweeps and frequency dwells. Frequency sweeps are tests where an response of an electrode was measured while the noise frequency was swept. The response is tested with and without a simulated touch present. Frequency dwells are tests where an response of an electrode is measured while the noise frequency is held constant at a given point. The response to several sequential touches is tested to compare the touched and untouched states. For more information, see Figure 57.
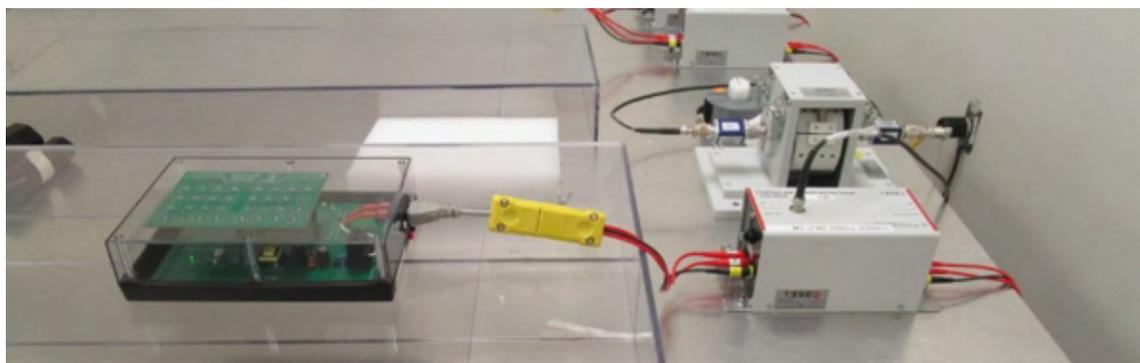
Figure 57. Conducted-Noise Test

Data plots in this section has two halves. Processed data is shown first, including the filtered count, long-term average (LTA), and touch threshold. The raw data from each frequency tap is shown to provide insight into the inputs to the signal-processing chain. If oversampling is applied in a data set, the raw data represents the last sample of all 4 frequencies.

10.2.1 CSM-MUTUAL

The CSM-MUTUAL conducted-noise testing primarily stresses the mutual-electrode geometry, the frequency-hopping oscillator, and the multi-frequency processing (MFP) algorithm. The test data indicates the importance of designing a good power supply for noise immunity. The CSM-MUTUAL design performs better with the PSM-UACTO3.3VDC supply than with the PSM-12VDCTO3.3VDC supply. In both cases, the design performed better with the common-mode choke installed.

10.2.1.1 Direct Power

Figure 58 shows the direct power case (CSM-MUTUAL only, with noise coupled directly onto the 3.3-V supply). Four data sets are shown: a no-touch sweep (Class B), a touched sweep (Class A), and two dwell tests.

The no-touch sweep in Figure 58 shows that the processed data has no glitches during the test. The filtered count remains consistent throughout the test with no unexpected fluctuations. Looking at the raw data (F0-F3), the fundamental conversion frequencies and their harmonics are identifiable. When the noise frequency overlaps with a conversion frequency or one of its harmonics, the measurements at that conversion frequency exhibit corrupted, unusable data. The other frequencies remain undisturbed. The direct power test case is a passing test.
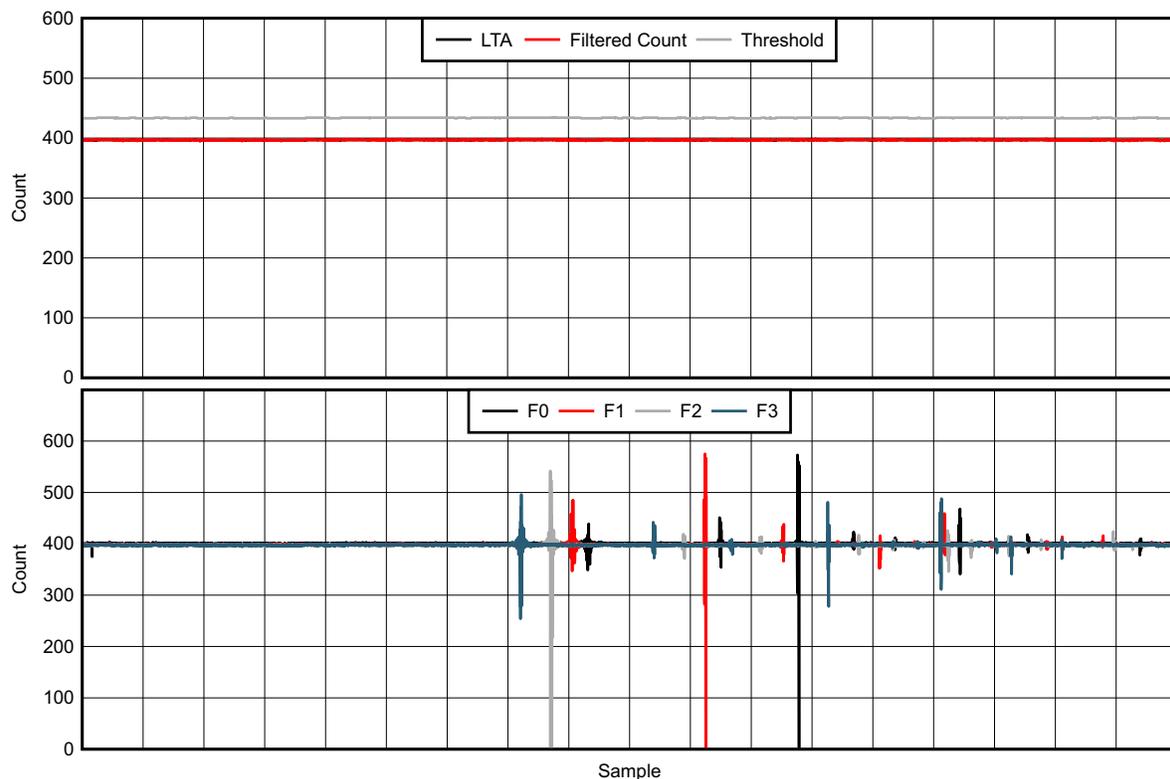
Figure 58. CSM-MUTUAL Direct Power; 3 V$_{rms}$; No Touch Sweep

The touched sweep in Figure 59 shows that the noise level increases when a button is touched. This effect is most evident in the raw data (F0 to F3). The filtered count has minor glitches that do not affect sensitivity and overall performance. The noise amplitude increases and the noise bandwidth expands. The frequency range at which a particular conversion frequency is susceptible to noise is referred to as the susceptibility band. For frequency hopping to be most effective, the susceptibility band must be as small as possible. The best methods to reduce the susceptibility band and improve overall noise immunity a to use filter capacitors on Rx lines, keep the Rx lines small and well-shielded, and use a good power supply. This is a passing test.
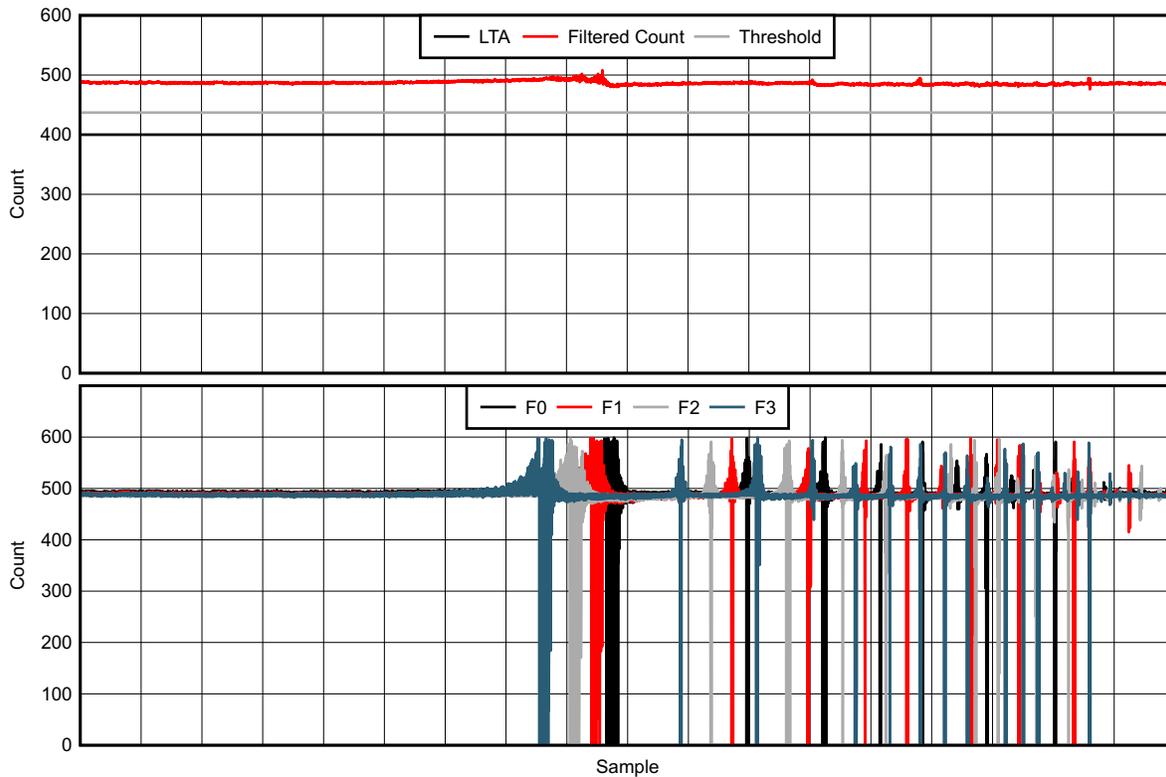
Figure 59. CSM-MUTUAL Direct Power; 3 V$_{rms}$; Touched Sweep

The 4-MHz dwell point was chosen because it directly overlaps with the primary, base-conversion frequency of 4 MHz. Figure 60 shows two sequential touches. That noise is present only in the raw data at F0; F1 to F3 are clean. The MFP algorithm can extract the true result. This is a passing test.
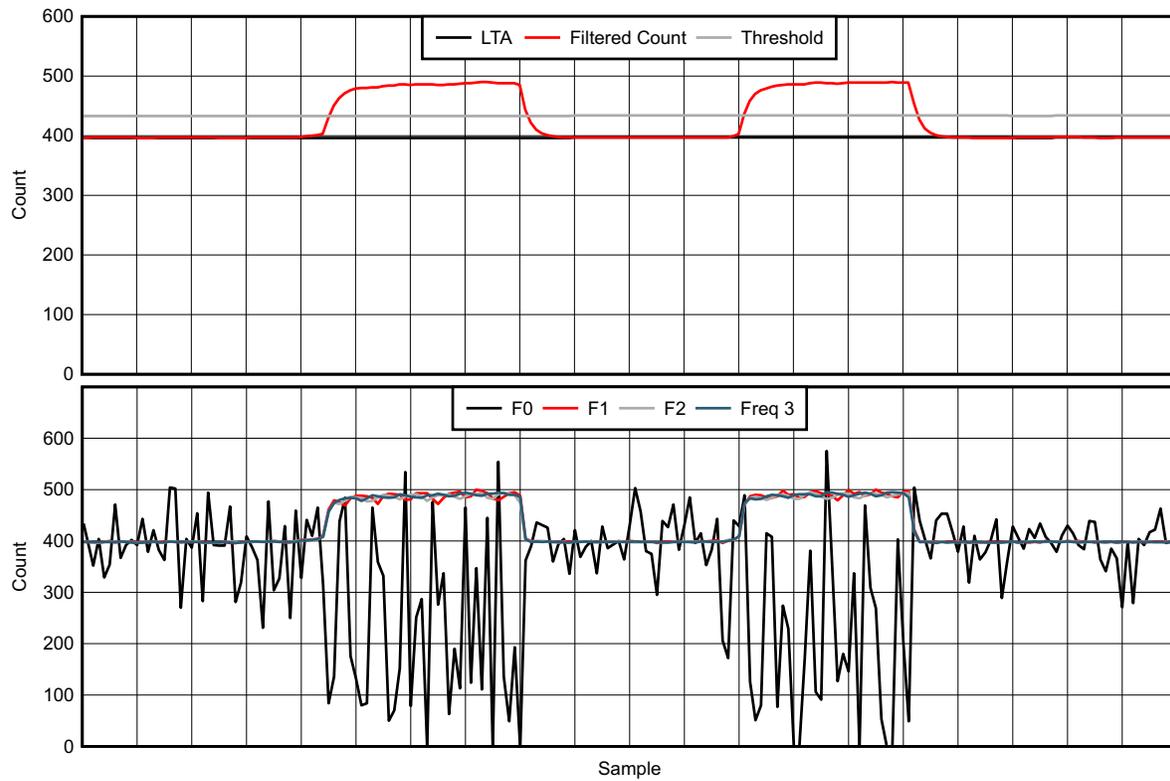
Figure 60. CSM-MUTUAL Direct Power; 3 V$_{rms}$; Dwell at 4 MHz

The 3.75-MHz dwell frequency was chosen because it is between F0 and F1 and has the most critical overlap frequency. The raw data for F0 and F1 are corrupted by noise, leading to additional jitter on the final, processed measurement. The system can detect a touch reliably with no variations in sensitivity or performance. For more information, see Figure 61.
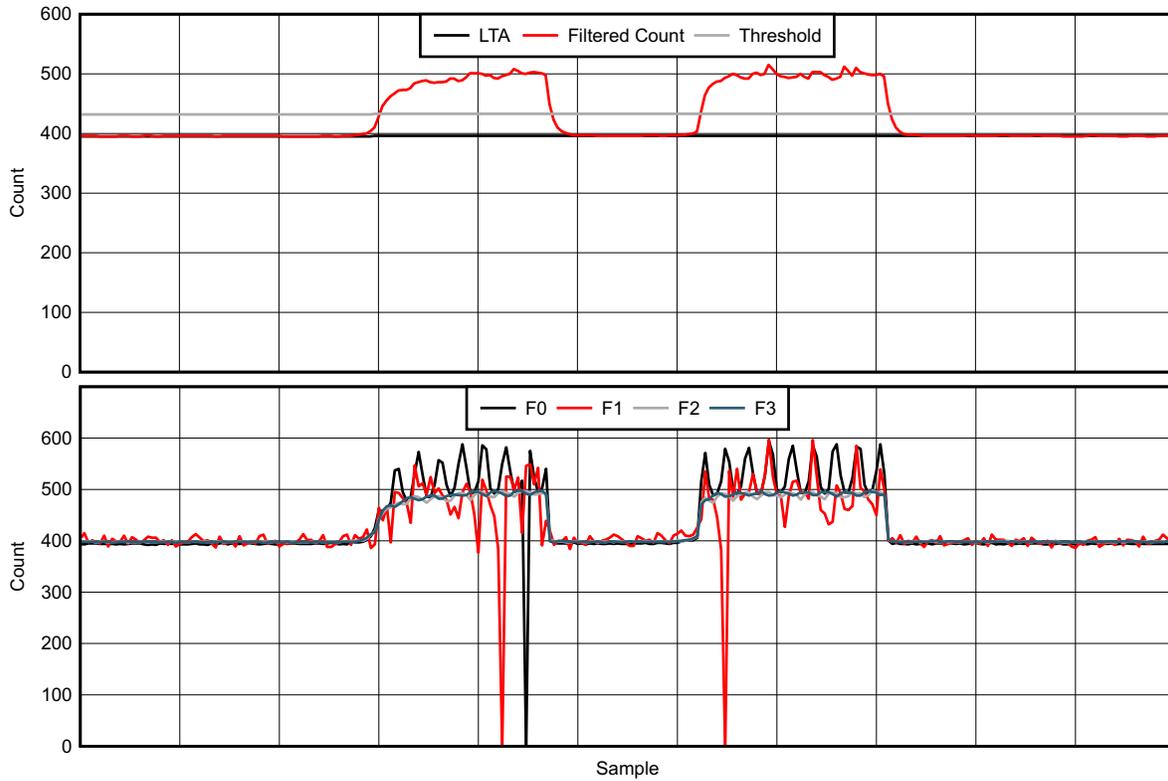
Figure 61. CSM-MUTUAL Direct Power; 3 V$_{rms}$; Dwell at 3.75 MHz

10.2.1.2 *PSM-12VDCTO3.3VDC*

This case adds the PSM-12VDCTO3.3VDC power supply. The data in Figure 62 shows that adding the linear-regulator stage in the PSM-12VDCTO3.3VDC does not improve the noise immunity of the solution in any significant way. The raw data is affected in the same way and the processed data resolves and reports the touch status correctly. This effect is an example of the nature of common-mode noise. Because noise currents flow through the ground connection, adding the 12-VDC to 3.3-VDC regulator failed to improve the immunity of the solution. A method to block common-mode currents from flowing into the CSM is required.
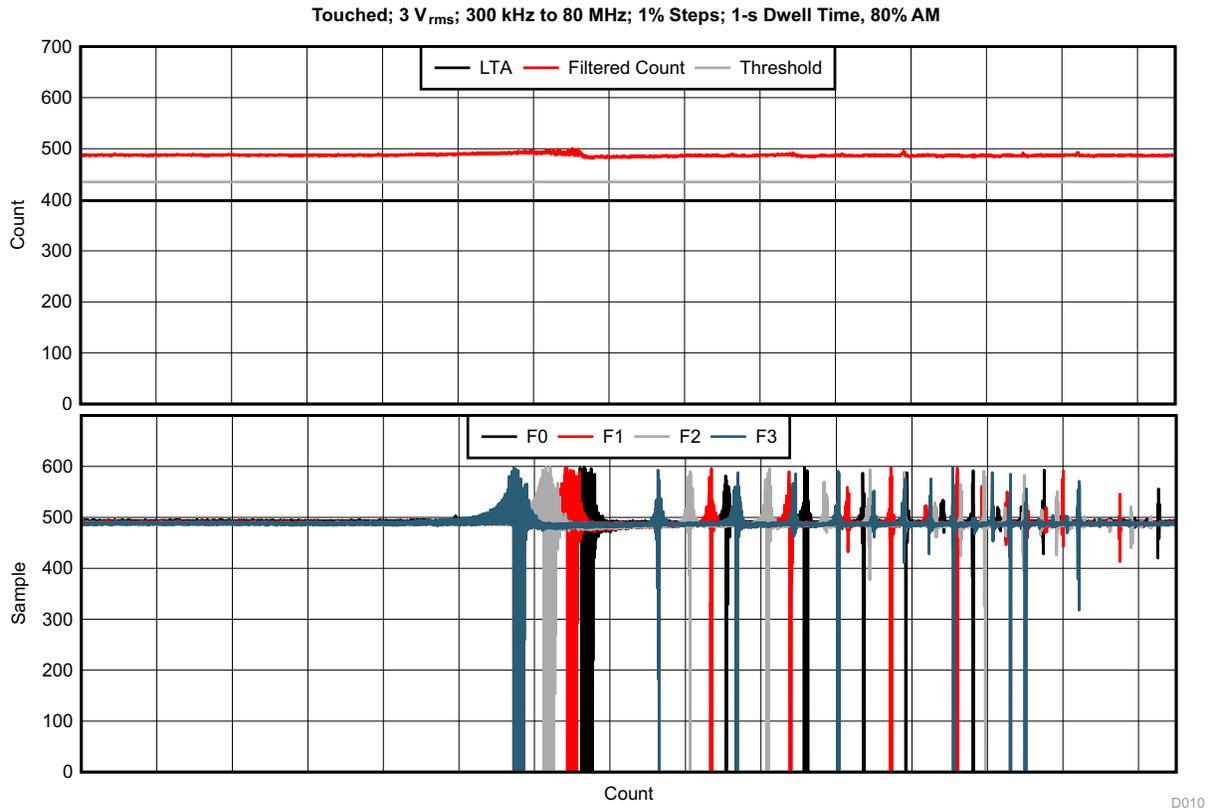
Figure 62. CSM-MUTUAL PSM-12VDCTO3.3VDC; 3 V$_{rms}$; Touched Sweep

As shown in Figure 63, adding the common-mode choke impacted the performance of the solution. The susceptibility band decreased when compared with the same supply and no common-mode choke (see Figure 62). This improvement in the raw data improved the filtered count data, which does not show any significant disturbances and looks as if no noise is present throughout the frequency band.
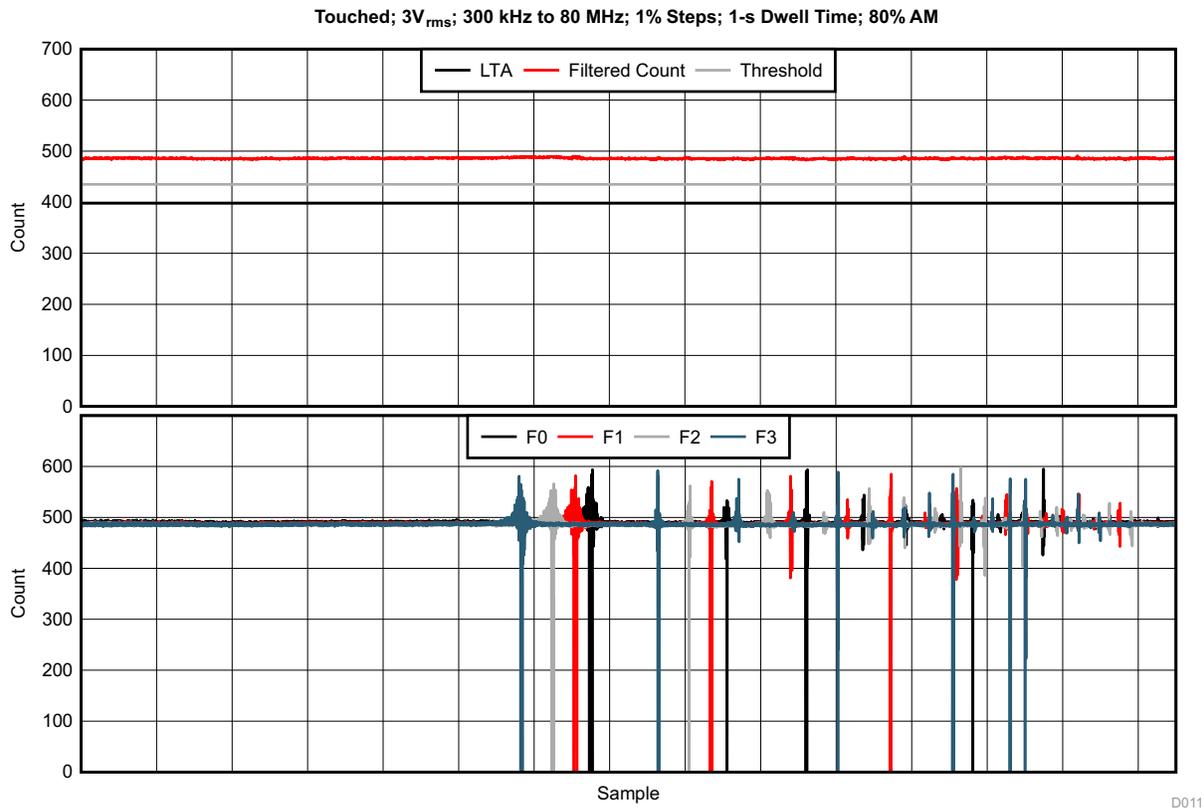
Figure 63. CSM-MUTUAL PSM-12VDCTO3.3VDC CMC; 3 V_{rms}; Touched Sweep

Figure 64 shows improvement compared to the data in Figure 61. The noise on F0 and F1 is attenuated and the raw data is improved. With the common-mode choke in place, tests were also run at 6 V_{rms} and 10 V_{rms}, as in Figure 65 and Figure 66.

Two Touches; 3V_{rms} ; 3.75 MHz; 80% AM
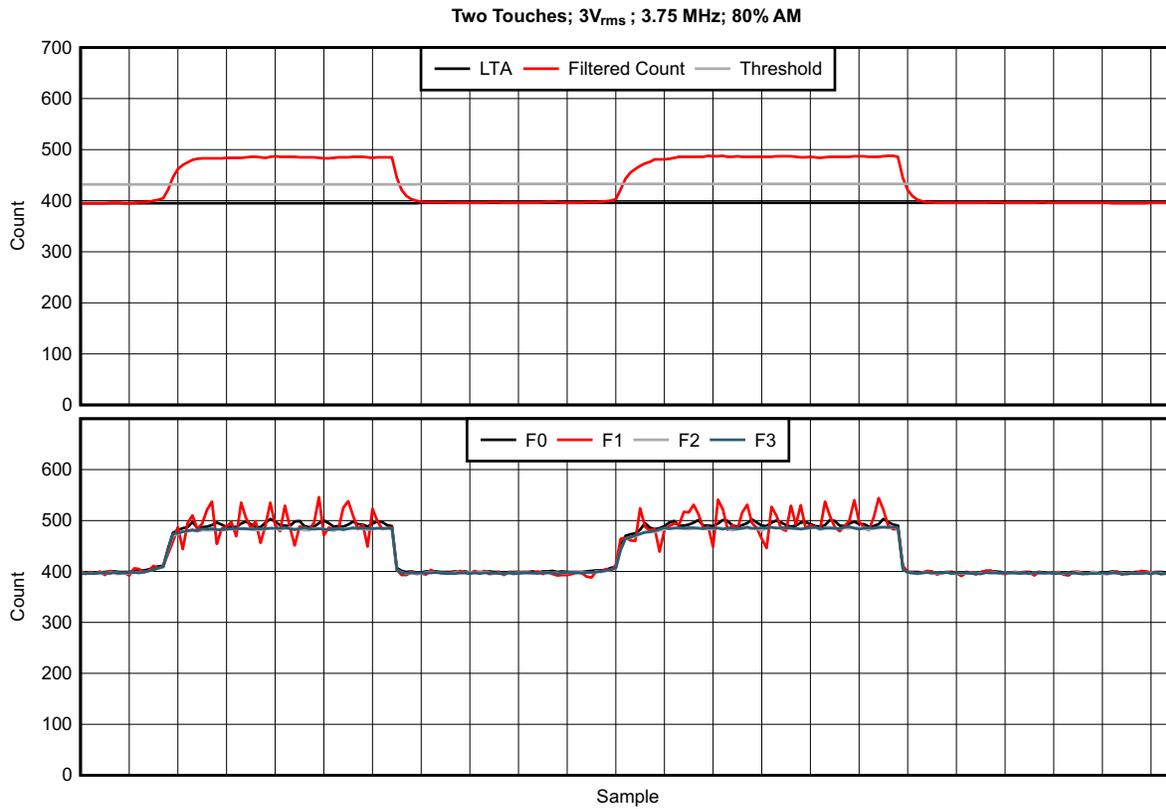
Figure 64. CSM-MUTUAL PSM-12VDCTO3.3VDC CMC; 3 V_{rms}; Dwell at 3.75 MHz

Touched; 6 V$_{rms}$; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM
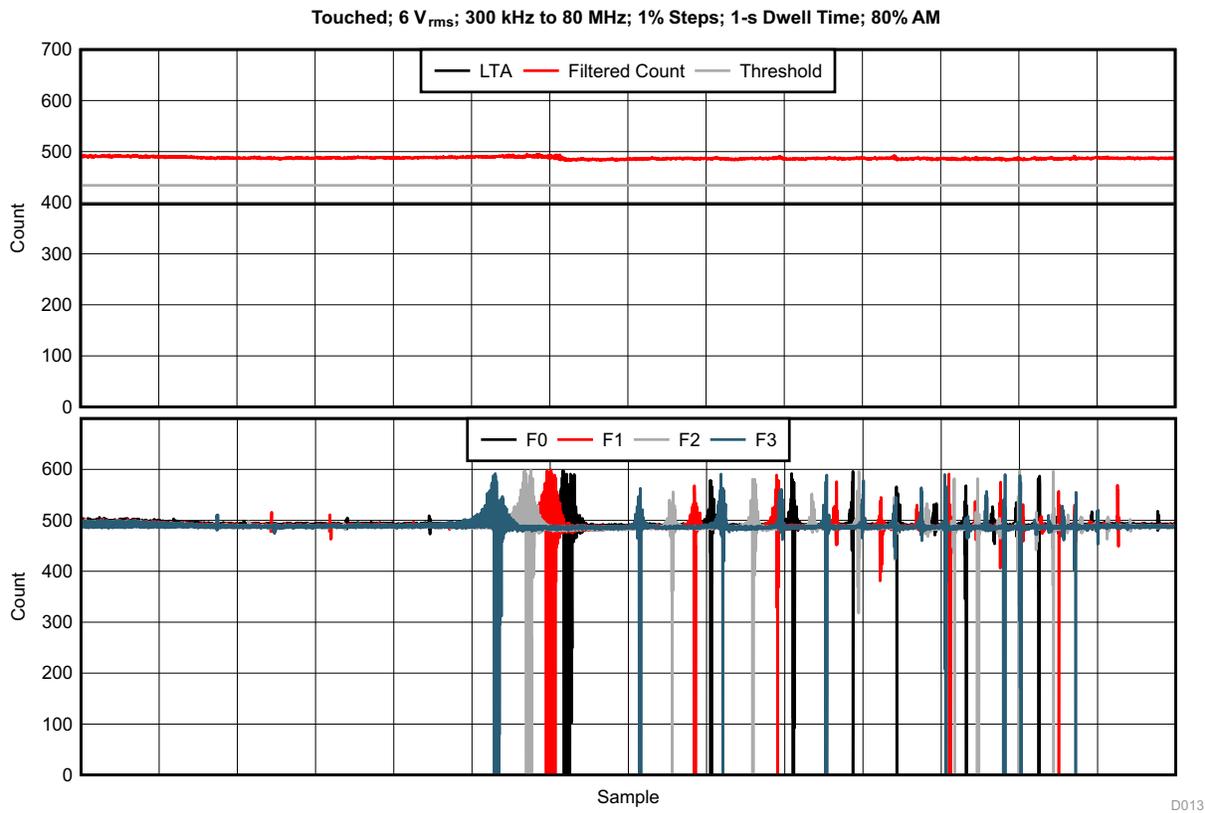
Figure 65. CSM-MUTUAL PSM-12VDCTO3.3VDC CMC; 6 V$_{rms}$; Touched Sweep

At 6 V$_{rms}$, the noise bands remained relatively narrow, and accurate touch detection was achieved.

Touched; 10-V$_{rms}$; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM
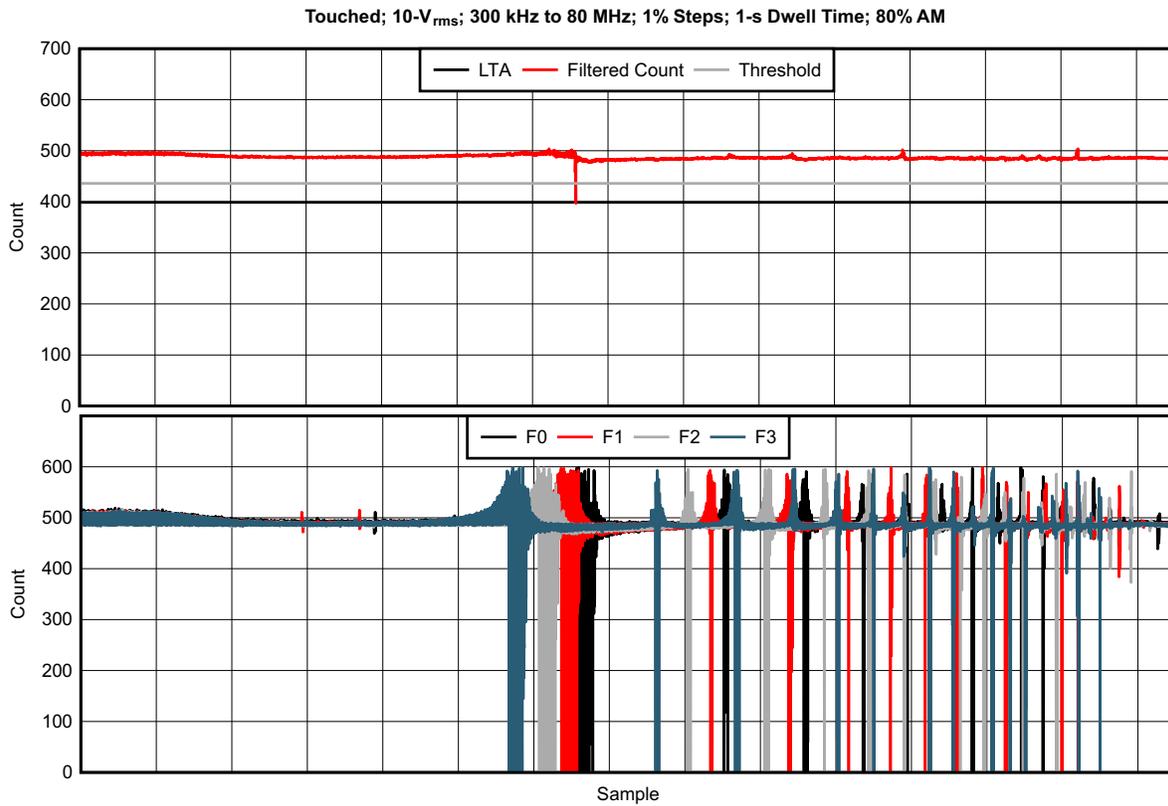
D014

Figure 66. CSM-MUTUAL PSM-12VDCTO3.3VDC CMC; 10 V$_{rms}$; Touched Sweep

At 10 V$_{rms}$, the signal shows minor variations in sensitivity and a significant corrupted measurement at the critical band between F0 and F1. This glitch qualifies this test as a failure because accurate detection was not maintained throughout the test.

10.2.1.3 *PSM-UACTO3.3VDC*

The following test case switches over from the 12-VDC supply to the universal AC supply (PSM-UACTO3.3VDC). This combination is tested without a common-mode choke populated. In the case of the universal AC supply, there is no direct connection between the CSM return and the power supply high-voltage return, because the supply is isolated by the flyback transformer and high-voltage capacitor. This lack of direct connection improves the immunity to common-mode conducted noise.

The CSM-MUTUAL with the PSM-UACTO3.3VDC performs slightly better than the PSM-12VDCTO3.3VDC and CMC configuration. The noise bands are narrow, which leads to great frequency-hopping performance as seen in Figure 67.

Touched; 3 V_{rms}; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM
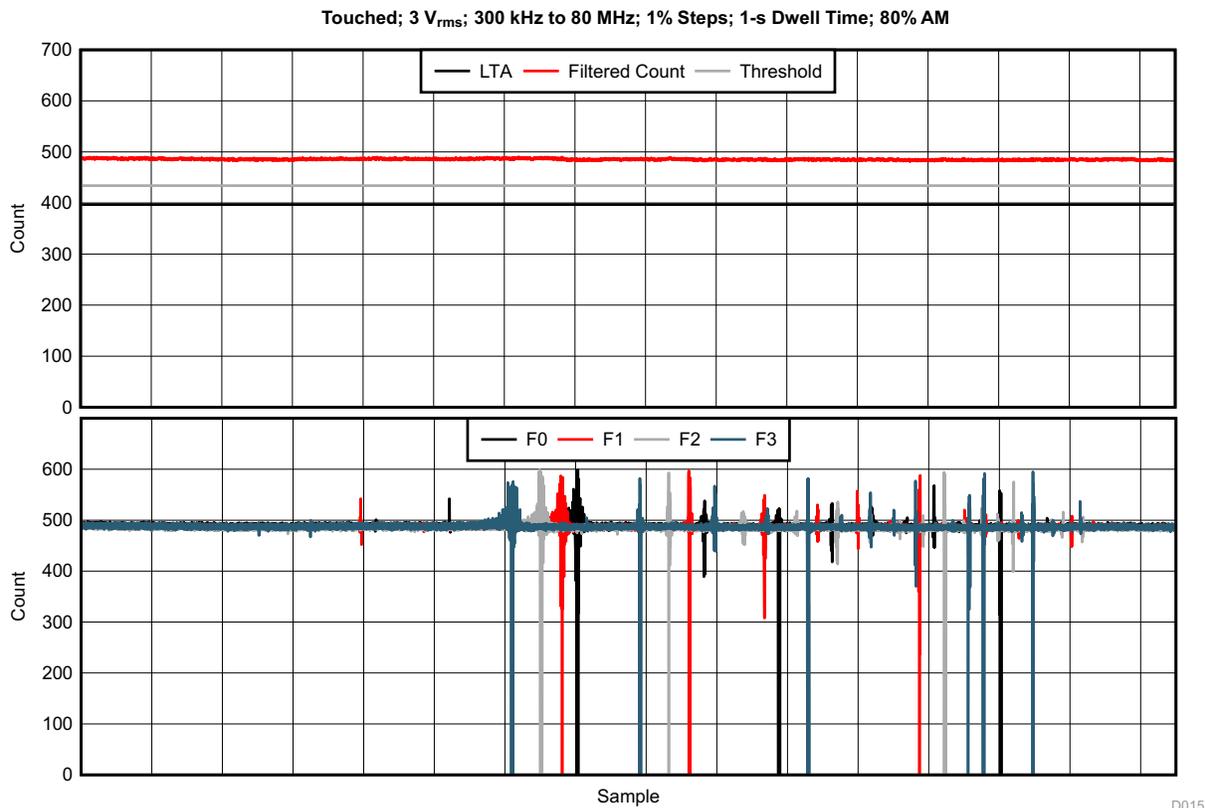
Figure 67. CSM-MUTUAL PSM-UACTO3.3VDC; 3 V_{rms}; Touched Sweep

Immunity to 6 V$_{rms}$ of common-mode noise can be achieved without a common-mode choke using the PSM-UACTO3.3VDC power supply. Figure 68 shows the response is clean.

Touched; 6 V$_{rms}$; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM
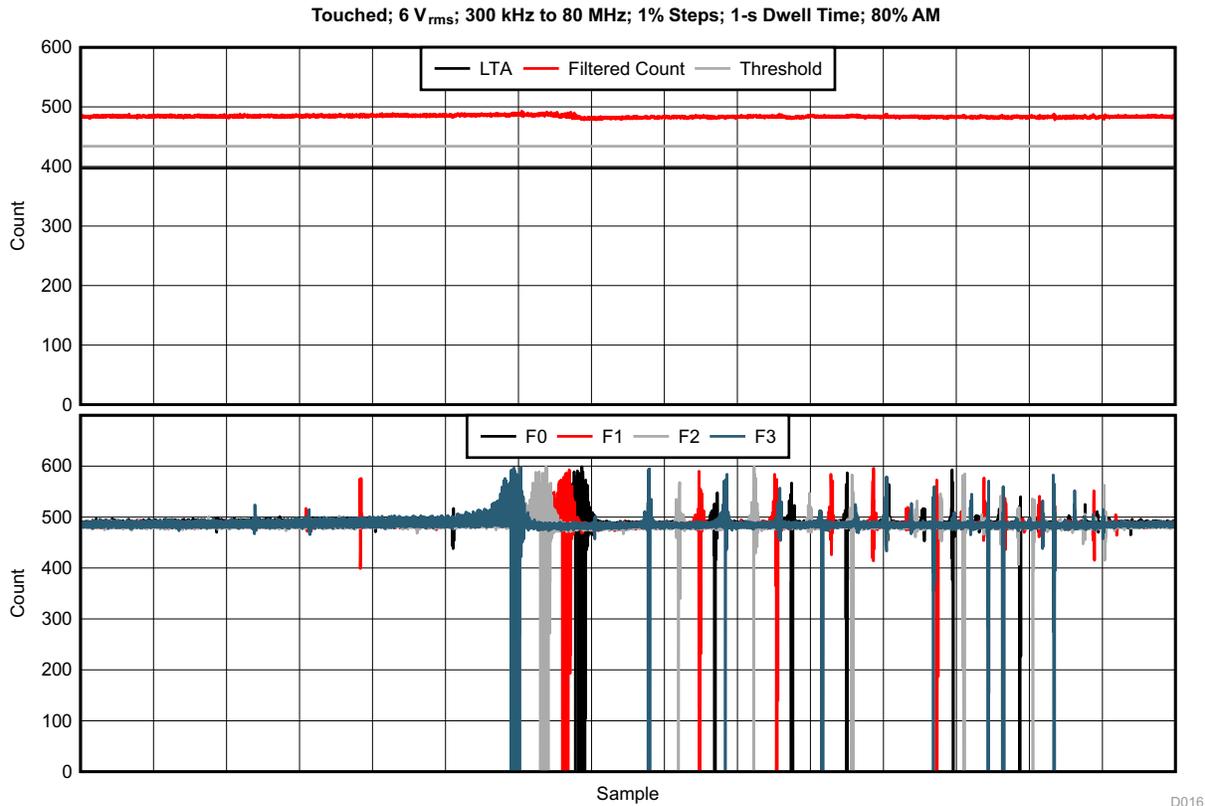
Figure 68. CSM-MUTUAL PSM-UACTO3.3VDC; 6 V$_{rms}$; Touched Sweep

10.2.1.4 PSM-UACTO3.3VDC With CMC

Adding the same common-mode choke to the PSM-UACTO3.3VDC supply provides the best noise immunity. Noise must pass through the parallel combination of stray winding capacitance in the isolation transformer and the high-voltage capacitor, after which it must pass through the common-mode choke.

Figure 69 verifies that with the best power-supply combination; the best performance is at 3 V_{rms}. The susceptibility bands are small and the filtered data is clean. Figure 69 is best contrasted with the direct supply case in Figure 59. The difference in the raw frequency data is compelling and shows the difference an isolated power supply can make when combined with a choke.

Touched; 3 V_{rms}; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM
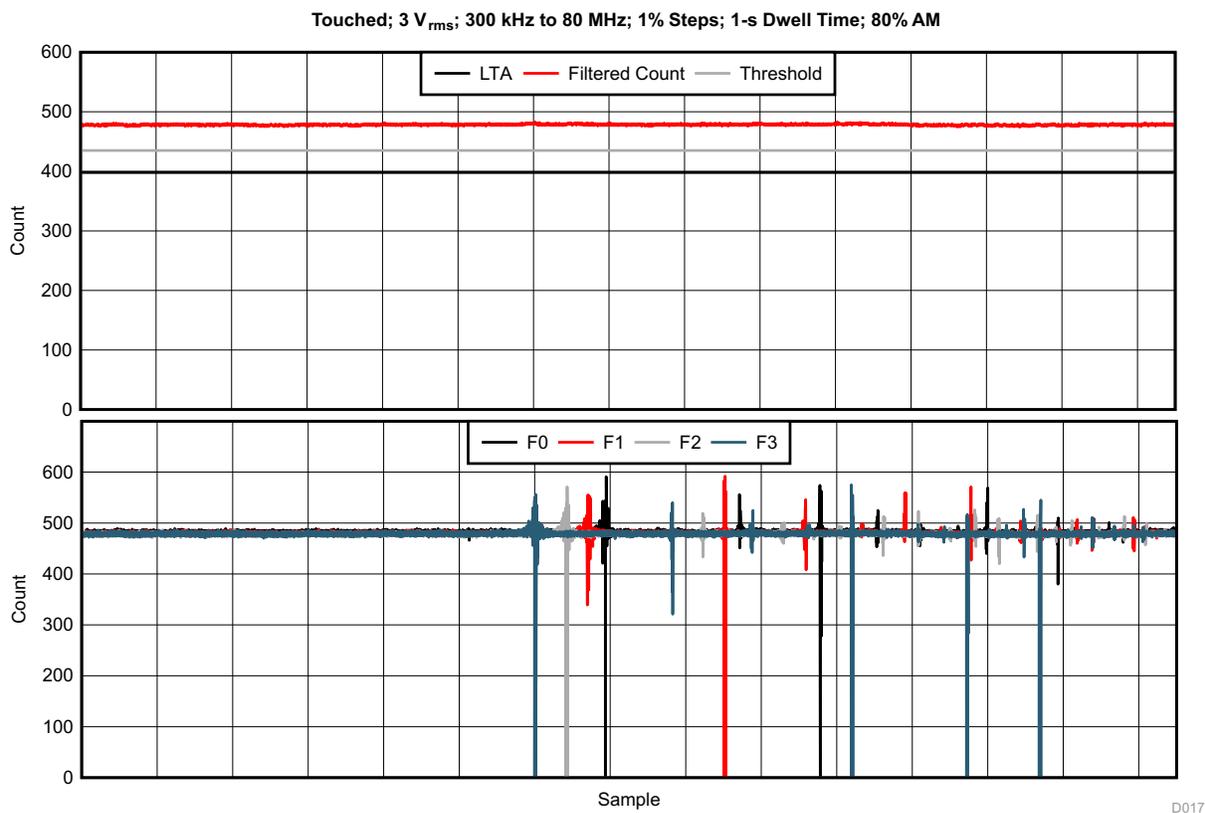
Figure 69. CSM-MUTUAL PSM-UACTO3.3VDC CMC; 3 V_{rms}; Touched Sweep

With the common-mode choke as shown in Figure 70, 10 V$_{rms}$ is also achievable. Usable processed data is obtained.

Touched; 10 V$_{rms}$; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM
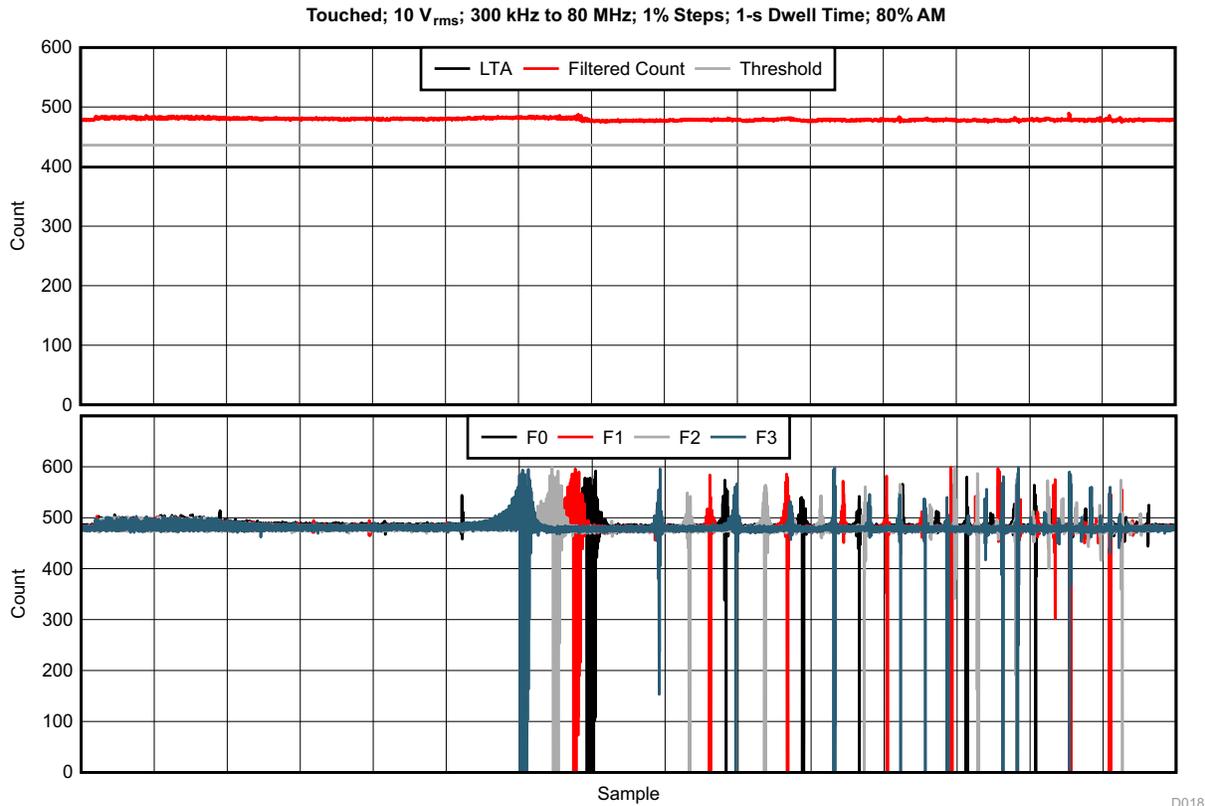
Figure 70. CSM-MUTUAL PSM-UACTO3.3VDC CMC; 10 V$_{rms}$; Touched Sweep

Figure 71 stresses this configuration even further to 15 V_{rms}. At 15 V_{rms}, the processed data shows signs of noise that can affect the application. Depending on the noise frequency, 15 V_{rms} can be achievable.

Touched; 15 V_{rms}; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM
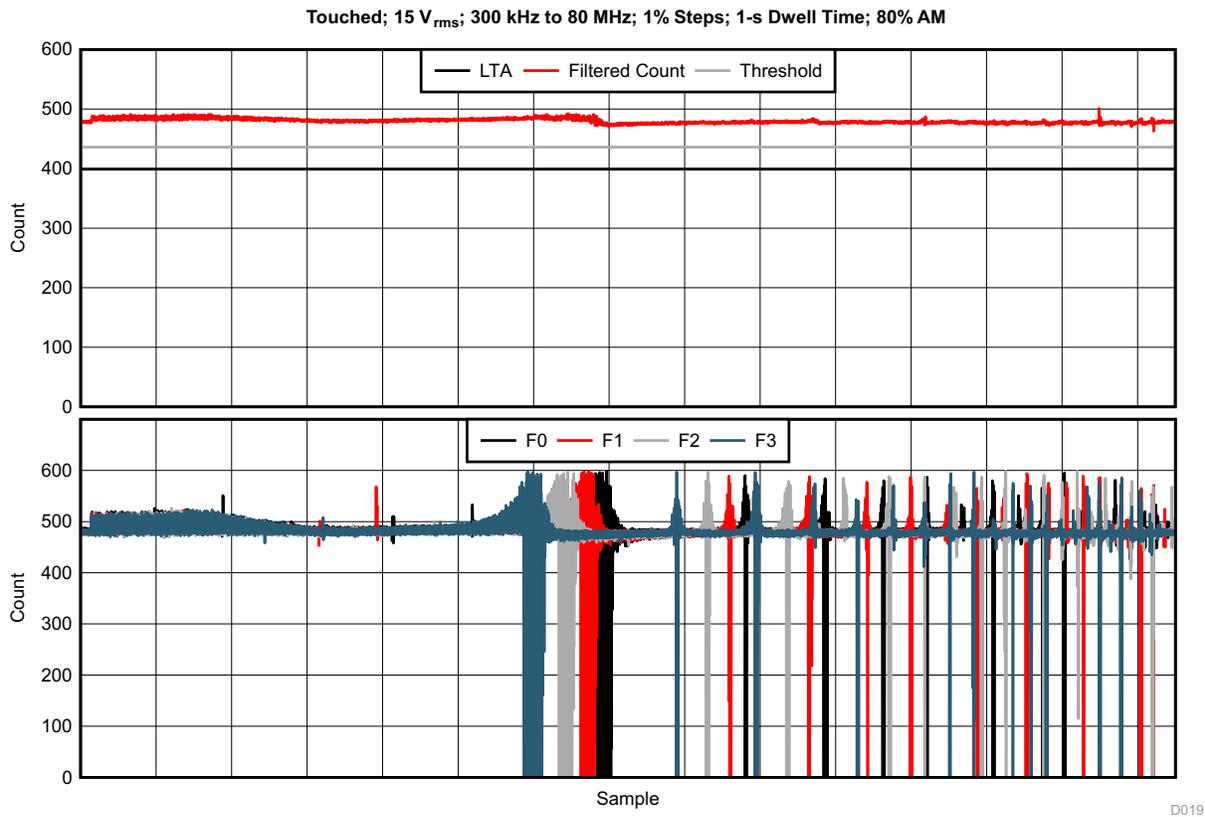
Figure 71. CSM-MUTUAL PSM-UACTO3.3VDC CMC; 15 V_{rms}; Touched Sweep

Figure 72 demonstrates that 20-V_{rms} class B immunity is achievable with the PSM-UACTO3.3VDC and CMC configuration. The processed signal has no disturbances indicating possible false detection scenarios.
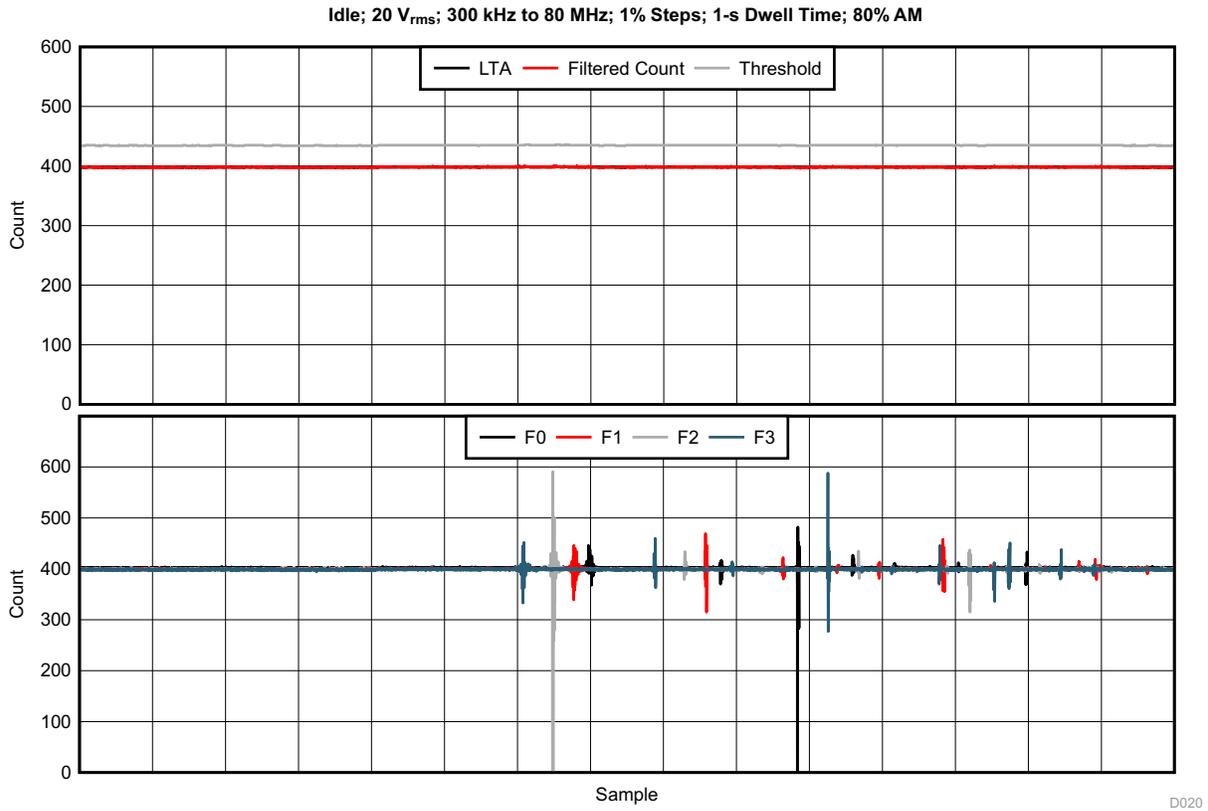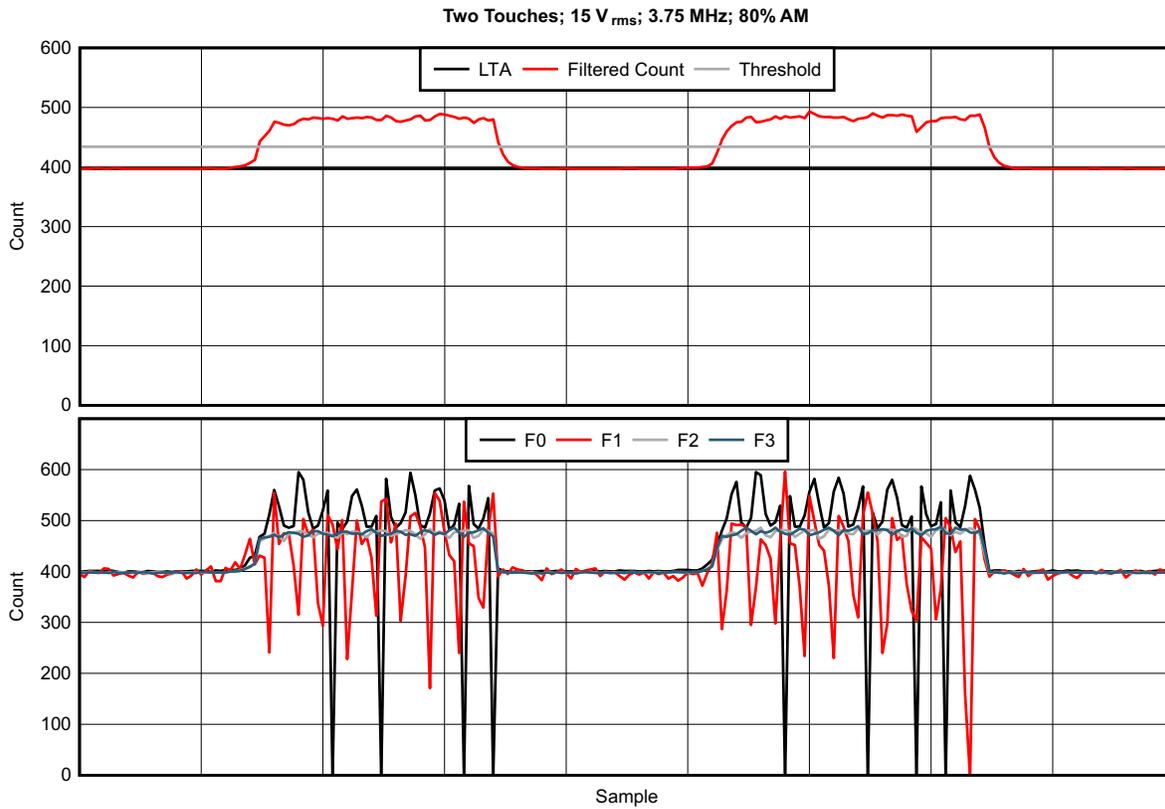

Figure 72. CSM-MUTUAL PSM-UACTO3.3VDC CMC; 20 V_{rms}; Idle Sweep

Figure 73 shows the response to two touches with 10 V$_{rms}$ of noise at the critical frequency of 3.75 MHz. Noise is present at F0 and F1, but the resolved signal is usable at this stress level.

Two Touches; 10 V$_{rms}$; 3.75 MHz; 80% AM
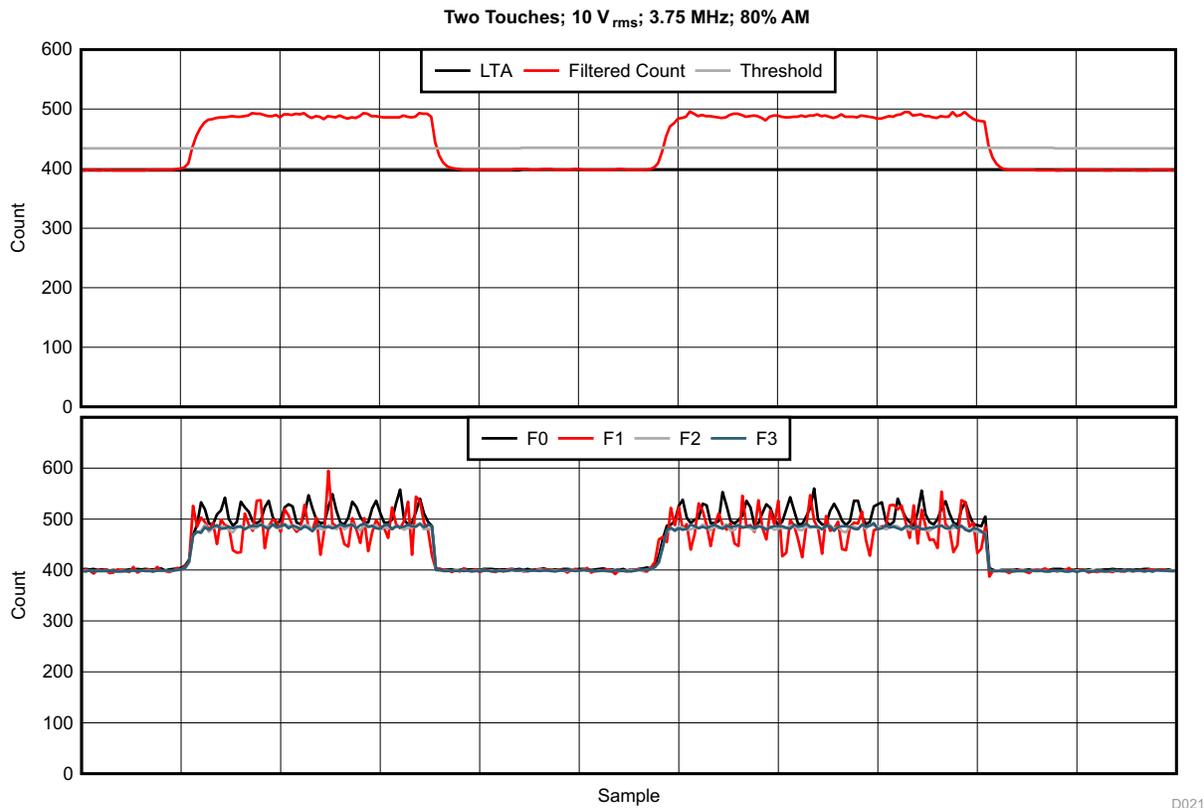
Figure 73. CSM-MUTUAL PSM-UACTO3.3VDC CMC; 10 V$_{rms}$; Dwell at 3.75 MHz

Figure 74 shows the performance of this configuration with 15 V$_{rms}$ of noise at the critical frequency of 3.75 MHz. F0 and F1 have considerable noise and the wide susceptibility bands begin to limit the performance of the frequency hopping and MFP algorithm. The processed data shows some noise.

Figure 74. CSM-MUTUAL PSM-UACTO3.3VDC CMC; 15 V$_{rms}$; Dwell at 3.75 MHz

10.2.2   CSM-SELF

The CSM-SELF conducted-noise testing primarily stresses the DTA algorithm. The self-capacitance sensors on board the CSM-SELF function in differently than the mutual-capacitance sensors on the CSM-MUTUAL. When a user is not touching a sensor, little to no noise is observable in the measurement. However, the presence of noise in the system increases the sensitivity of the measurement to touch.

Like the CSM-MUTUAL test data, this data strongly indicates the importance of designing a good power supply for noise immunity. The CSM-SELF design performs better with the PSM-UACTO3.3VDC supply than with the PSM-12VDCTO3.3VDC supply. In both cases, the design performed better with the common-mode choke installed.

10.2.2.1   *PSM-12VDCTO3.3VDC*

The first self-capacitance test cases examines the CSM-SELF with the PSM-12VDCTO3.3VDC power supply.

Figure 75 shows the response of a button on the CSM-SELF to 3 V_{rms} conducted noise. Additional sensitivity is present, particularly in the raw frequency data. The top half of Figure 75 shows the threshold-adjustment tracking. Oversampling and IIR filtering removes most of the significant periodic noise in the signal. When that component is removed, managing the increase in sensitivity with the DTA tuning is important.
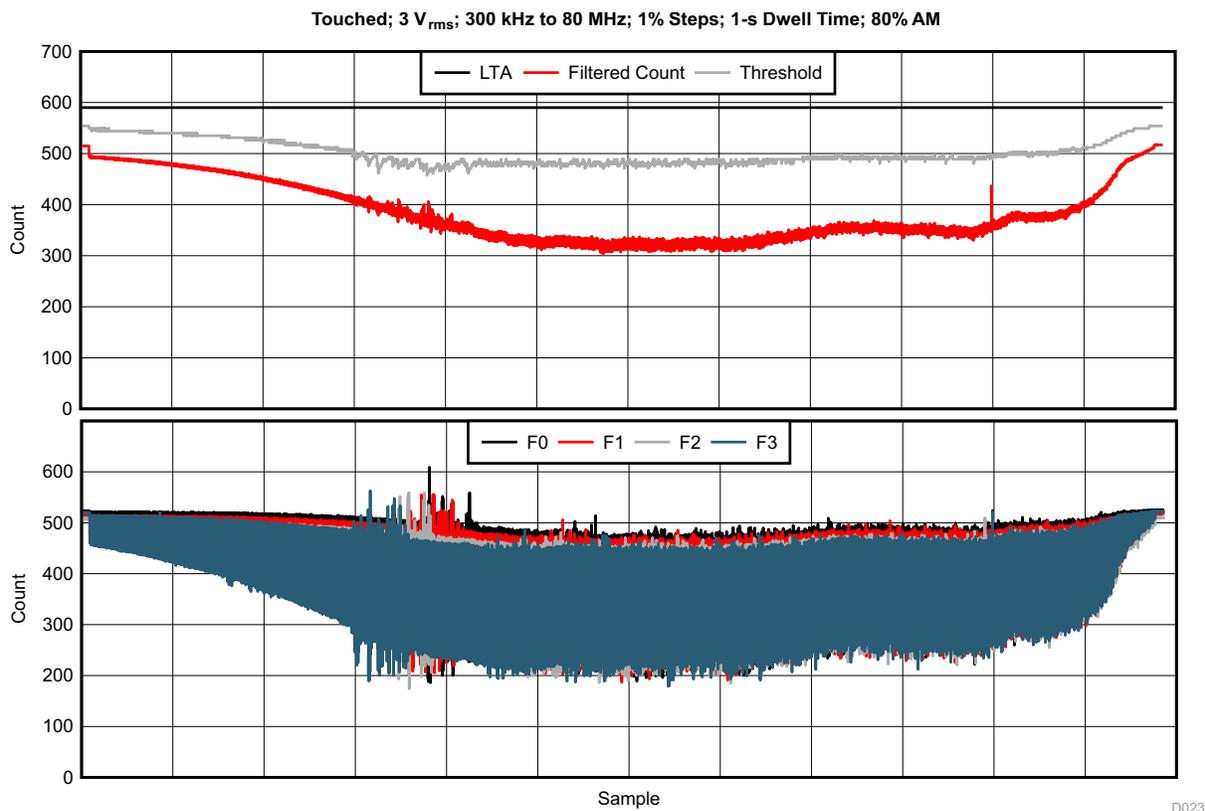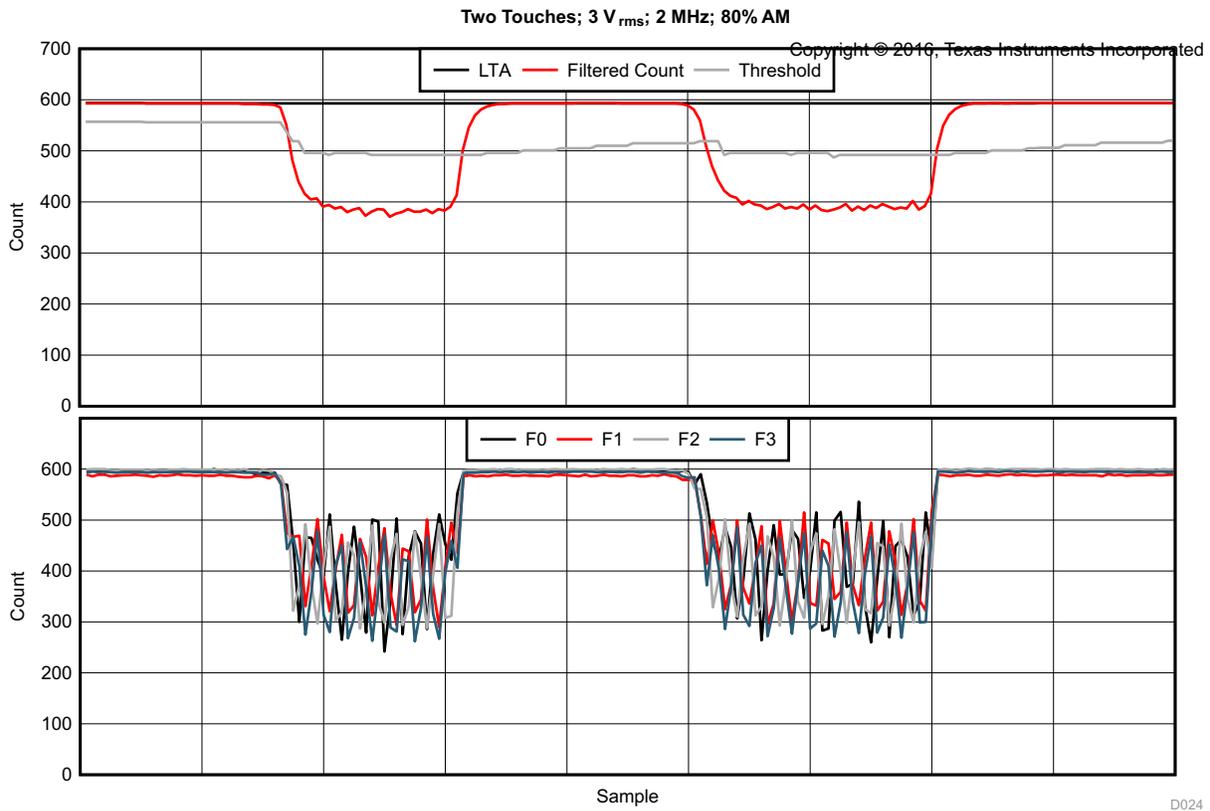

Figure 75. CSM-SELF PSM-12VDCTO3.3VDC; 3 V_{rms}; Touched Sweep

Figure 76 shows the response to two touches, with 3 V$_{rms}$ of noise at the F0 base conversion frequency of 2 MHz. The noise is invisible to the system when the touch is not present. Figure 76 shows the tracking of the DTA algorithm as it responds to the two touches. Figure 76 shows the importance of applying enough de-bounce and IIR filtering to let the DTA tracking settle.

Figure 76. CSM-SELF PSM-12VDCTO3.3VDC; 3 V$_{rms}$; Dwell at 2.0 MHz

10.2.2.2   *PSM-12VDCTO3.3VDC with CMC*

Adding the common-mode choke to the PSM-12VDCTO3.3VDC significantly attenuates the noise at 3 V_{rms}, as shown in Figure 77. The fluctuation humps in sensitivity are attributed to common-mode resonance in the EUT and test system at different frequencies.
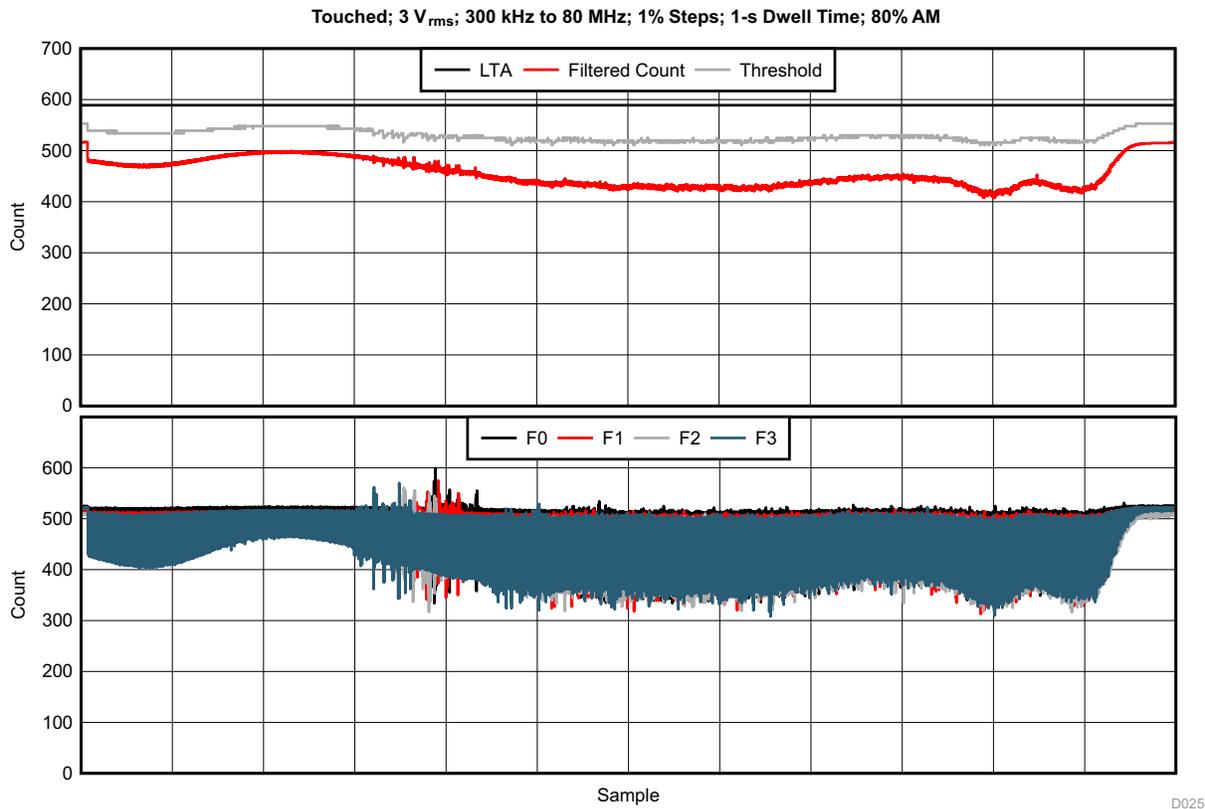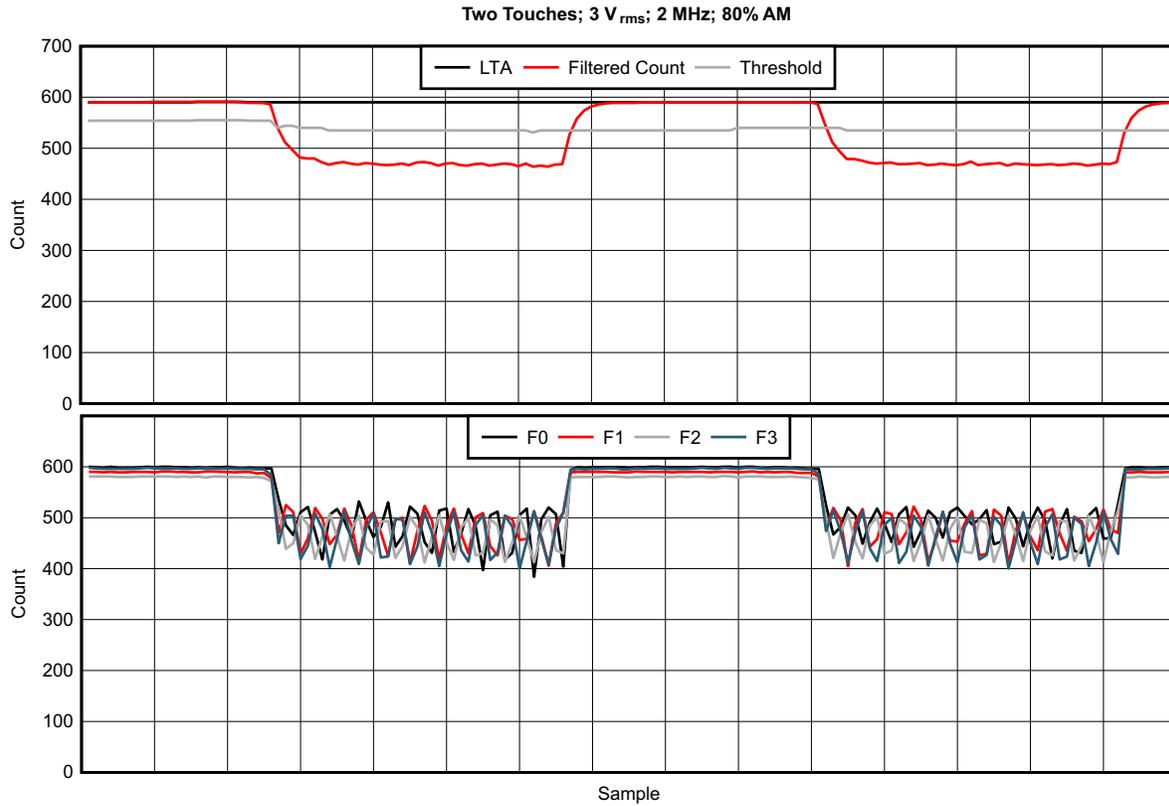
Touched; 3 V_{rms}; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM

Figure 77. CSM-SELF PSM-12VDCTO3.3VDC CMC; 3 V_{rms}; Touched Sweep

Figure 78 shows how the DTA algorithm can adjust the threshold when the common-mode choke is used. Oversampling and IIR filtering clean the periodic component of the signal completely.

Two Touches; 3 V$_{rms}$; 2 MHz; 80% AM

Figure 78. CSM-SELF PSM-12VDCTO3.3VDC CMC; 3 V$_{rms}$; Dwell at 2.0 MHz

Figure 79 shows the effect of 10-V_{rms} conducted noise on this configuration. The varying sensitivity changes with frequency before beginning a steady rolloff at the end of the sweep. This rolloff occurs because this is the 60- to 80-MHz noise portion of the test, which creeps greater than the low-pass cutoff of the CapTIvate I/O (I/O capacitance combined with the series resistance on the sensing line).
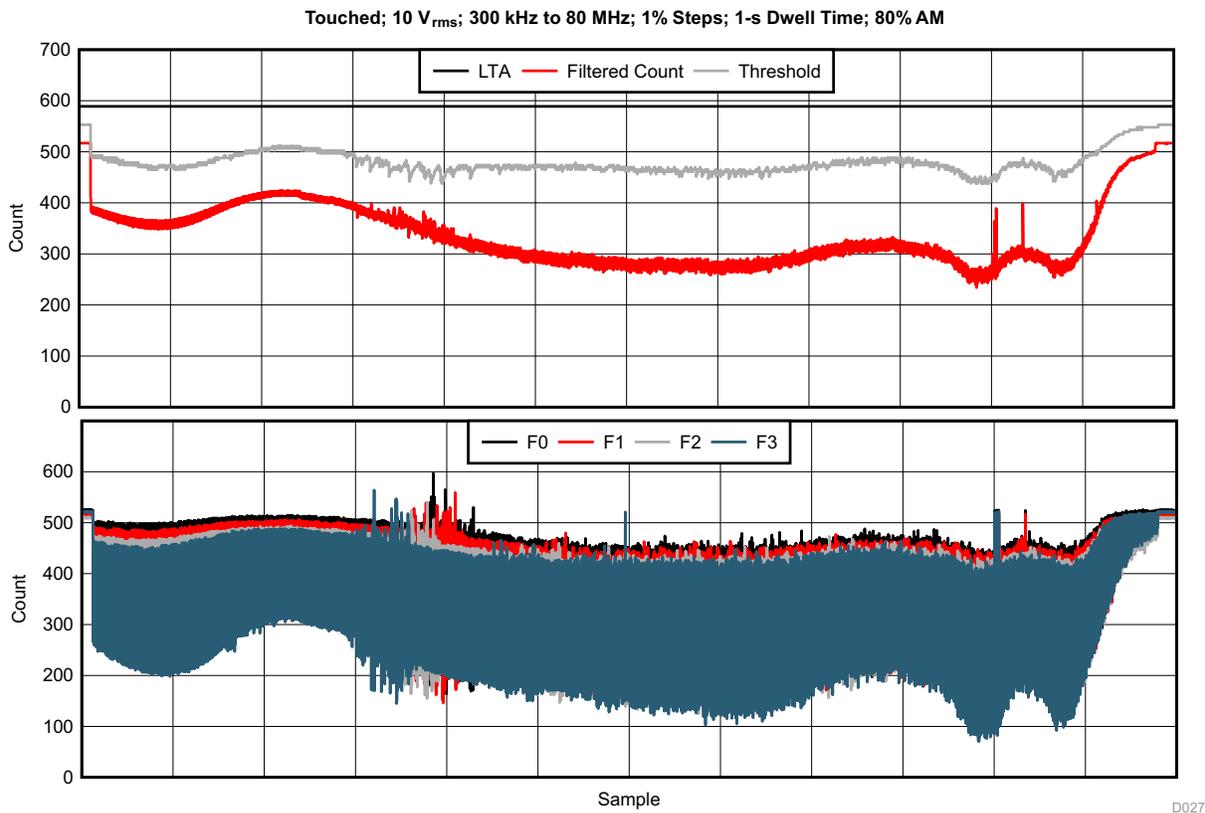
Touched; 10 V_{rms}; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM

Figure 79. CSM-SELF PSM-12VDCTO3.3VDC CMC; 10 V_{rms}; Touched Sweep
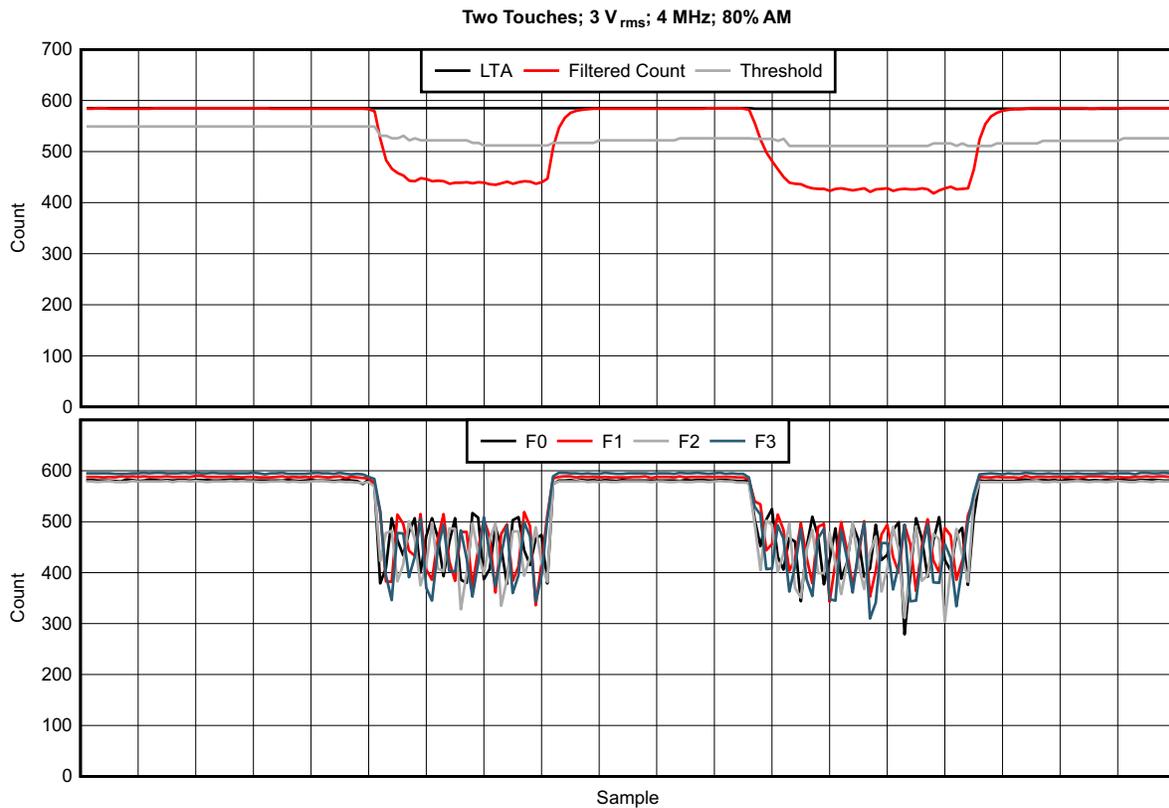
10.2.2.3 *PSM-UACTO3.3VDC*

Pairing the CSM-SELF with the PSM-UACTO3.3VDC power supply provides improved performance over the PSM-12VDCTO3.3VDC power supply. Figure 80 demonstrates that at 3 V_{rms}, the DTA algorithm is not required to adjust the touch threshold significantly to maintain the desired sensitivity. The oversampling and IIR filters produce clean samples from the raw inputs.
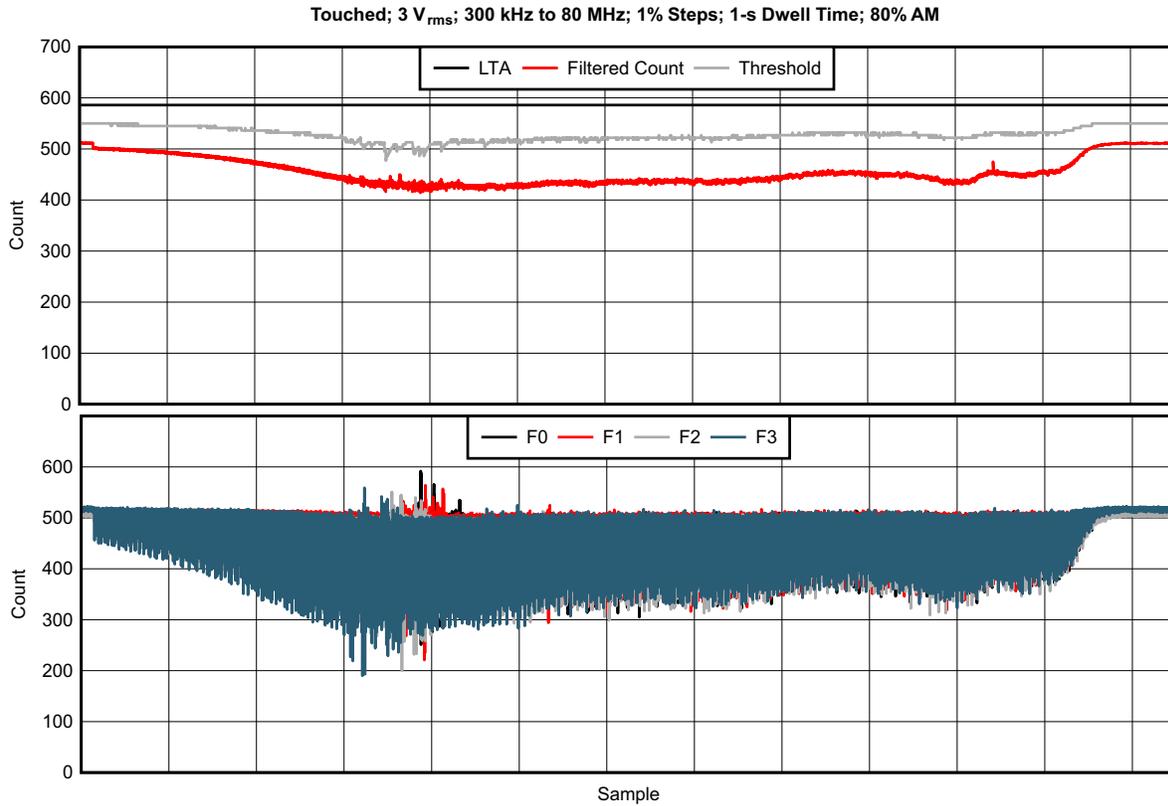
Figure 80. CSM-SELF PSM-UACTO3.3VDC; 3 V_{rms}; Touched Sweep

When compared to Figure 75, Figure 81 shows the benefits of the PSM-UACTO3.3VDC supply. Few DTA corrections are required in this example.

Figure 81. CSM-SELF PSM-UACTO3.3VDC; 3 V_{rms}; Dwell at 2.0 MHz

At 10$_{Vrms}$, the DTA algorithm must apply more threshold compensation to maintain a consistent sensitivity. Figure 82 shows the tracking performance with the PSM-UACTO3.3VDC. The threshold spikes around the fundamental frequencies. This spiking results from the large noise around the fundamental conversion frequencies. The higher-noise levels lead the DTA algorithm to pull the threshold lower. Touch detection remains possible even with these disturbances.
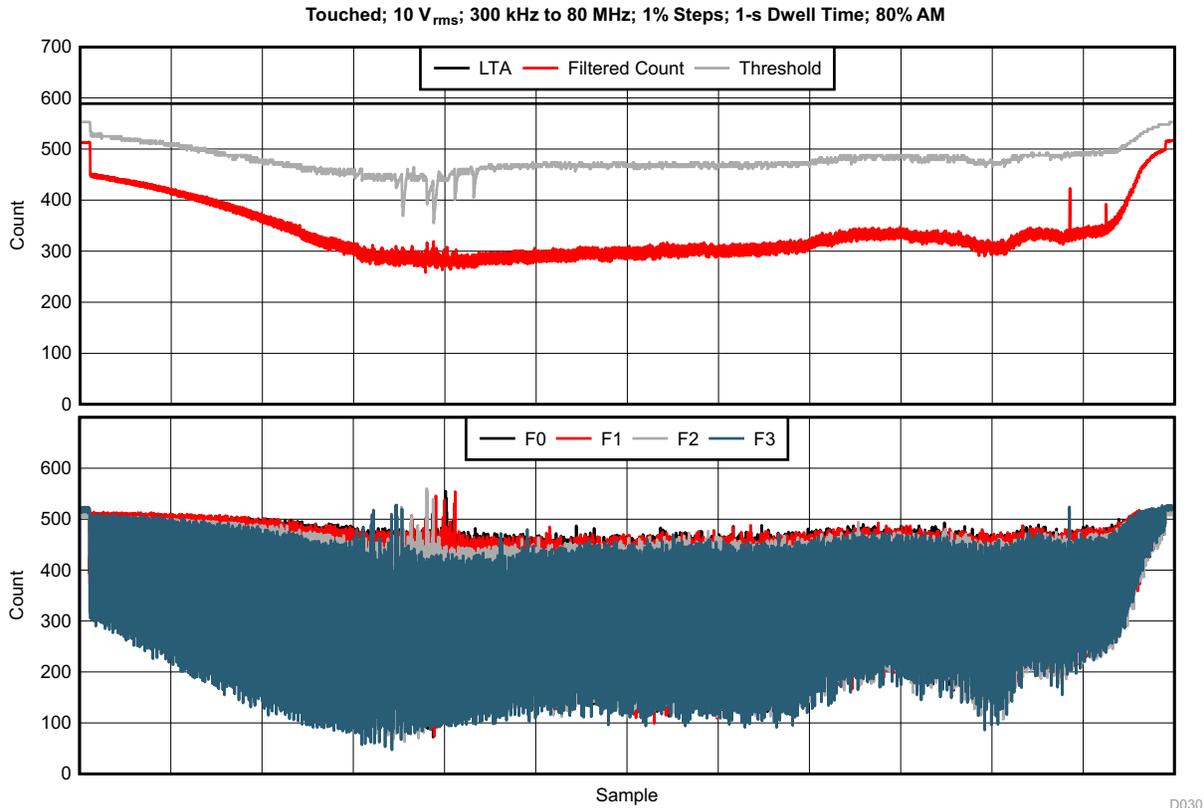
Touched; 10 V$_{rms}$; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM

Figure 82. CSM-SELF PSM-UACTO3.3VDC; 10 V$_{rms}$; Touched Sweep

10.2.2.4 *PSM-UACTO3.3VDC With CMC*

Combining the PSM-UACTO3.3VDC with the common-mode choke provides the best power supply for the CSM-SELF module, as with the CSM-MUTUAL module. Figure 83 demonstrates that with good power-supply design, minor correction is required to pass at 3 V_{rms}. There is no significant variation in sensitivity. To maintain the desired level of sensitivity, the threshold does not require major adjustment from the DTA algorithm.
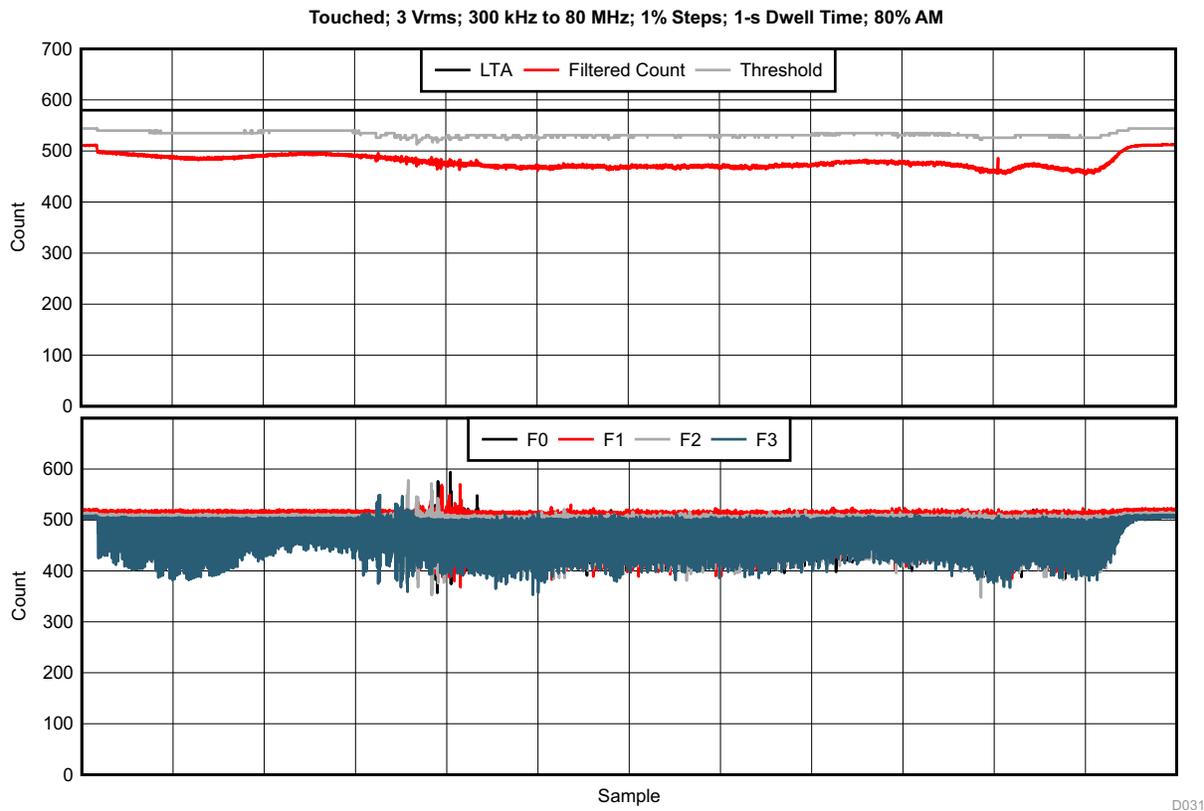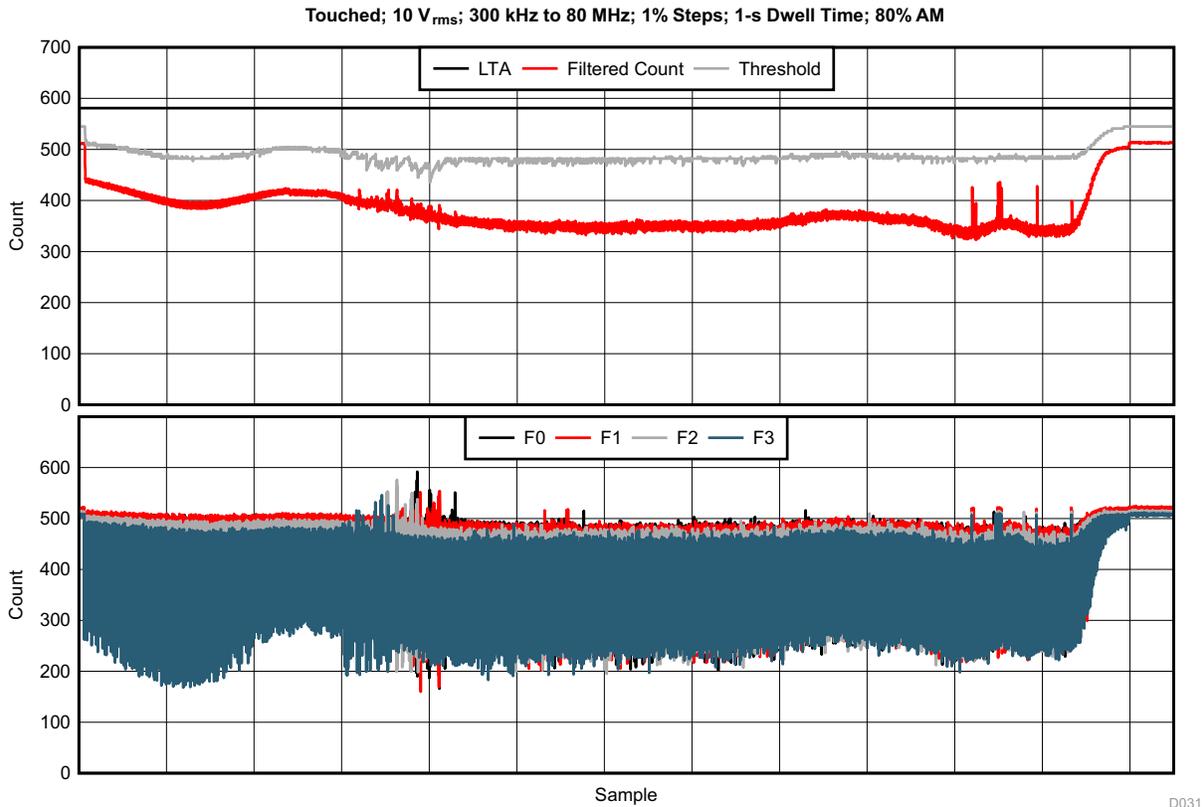
Figure 83. CSM-SELF PSM-UACTO3.3VDC CMC; 3 V_{rms}; Touched Sweep

Figure 84 shows that tolerance of noise at 10 V$_{rms}$ is achievable with this power supply.

Touched; 10 V$_{rms}$; 300 kHz to 80 MHz; 1% Steps; 1-s Dwell Time; 80% AM

Figure 84. CSM-SELF PSM-UACTO3.3VDC CMC; 10 V$_{rms}$; Touched Sweep

Figure 85 shows the response of the CSM-SELF with the PSM-UACTO3.3VDC with a common-mode choke to two touches in the presence of 10-Vrms conducted noise. The DTA algorithm is adjusting the threshold.
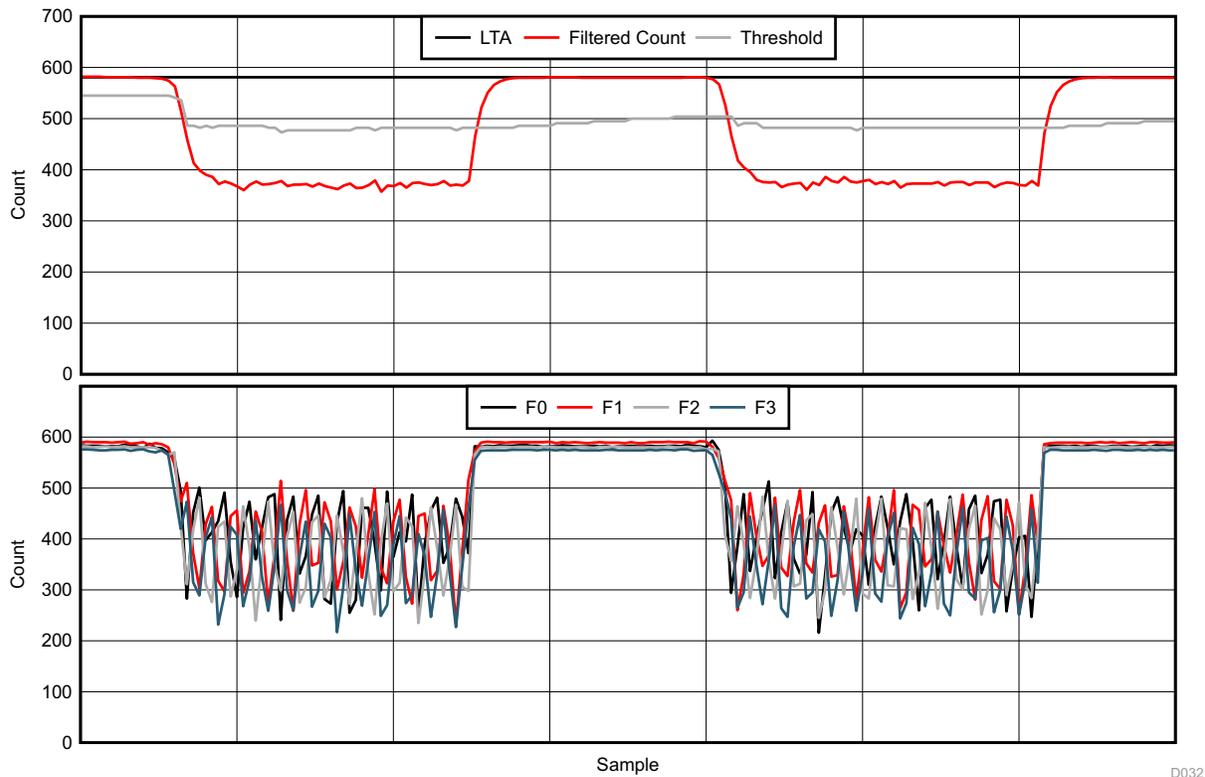
Figure 85. CSM-SELF PSM-UACTO3.3VDC CMC; 10 V$_{rms}$; Dwell at 2.0 MHz

Figure 86 shows that there is no disturbance in the measurement at 20 V_{rms} with no touch that indicates false touch detections. The DTA algorithm is responding around the fundamental frequencies, even though the filtered count does not show any noise.
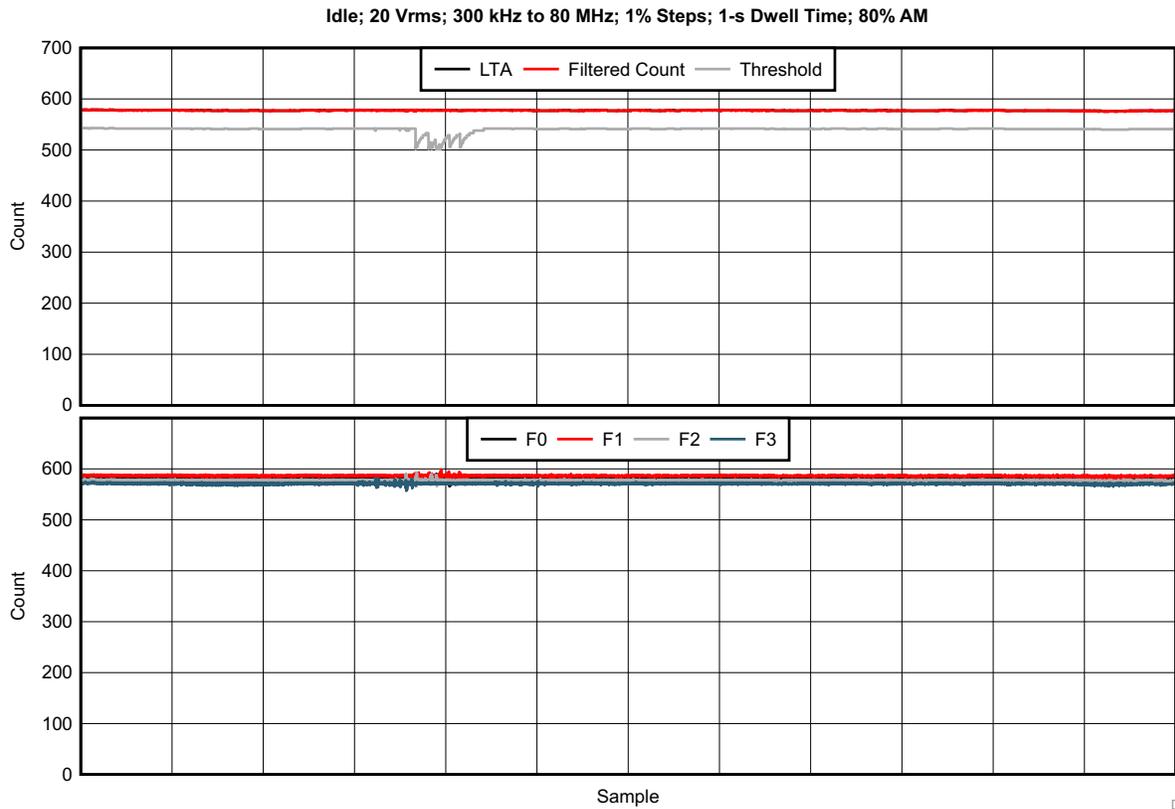
Figure 86. CSM-SELF PSM-UACTO3.3VDC CMC; 20 V_{rms}; Idle Sweep

Figure 87 shows the slider linearity for a right sweep, a left sweep across the slider with 10 V_{rms} conducted noise present at 2 MHz (overlapping the F0 conversion frequency), and the delta values for each of the four elements in the slider. The delta values are calculated as the LTA minus the filtered count. The slider position is calculated from the delta calculation. The common-mode rejection during each sample (as a result of the parallel scanning) combined with the intense oversampling and IIR filtering provided a smooth and linear slider even with 10 V_{rms} of conducted noise. This is a rough test conducted by moving a finger at close to a constant speed across the sensor.
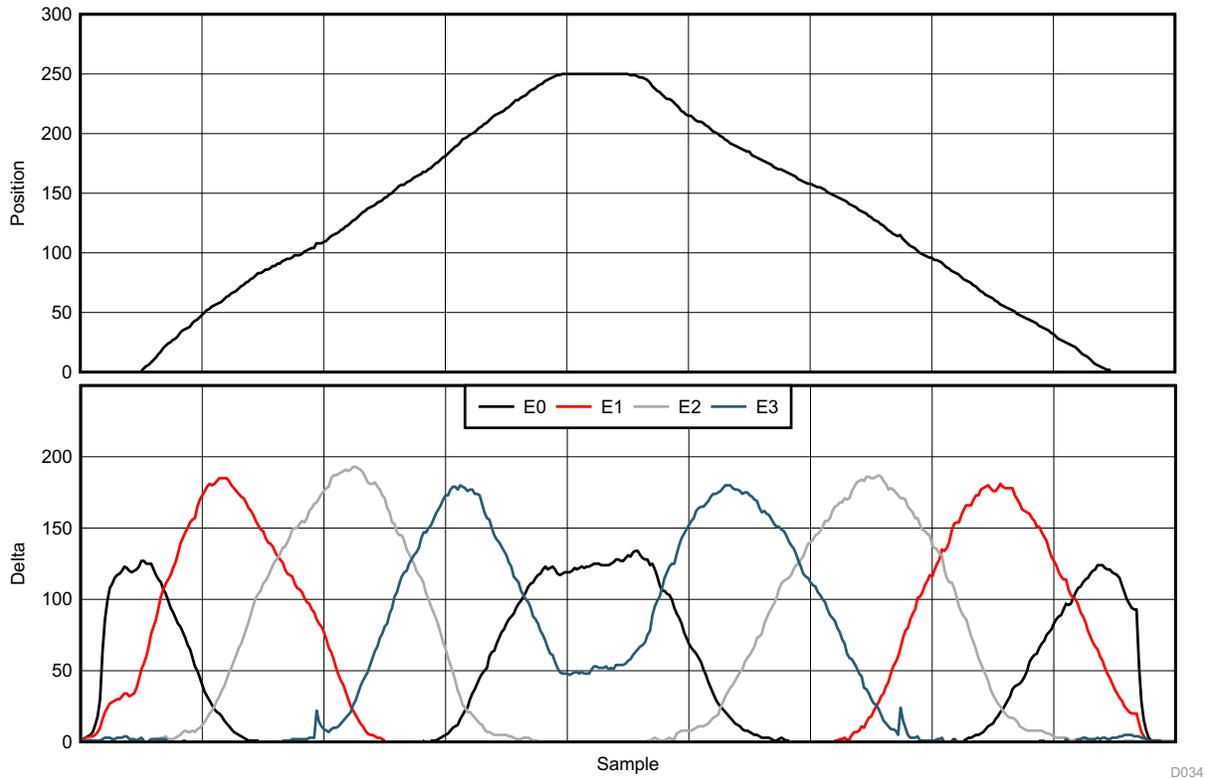
Figure 87. CSM-SELF PSM-UACTO3.3VDC CMC; 10 V_{rms}; Slider Linearity Test

10.3 *Electrical Fast Transient and Burst Immunity (IEC 61000-4-4)*

The CSM-SELF and CSM-MUTUAL were tested for immunity to electrical fast transients and bursts per the IEC 61000-4-4 standard. For this testing, the PSM-12VDCTO3.3VDC and PSM-UACTO3.3VDC were used without common-mode chokes. The tested configurations follow:

*   CSM-MUTUAL REVB with PSM-UACTO3.3VDC
*   CSM-MUTUAL REVB with PSM-12VDCTO3.3VDC
*   CSM-SELF REVB with PSM-UACTO3.3VDC
*   CSM-SELF REVB with PSM-12VDCTO3.3VDC

Per the IEC standard, class B testing was conducted at 5-kHz and 1000kHz burst rates with positive and negative pulses and L, N, and L+N coupling modes. The following configurations were tested:

*   ±4 kV, 5 kHz, L coupling
*   ±4 kV, 100 kHz, L coupling
*   ±4 kV, 5 kHz, N coupling
*   ±4 kV, 100 kHz, N coupling
*   ±4 kV, 5 kHz, L+N coupling
*   ±4 kV, 100 kHz, L+N coupling

All tested unit configurations passed all test scenarios. Early EFT testing clarified the importance of analog concepts such as reducing cable sizes to the shortest lengths possible and digital concepts such as writing EMC hardened software.

During EFT testing, the internal device data log on the MSP430FR2633 and the status LEDs were used to verify that the system avoided malfunction during testing.

The soft errors tested for follow:

*   No false touch detections
*   No undesired IC resets (brownout or other)
*   No nonrecoverable I^2C errors when communicating with the I^2C I/O expanders
*   No FRAM bit error detections
*   Full operation after test is complete with no user intervention

For more information, see Figure 88.
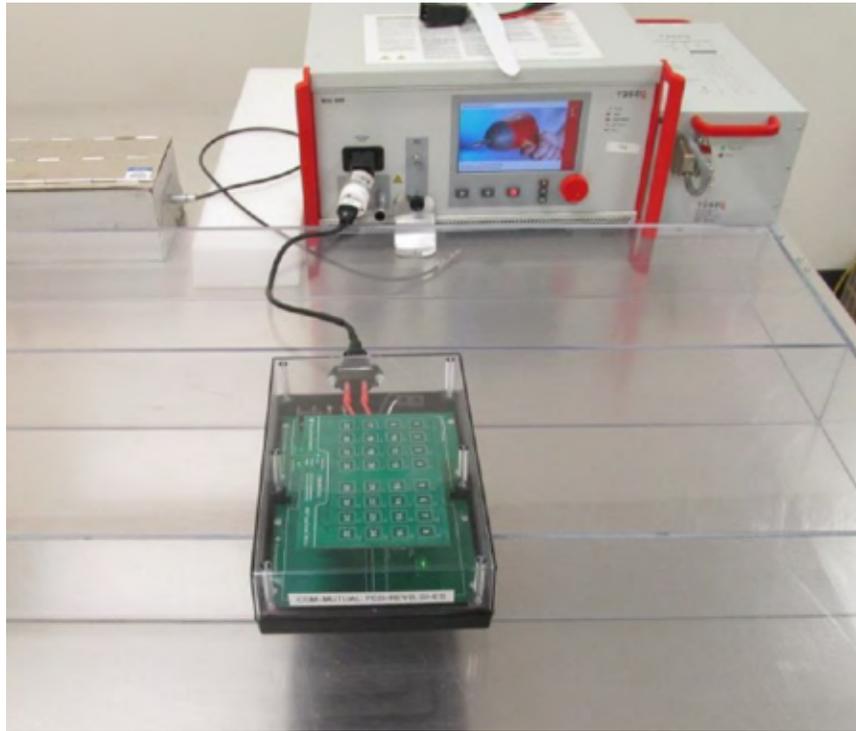
Figure 88. EFT Test

10.4 *Electrostatic Discharge Immunity (IEC 61000-4-2)*

The CSM-SELF and CSM-MUTUAL were tested for immunity to electrostatic discharge per the IEC 61000-4-2 standard. For this testing, the PSM-UACTO3.3VDC was used without a common-mode choke. The tested configurations follow:

- CSM-MUTUAL REVB with PSM-UACTO3.3VDC
- CSM-SELF REVB with PSM-UACTO3.3VDC

Per the IEC standard, class B testing was conducted with contact and air discharge. The following configurations were tested:

- ±8 kV, contact, horizontal-coupling plane
- ±8 kV, contact, vertical-coupling plane
- ±15 kV, air, power-entry connector
- ±15 kV, air, over electrode area
- ±15 kV, air, around side of enclosure

All tested unit configurations passed all test scenarios.

During ESD testing, the internal device data log on the MSP430FR2633 and the status LEDs were used to verify that the system avoided malfunction during testing.

The soft errors were tested for follow:

- No false touch detections
- No undesired IC resets (brownout or other)
- No nonrecoverable I^{2}C errors when communicating with the I^{2}C I/O expanders
- No FRAM bit error detections
- Full operation after test is complete without user intervention

For more information, see Figure 89.
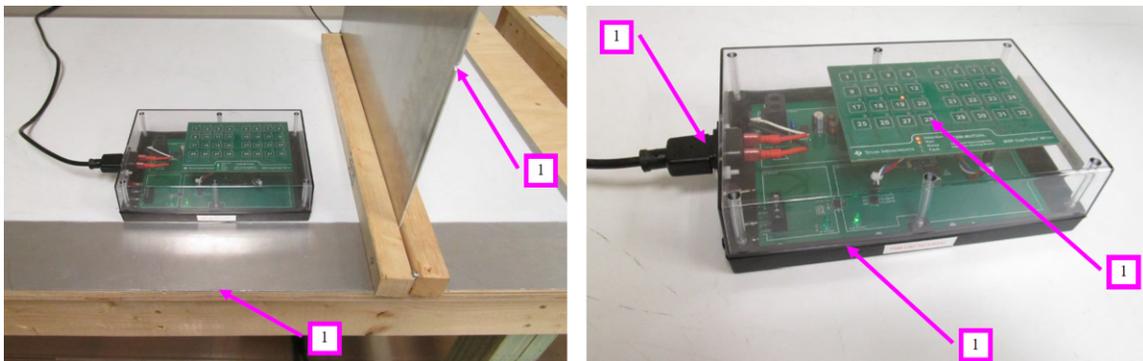
Figure 89. ESD Test

10.5 Third Party Certifications

Northwest EMC in Plano, TX validated the internal test findings of the TIDM-CAPTOUCHEMCREF. The following two assemblies were validated:

- CSM-MUTUAL REVB with PSM-UACTO3.3VDC (no common-mode choke)
- CSM-SELF REVB with PSM-UACTO3.3VDC (no common-mode choke)

Detailed test reports are available in *Enabling noise-tolerant capacitive-touch HMIs with MSP CapTIvate™ technology* (SLAY045).

Table 15 lists the tests conducted at Northwest EMC.

Table 15. Northwest EMC Exernal Tests

Configuration	IEC61000-4-6 Conducted Noise Immunity, Class A	IEC61000-4-6 Conducted Noise Immunity, Class B	IEC61000-4-4 EFT/B Immunity, Class B	IEC61000-4-2 ESD Immunity, Class B
PSM-UACTO3.3VDC; CSM-MUTUAL	3 V_{rms}	10 V_{rms}	±4 kV	±8-kV contact; ±15-kV air
PSM-UACTO3.3VDC; CSM-SELF	3 V_{rms}	10 V_{rms}	±4 kV	±4-kV contact; ±8-kV air

11 Conclusions

The test data shows the importance of a three-sided approach to electromagnetic compatibility. To rely on signal-processing algorithms to achieve immunity is not enough. Begin with well-designed hardware, including the PCB to the wire harnesses to the mechanical enclosure. The test data shows the difference a well-designed power supply can make limiting noise current paths. The difference between worst-case direct power and the best case of isolated AC with common-mode choke was visible for both self- and mutual-capacitance sensors, specifically with regard to conducted-noise immunity. For self capacitance, less special processing is required to achieve 3-V_{rms} immunity when the PSM-UACTO3.3VDC supply was used and configured with a small common-mode choke.

A capacitive-sensing IC with integrated noise-immunity features, such as the MSP430FR2633 MCU with CapTIvate touch technology. The flexibility of the CapTIvate touch technology allowed for aggressive layout techniques to be used, improving noise immunity to conducted disturbances, fast transients, and ESD. The frequency-hopping features of the MCU make the signal-processing algorithms effective and the fact that CapTIvate supports self-capacitance and mutual-capacitance sensors on the same device provides the opportunity to develop unique designs that use both topologies. An example of this is a design that uses mutual capacitance for a keypad and self capacitance for a slider.

11.1 Mutual Versus Self Capacitance for Noise-Tolerance Applications

The test data shows that mutual capacitance is the easier technology with which to develop noise-immunity applications. No special fine tuning is required in the CapTIvate software library to enable mutual-capacitance designs with noise immunity. The sensitivity to touch in the presence of noise remained consistent and the unique narrow susceptibility bands with mutual capacitance allow the multi-frequency processing algorithm to be effective removing the effects of noise from the perspective of the application. Because mutual capacitance is not subjected to variations in sensitivity even when subjected to noise, this capacitance is a more adaptable technology to a variety of noise sources, whether they are inside or outside a product. The immunity solution does not rely on measuring the noise to counteract it; the system adapts by moving between frequencies.

Self capacitance allows for slightly higher-noise levels to be reached with the added task of dialing in the DTA algorithm during design. The algorithm works well for applications that require only 3 V_{rms} conducted-noise immunity, especially if they have a well-designed power supply. Self capacitance supports higher-resolution sliders and wheel sensors with noise immunity and is a good choice for designs that require these sensors. The DTA algorithm works well for the conducted noise during IEC 61000-4-6 testing. There are situations that can upset the DTA algorithm—situations where the noise in the system is inconstant and is toggled on and off. The DTA algorithm relies on the ability to measure the noise in the system over

a period of time to determine how to compensate for the effects of the noise. In a product that is experiencing RF interference that is periodic (such as in the IEC 61000-4-6 test), the DTA algorithm works well. If the noise is transient (engaging and disengaging faster than the DTA algorithm can track it), the peak-detect nature of the DTA causes the adjusted, larger threshold to hold for too long, potentially masking valid touches. In this way, the DTA tries to prevent false touch detections.

The technology selected for a particular design is determined by the requirements of the application. Self-capacitance sensing is a good path for sliders, wheels, and buttons, where thick overlays are mandatory. Mutual-capacitance sensing is ideal for keypad applications because it is easy to initialize a design if proper layout techniques are followed. The CSM-MUTUAL panel has 32 buttons from 16 sensing pins. If fewer buttons are required, the oversampling, IIR filtering, and debounce settings can be increased, further improving the noise immunity of the solution.

11.2 Beyond IEC 61000-4 Standardized Testing

IEC 61000-4-x tests provide a common platform for ensuring that testing can be replicated in different EMC immunity categories. The tests simulate examples of real-world scenarios that a product might encounter while deployed in the field. The tests are the first steps to understand the weaknesses in a system to determine where to spend time developing and improving the robustness of a solution. Reasons exist to go further than the testing described in IEC 61000-4.

When developing a product, consider all noise sources that can exist inside and outside the product. Industrial equipment and tools applications place unique stresses on capacitive-sensing interfaces because they often involve switching of high-current inductive loads such as motors. AC and DC motors in products may generate noise that looks similar to conducted noise and EFT simultaneously. In these cases, in-system testing is more valuable than standardized testing. In-system testing is also valuable with power supplies because so many power supply topologies and styles exist, test a capacitive-touch interface with the power supply with which it is installed to determine if the power supply generates any unwanted interference (as in low-cost SMPS units). Power-supply noise is easy to work around because it is known at design time. Changing the conversion frequency or applying a basic passive filter can address many issues caused by noisy power supplies.

12 Design Files

Design documents, firmware, software, schematics, bill of materials, layer plots, Altium projects, Gerber files, assembly drawings, are available from http://www.ti.com/tool/TIDM-CAPTOUCHEMCREF.

13 References

- *CapTIvate™ Technology Guide* (http://www.ti.com/captivatetechguide)
- *Enabling noise-tolerant capacitive-touch HMIs with MSP CapTIvate™ technology* white paper (SLAY045)
- *MSP430™ System-Level ESD Considerations* application report (SLAA530)

14 About the Author

WALTER SCHNOOR is a system applications engineer at TI. Walter focuses on capacitive-touch solution design, hardware development, software development, and ecosystem development. He has been working at TI since 2012. Walter earned his BS in Electrical and Computer Engineering (BSECE) from Calvin College in Grand Rapids, MI.

KURT SCHMIDT has been with TI since 2007 working as an Analog Field Applications Engineer. He has broad experience in test, measurement, control, power, and embedded systems in the Industrial, Medical, and Test and Measurement markets. Kurt has authored/coauthored multiple U.S. Patents and holds a BSEET and ASECT from Milwaukee School of Engineering in Milwaukee, WI.

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        3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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    CAUTION

    This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

    Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

    FCC Interference Statement for Class A EVM devices

    NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

 3.2.1   *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

 3.3.1   *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に 輸入される評価用キット、ボードについては、次のところをご覧ください。 http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

 3.3.2   *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,

2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or

3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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いないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの
措置を取っていただく必要がありますのでご注意ください。

1.　電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用
　　いただく。
2.　実験局の免許を取得後ご使用いただく。
3.　技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。
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4　*EVM Use Restrictions and Warnings:*

  4.1　EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

  4.2　User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

  4.3　*Safety-Related Warnings and Restrictions:*

    4.3.1　User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

    4.3.2　EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

  4.4　User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5.　*Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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