TI Designs

Automotive Two-Axis Power Seat Drive Reference Design

Description

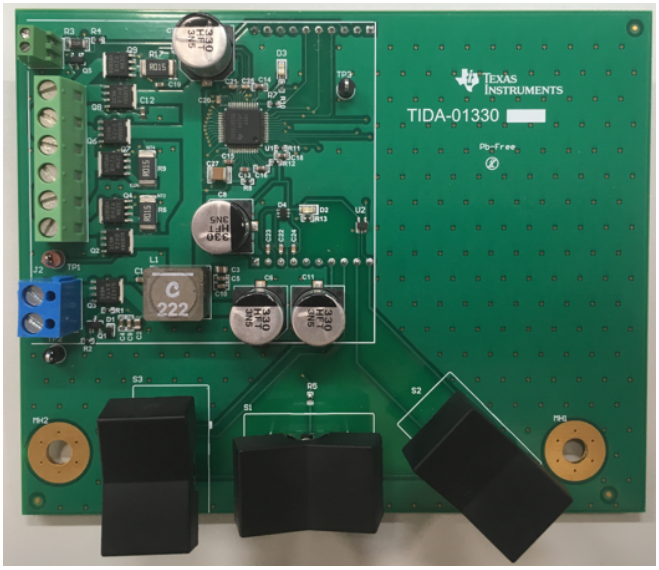
The TIDA-01330 design implements the drive circuits for two independent brushed DC motors. It provides a solution for automotive power seats with a highly-integrated two-axis driver, reducing the overall bill of materials. The interface to a simple microcontroller Illustrates how the design reduces the processing burden on the control software.

In addition to the drive circuit for two motors, this TI Design also includes current feedback sense circuits and other diagnostic features to ensure reliable operation and detection of faults. Additionally the control circuit for an LED illumination element is implemented, as well as the feasibility of providing tactile feedback to the seat occupant by vibrating in either axis.

Resources

TIDA-01330	Design Folder
DRV8305-Q1	Product Folder
SN74AHC1G00-Q1	Product Folder
MSP430G2553-Q1	Product Folder

TI E2E™ Community — ASK Our E2E Experts

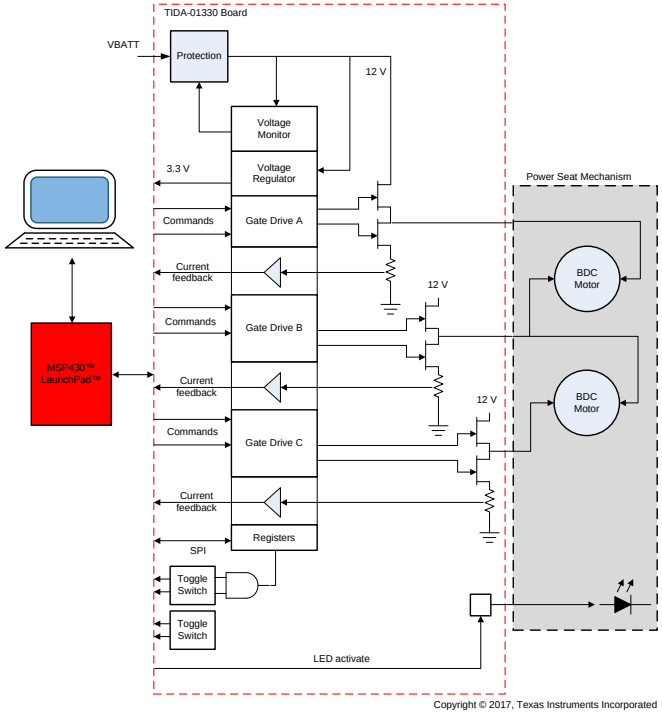


Features

- Drives Two Independent Brushed DC Motors
- Up to 10-A Motor Current (Each Axis)
- Current Feedback on Each Axis
- Reverse Battery Protection
- Low-Pass Filtering on Battery Power
- Drives LED for Floor Illumination
- Simple Microcontroller Interface
- Reduced Bill of Materials

Applications

- Power Seat Height and Forward and Backward Adjustment
- Power Seat Back Recline Adjustment and Power Fold
- Other Two-Axis Brushed DC Motor Drives



1 System Overview

1.1 System Description

The TIDA-01330 design drives two brushed DC motors that are part of an automotive power seat assembly. This TI Design uses the DRV8305-Q1 motor driver, which includes gate drivers for three half-bridges, current sense amplifiers, input voltage monitoring, and a wide-input linear regulator. In response to user inputs on toggle switches, one or both of the motors will be driven with up to 10 A of continuous current from the 12-V automotive power system.

The DRV8305-Q1 monitors the input power voltage and turns off a power field-effect transistor (FET) when the input voltage is not within the allowed range, protecting the circuit from fault conditions such as reverse battery. A low-pass filter on the input power line reduces both the incoming noise from external sources and attenuates any noise generated by the motors before reaching the external power bus.

Current sense amplifiers provide feedback signals proportional to the motor currents, allowing the microcontroller to monitor the motor state and halt the motor drive when high currents indicate a limit-of-travel has been reached.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Number of axis	2	Section 4.2.2
Motor type	Brushed direct current (BDC)	Section 4.2.1
Input power	12-V automotive battery system	Section 2.3
Maximum input voltage	40 V	Section 4.1.1
Minimum input voltage (operational)	5.5 V	Section 4.1.1
Reverse battery input (steady-state)	–18 V	Section 2.3.1
Maximum continuous motor current (each)	10 A	Section 5.3
Quiescent-state current consumption	30 mA	Section 4.1.1
Default motor current feedback scale factor	150 mV / A	Section 2.7
Default motor current feedback offset	1.65 V	Section 2.7
LED drive	Low-side switched	Section 2.10
Form factor	126×101-mm (5×4-inch) rectangular PCB with connections for LaunchPad™	Section 2.1

1.3 Block Diagram

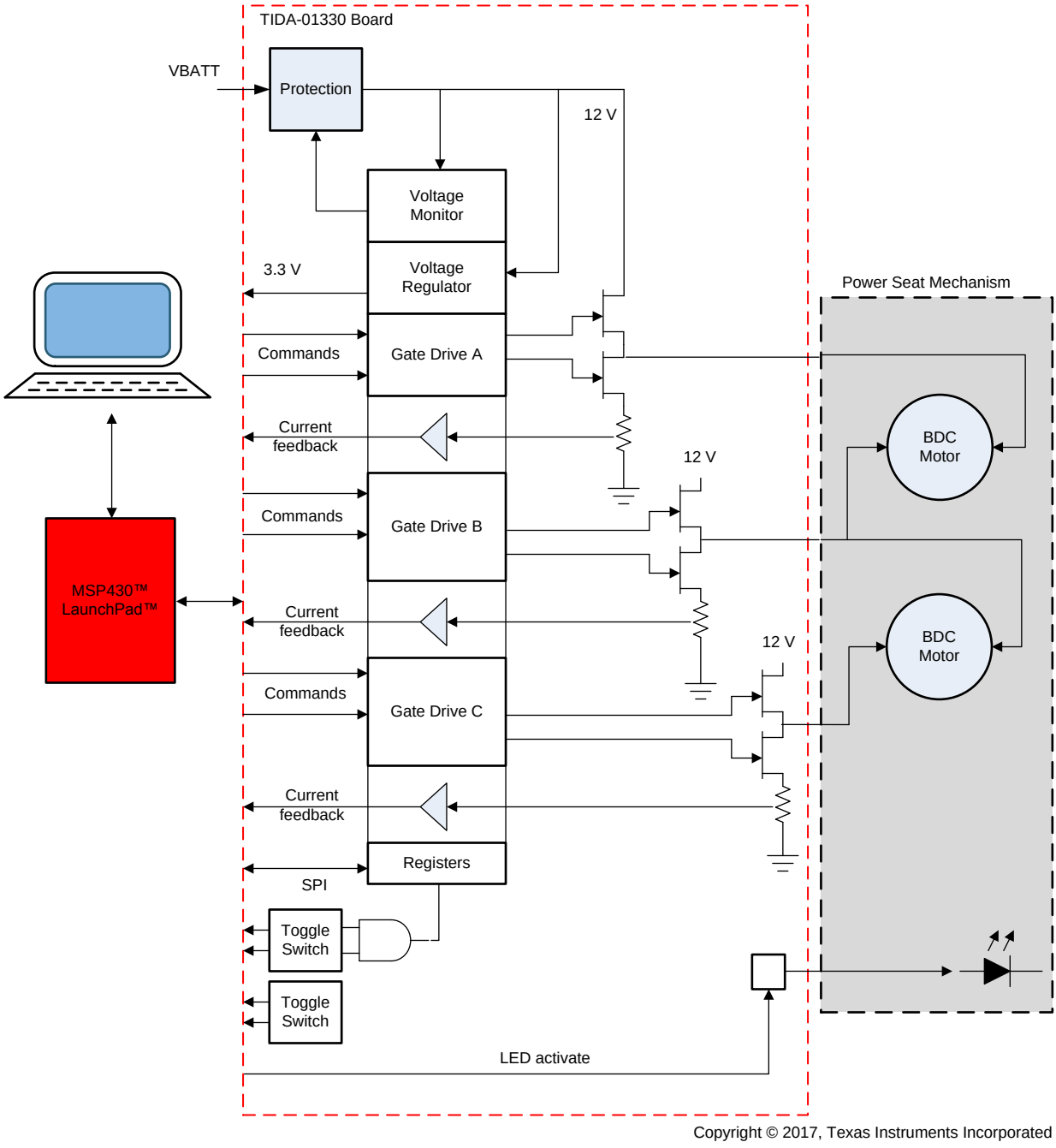


Figure 1. TIDA-01330 Block Diagram

1.4 Highlighted Products

1.4.1 DRV8305-Q1

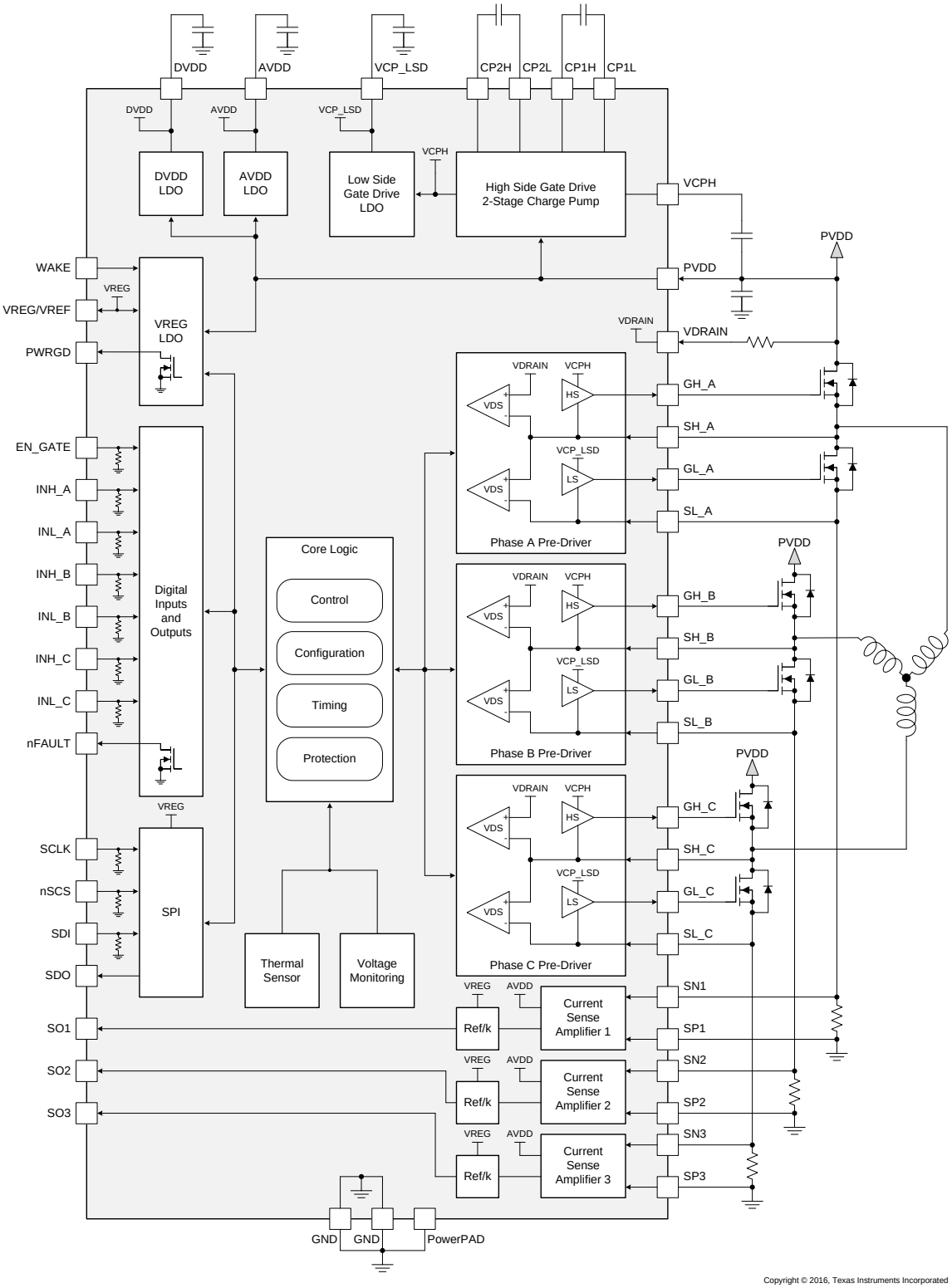


Figure 2. DRV8305-Q1 Functional Block Diagram

The DRV8305-Q1 device is a gate driver IC for motor-drive applications. The device provides three high-accuracy half-bridge drivers, each capable of driving a high-side and low-side N-channel MOSFET. A charge pump driver supports 100% duty cycle and low-voltage operation for cold crank situations. The device can tolerate load dump voltages up to 45 V.

The DRV8305-Q1 device includes three bidirectional current-shunt amplifiers for accurate low-side current measurements that support variable gain settings and an adjustable offset reference. It also has an integrated voltage regulator to support an MCU or other system power requirements. The voltage regulator can be interfaced directly with a LIN physical interface to allow low-system standby and sleep currents.

The gate driver uses automatic handshaking when switching to prevent current shoot through. The VDS of both the high-side and low-side MOSFETs is accurately sensed to protect the external MOSFETs from overcurrent conditions. The SPI provides detailed fault reporting, diagnostics, and device configurations such as gain options for the current shunt amplifier, individual MOSFET overcurrent detection, and gate-drive slew-rate control.

1.4.2 MSP430G2553-Q1

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers is optimized to achieve extended battery life in low-power applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 1 μs. The MSP430G2553-Q1 is an ultra-low-power mixed signal microcontroller with built-in 16-bit timers, up to 24 I/O capacitive-touch enabled pins, a versatile analog comparator, a 10-bit analog-to-digital converter (ADC), and built-in communication capability using the universal serial communication interface.

- Qualified for automotive applications
- Ultra-low-power consumption
- Ultra-fast wakeup from standby mode in less than 1 μs
- 10-bit 200-ksps ADC with internal reference, sample-and-hold, and autoscan

1.4.3 SN74AHC1G00-Q1

The Texas Instruments advanced high-speed CMOS (AHC) logic family provides a natural migration for high-speed CMOS (HCMOS) users who need more speed for low-power, and low-drive applications. Unlike many other advanced logic families, AHC does not have the drawbacks that come with higher speed, for example, higher signal noise and power consumption. The SN74AHC1G00-Q1 is a single two-input positive NAND gate with features well suited for automotive applications:

- Qualified for automotive applications
- Operating range of 2 to 5.5 V
- Low power consumption, 10-μA max Icc
- Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall time
- Output drive is ±4 mA at 3.3-V VCC
- ESD protection exceeds JESD 22
  - 2000-V human-body model (A114-A)
  - 200-V machine model (A115-A)
  - 1000-V charged-device model (C101)
- Microgate logic (single-gate) version that simplifies routing

2 System Design Theory

The following sections describe the considerations behind the design of each part of the system.

2.1 PCB and Form Factor

The size of the PCB was constrained by two features:

- Mechanical features of the test article power seat assembly
- Interface to MSP430 LaunchPad board

Mounting holes on the side of the power seat assembly dictate that the board be at least 5 inches in length. The spacing of the mounting holes allowed sufficient room for the use of large toggle switches for the user inputs. These toggle switches were mounted between the mounting holes to give structural support to avoid excessive board bend when the switches are pushed.

The spacing of the LaunchPad connectors required at least 2 inches of board height, and because the LaunchPad was mounted on the back side of the TIDA-01330 board, the board height was increased to 4 inches to allow for clearance between the LaunchPad board and the power seat structure.

In a production version of this TI Design, these constraints would not apply, as the MSP430G2553-Q1 would be mounted on the driver board, and the driver board would most likely be mounted under the seat, rather than as part of the switch assembly.

The PCB layer stack-up was constrained to two layers to reduce production cost. This is in accordance with the cost constraints generally in place for automotive systems, and especially body electronics. With only two layers, special consideration had to be taken for routing, especially with regards to the high-current traces for power and motor voltages.

2.2 General Considerations for Component Selection

In general, components were selected based on the performance requirements of the expected applications. Where practical, components with automotive ratings were selected. For active components, the components selected are AEC-Q100 qualified to either temperature grade 0 or temperature grade 1.

Capacitors are generally X7R grade (−55°C to 125°C) or higher, with size and value selected for the expected extremes of operation conditions. The voltage rating of the capacitors must be greater than the maximum voltage they could experience, and 2× the typical operating voltage to avoid DC bias effects. The amount of output capacitance used depends on output ripple and transient response requirements, and many equations and tools are available online to help estimate these values.

Consider the possible maximum voltage that could be experienced by the components. Capacitors must be derated by a minimum of 25% due to the drop in capacitance at 100% rated DC voltage of X7R and C0G/NP0 ceramic capacitors (that is, max voltage 40 V; Capacitor voltage rating = 40 V × 1.25 = 50 V). The derating also helps protect components from unexpected voltage spikes in the system. During the design process, the amount of BOM line items was considered. Therefore, capacitor voltage ratings may have been increased above the minimum desired rating. As an example, if there was one 1-μF, 25-V capacitor but nine 1-μF, 50-V capacitors, then the lone capacitor would be selected as a 50-V capacitor and the schematic would contain a note indicating that the voltage rating was increased for BOM simplicity.

For improved accuracy, all feedback resistor dividers must use components with 1% or better tolerance. Resistance tolerance in this TI Design was selected to reduce the total amount of BOM line items. In the design considerations, it is noted where 5% or 10% precision resistors may be used to reduce the cost of a specific individual resistor. Using less precise resistors for cost reasons should be weighed against reducing the amount of BOM line items and ordering in higher volumes to reduce total BOM cost.

2.3 12-V Input Protection

The 12-V supply may experience several excursions from the nominal 12-V value. This TI Design includes protection against such typical hazards as reverse battery conditions, and high-frequency electrical noise.

2.3.1 Reverse Battery Protection

Reverse battery protection is required in nearly every electronic subsystem of a vehicle, both by OEM standards as well as ISO 16750-2, an international standard pertaining to supply quality. The DRV8305-Q1 is designed to support an external reverse supply protection scheme. The VCPH high-side charge pump is able to supply an external load up to 10 mA. This feature allows implementation of an external reverse battery protection scheme using a MOSFET and a BJT, as shown in Figure 3.

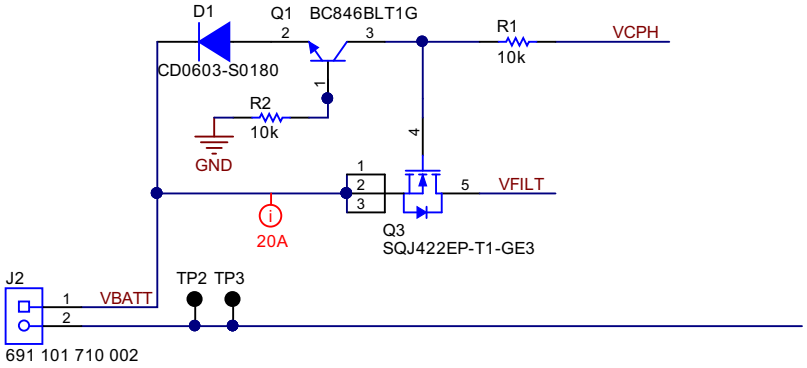


Figure 3. Reverse Battery Protection Circuit

The MOSFET gate and BJT may be driven by VCPH with a current limiting resistor. The current limiting resistor must be sized not to exceed the maximum external load on VCPH; R1 has a value of 10 kΩ, limiting the load on VCPH to less than 1 mA.

For this design, the reverse polarity MOSFET must be rated at least as high as the expected input voltage; the SQJ422EP is rated for 40 V. Compared to the FETs used to drive the motor phases, there is no emphasis on switching speed for the reverse-polarity FET, therefore, this device was selected primarily based on a low on-state resistance, rather than low gate capacitance.

The VDRAIN sense pin is protected against reverse supply conditions by use of a current limiting resistor, R8. The current limit resistor must be sized not to exceed the maximum current load on the VDRAIN pin. As recommended, R8 has a value of 100 Ω between VDRAIN and the drain of the external high-side MOSFET (see DRV8305-Q1 datasheet[1]).

The BJT (Q1) and diode (D1) serve to pull the gate of the FET low when reverse battery conditions exist. This prevents any inadvertent turnon of the reverse polarity FET due to sneak paths.

2.3.2 12-V Input Filtering

Another consideration for the front-end protection is the input filtering. This TI Design uses a set of capacitors and inductor to form a pi filter to remove unwanted AC components on the 12-V supply line. Due to the bidirectional format of the pi filter, incoming transients are blocked from entering the board, and any switching noise or clock noise generated on the board is blocked from propagating into the rest of the vehicle.

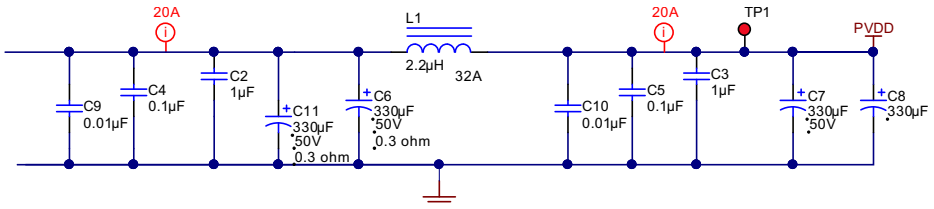


Figure 4. Electrical Schematic of Input Power Filtering

In general, the optimal amount of capacitance on the output side of the 12-V filtering may depend on the specifics of the application, including the current and electromagnetic compatibility (EMC) considerations. The pi filter implemented in this TI Design has relatively symmetric components, providing an LC filter in both directions. The corner frequency is selected such that frequencies above 10 kHz are significantly attenuated.

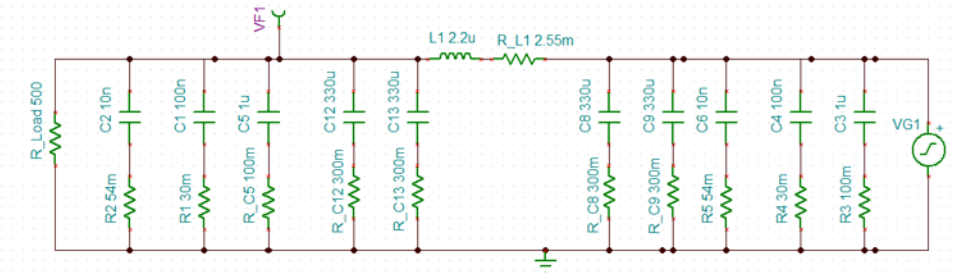


Figure 5. TINA Electrical Simulation Model of the Input Power Filtering Circuit, Including Equivalent Series Resistance (ESR)

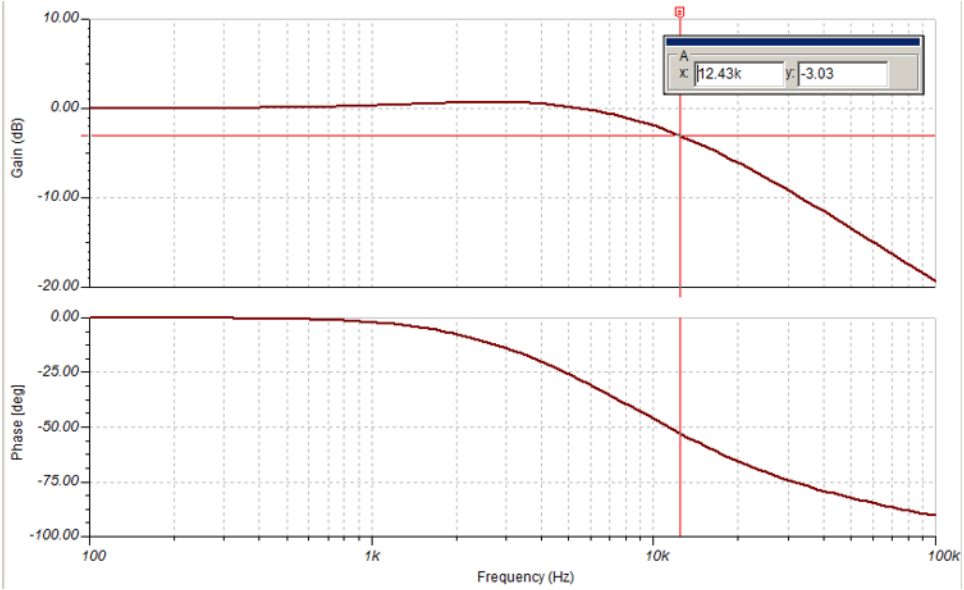


Figure 6. Frequency Response of TINA Simulation for Input Power Filtering Circuit

Selection criteria for the input power inductor (L1) include inductance value, rated current, series resistance, power rating (internal temperature rise), and size. Table 2 shows some candidate inductors, with the parameters compared as part of the selection tradeoff. The XAL1010-222 was selected for this TI Design based on the need for compact size and the 20-A current expectation for the applications.

Table 2. Shielded Power Inductor Parametric Comparison

PARAMETER	SRP1245A-1R0M	SRP1265A-2R2M	XAL6030-102ME	XAL1010-102ME	XAL1010-222	DRA127-1R0-R
Manufacturer	Bourns	Bourns	Coilcraft	Coilcraft	Coilcraft	Cooper Bussman
Inductance (μH)	1	2.2	1	1	2.2	1
I_{RMS} (A)	29	22	13	32	32	19.2
I_{SAT} (A)	50	37	23	55	34	40
DCR mΩ (typ)	2.5	3.8	6.2	1.1	2.55	1.7
Max temp (°C)	150	150		165	165	165
Temp rise at 20 A (°C)	15	26	20	< 20	< 20	40
Area (mm^2)	179	179	44	124	124	58
Height (mm)	5	6	3	10	10	3.6

2.4 3.3-V Power Supply

The DRV8305-Q1 integrates a 50-mA, LDO voltage regulator (VREG) that is dedicated for driving external loads such as an MCU directly. The VREG regulator also supplies the reference for the SDO output of the SPI bus and the voltage reference for the amplifier output bias. The three different DRV8305-Q1 device versions provide different configurations for the VREG output. For the DRV83053Q used in this TI Design, the VREG output is regulated at 3.3 V.

The DRV8305-Q1 VREG voltage regulator also features a PWRGD pin to protect against brownouts on externally driven devices. The PWRGD pin is often tied to the reset pin of a microcontroller to ensure that the microcontroller is always reset when the VREG output voltage is outside of its recommended operation area. The voltage regulator also has undervoltage protection implemented for both the input voltage (PVDD) and output voltage (VREG).

2.5 Gate Drivers

The DRV8305-Q1 gate driver uses a complimentary push-pull topology for both the high-side and the low-side gate drivers. Both the high side (GHx to SHx) and the low side (GLx to SLx) are implemented as floating gate drivers in order to tolerate switching transients from the half-bridges. The high-side and low-side gate drivers use a highly adjustable current control scheme in order to allow the DRV8305-Q1 to adjust the VDS slew rate of the external MOSFETs without the need for additional components. The scheme also incorporates a mechanism for detecting issues with the gate drive output to the power MOSFETs during operation.

The charge pump capacitors C13 and C15 follow the recommendations of the DRV8305-Q1 datasheet. These components are 0.047-µF ceramic capacitors, with voltage rating of 100 V (more than twice the design limit of 40 V on VBATT) and temperature code X7R for temperatures up to 125°C.

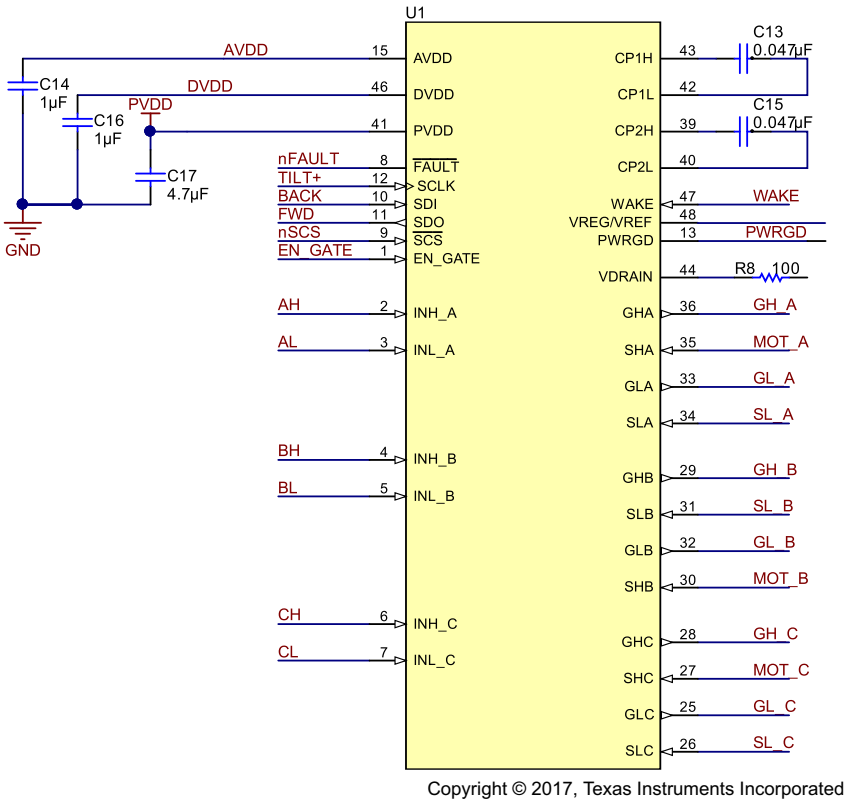


Figure 7. Gate Drive Circuit Electrical Schematic

2.6 Motor Drive Stages (Half-Bridges)

The motor drive stage consists of the three pairs of N-channel MOSFETs (high-side and low-side), and the large capacitors that supply the immediate bursts of current during each FET transition. Due to the integrated features of the DRV8305-Q1 gate driver, few other components are needed to optimize the performance of the drive stage.

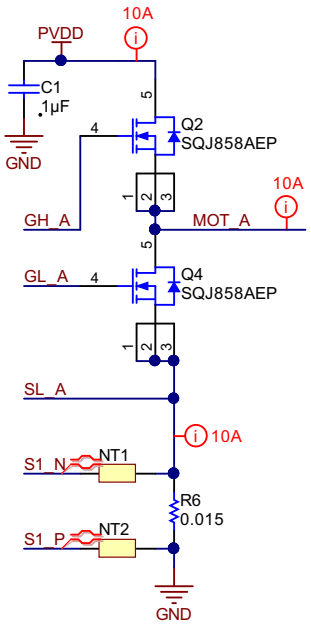


Figure 8. Electrical Schematic Phase A Motor Drive Circuit

Selecting the FETs for the motor drive stages involves a trade-off between component size, on-state resistance, and allowable drain-to-source voltage. The SQJ858 was selected as meeting the requirements for at least 40V drain-to-source voltage rating, maximum current of over 20 A, drain-to-source resistance below 10 mΩ, and small area. For similar industrial applications, which do not require a full automotive component qualification, the CSD18540Q5B from Texas Instruments has similar electrical parameters. The CSD18540Q5B also has a pin-compatible package as the SQJ858, allowing direct replacement with no board re-layout.

Another significant design consideration of the drive stage is the selection of the electrolytic capacitors. Selection of the electrolytic capacitors depends on meeting the requirements for high capacitance in a small size, wide temperature range, long lifetime rating, and a high value of rated ripple current. The EEE-FT1H331 capacitor was selected as having the best combination of capacitance value, size, temperature rating, ripple current, and ESR.

2.7 Current Sense

When the motors are driven, the current through the motor is sampled by the microcontroller as part of the motor control algorithm. The circuit shown in Figure 9 shows a TINA simulation schematic; here the motor current is represented as an input signal, with filtering, amplification, and offset to the center of the ADC input range. This circuit is used for each of the three half-bridges.

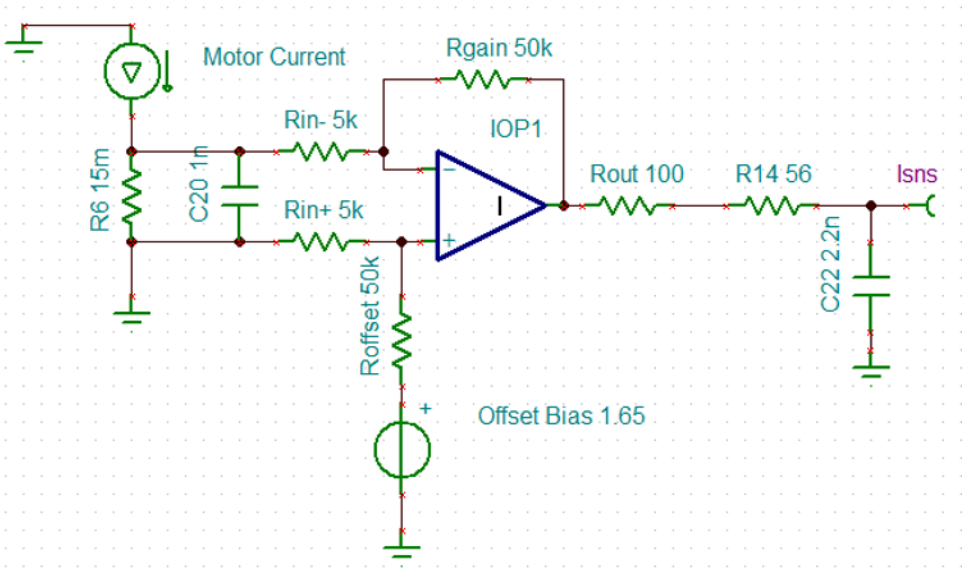


Figure 9. TINA Simulation Schematic of Current Sense Circuit

The low-side current through phase A flows through R6, giving a scale factor of 15 mV/A. Differential low-pass filtering is provided by C20, with an RC time constant of 15 ps (15 mΩ × 1 nF), so this only affects very high frequencies. The TINA-simulated frequency response of the circuit is shown in Figure 10. The low-frequency gain of –16.5 dB corresponds to the current sense scale factor of 150 mV/A of motor current.

The differential gain amplifier circuits (integrated as part of the DRV8305-Q1) have a differential gain and offset which can be selected from several settings through the SPI port. For this TI Design, the differential setting of 10 is used, with an offset of half of the 3.3-V supply (1.65 V) provided by the DRV8305 internal voltage. After the gain provided by the op amp circuit, the motor current scale factor at the input to the ADC is 150 mV/A, with a voltage of 1.65 V representing zero motor current. Thus, with a range of 0 to 3.3 V at the input of the ADC, motor currents of ± 11 A may be measured.

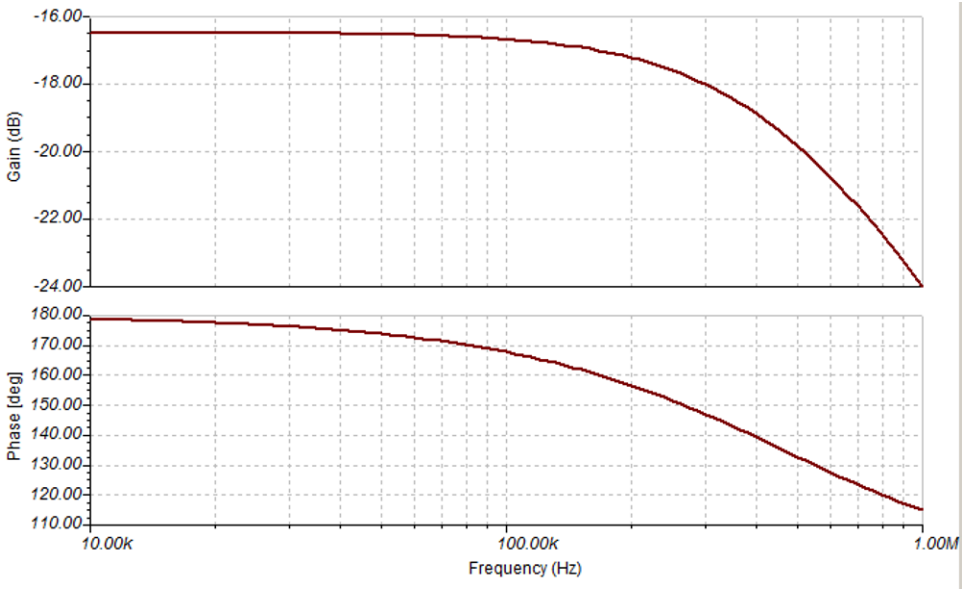


Figure 10. TINA Simulation Output Showing AC Response of Motor Current Sense Circuit

2.8 LaunchPad

The microcontroller on the LaunchPad receives inputs from the user and from the TIDA-01330 board regarding the state of the system and creates outputs to the TIDA-01330 board to control the power seat motors and LED indicators. The two 10-pin connectors supply 3.3 V of power to the LaunchPad, and carry the digital input and output signals, as well as the analog Current_Sense signals.

2.8.1 3.3-V Power to LaunchPad

The 3.3-V supply is generated on the TIDA-01330 board, and supplied to the LaunchPad through pins J3-1 (3p3V) and J4-10 (GND). The LaunchPad also has a USB connector, which allows users to connect to a computer when programming the LaunchPad. In order to avoid ground loops and power supply contention with the supply on the USB pins, jumpers should be removed from the LaunchPad as described in Section 3.1. If another microcontroller is used, the total 3.3-V supply current should be kept less than 50 mA.

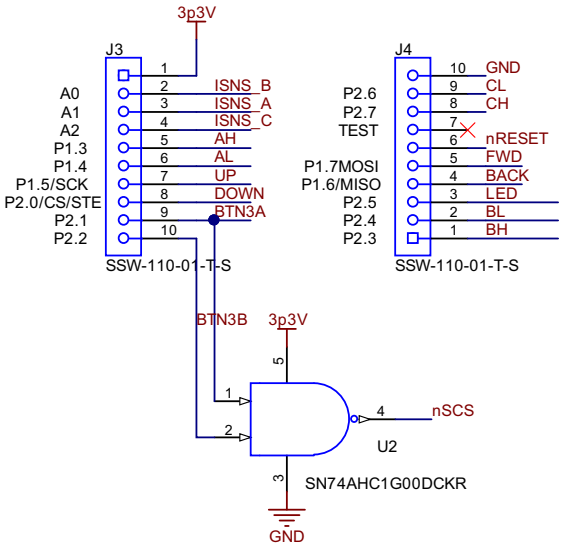


Figure 11. Electrical Schematic of Connections to LaunchPad

NOTE: This board is intended for use with the MSP430G2 LaunchPad with MSP430G2553.

2.8.2 GPIO Signals

General purpose input/output (GPIO) signals are used for the several digital signals that control and monitor the operation of the motor drive circuits. These signals are summarized in Table 3.

Table 3. LaunchPad Interface GPIO Signal Assignments

SIGNAL	DIRECTION	CONNECTOR PIN	LAUNCHPAD GPIO	DESCRIPTION
AH	From microcontroller to DRV8305-Q1	J3-5	Port 1 bit 3	Sets state of A half-bridge high-side switch
AL	From microcontroller to DRV8305-Q1	J3-6	Port 1 bit 4	Sets state of A half-bridge low-side switch
BH	From microcontroller to DRV8305-Q1	J4-1	Port 2 bit 3	Sets state of B half-bridge high-side switch
BL	From microcontroller to DRV8305-Q1	J4-2	Port 2 bit 4	Sets state of B half-bridge low-side switch
CH	From microcontroller to DRV8305-Q1	J4-8	Port 2 bit 7	Sets state of C half-bridge high-side switch
CL	From microcontroller to DRV8305-Q1	J4-9	Port 2 bit 6	Sets state of C half-bridge low-side switch
UP	From user button to microcontroller	J3-7	Port 1 bit 5	Seat height Up command signal
DOWN	From user button to microcontroller	J3-8	Port 2 bit 0	Seat height Down command signal
FWD	From user button to microcontroller	J4-5	Port 1 bit 7	Seat position forward command signal
BACK	From user button to microcontroller	J4-4	Port 1 bit 6	Seat position backward command signal
BTN3A	From user button to microcontroller	J3-9	Port 2 bit 1	Optional button signal (for example, LED command)
BTN3B	From user button to microcontroller	J3-10	Port 2 bit 2	Optional button signal (for example, seat vibrate)
LED	From microcontroller to DRV8305-Q1	J4-3	Port 2 bit 5	Sets state of LED drive circuit

2.8.3 SPI Port

In order to reduce the cost and complexity of the microcontroller interface, the simple 20-pin LaunchPad format is implemented; however, this restricts the number of microcontroller GPIO signals available for the SPI port, which is used to set the parameters and read the registers of the DRV8305-Q1. The two-input NAND gate (U2) is used to provide a chip select signal to the SPI port on the DRV8305-Q1. Because the mechanical arrangement of the user switches will not permit both signals (BTN3A and BTN3B) to be pushed simultaneously, these two signals can be used to generate the chips select (nSCS) when both are set to a logic high state by the microcontroller. This combination can not be selected by the user interface, thus preventing any accidental enabling of the DRV8305-Q1 SPI port.

Because the DRV8305-Q1 will only respond to SPI signals when the nSCS signal is low, the GPIO signals used for FWD, BACK, and UP button signals can also be re-used for MOSI, MISO, and SCK, respectively. Thus the microcontroller can select SPI operation by setting both BTN3A and BTN3B high, and using MOSI, MISO, and SCK to communicate with the DRV8305-Q1. If the user switches are depressed during SPI communication, this will corrupt the SPI message and require repeated messages. Therefore, the user switches should not be used during the initialization period or update status periods if the SPI port is used to communicate. In Section 4, the default settings of the DRV8305-Q1 registers were used, showing that operation without SPI communication is also feasible.

2.9 Indicators

Two LED indicators are included to allow visual recognition of the state of the drive board. The green LED D3 is controlled by the Power Good (PWRGD) signal from the DRV8305-Q1 device. The PWRGD pin protects against brownouts on externally driven devices. The PWRGD pin is tied to the reset pin of the LaunchPad microcontroller to ensure that the microcontroller is always reset when the VREG output voltage is outside of its recommended operation area. When the voltage output of the VREG regulator drops or exceeds the set threshold (programmable), the PWRGD pin will go low for a period of 56 μs. After the 56-μs period has expired, the VREG voltage will be checked and PWRGD will be held low until the VREG voltage has recovered. The voltage regulator also has undervoltage protection implemented for both the input voltage (PVDD) and output voltage (VREG).

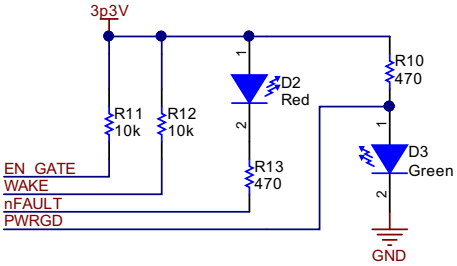


Figure 12. LED Indicator Schematic

The red LED D2 is controlled by the Fault (nFAULT) signal from the DRV8305-Q1 device. The DRV8305-Q1 integrates extensive error detection and monitoring features. These features allow the design of a robust system that can protect against a variety of system related failure modes. The DRV8305-Q1 classifies error events into two categories and takes different device actions dependent on the error classification. The first error class is a warning. There are several types of conditions that are classified as warning only. Warning errors are report only and the DRV8305-Q1 will take no other action effecting the gate drivers or other blocks. When a warning condition occurs, it will be reported in the corresponding SPI status register bit and on the nFAULT pin with a repeating 56-μs pulse low followed by a 56-μs pulse high. A warning error can be cleared by an SPI read to the corresponding status register bit. The same warning will not be reported through the nFAULT pin again unless that warning or condition passes and then reoccurs.

The second error class is a fault. Fault errors will trigger a shutdown of the gate driver with its major blocks and are reported by holding nFAULT low with the corresponding status register asserted. Fault errors are latched until the appropriate recovery sequence is performed by the microcontroller:

1. A fault error is reported by holding the nFAULT pin low and asserting the FAULT bit in register 0x1.
2. The error type will also be asserted in the SPI registers.
3. A fault error is a latched fault and must be cleared with the appropriate recovery sequence.
4. If a fault occurs during a warning error, the fault error will take precedence, latch nFAULT low, and shutdown the gate driver.
5. The output MOSFETs will be placed into their high impedance state in a fault error event.
6. To recover from a fault type error, the condition must be removed and the CLR_FLTs bit asserted in register 0x9, bit D1 or an EN_GATE reset pulse issued.
7. The CLR_FLTS bit self clears to 0 after fault status reset and nFAULT pin is released.

See Section 7.3.8.1 of the DRV8305-Q1 datasheet[1] for more information on the faults and warnings.

2.10 Footwell LED Drive Circuit

An LED assembly is included as part of some automotive seats, to provide illumination of the passenger footwell behind the seat. This LED can also function to warn passengers behind the power seat that the seat is moving backwards, to make them aware of potential pinching of passengers or objects behind the seat.

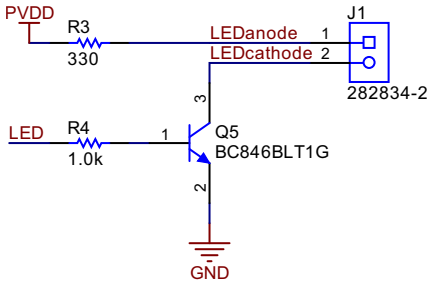


Figure 13. Electrical Schematic of Footwell Illumination Circuit

In this TI Design, a simple npn bipolar transistor is used to drive the external LED. To prevent the possibility of shorting the 12-V supply to ground in the case of a wiring fault, a current-limiting resistor (R3) is put in series with the anode connection. The value of 330 Ω sets a limit of 36 mA for a 12-V nominal battery voltage. A relatively large size resistor (1206) is used due to the potential of high power dissipation during such a fault condition.

2.11 Extension to Additional Motors

In general, the number of motors that can be driven in both directions (bi-directional motion) is *n-1* where *n* is the number of half-bridges (high-side and low-side switches) available to drive the motors. If more than two brushed motors are to be driven, additional half-bridge drives are needed; Figure 14 illustrates an extension of this TI Design, where two DRV8305-Q1 can be used to drive six half-bridges, and control the bidirectional motion of up to five brushed DC motors.

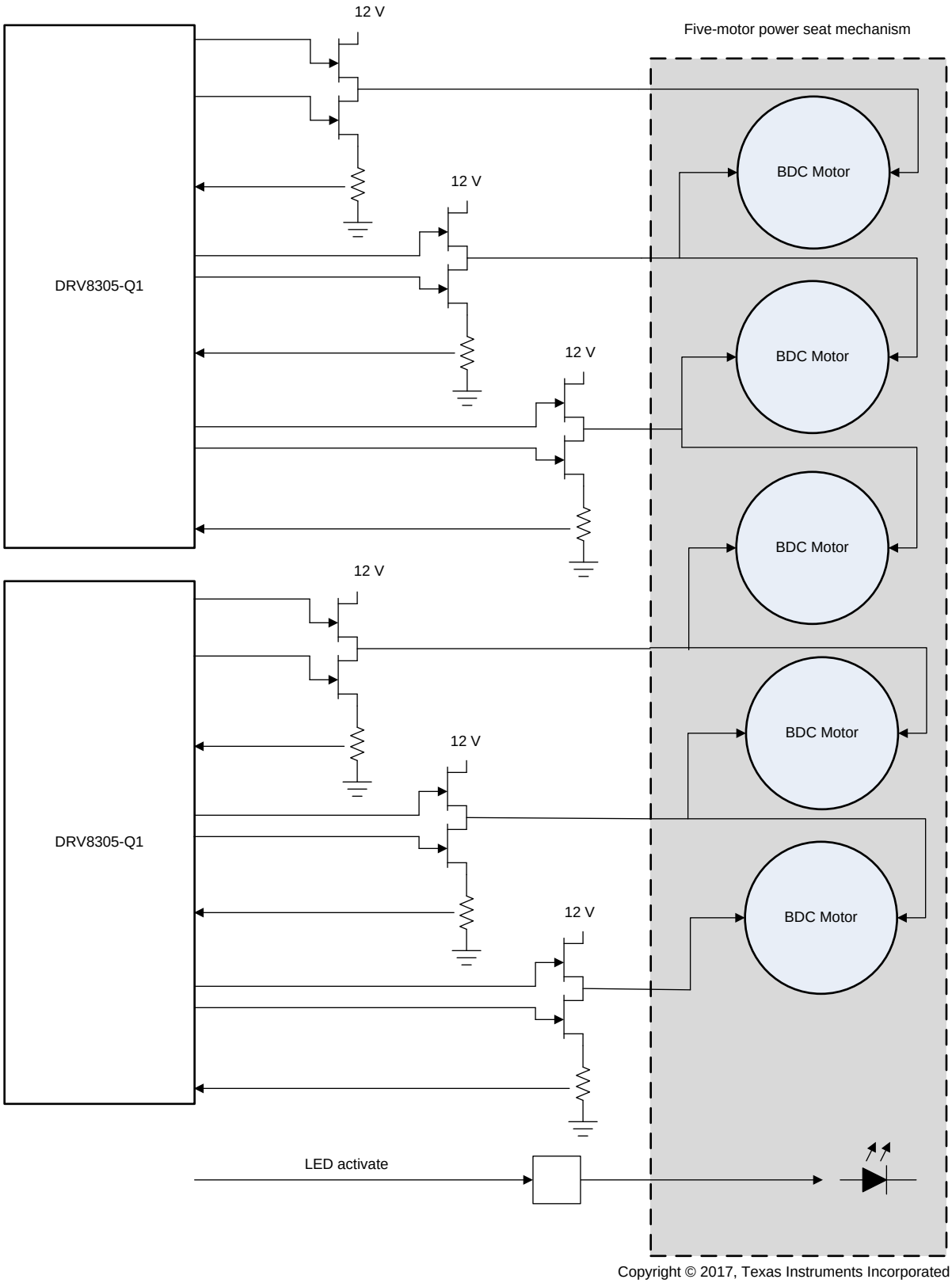


Figure 14. Extension of TIDA-01330 to Five-Axis Application

3 Getting Started Hardware and Software

3.1 Hardware

The reference platform comprises of three different pieces of hardware as listed:

- TIDA-01330 board
- MSP430G2553 LaunchPad board
- Power seat assembly with two brushed DC motors and LED illumination

3.1.1 LaunchPad Jumpers

Before installing the TIDA-01330 board on the MSP430 LaunchPad, several jumpers should be removed from the LaunchPad headers. On header block J3, remove the jumpers marked VCC, TXD, and TXD. The jumpers marked TEST and RST may be left installed. On the header block J5, remove both jumpers, marked P1.0 and P1.6, as these input/output pins are used by the TIDA-01330 board.

3.1.2 LaunchPad Installation

Install the TIDA-01330 board on the LaunchPad board, making sure to alight all ten pins of each of the two 10-pin headers. The orientation is such that the USB connector on the LaunchPad board will be on the same side as the terminal blocks on the TIDA-01330 board.

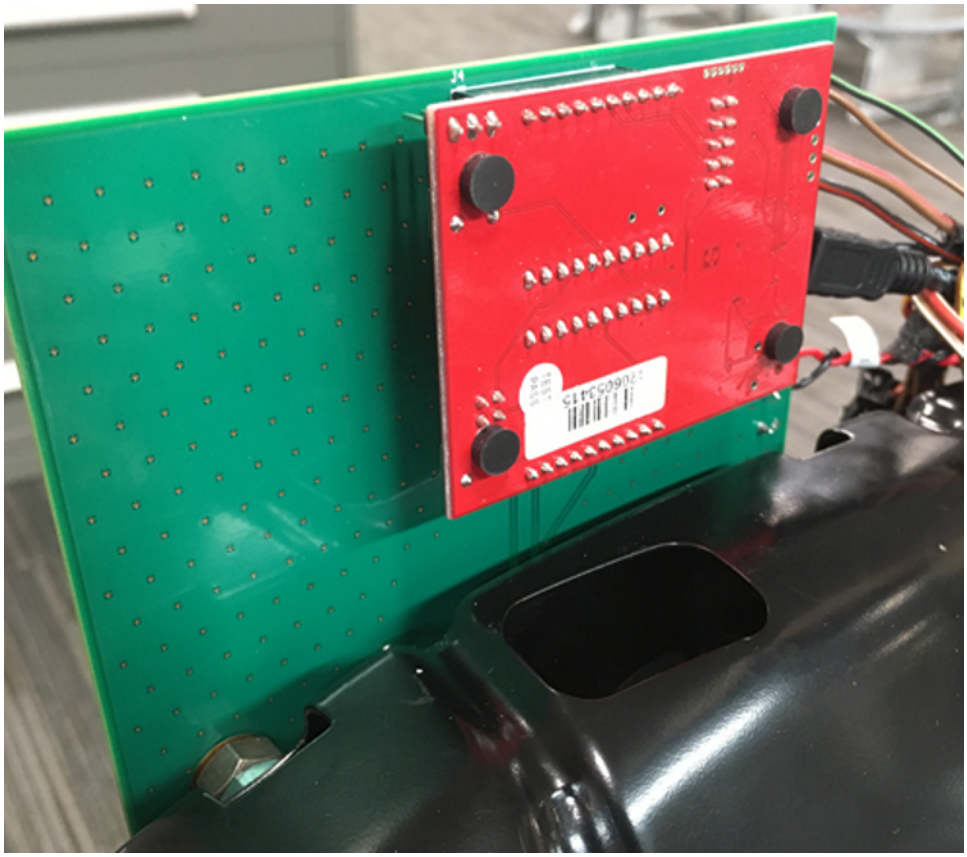


Figure 15. MSP430 LaunchPad Mounted on Back of TIDA-01330 Board

3.1.3 Power Supply

A power supply capable of supplying at least 10 A at 12 V is needed for operation of a typical power seat assembly. The actual maximum power will depend on the size and rating of the drive motors. Connect the power supply to terminal block J3, with the 12-V line on J3-2 and the 12-V return on J3-1, as shown in Figure 16.

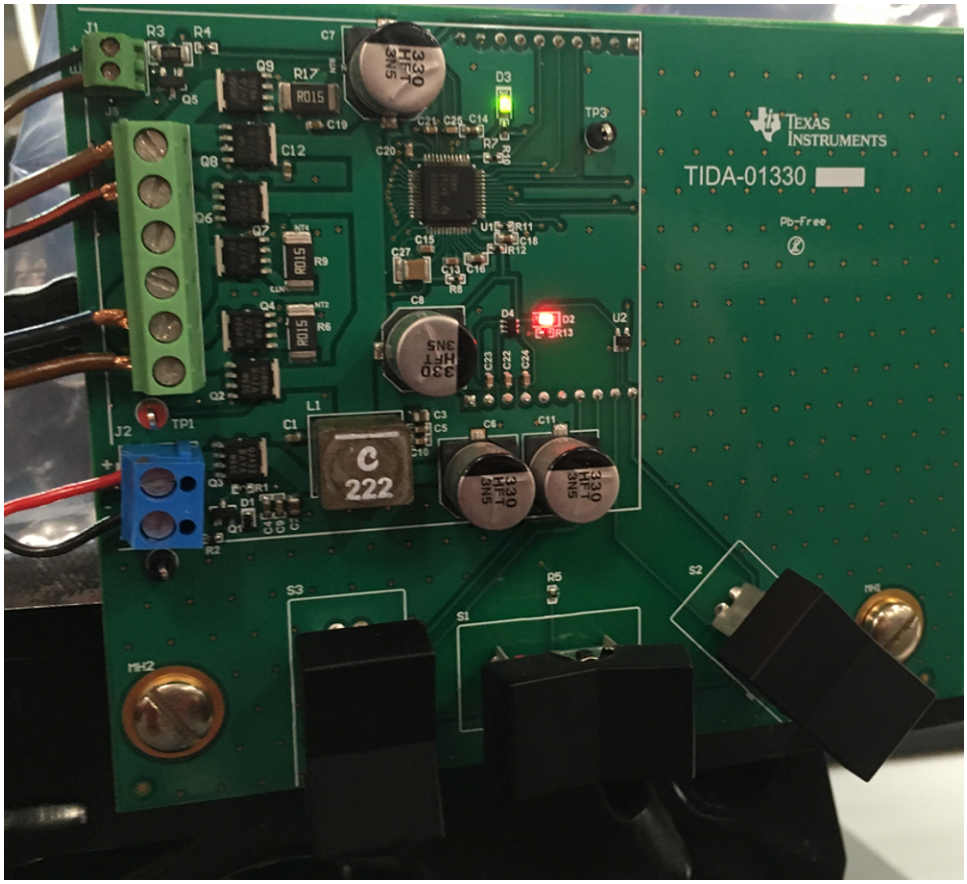


Figure 16. Wiring Connections to TIDA-01330 Board

3.1.4 Motor Connections

A six-contact terminal block (J5) provides two connection points to each of the three half-bridge driver outputs. This allows flexibility for designers to use any of the three half-bridges as the common drive phase for the two motors. The polarity of each motor connection depends on the wiring arrangement of the two phases to which it is connected. For the test results discussed in this design guide, the B-phase half-bridge output was common to both the seat forward and backward adjustment motor and the seat height adjustment motor.

3.1.5 USB Connection to PC

The MSP430 LaunchPad can be programmed and controlled using a personal computer through the USB port and onboard emulator. Find more information at http://www.ti.com/launchpad.

3.2 Software

The TIDA-01330 reference design includes a simple parallel interface that mates electrically and mechanically to the MSP430 G2553 LaunchPad. Bit-wise control of the individual inputs and outputs is implemented with simple functions that control the GPIO pins on the LaunchPad.

3.2.1 Digital Output Functions

The following functions are used to control the digital outputs from the MSP430G2553 LaunchPad to the TIDA-01330 board:

Table 4. Digital Output Functions

FUNCTION	DESCRIPTION
set_A_off()	Turn off both the high-side and low-side FETs of half-bridge A
set_B_off()	Turn off both the high-side and low-side FETs of half-bridge B
set_C_off()	Turn off both the high-side and low-side FETs of half-bridge C
set_A_high()	Turn on the high-side FET and turn off the low-side FET of half-bridge A
set_B_high()	Turn on the high-side FET and turn off the low-side FET of half-bridge B
set_C_high()	Turn on the high-side FET and turn off the low-side FET of half-bridge C
set_A_low()	Turn off the high-side FET and turn on the low-side FET of half-bridge A
set_B_low()	Turn off the high-side FET and turn on the low-side FET of half-bridge B
set_C_low()	Turn off the high-side FET and turn on the low-side FET of half-bridge C
turn_on_LED()	Turn on the npn transistor Q5 (low-side drive to LED cathode)
turn_off_LED()	Turn off the npn transistor Q5

3.2.2 Digital Input Functions

The following functions are used to read the digital inputs from the TIDA-01330 board to the MSP430 G2553 LaunchPad:

Table 5. Digital Input Functions

FUNCTION	DESCRIPTION
up_button()	Input from up contact on up and down switch
down_button()	Input from down contact on up and down switch
fwd_button()	Input from forward contact on forward and backward switch
back_button()	Input from backward contact on forward and backward switch
tiltup_button()	Input from upper contact on third switch
tiltdn_button()	Input from lower contact on third switch

In order to digitally filter the push button inputs, these signals are sampled 10 times sequentially. For example, if 9 or 10 of the samples are high, the Up_Button() function returns a logic 1. If zero or one of the samples are high, the function returns a logic 0. If the number of high samples is more than 1 but less than 9, another sequence of ten samples is taken. This method ensures that a single erroneous sample will not cause a false reading of the push buttons.

3.2.3 Analog Input Functions

Although not implemented as part of this TI Design, the current through the low side of each of the three half-bridges can be sampled by the ADCs on the MSP430. For more information about using the MSP430 ADCs, see the references listed in Section 7.

Table 6. Analog Inputs

SIGNAL	LAUNCHPAD ADC INPUT	DESCRIPTION
ISNS_A	A1 (J3-3)	Current sense from half-bridge A low-side
ISNS_B	A0 (J3-2)	Current sense from half-bridge B low-side
ISNS_C	A2 (J3-4)	Current sense from half-bridge C low-side

4 Testing and Results

4.1 Power Supplies

4.1.1 Input Power

The board should operate as expected when the applied automotive power is in the range specified for operating conditions. Further, the board should survive exposure to applied voltages specified for survivability conditions.

The function of the integrated 3.3-V supply serves to indicate board operation for the range of input supply. In the following plots, the 3.3-V supply is operational for applied input supply voltages from about 5 to 40 V. The detail plot shows that as the input supply rises from zero, the 3.3-V supply turns on when the input power is about 5.1 V, and remains stable for input supply voltages up to 40 V. As the applied input power is reduced, the 3.3-V supply drops out when the input supply drops below about 4.5 V. This hysteresis in the voltage regulator turnon prevents supply oscillation when the input power transitions.

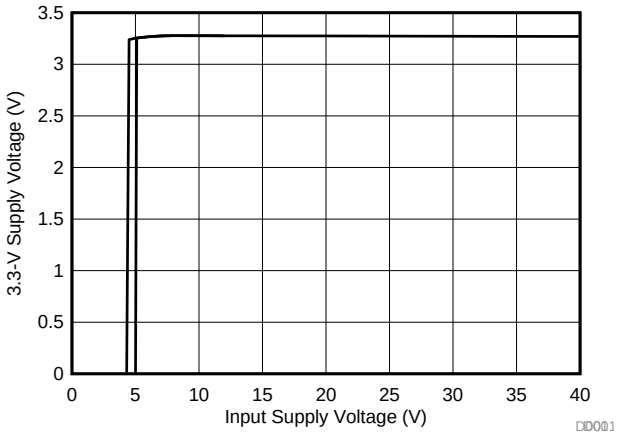


Figure 17. Board's 3.3-V Supply Operates for Wide Range of Input Supply

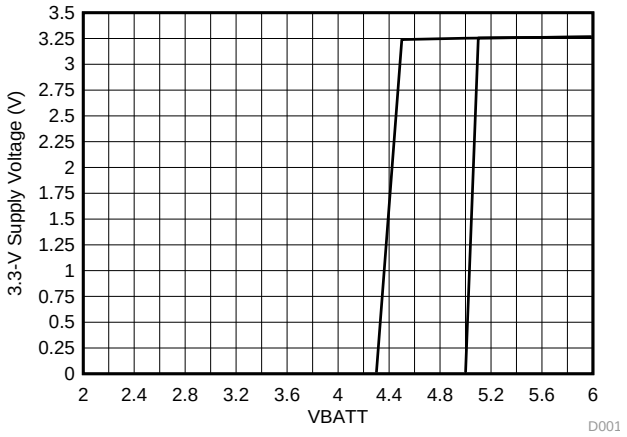


Figure 18. Detail of 3.3-V Supply Turnon and Turnoff Points, Indicating Hysteresis

When the input supply is negative, there should be no operation of the board, and the power dissipation should be very low. As shown in Figure 19, the reverse leakage current is less than 50 mA for reverse battery voltages up to –18 V.

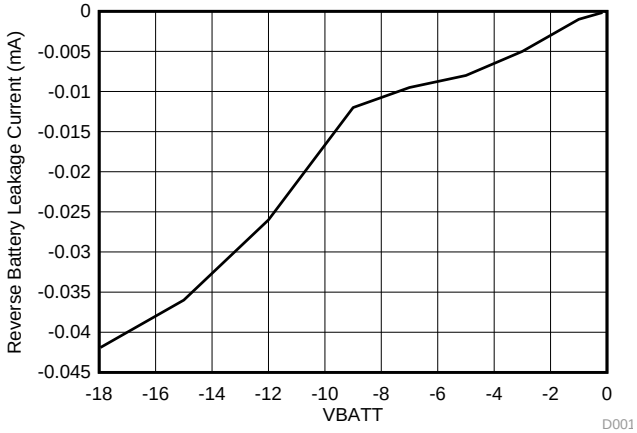


Figure 19. Reverse Battery Conditions With Very Low Input Leakage Current From Negative Supply

Table 7 shows the current from VBATT into the board under various conditions.

Table 7. Input Current From VBATT Under Various Conditions

CONDITION	CURRENT FROM VBATT	POWER DISSIPATION
Without LaunchPad, EN_GATE = Low	8 mA	96 mW
With LaunchPad idle, EN_GATE = Low	15 mA	180 mW
Without LaunchPad, EN_GATE = High	26 mA	312 mW
With LaunchPad running, EN_GATE = High	26 mA	312 mW

4.1.2 3.3-V Supply

The output voltage of the integrated 3.3-V supply has very little variation as the input supply voltage (VBATT) varies over the operational range, as shown in Figure 20. The 3.3-V supply is within 1.5% of the nominal value for all voltage in the measured range. This allows use of the supply for not only circuit biasing, but also as a reference for analog feedback signals, such as the motor current sense signals.

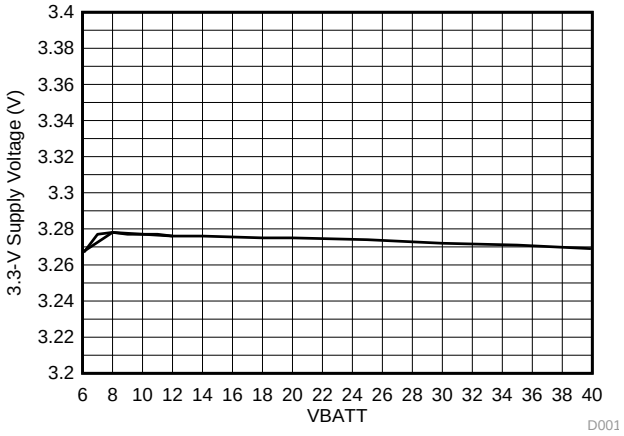


Figure 20. 3.3-V Supply Variation With Input Supply (VBATT) Over Wide Operating Range

4.2 Motor Drive

The motor drive functions were tested using an automotive seat assembly, which includes motors to adjusts the seat position (forward and back adjustment) and seat height. The seat assembly is from an Audi® A4. The brushed DC motors that move the seat are typical of this type of end-equipment.

Figure 21. TIDA-01330 Board Mounted on Test Hardware

4.2.1 Single-Motor Operation

Single-motor operation represents the most typical use case for power seats controlled by user buttons. In this case, the user adjusts either the seat in the forward or backward position or the seat height by pressing a single button. Single motor operation encompasses several phases of operation, such as the start-up phase, the normal (steady-state) phase, motor stall when a travel limit or obstacle is encountered, and variation in speed due to changes in the occupant load, mechanism geometry, or supply voltage.

4.2.1.1 Normal-Motor Operation

In normal operation, the motor has reached a steady-state speed of rotation. This is typical within a short period after the supply voltage has been switched on to any of the motors, with a constant supply and occupant load. For the test hardware used in this TI Design, the forward and backward carriage exhibited a steady-state motion at a speed of about 0.6 in (15 mm) per second. The height adjustment exhibited similar operation, but due to the geometry of the mechanism, the adjustment speed varied nonlinearly over the range of travel.

4.2.1.2 Motor Speed Variation

The speed of a brushed DC motor varies with increasing speed as the applied voltage is increased and decreasing speed as the load torque is increased. This was tested for the horizontal (forward or backward) adjustment with results shown in Figure 22. This plot shows the variation in the seat adjustment speed as the automotive battery voltage (12 V nominal) was varied between 6 and 20 V. The two traces indicate the limit-to-limit travel time in either the forward or backward direction. Total travel length is about 10 in (25 cm) for the test hardware used. There is little difference between the forward speed and backward speed. There was no load other than the seat mechanism itself for these tests.

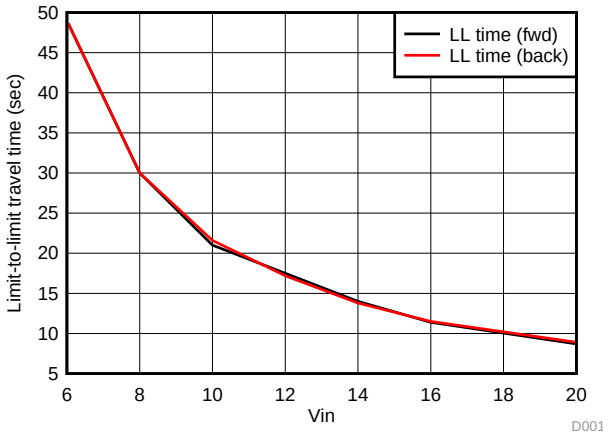


Figure 22. Seat Horizontal (Forward and Back) Adjustment Speed Varies With Applied Supply Voltage

The vertical seat adjustment shows somewhat similar results as the horizontal adjustment. Figure 23 shows the variation in vertical adjustment speed as the input supply (VBATT) is varied between 10 and 14 V. However, these measurements do indicate a difference between the horizontal and vertical adjustments; in the horizontal adjustment measurements, there is very little difference between the forward speed and the backward speed, but in the vertical adjustment measurements, there is significant difference between the upward speed and the downward speed.

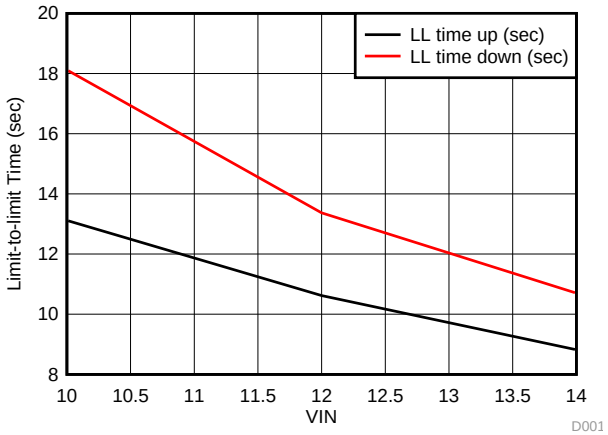


Figure 23. Seat Vertical (Up and Down) Adjustment Speed Varies With Applied Supply Voltage

One explanation for the variation in speed upward and downward is that the seat mechanism is designed for adjustment while occupied. Examination of the vertical adjustment mechanism reveals a wound torsion spring inserted in the mechanical axis, as shown in Figure 24. This spring applies a torque to the mechanism that tends to raise the seat height. As such, the downward force due to the weight of the seat and occupant are counter-balanced. The inclusion of this spring explains the observed data—when there is no seat occupant, the spring torque applies an upward bias to the mechanism, thus the downward speed is slower than the upward speed.

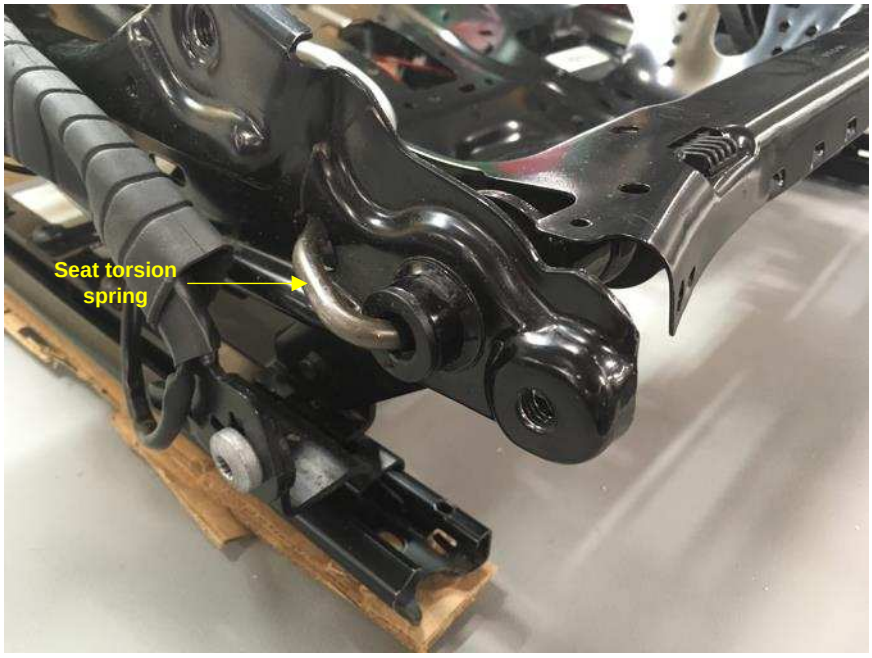


Figure 24. Torsion Spring Applies Upward Bias to Seat Height Adjustment Torque

To verify that the spring bias was counterbalancing the vertical load, additional measurements were taken with an occupant in the seat. This applied a downward force of about 80 kg during the operation of the seat adjustment. The results shown in Figure 25 and Figure 26 show that both the upward and downward speeds are affected by the load of the occupant, as expected. From these plots, the upward speed decreased and the downward speed increased when the occupant load was applied. Based on the crossover point where the upward and downward travel time (limit to limit) was equal, the torsional spring applies an upward torque corresponding to an occupant load of approximately 45 kg.

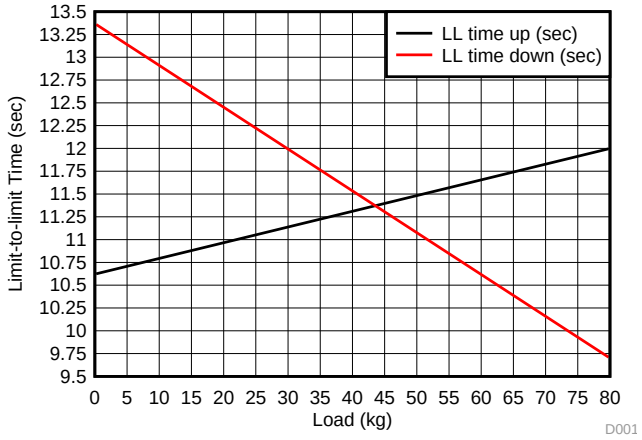


Figure 25. Variation of Up and Down Speed versus Seat Load, VBATT = 12 V

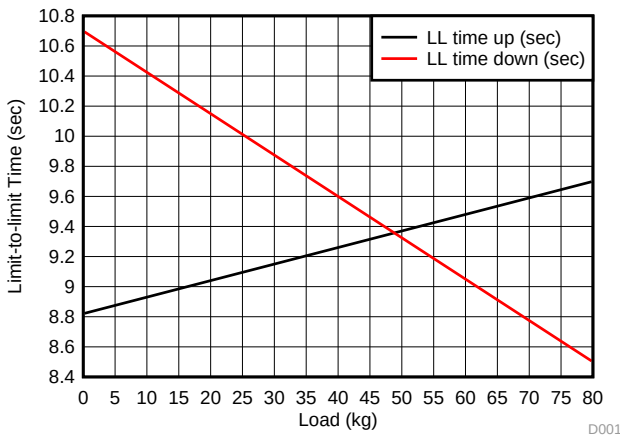


Figure 26. Variation of Up and Down Speed versus Seat Load, VBATT = 14 V

4.2.1.3 Motor Start-up

In the software code used for testing, the pushbuttons are continuously monitored until a button signal is detected. At that point the corresponding motor is activated by sending GPIO signals to the DRV8305-Q1, which turns on one high-side FET and one low-side FET. However, because the mechanical pushbutton switches can exhibit switch bounce, the signals from the switches are digitally filtered. The effect of this filtering is shown in Figure 27 where the switch signal is shown in blue on trace 1, and exhibits several cycles of switch bounce. Trace 2 in pink is the low-side drive to the corresponding motor, which does not react to the first switch transition.

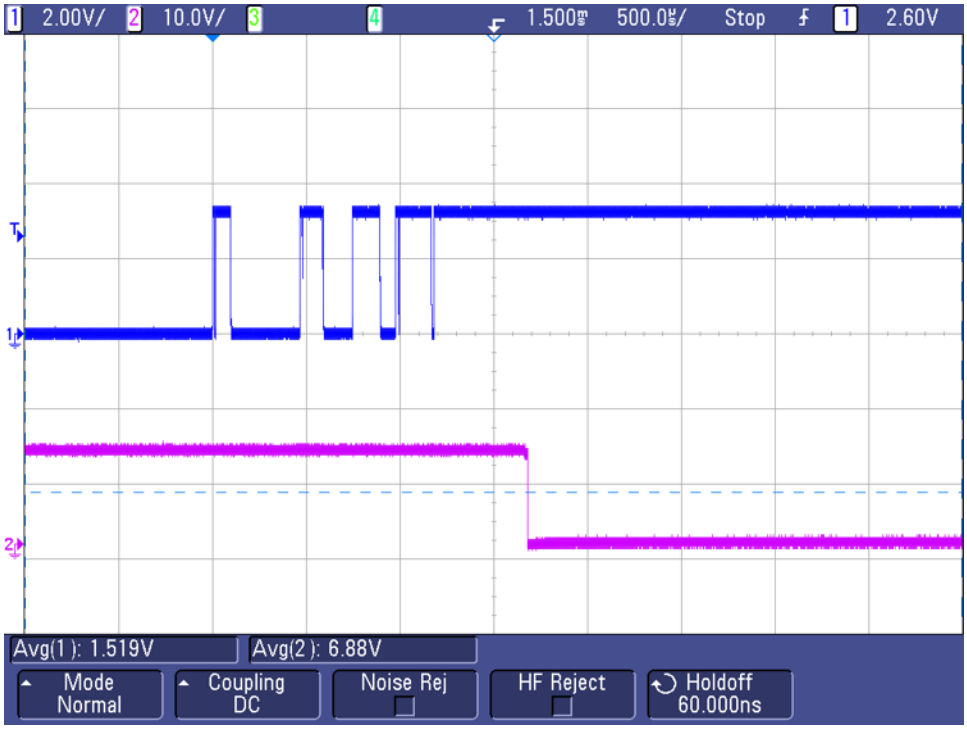


Figure 27. UP Button Signal (Channel 1: Blue) Exhibits Switch Bounce, Filtered Before Causing Motor Voltage (Channel 2: Pink) to Drive Low

Once the motor is switched on, the motor current makes an initial large transition, followed by a reduction to the steady-state value as the motor rotation reaches normal speed. This is illustrated in Figure 28 where channel 1 in blue is the amplified motor current signal ISNS_A. At this point, the scale factor of ISNS_A is 150 mV/A. The current signal is offset to half-supply (about 1.65 V), which is indicated by the horizontal cursor. The polarity of the current signal is such that a low-side current from the motor causes a decrease in the signal voltage from the 1.65-V reference point. Channel 2 is the corresponding low-side motor voltage MOT_A, which drops from 12 V to about zero when the motor is activated.

When first activated, the motor is not turning, so there is no back EMF due to rotation. Thus the motor current increases rapidly, with a curve set by the winding inductance and resistance. As the motor begins to turn, the back EMF is proportional to the speed, and the current begins to decrease. As the motor speed reaches a steady state, the current is centered about 150 mV below the 1.65-V reference, indicating about 1 A of motor current. The signal also exhibits significant ripple as the brushed motor rotates, which is expected as the windings and permanent magnet field move with relation to each other. The fundamental frequency of the current ripple can be used as an indicator of motor speed.

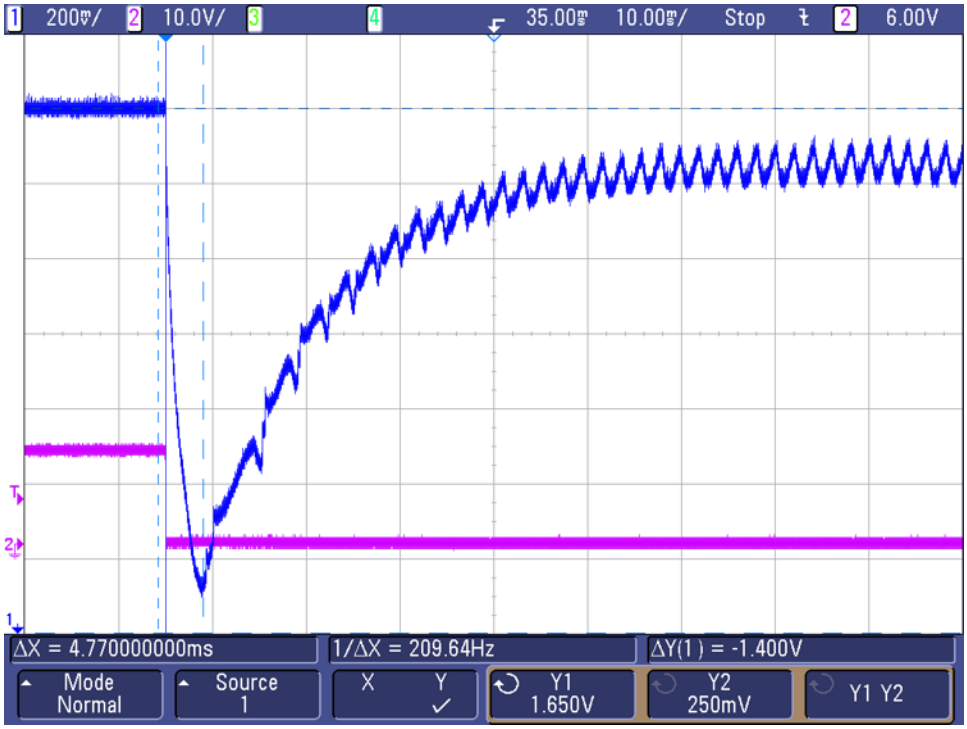


Figure 28. Motor Start-up With Motor Current Sense (Channel 1: Blue) and Motor Low-Side Voltage (Channel 2: Pink)

Figure 29 is an detail of the first few milliseconds of motor operation. Here the curve of the initial motor current shows the typical shape associated with a first-order LR circuit. In this case, the electrical time constant of the motor winding inductance (L) and winding resistance (R) is such that the current reaches a maximum at about 1.4 ms.

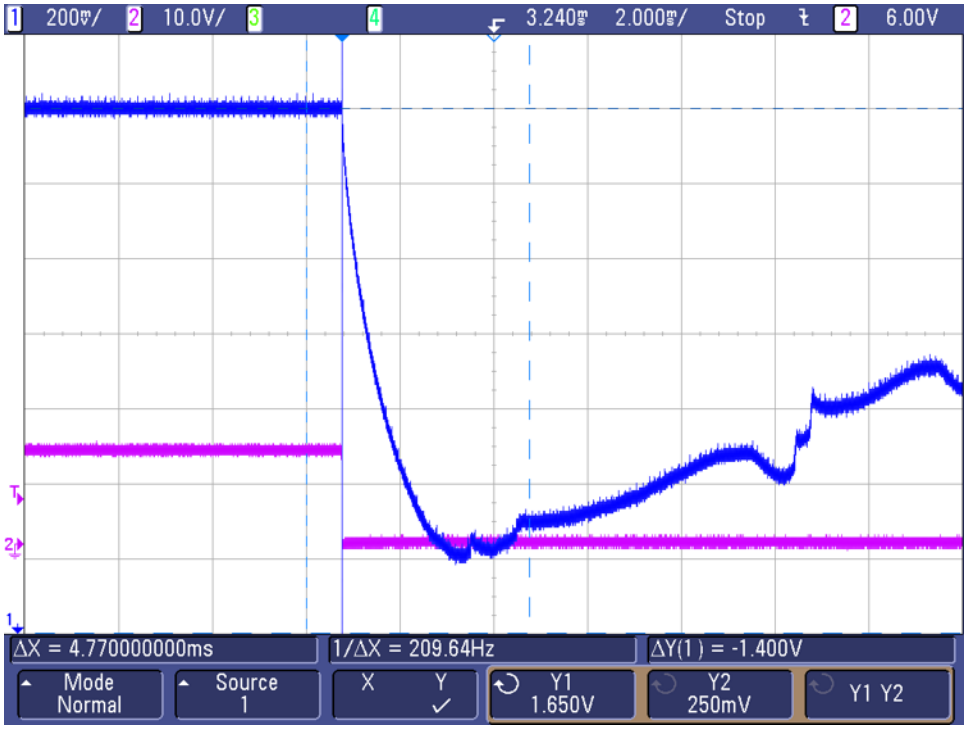


Figure 29. Detail of Motor Start-up Showing Initial Transient on Motor Current Sense (Channel 1: Blue) and Motor Low-Side Voltage (Channel 2: Pink)

4.2.1.4 Motor Stall

When the seat mechanism reaches a limit of mechanical travel, the motor will stall, causing the back EMF to decrease, and the motor current will increase to a limit set by the drive circuit and the resistance of the motor windings. This current increase can be monitored and used to detect when the motor has stopped.

Figure 30 shows this process, with the motor current signal in blue on Channel 1 moving away from the 1.65-V zero-current reference as the motor comes to a stop. The motor speed can be inferred from the ripple peaks, which become more widely spaced as the motor slows. In the middle of Figure 30, the motor has come to a stop, and the steady-state stall current is about 1.4 V × (1 A / 0.15 V) = 9.3 A.

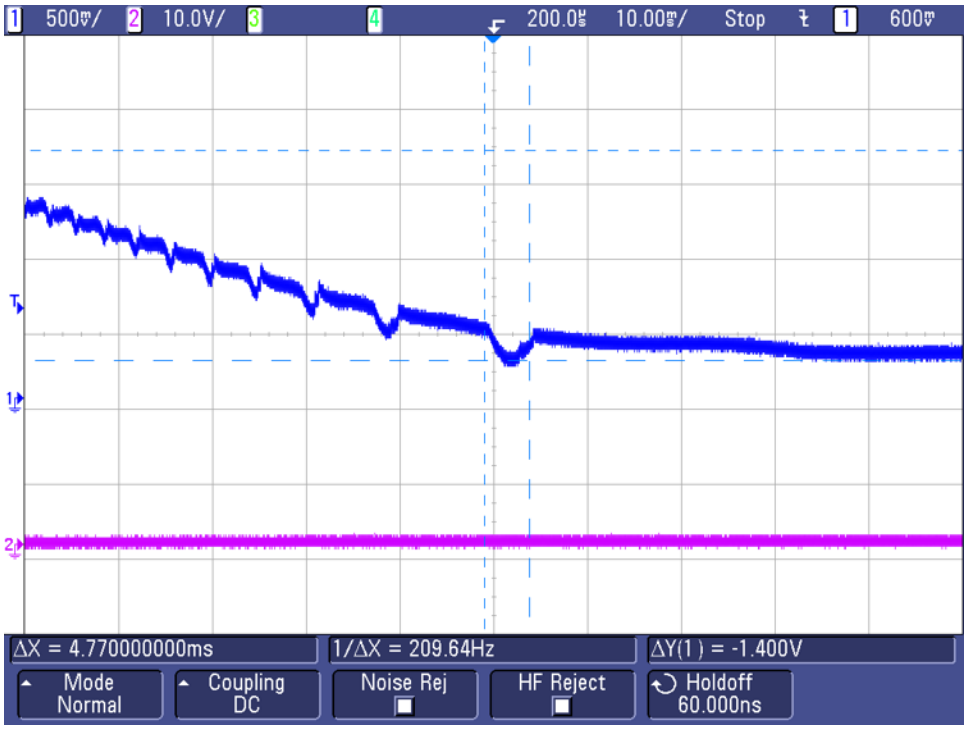


Figure 30. Motor Stall Showing Current Sense (Channel 1: Blue)

The stall current can be used to detect when the motor has reached a mechanical limit, or run into an obstacle. However, recall from Figure 29 that there is also an initial current spike when the motor is first activated. So either the stall current limit threshold must be carefully determined to differentiate from the initial current spike, a time-dependent filter must be applied to avoid tripping during the initial spike, or some combination of these two elements.

4.2.2 Two-Motor Operation

To operate both motors at the same time, there are two cases to be considered. In one case, the shared half-bridge need not change state when driving the two motors. In the second case, the shared half-bridge must change state when driving the two motors.

In the first case, half-bridge B can be set to either high or low, depending on the direction of motion, and half-bridges A and C will be the complementary state (low or high) of half-bridge B.

For the second case, when the shared half-bridge must change state, both motors can be operated by applying alternating voltages to the motor A, B, and C outputs as discussed in Section 2.6.

Figure 31 illustrates the eight states of driving either one or two motors, with the corresponding states of the A, B, and C half-bridges. In two of the two-motor cases, [Up and Forward] and [Down and Backward], the shared B half-bridge must switch between the high-output state and the low-output state to drive the two motors. In the other two two-motor states, [Up and Backward] and [Down and Forward], the shared B half-bridge need not switch because both motors need the same state for driving in the selected direction.

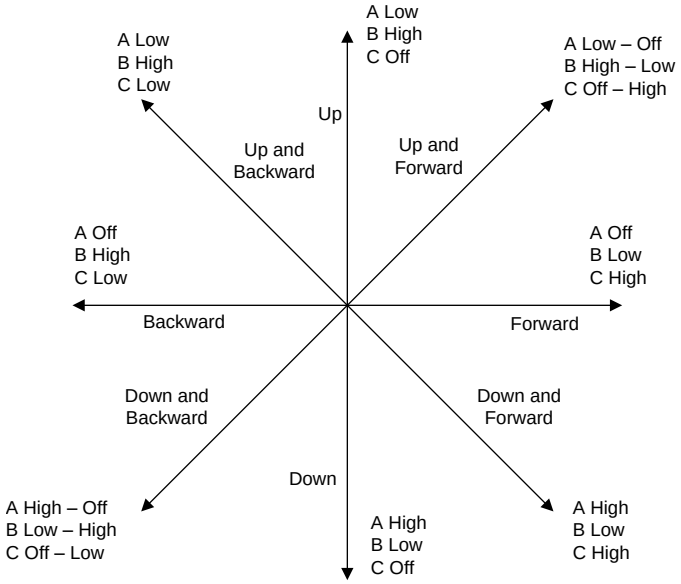


Figure 31. TIDA-01330 Seat Directions and Motor Phase Polarities

In the following figures, the effect of varying the dwell time between switching the polarity of the shared half-bridge is examined. Dwell time is the period during which one motor is being actively driven and the other motor is not being actively driven. In all the following cases, the dwell time for each of the two motors is equal, thus the drive voltage to each motor is approximately 50% of the applied VBATT. During the transition between driving one motor and the other, there is dead-time when neither motor is actively driven. This is necessary to avoid current flowing directly through any half-bridge from PVDD to GND, also called shoot-through current. As the dwell time for each motor is reduced, the dead-time becomes a larger fraction of the total, reducing the overall drive voltage for the motors.

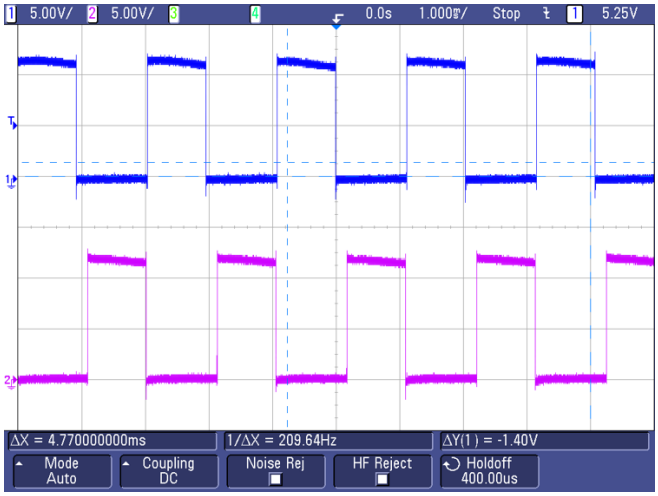


Figure 32. Two-Motor Operation With 1000-Cycle Dwell

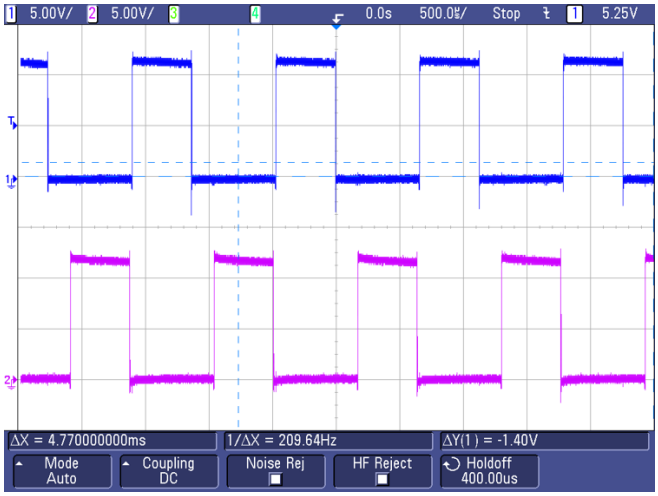


Figure 33. Two-Motor Operation With 500-Cycle Dwell (High-Side)

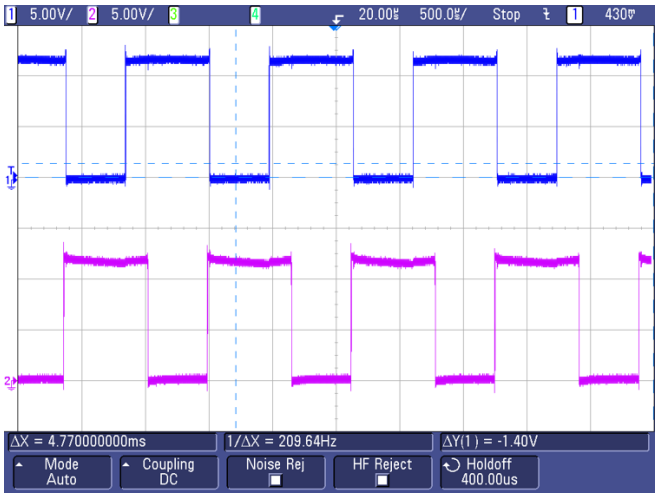


Figure 34. Two-Motor Operation With 500-Cycle Dwell (Low-Side)

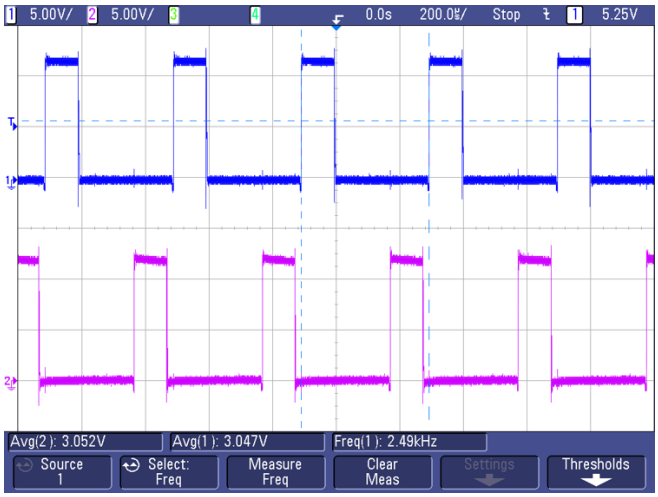


Figure 35. Two-Motor Operation With 100-Cycle Dwell

4.3 Seat Vibration Using Motor

One feature possible with this TI Design is vibration of either motor or both. The rapid driving of either motor in a reciprocating motion causes both an audible noise and tactile vibration. This feature can be used to alert the occupant of a potential problem such as lane departure, or drowsy driver, as detected by an onboard vision system.

For the particular test hardware used for this design guide, the height adjustment motor and geartrain seemed to give a better response to rapid reciprocating drive. Figure 36 shows the motor voltages on MOT_A and MOT_B while the height adjustment motor was being driven rapidly up and down. For the particular software setting shown, the period of vibration is about 27 Hz, which provided both an audible rumble and an easily detected vibration of the seat mechanism.

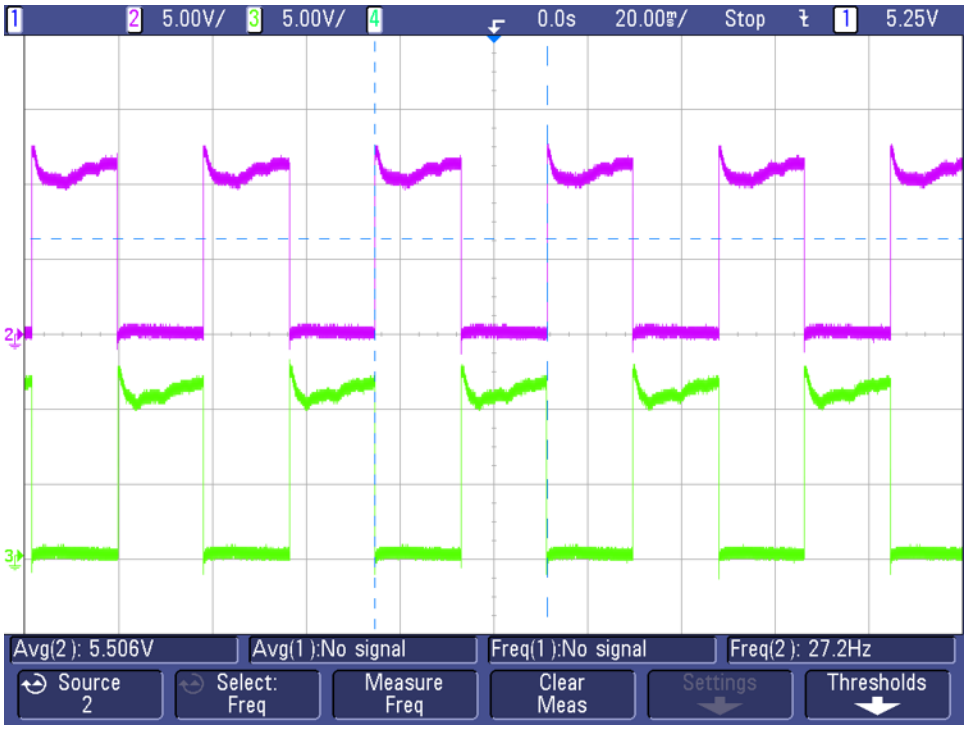


Figure 36. Height Adjustment Motor Voltages During Seat Vibration

4.4 Diagnostics

Several diagnostic features are available in this TI Design, including measurements of the current through each motor, the temperature, and checks on the 12-V supply and drain-to-source voltage of each half-bridge. The current sense for each motor is provided to the LaunchPad microcontroller ADC, the other diagnostic features are accessible through the registers of the DRV8305-Q1.

4.4.1 Motor Current Sense

The motor current flows through a 15-mΩ resistor on the low-side drive circuit of each half-bridge. The voltage across the sense resistor is then amplified by the integrated current sense amplifiers in the DRV8305-Q1, with a differential gain of 10, and an offset voltage equal to half the 3.3-V supply. This gives an overall scale factor of 150 mV/A with a 1.65-V offset at the input to the microcontroller ADC.

$$V_{Current\_Sense} = \frac{V_{3.3V\_Supply}}{2} - I_{Motor} \times 150 \frac{mV}{A} \quad (1)$$

The current sense circuit was tested by turning on one of the low-side FETs (Q4), and applying a test voltage to the corresponding output phase (MOT_A). This causes a current through the sense resistor (R6). The current sense signal (ISNS_A) is then measured at the input to the microcontroller ADC (J3-3).

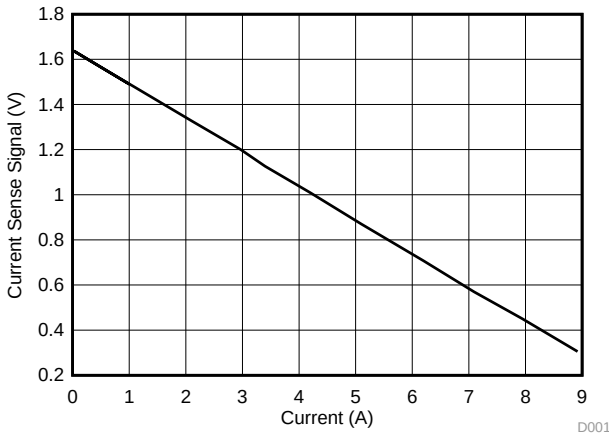


Figure 37. Test Results for Current Sense Circuit

4.4.2 Temperature Sense

A multi-level temperature detection circuit is implemented in the DRV8305-Q1. Depending on the temperature detected by the internal sensor, a warning or fault may be indicated in the device register, the nFAULT signal, or by shutting down the device.

- Flag Level 1 (TEMP_FLAG1): Level 1 over-temperature flag. No warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D3.
- Flag Level 2 (TEMP_FLAG2): Level 2 over-temperature flag. No warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D2.
- Flag Level 3 (TEMP_FLAG3): Level 3 over-temperature flag. No warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D1.
- Flag Level 4 (TEMP_FLAG4): Level 4 over-temperature flag. No warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D8.
- Warning Level (OTW): Over-temperature warning only. Warning reported on nFAULT. Real-time flag indicated in SPI register 0x1, bit D0.
- Fault Level (OTSD): Over-temperature fault and latched shut down of the device. Fault reported on nFAULT and in SPI register 0x3, bit D8.

SPI operation is still available, and register settings will be retained in the device during OTSD operation as long as PVDD is within operation range. An OTSD fault can be cleared when the device temperature has dropped below the fault level and a CLR_FLTS is issued. During testing, the temperature was not intentionally elevated to trigger any temperature warnings or faults. The nFAULT signal was monitored by means of the red LED to determine if any faults had been detected by the DRV8305-Q1.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01330.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01330.

5.3 PCB Layout Recommendations

Because the motors require relatively high currents, up to 10 A, case should be taken in designing the traces for the high currents. For example, PVDD is the trace that brings the filtered 12-V nominal supply to the half-bridges. As shown in Figure 38, the high-current traces for PVDD are all on the top layer, and are wide to allow high current with low resistance and low power dissipation. The highlighted green section of PVDD trace is 150 mils (6 mm) wide. The traces of PVDD that branch off to the high-side FETs of each half-bridge are also kept as short as possible.

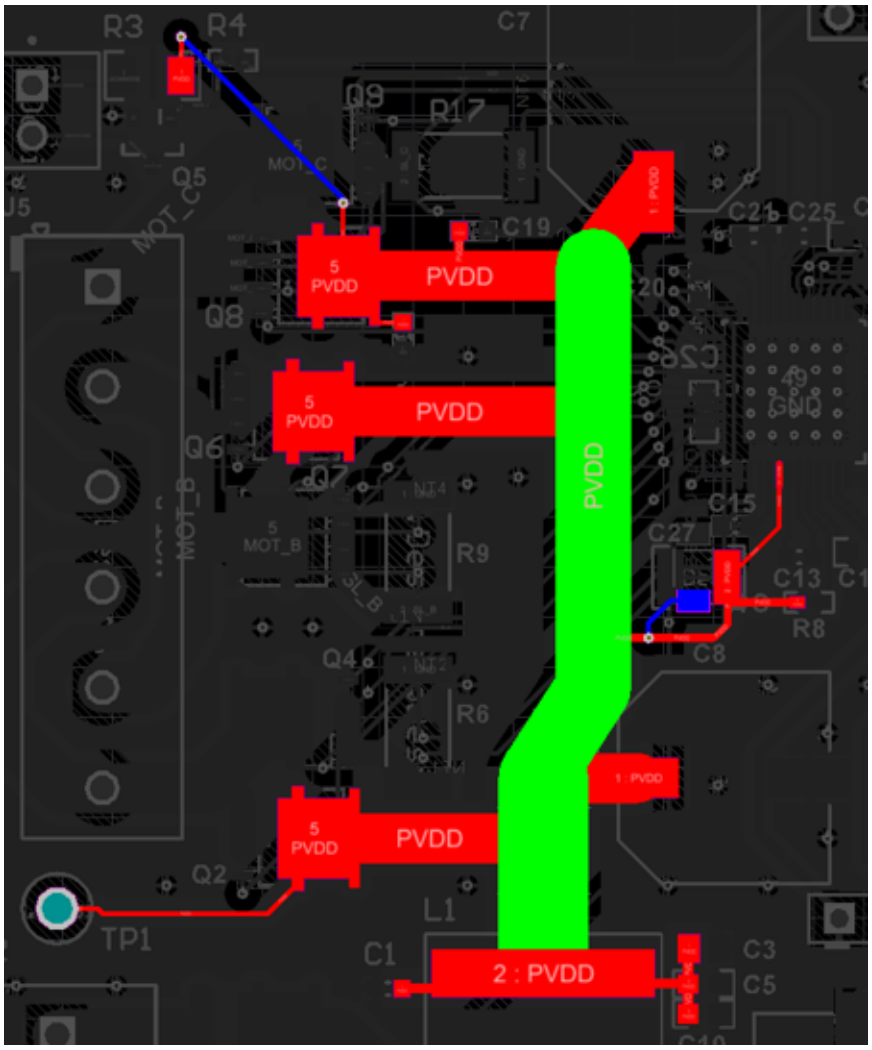


Figure 38. PVDD Traces are Wide to Carry High Currents

The traces for the signals from the output of each half-bridge to the motor connector pins are also wide and short, for low resistance while carrying high currents. These are shown in Figure 39, Figure 40, and Figure 41.

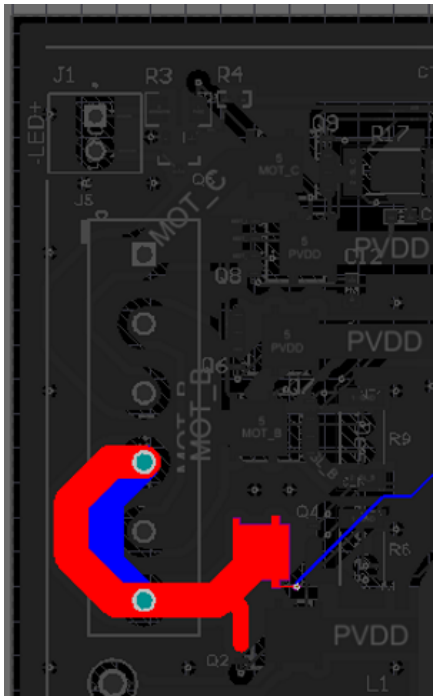


Figure 39. MOT_A Trace

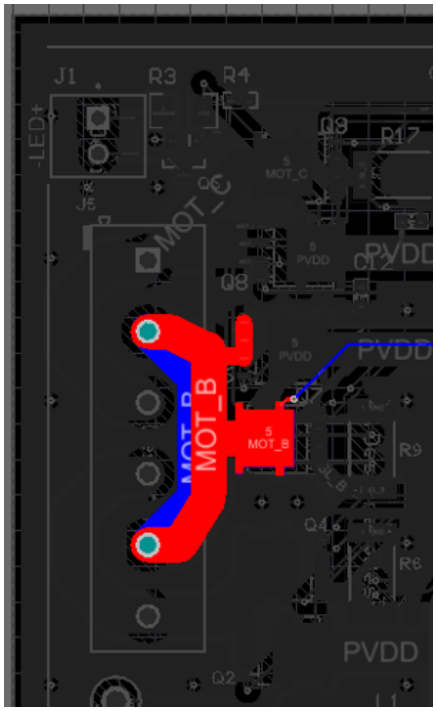


Figure 40. MOT_B Trace

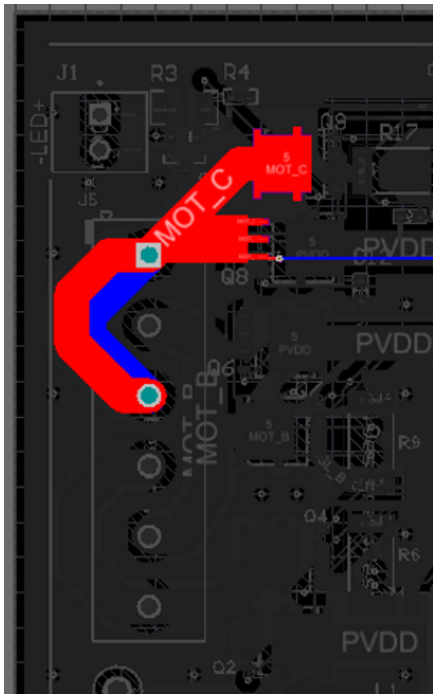
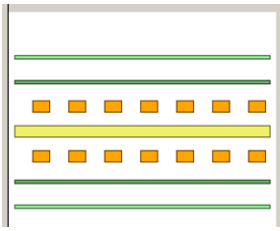


Figure 41. MOT_C Trace

In order to reduce manufacturing costs, the board is fabricated with only two signal layers. The copper thickness of the top and bottom signal layers are 3.6 mils (2-oz. copper plus plating). This allows high currents in the traces without excessive temperature rise.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Cov...	Surface Material	0.4	Solder Resist	3.5
Top Layer	Signal	Copper	3.6		
Dielectric1	Dielectric	Core	55	FR-4	4.8
Bottom Layer	Signal	Copper	3.6		
Bottom Solder	Solder Mask/Cov...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

Figure 42. PCB Layer Stack-up

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01330.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01330.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01330.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01330.

6 Software Files

To download the software files, see the design files at TIDA-01330.

7 Related Documentation

1. Texas Instruments, *DRV8305-Q1 Three-Phase Automotive Smart Gate Driver With Three Integrated Current Shunt Amplifiers and Voltage Regulator*, DRV8305-Q1 Datasheet (SLVSD12)
2. Texas Instruments, *MSP430G2x53 Automotive Mixed-Signal Microcontrollers*, MSP430G2553-Q1 Datasheet (SLAS966)
3. Texas Instruments, *Automotive Catalog Single Two-Input Positive-NAND Gate*, SN74AHC1G00-Q1 Datasheet (SLOS424)
4. Texas Instruments, *Introduction to MSP430 ADCs*, Seminar (SLAP115)

7.1 Trademarks

8 Terminology

ADC— Analog-to-digital converter

BDC Motor—Brushed direct-current motor

GPIO— General purpose input/output

Half-bridge— The combination of a high-side and low-side switch, typically implemented with two transistors such as FETs

LED— Light emitting diode

PWM— Pulse-width modulation

SPI— Serial peripheral interface, a common chip-to-chip communication implementation

TINA— An analog simulation program; TINA-TI is available free from Texas Instruments (http://www.ti.com/tool/tina-TI)

9 About the Author

CLARK KINNAIRD is a systems applications engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, Clark works on various types of motor drive end-equipment, creating reference designs for automotive manufacturers. Clark earned his bachelor of science and master of science in engineering from the University of Florida, and his Ph.D. in electrical engineering from Southern Methodist University.

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