TI Designs

High-Precision Reference Design for Buffering a DAC Signal

Description

This reference design features the industry's first zero-crossover and zero-drift amplifier (OPA388) to buffer the analog output of a digital-to-analog converter (DAC). It demonstrates the importance of the zero-crossover and zero-drift feature and how they can minimize the integral nonlinearity (INL) of the system as well as make use of the full-scale range of the DAC (DAC8830).

Resources

TIDA-01402	Design Folder
OPA388	Product Folder
DAC8830	Product Folder
REF5050	Product Folder

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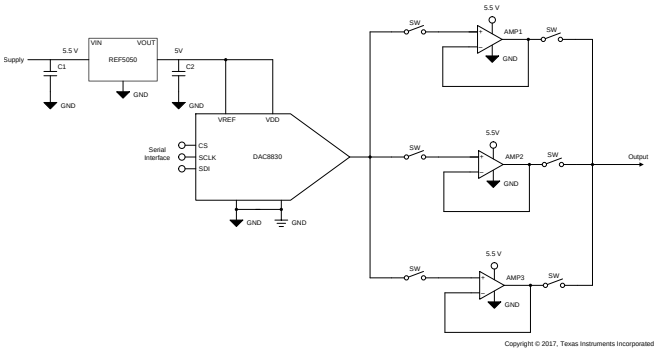
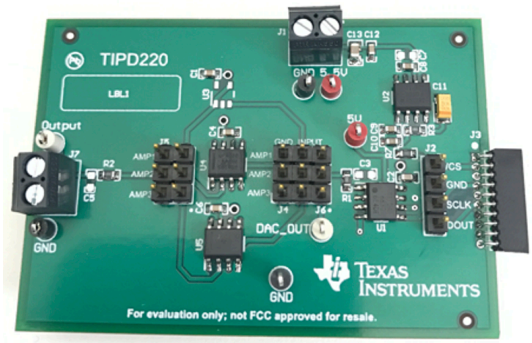
Features

- 16-Bit Resolution Digital Input Output Driver
- 2.7- to 5.5-V Single-Supply Operation
- High Accuracy, INL < 0.5 LSB
- Fast SPI, up to 50 MHz
- Industry-Standard Pin Configuration
- OPA388 Zero-Crossover, Zero-Drift Amplifier

Applications

- Field Transmitter
- Data Acquisition
- Wireless Infrastructure
- Test and Measurement





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1 System Overview

1.1 System Description

This TI reference design features a precision voltage-output digital-to-analog converter (DAC) that provides excellent linearity and a buffered output with different precision operational amplifiers. This TI Design demonstrates the importance of having an op amp with zero-crossover and zero-drift to minimize the integral nonlinearity (INL) of the system, giving a precision analog output. The design provides a solution of linearization throughout the full scale range of the DAC using a zero-crossover, zero-drift device as the buffered output. This design guide addresses component selection, design theory, and test results of the TIDA-01402 reference design. The following subsections describe the various devices within this reference design system and highlight the characteristics most critical in implementing the corresponding functions.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Resolution	16-bit resolution
Output range	0 V_{REF}
Linearity error	INL < 0.5 LSB
DNL	0.5 LSB
Gain drift	0.1 ppm/°C
Zero-crossover	140-dB CMRR True RRIO

1.3 Block Diagram

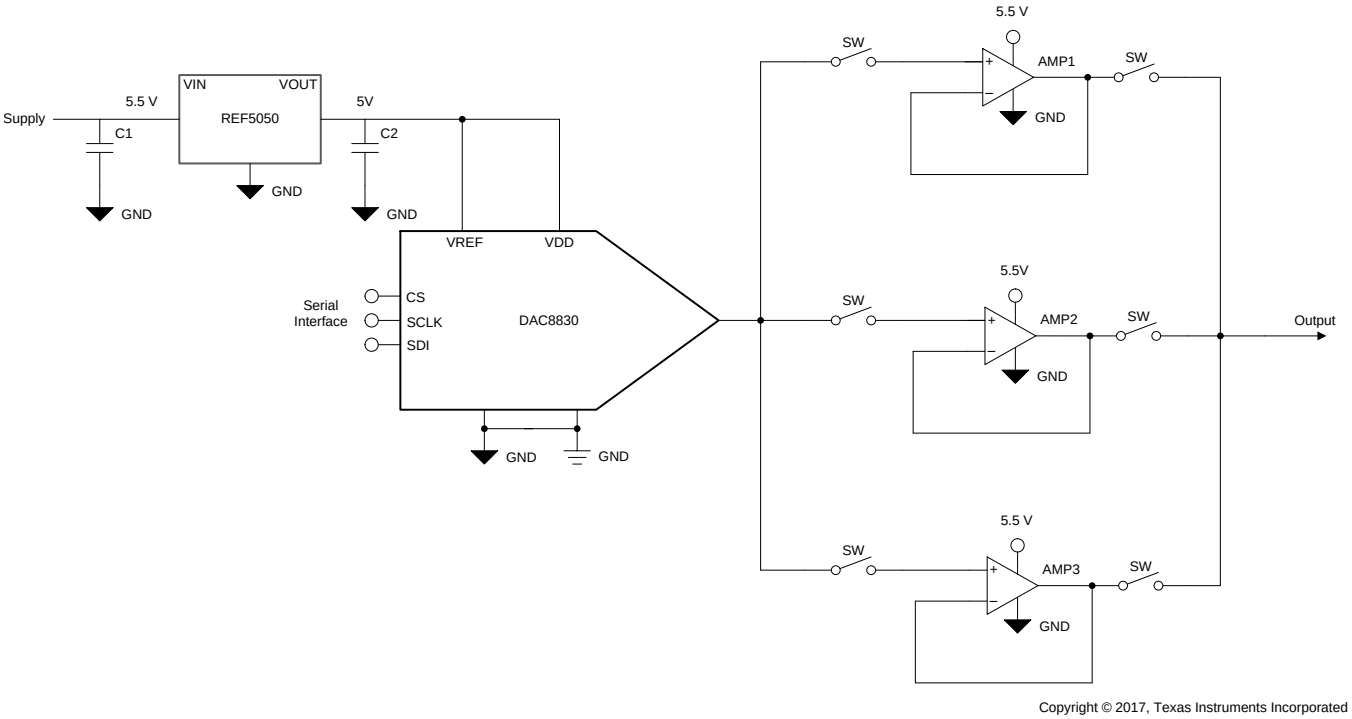

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Figure 1. TIDA-01402 Block Diagram

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1.4 Highlighted Products

The TIDA-01402 reference design features the following devices:

- OPA388 (Section 1.4.1): Precision, Zero-Drift, Zero-Crossover, True RRIO Operational Amplifier
- DAC8830 (Section 1.4.3): 16-Bit, Single-Channel, Ultra-Low-Power, Voltage Output DAC
- REF5050 (Section 1.4.4): 3 µVpp/V Noise, 3 ppm/°C Drift Precision Voltage Reference

For more information on each of these devices, see their respective product folders at TI.com.

1.4.1 OPA388

The OPAx388 is a family of ultra-low-noise, zero-drift, zero-crossover, rail-to-rail input and output op amp. These devices operate from 1.8 to 5.5 V, excellent AC performance, and only 0.25 µV of offset and 0.005 µV/°C of drift over temperature. The OPAx388 is ideal for driving high-precision, analog-to-digital converters (ADCs) or buffering the output of high-resolution, DACs, as well as a wide range of general purpose applications.

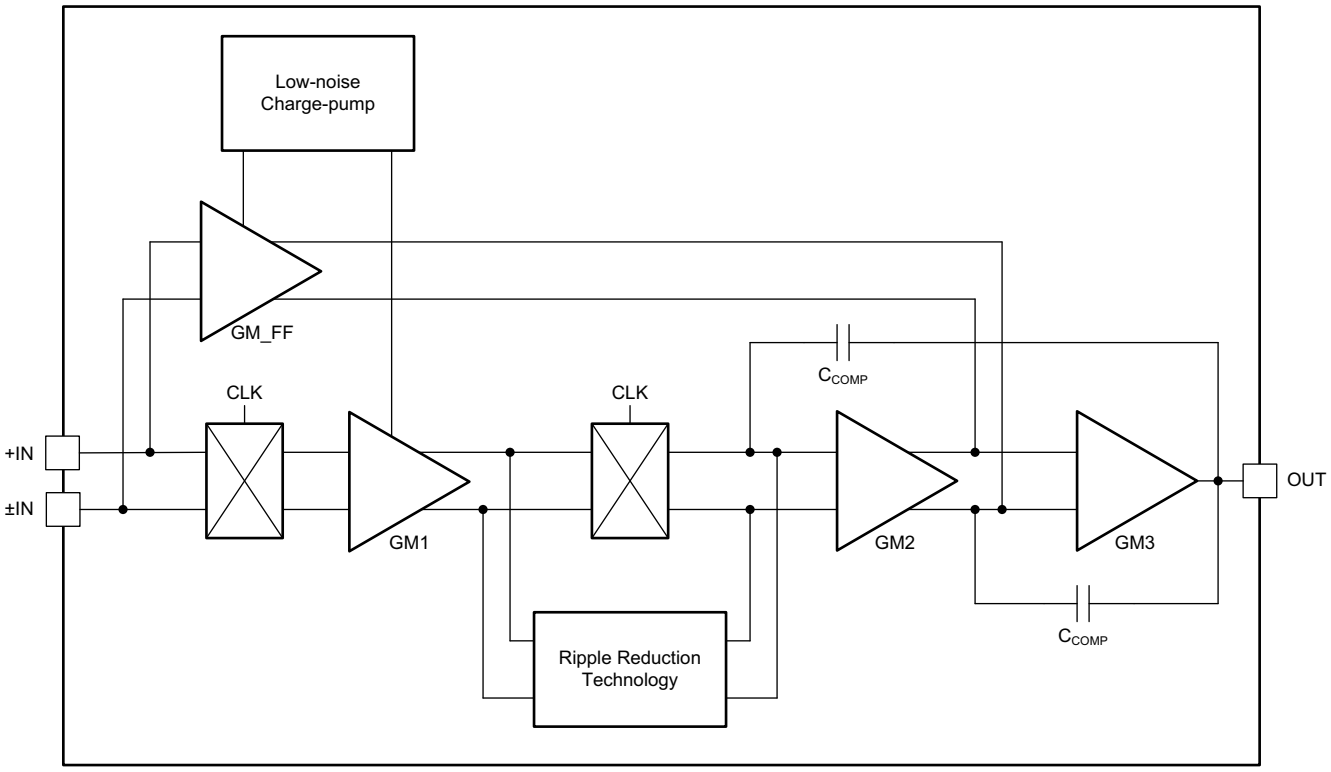

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Figure 2. OPA388 Functional Block Diagram

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1.4.2 OPA340

The OPA340 device operates on a single supply as low as 2.5 V with an input common-mode voltage range that extends 500 mV below ground and 500 mV above the positive supply. Output voltage swing is to within 1 mV of the supply rails with a 100-kΩ load. These devices offer excellent dynamic response (BW = 5.5 MHz, SR = 6 V/µs), yet the quiescent current is only 750 A. The devices class AB output stage is capable of driving 600-Ω loads series and extends 500 mV beyond the supply. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications.

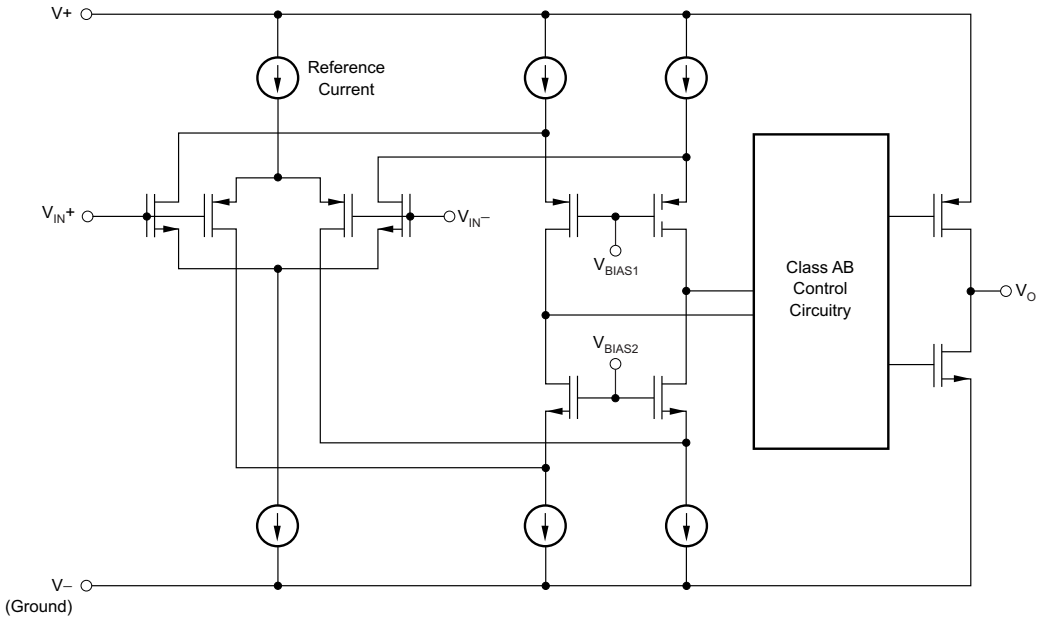

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Figure 3. OPA340 Functional Block Diagram

1.4.3 DAC8830

The DAC8830 is a single, 16-bit, serial-input, voltage-output DACs operating from a single 3- to 5-V power supply. This device provide excellent linearity (1 LSB INL), low glitch, low noise, and fast settling (1.0 µS to 1/2 LSB of full-scale output) over the specified temperature range of –40°C to 85°C. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer. The DAC8830 output is 0 V to V_{REF}.

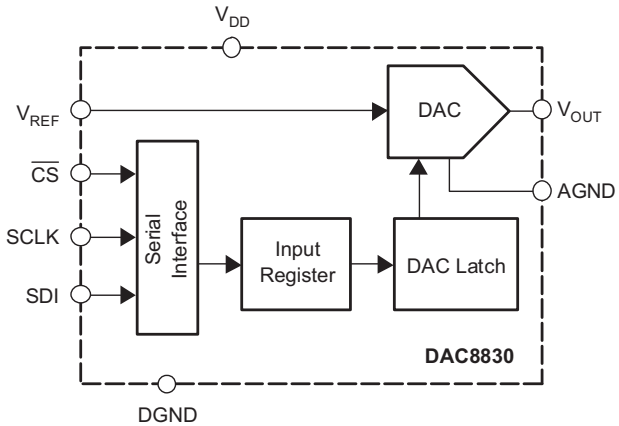

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Figure 4. DAC8830 Functional Block Diagram

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1.4.4 REF5050

The REF5050 is a low-noise, low-drift, very high precision voltage reference. This reference is capable of both sinking and sourcing current, and has excellent line and load regulation. Excellent temperature drift (3 ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. These features, combined with very low noise, make the REF5050 ideal for use in high-precision data acquisition systems.

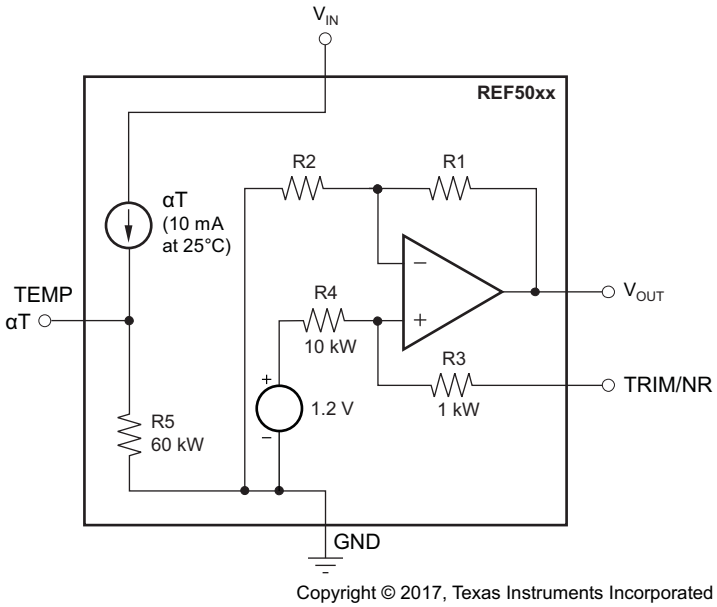

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Figure 5. REF5050 Functional Block Diagram

1.5 Design Theory

INL is the maximum deviation between the ideal output of a DAC and the actual output level after offset and gain error have been calibrated out of the measurement. This specification is important for measuring error in a DAC. For applications that require extremely high precision, INL is the most valuable specification to consider. This is because there is no way to externally compensate INL like one can offset, gain, and zero-code errors. This means for high-precision applications picking a DAC with high linearity such as the DAC8830 is vital as well as the amplifier chosen for the buffered output. The datasheet of the DAC8830 recommends an operational amplifier with low-offset to eliminate the need of offset trims. With a 16-bit DAC and 5-V reference, the LSB voltage is 76 µV.

Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately 6.25 kΩ) adds to the zero-code error. Rail-to-rail input and output performance are required. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but in order to minimize gain errors the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3-dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3-dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier. The OPA388 and OPA340 both meet these requirements as shown in Table 2; however, the OPA340 will effect the INL because it has a crossover region due the two-input differential pairs needed to achieve rail-to-rail input. The OPA388 is a zero-crossover part that uses a charge-pump topology resulting in no crossover region that would effect the INL.

Table 2. Specification Comparison of OPA388 and OPA340

DEVICE	V_{OS} TYPICAL (µV)	INPUT BIAS CURRENT TYPICAL (pA)	RAIL-TO-RAIL	SLEW RATE (V/µS)	UNITY GAIN BANDWIDTH (MHz)
OPA388	±0.25	±30	RRIO	5	10
OPA340	±150	±0.2	RRIO	6	5.5

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The internal structure of a traditional rail-to-rail CMOS op amp consists of two differential transistor pairs. In operation, the op amp switches from one pair to the other. This error induced transition region is called the crossover region. Devices with zero-crossover technology eliminate this input offset crossover region. The zero-crossover feature eliminates this input offset transition region that traditional rail-to-rail CMOS op amps have. Eliminating this region provides a highly linear common-mode voltage (V_{CM}) range, assuring maximum linearity and lowest distortion for buffering DAC outputs.

As previously stated, a traditional rail-to-rail input CMOS architecture has two differential pairs. Figure 6 highlights both circled in red and blue. The differential pair consisting of two PMOS transistors is circled in blue and operates for common-mode input voltages from V_{EE} to V_{CC}-1.8V. The other differential pair consisting of two NMOS transistors is circled in red and operates for common-mode input voltages ranging from V_{CC}-1.8V to V_{CC}.

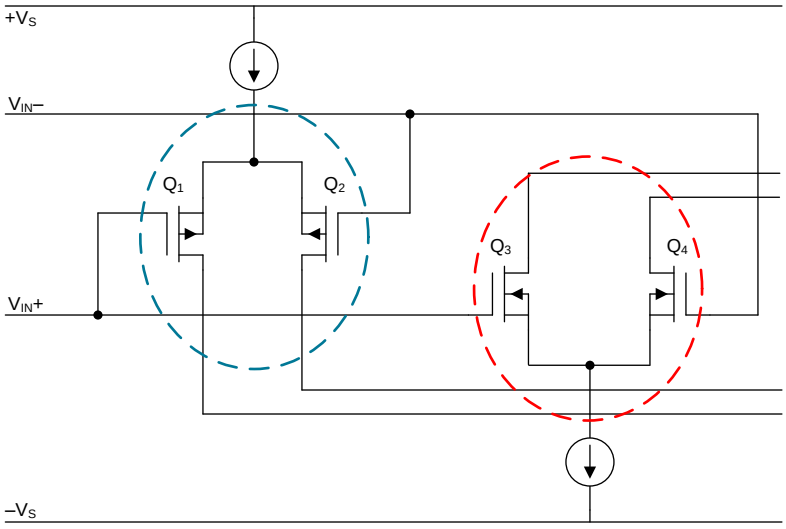

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Figure 6. Simplified Traditional Rail-to-Rail Input Topology

These two input transistor pairs will have independent and uncorrelated input offset voltages. This means the PMOS pair and the NMOS pair will intrinsically have different input offset voltage values. During the transition from one PMOS pair to the NMOS pair, and vice versa, there is a crossover region at 1.8 V below the positive rail where both inputs are conducting. Within this region, the DC input offset voltage can change, which may cause a shift in the amplifiers AC parameters. This is input crossover distortion where the non-linearity introduces a common-mode dependent offset and harmonic distortion. Using the TINA-TI™ SPICE tool (available at http://www.ti.com/tool/tina-ti), this offset error can be simulated.

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Figure 7 shows a buffer, non-inverting configuration with a typical rail-to-rail input CMOS amplifier. In non-inverting configurations, the common-mode signal is equal to the input signal.

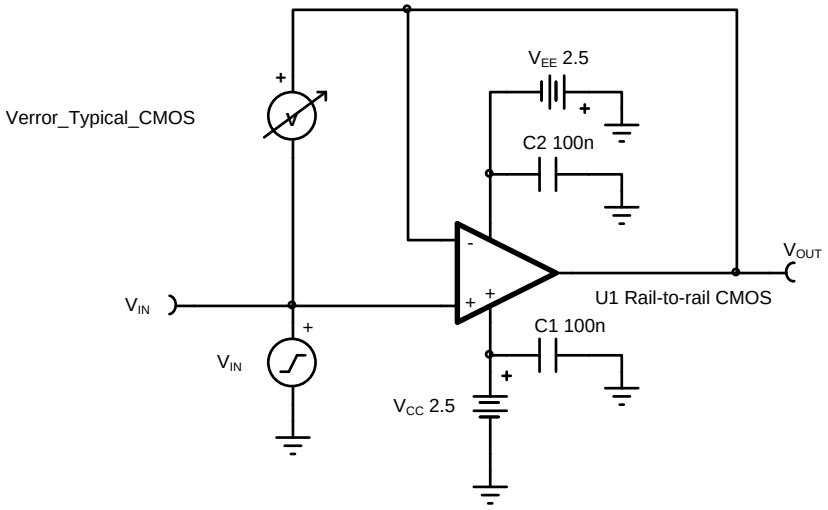

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Figure 7. TINA-TI Schematic for measuring V_{ERROR} of Traditional Rail-to-Rail CMOS Amplifier

Figure 8 shows the simulated results of applying a –2.4- to 2.4-V DC transfer sweep on a buffer configuration. The graph clearly shows Verror_Typical_CMOS abruptly shift when the common-mode voltage is within the crossover region. This crossover distortion varies on different devices with this input architecture. As with any error source, consider the error budget and decide if this error can be tolerated. If this error source is beyond the error budget, an alternative device is needed that has the zero-crossover feature.

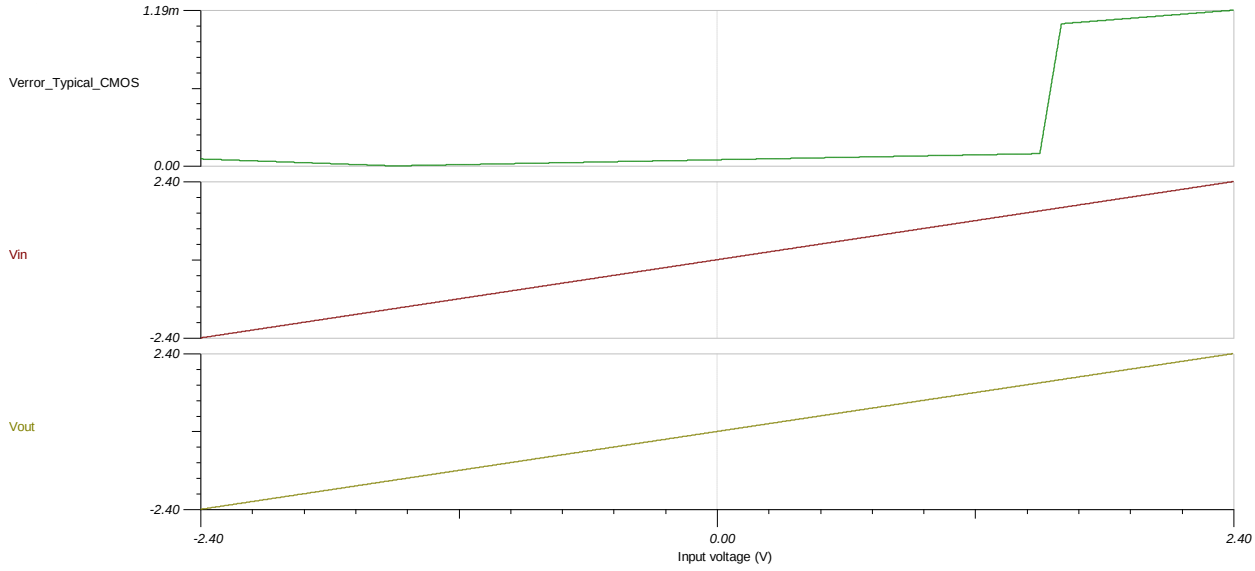

Figure 8. TINA-TI Simulation Results for Measuring Traditional Rail-to-Rail CMOS Op Amp V_{ERROR}

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Zero-crossover topology uses a charge pump to achieve voltages beyond the input rail with a single differential transistor pair. This use of a single stage ensures a linear output without distortion over the entire common-mode range. Devices such as the OPA388 include an internal charge pump that powers the amplifier input stage with an internal supply rail that is higher than the external power supply. The internal supply rail allows a single differential pair to operate and to be linear across the entire input common-mode voltage range, as shown in Figure 9.

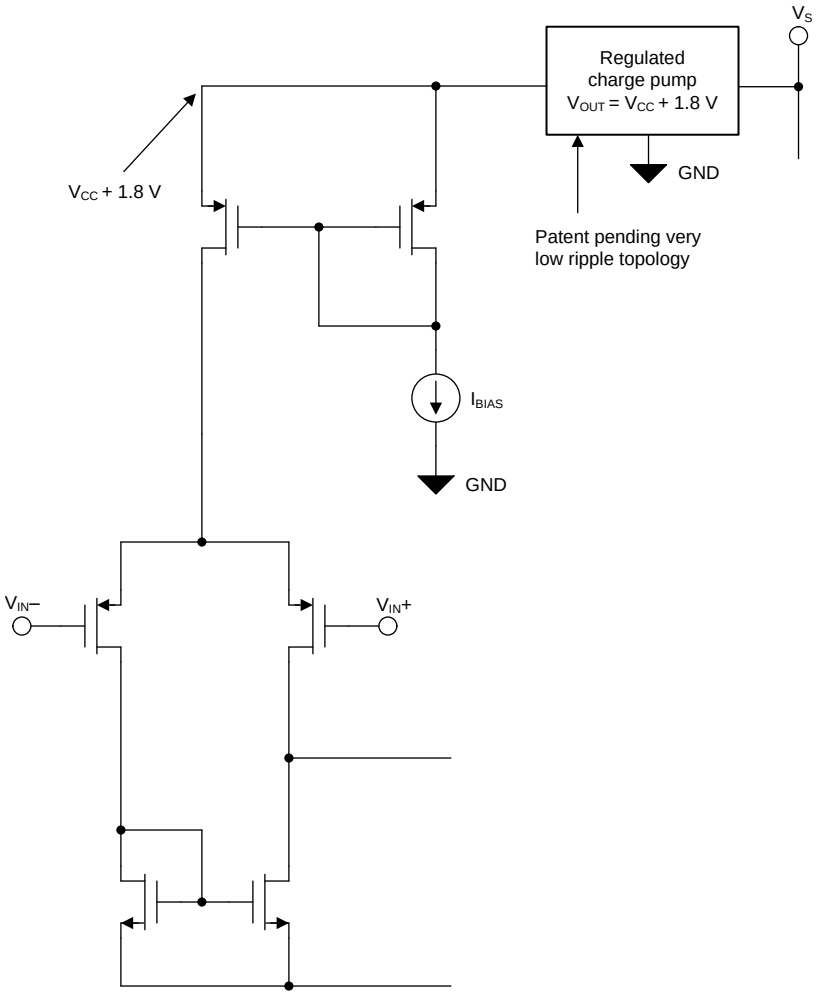

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Figure 9. Zero-Crossover Charge-Pump Topology

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Figure 10 shows a simplified representation of the charge pump used in zero-crossover devices. In this case, the charge pump boosts the supply voltage up by 1.8 V while still maintaining a low power budget. This is enough to overcome the 1.8-V drop from the positive rail on the PMOS transistor input pair. One concern that often accompanies charge pump circuits is the noise generated from the use of a switching capacitor to achieve a voltage boost. However, in the case of the OPA388, the amount of noise generated by the charge pump's ripple design is lower than the noise floor, and thus unnoticeable. Using the TINA-TI SPICE tool, Figure 10 shows a buffer configuration with the zero-crossover OPA388. As stated in the previous section, this non-inverting configuration was chosen because the common-mode signal is equal to the input signal.

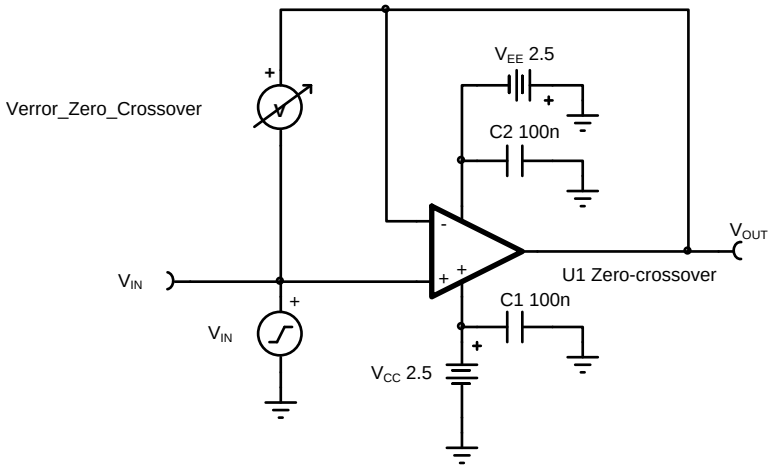

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Figure 10. TINA-TI Schematic for Measuring V_{ERROR} of Zero-Crossover Amplifier

Figure 11 shows the simulated results of applying a –2.4- to 2.4-V DC transfer sweep on a buffer configuration. The Verror_Zero_Crossover trace in Figure 11 no longer shows an abrupt shift with input common-mode change because there is no crossover region.

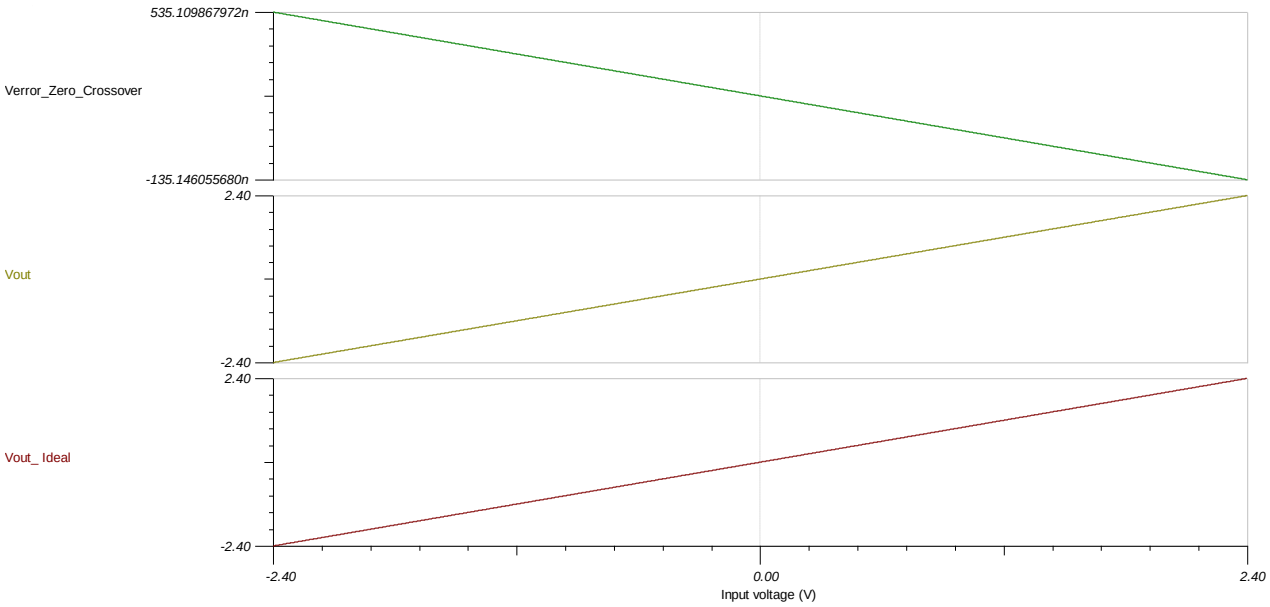

Figure 11. TINA-TI Simulation Results for Measuring Zero-Crossover Op Amp V_{ERROR}

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The OPA388 and a typical CMOS amplifier were used in identical, unity-gain buffering configurations (see Figure 12). These amplifiers were both fed a pure sine wave with an amplitude of 2 V (4 V_{P-P}). The outputs of these circuits were captured in the FFT spectrum. Figure 12 illustrate the output voltage spectrum for the OPA388 and a typical CMOS rail-to-rail amplifier, respectively. The output of the OPA388 has very few spurs and harmonics when compared to the typical rail-to-rail CMOS amplifier. This is the effect of eliminating the crossover region with zero-crossover technology.

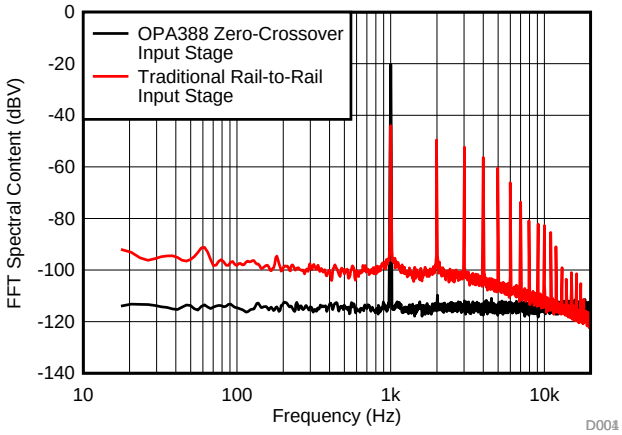

Figure 12. Buffer FFT Spectrum Comparison

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2 Getting Started Hardware

2.1 Hardware

This section provides an overview of the TI Design hardware and instructions on setting up and using this board.

This hardware features a 16-bit resolution DAC, precision low-noise voltage reference, and three channels to select between different op amps as a buffered output.

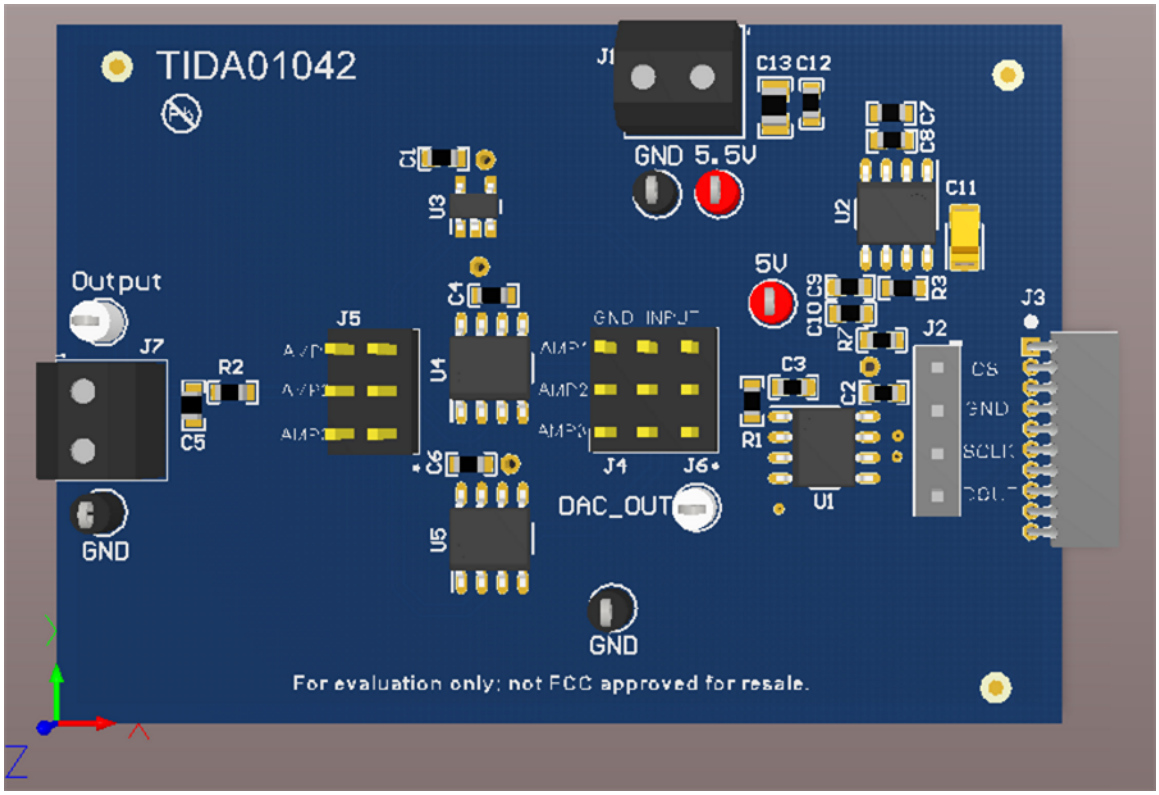

Figure 13. 3D Model Top View of TI Reference Design Board

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The board is supplied through connector J1 with a 5.5-V supply. The analog section is directly powered by a 5.5-V DC supply, the digital section has a dedicated 5-V supply on the board provided by the REF5050.

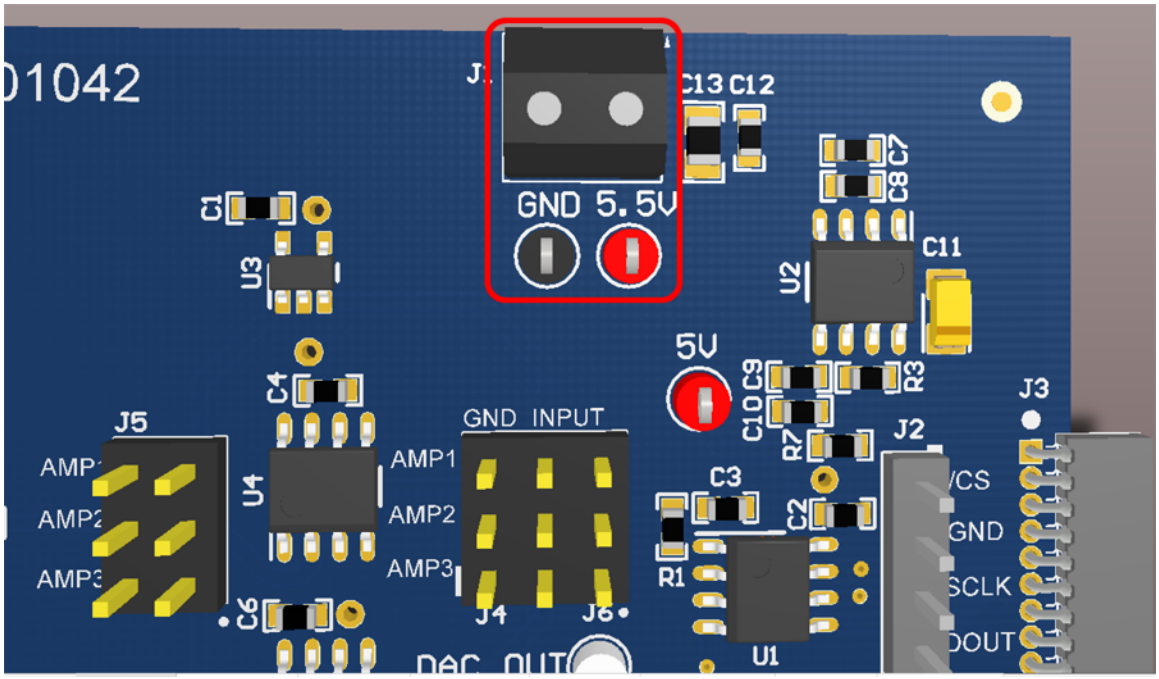

Figure 14. Terminal J1 for 5.5-V DC Supply

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Connector J3 is used for the serial peripheral interface (SPI) to send digital values to DAC8830. The dot near the J3 designator on the board indicates pin 1.

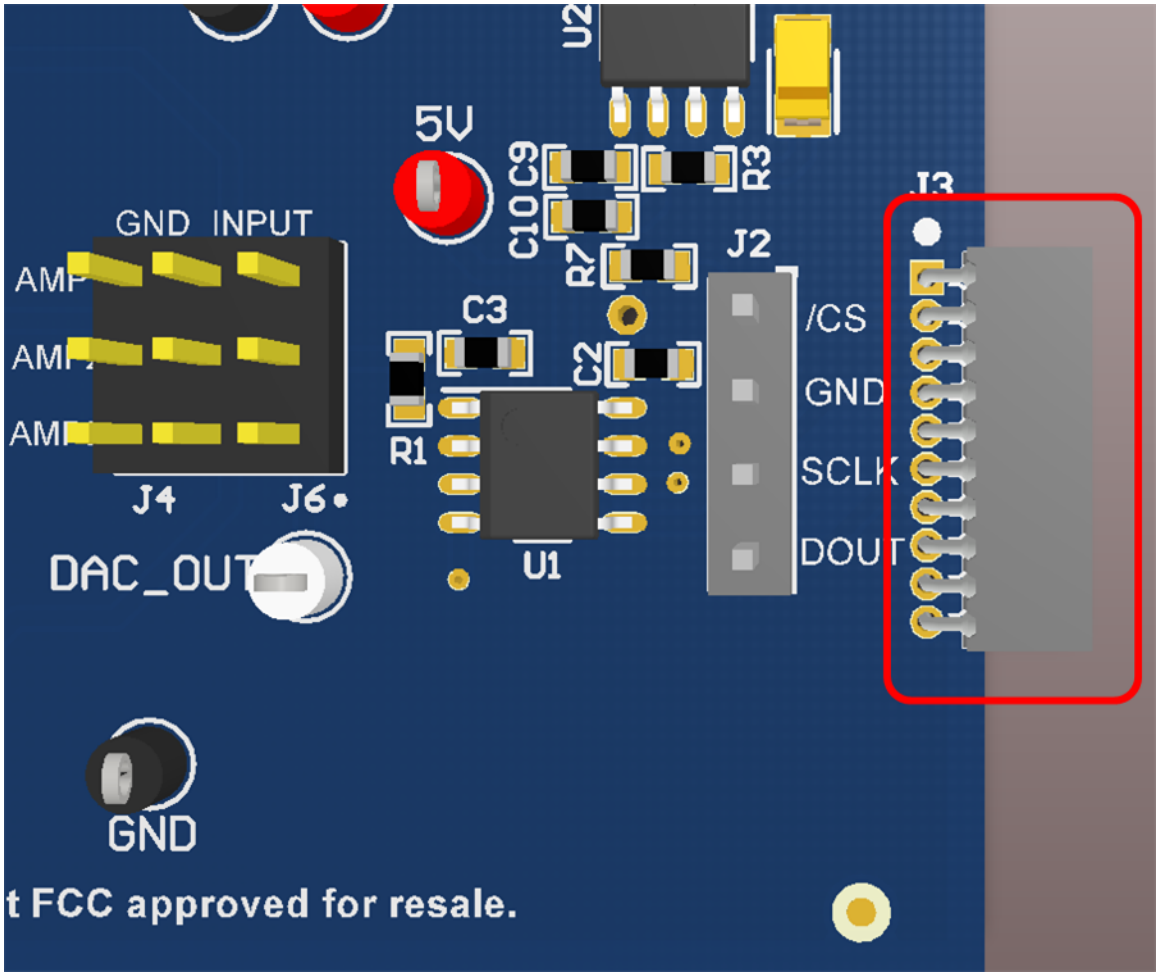

Figure 15. SPI Female Connector J3

Figure 16 shows schematic designation of the following pins needed for SPI: CS, GND, SCLK, and DOUT.

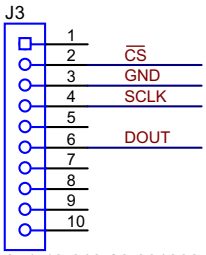

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Figure 16. SPI Connector J3 Pin Designation

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Connector J2 can be used to measuring the SPI signals for debugging.

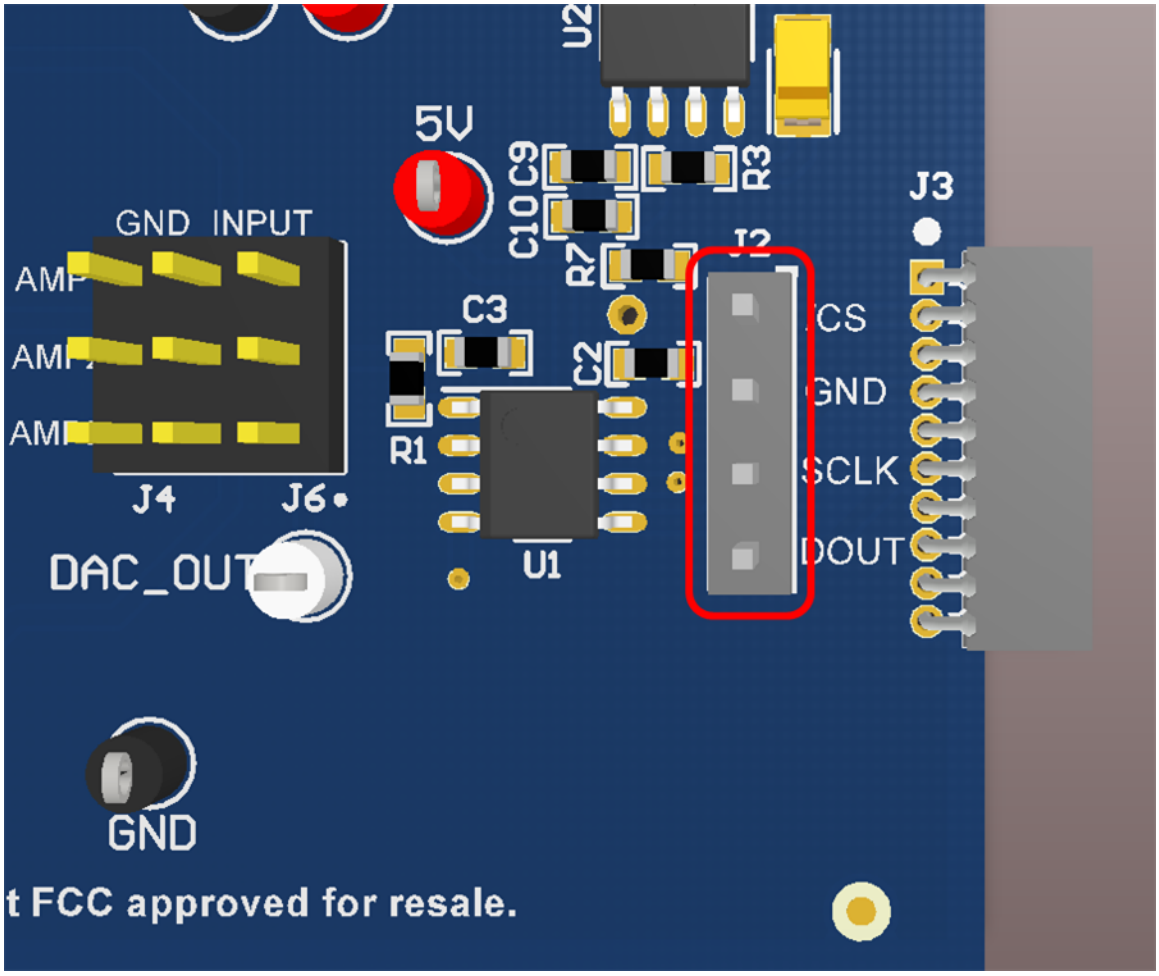

Figure 17. J2 SPI Probing Pins

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Connector J7 is the output of the chosen operational amplifier to buffer the DAC output.

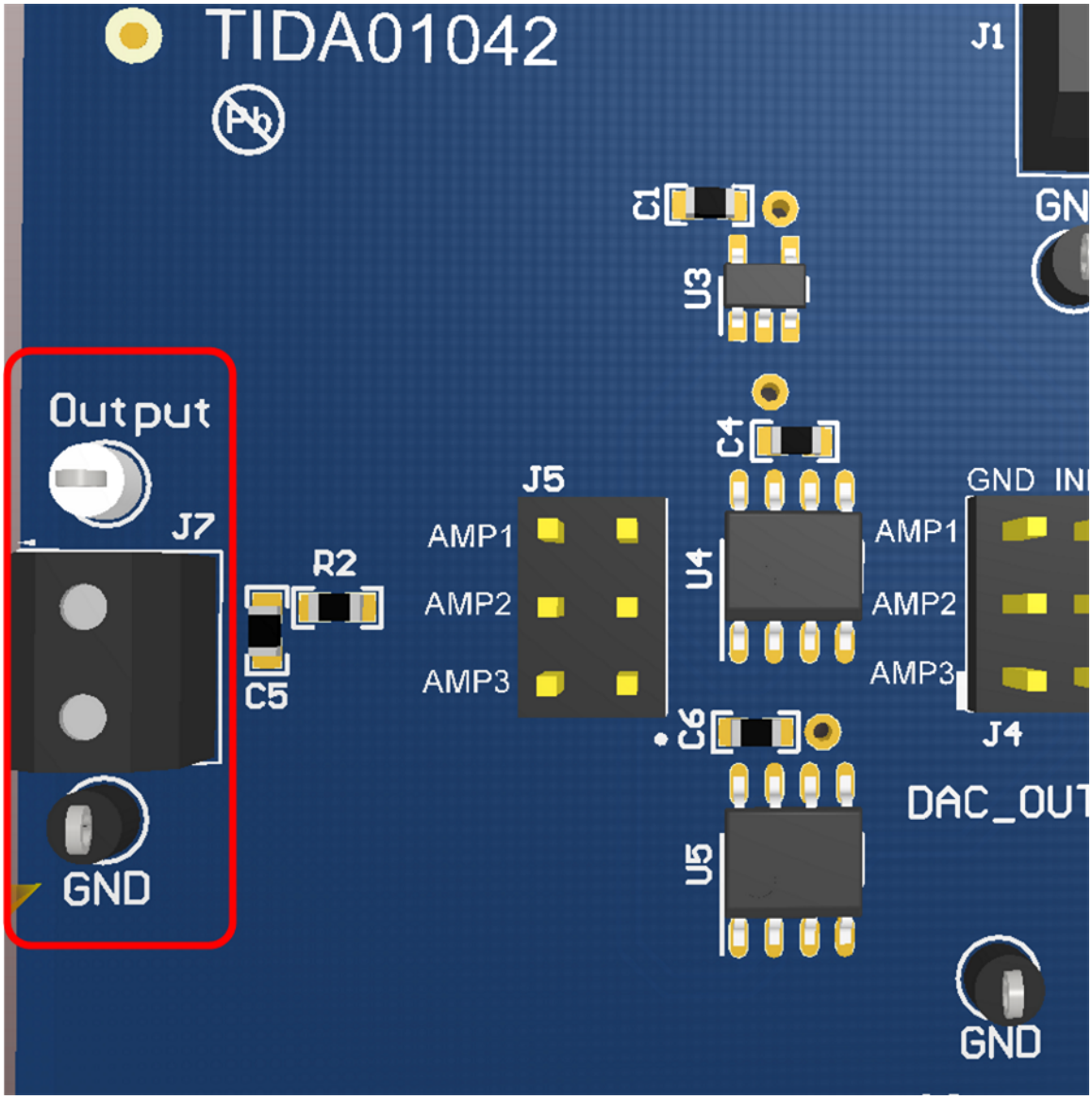

Figure 18. Terminal J7 Buffer Amplifier Output

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Connector J4 and J6 are jumper headers. This header will connect the output of the DAC to one of the op amps and ground the input of the unused amplifiers.

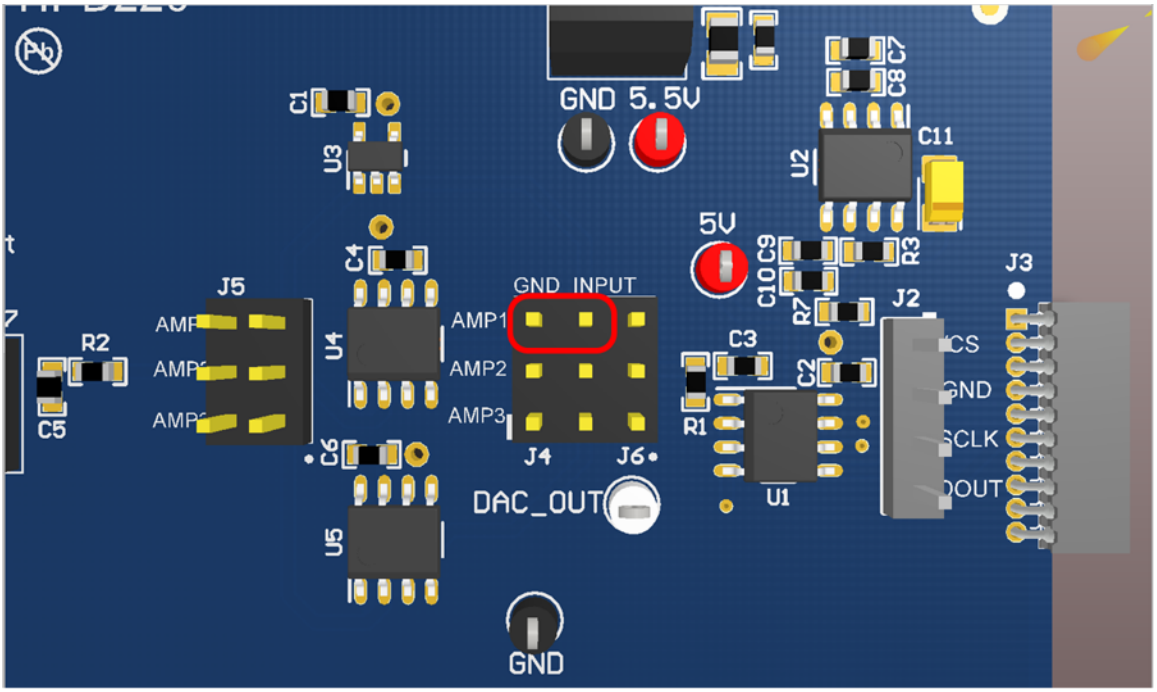

Figure 19. Header Connecter for Ground Unused Amplifier Input

Figure 20 shows the position the jumper has to be to connect the DAC to the AMP1.

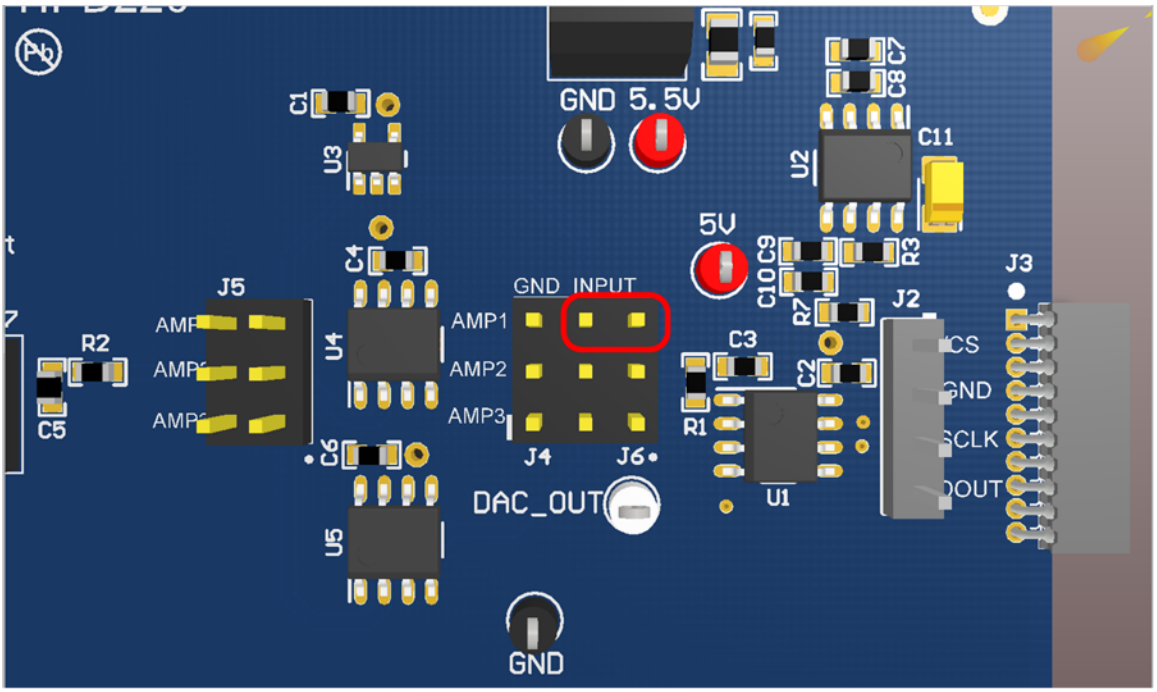

Figure 20. Header Connecter for Connecting Amplifier's Input to DAC Output

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Figure 21 shows the position the jumper has to be to ground AMP1 and AMP3.

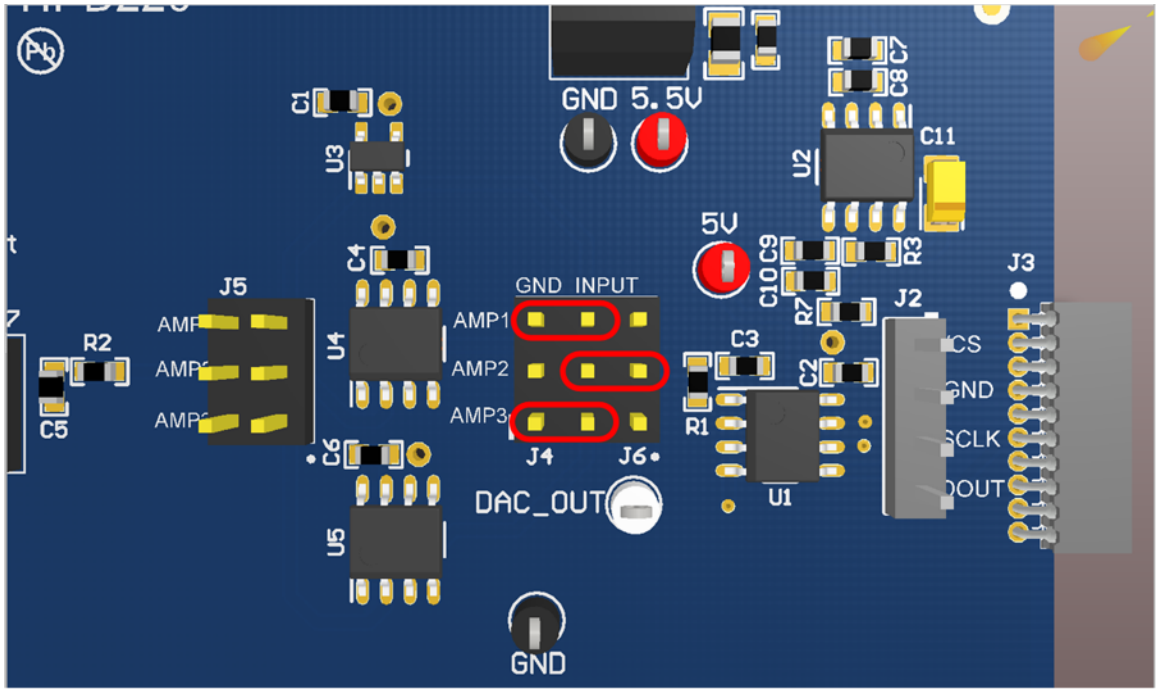

Figure 21. Jumper Position to Ground AMP1 and AMP3 Input and Connect AMP2 to DAC8830

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Connector J5 is a jumper header. This header will connect the output of the op amp to connector J7 for measurement probing. As shown in Figure 22, one jumper is only need to connect the amplifier of interest; the other two amplifiers must be left open (no jumper).

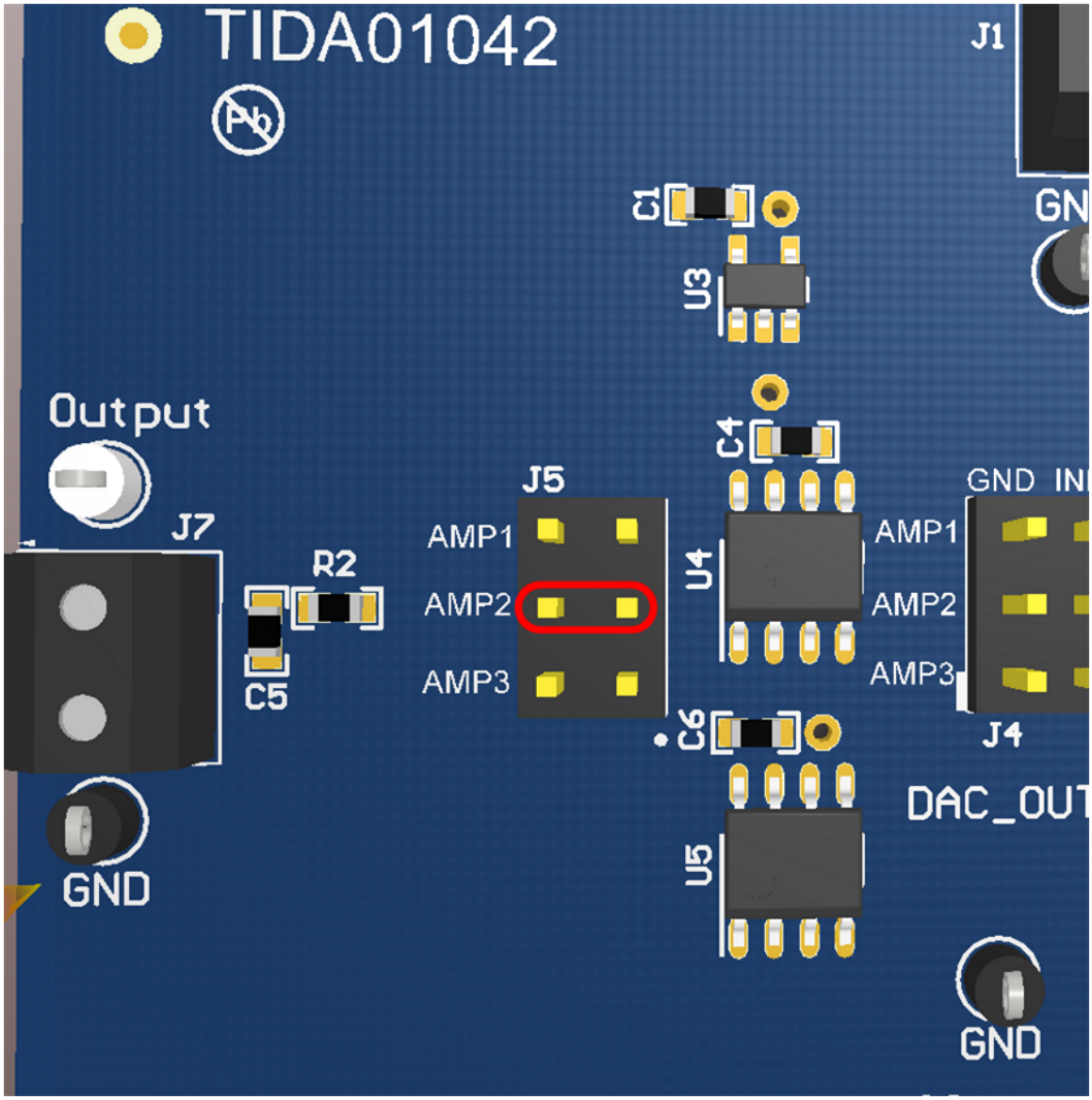

Figure 22. Header Connecter J5 Connection to Terminal Block J7

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3 Testing and Results

This TI Design linearity test was performed using an Analogic AN3200 DC Voltage Calibrator, an Agilent 3458A digital multimeter, NI USB-8452, and a PC running the LabVIEW™ software. The board was tested for all codes of the device and was allowed to settle for 1ms before the meter is read. This process is repeated for all codes to generate the measurements for INL results for different op amp buffered outputs. The results of the DAC INL characterization test is shown in Figure 27 as well as an output buffer comparison between the OPA388 and OPA340 in Figure 28.

3.1 Test Setup

The TI Design INL test was performed using an Analogic AN3200 DC Voltage Calibrator shown in Figure 23, which provided 5.5 V of power to the board.

Figure 23. Analogic AN3200 DC Voltage Calibrator

The Agilent 3458A digital multimeter shown in Figure 24 is connected to the output to measure the voltage associated with the binary value sent to the DAC.

Figure 24. Agilent 3458A digital multimeter

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The NI USB-8452 is an interface used for connecting to the TI Design board and communicate through SPI.

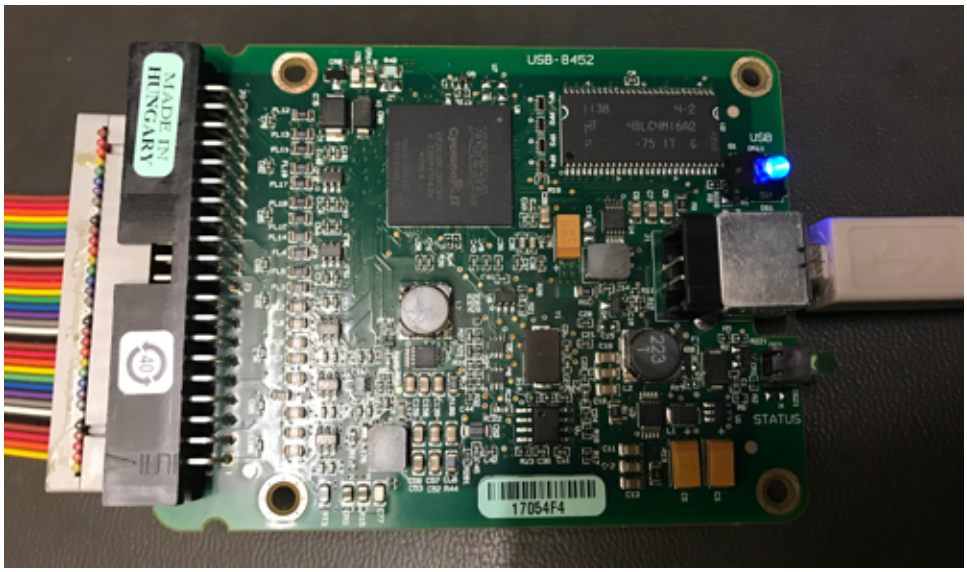

Figure 25. NI USB-8452 Interface Board

The PC running the LabVIEW software to increment the code and collect the measured data. Figure 26 shows the overall test setup for measuring INL.

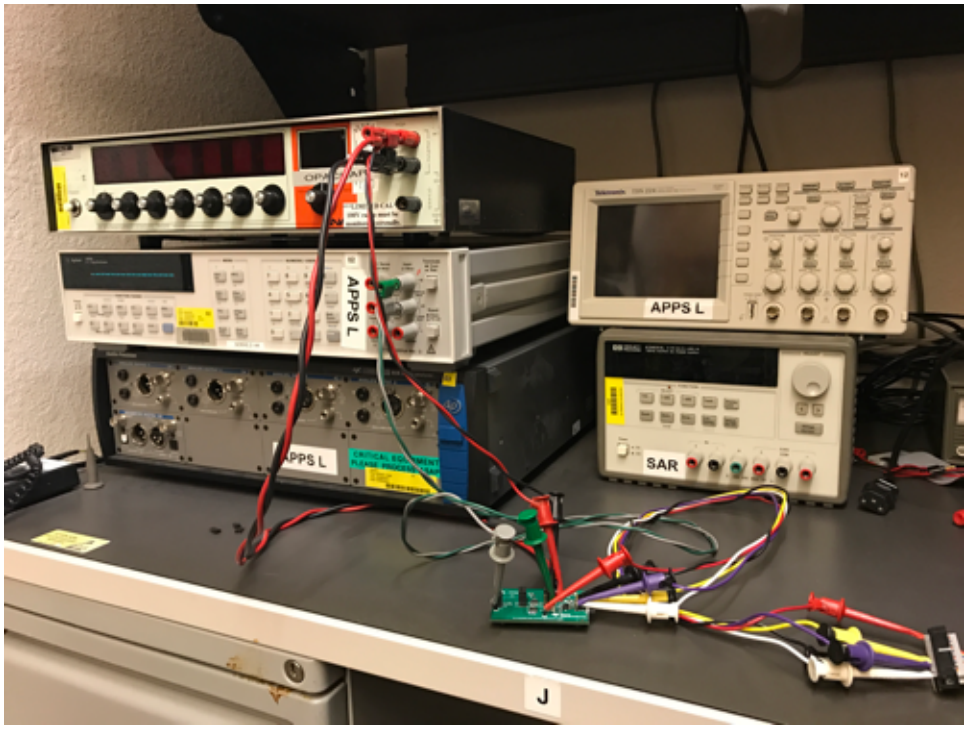

Figure 26. Test Setup for Measuring INL

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3.2 Test Results

The results of the DAC INL characterization test is shown in Figure 27 as well as an output buffer comparison between the OPA388 and OPA340 in Figure 28.

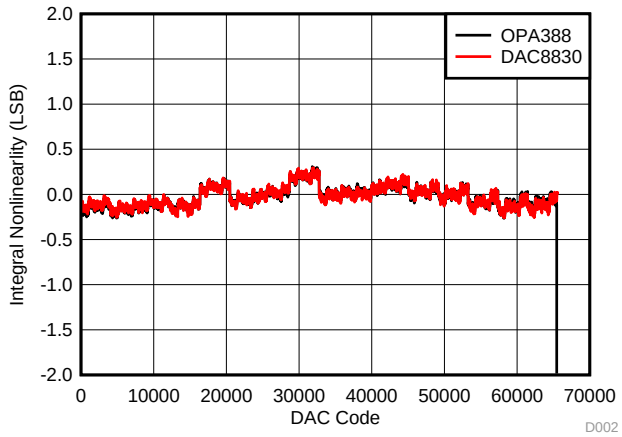

Figure 27. INL Measurement of DAC8830 Only versus OPA388

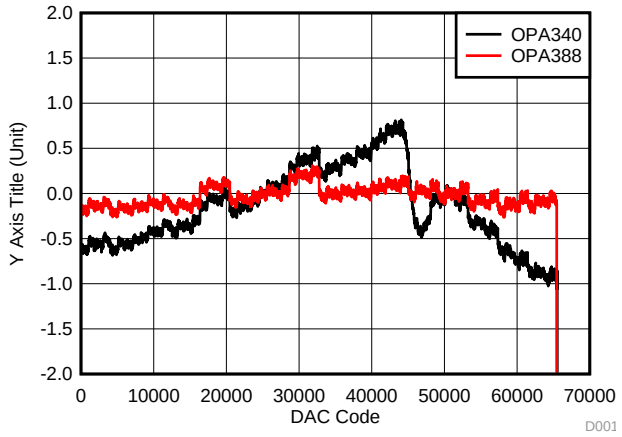

Figure 28. INL Measurement of OPA388 versus OPA340

These results show that a zero-crossover device such as the OPA388 shows almost no deviation from the DAC INL. This means the OPA388 minimally effects the linearity of the DAC. On the other hand, the OPA340 shows a major shift of greater than 1 LSB in the INL within the op amp's crossover region.

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01402.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01402.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01402.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01402.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01402.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01402.

5 Related Documentation

1. Texas Instruments, *Zero-crossover Amplifiers: Features and Benefits*, Zero-crossover Technote (SBOA181)
2. Texas Instruments, *Zero-drift Amplifiers: Features and Benefits*, Zero-drift Technote (SBOA182)

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