Design Guide: TIDA-010243

Cost-Effective, 3-Phase CT Electricity Meter Reference Design Using Standalone ADC

Description

This reference design implements Class 0.1 three-phase energy measurement using a high-performance, multichannel analog-to-digital converter (ADC), which samples current transformers (CT) at 8 kHz to measure the current and voltage of each leg of the AC mains. The reference design achieves high accuracy across a wide input current range (0.01 A – 100 A) and supports high sampling frequencies necessary for power quality features such as individual harmonic analysis. An ADC sample rate of 32 kSPS can be achieved when using a TI Arm® Cortex®-M0+ host microcontroller for metrology. The necessary software functionality is implemented by porting the ADC Energy Metrology library to MSPM0G3507 and can be compiled with Code Composer Studio™.

Features

- 3-phase metrology for electricity meters that meets ANSI C12.20 Class 0.1 active energy accuracy requirements across 2000:1 input range
- Active and reactive energy and power, root mean square (RMS) current and voltage, power factor, and line-frequency calculations
- Isolated RS-232 and RS-485 with 5-kV_{RMS} isolation
- Tested across 10 mA to 100 A and 9-V to 270-V input range
- Software for energy metrology and displaying results on a Microsoft® Windows® PC GUI

Applications

- Electricity meter
- Power quality meter
- Power quality analyzer

Resources

TIDA-010243	Design Folder
MSPM0G3507, ADS131M08	Product Folder
THVD1400, TRS3232E, TPS3840	Product Folder
TMAG5273, ISO6731, ISO6720	Product Folder

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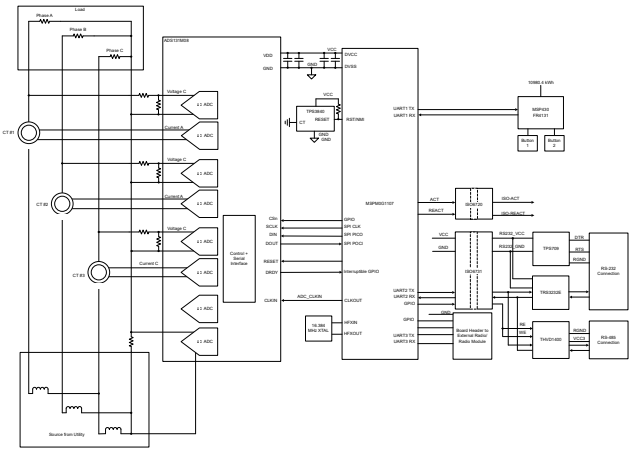

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1 System Description

1.1 End Equipment

Electricity meters and Power quality meters are two popular system designs for accurate energy measurement in compliance with IEC and ANSI standards. The energy measurement is the basic functionality for both and calculates various metrology parameters. Some of the parameters are included in the following list:

- Total and per-phase active (kWh), reactive (kvarh), and apparent energy (kVAh) with pulse-generation outputs
- Total and per-phase active (kW), reactive (kvar), and apparent power (kVA)
- Per-phase voltage and current root mean square (RMS)
- Line frequency

Typical sensors used are either current transformers (CT), shunts, or Rogowski coils.

In addition, multiple power quality parameters in a polyphase energy measurement system can be also calculated, including:

- Per-phase voltage total harmonic distortion (THD)
- Per-phase current THD
- Voltage phase-to-phase angle
- Per-phase zero crossing

TIDA-010243 is a Class 0.1 high-accuracy 3-phase CT electricity meter reference design, using a single 8-channel standalone ADS131M08 ADC and cost-effective MSPM0G3507 MCU. The reference design can also be used for energy metering in popular products such as Level 2 EV chargers and AC wallboxes.

1.2 Electricity Meter

Utility providers and their customers are driving the need for more features from electricity meters. Advanced features, such as harmonic analysis, are increasingly being required from meters which mandates higher processing and accuracy requirements for the MCUs. As an example, adding harmonic analysis capabilities to an electricity meter can require an increase in the sample rate of the meter to capture the desired frequency range. Often such increases in sample frequency must be done without compromising on accuracy, while the higher sample rate, in turn, also requires more processing.

As both the accuracy requirements and amount of processing expected from electricity meters rapidly increase, it becomes more and more difficult to solve this with a single metrology system on chip (SoC). A common solution to this problem is to utilize a dual-chip approach with a standalone ADC and a standard host microcontroller (MCU). Using an accurate state-of-the-art standalone ADC typically has the following advantages:

- Enables meeting the most stringent of accuracy requirements
- Enables meeting minimum sample rate requirements (without compromising on accuracy) that cannot be obtainable with application-specific products or metrology SoCs
- Enables flexibility in selecting the host microcontroller, because the MCU only needs to meet the application requirements, such as processing capability, minimum RAM and Flash storage for logging energy usage, and microcontroller security features for ensuring meter data security

To properly sense energy consumption, voltage and current sensors translate mains voltage and current to a voltage range that an ADC can sense. To sense the energy consumption when a multiphase distribution system is used, it is necessary for the current sensors to be isolated so the sensors can properly determine the current drawn from the two different lines without damaging the ADC. As a result, current transformers, which inherently have isolation, have historically been used for the current sensors for split-phase, two-phase, and three-phase electricity meters.

In this reference design, Class 0.1 three-phase CT-based energy measurement is implemented by using a standalone ADC device, which senses the mains voltage and current. When there are new ADC samples available, the host MCU communicates to the standalone ADC via SPI bus to read out the new samples and calculate multiple metrology parameters. In addition, the host also communicates to a PC GUI through either the isolated RS-232 circuitry or isolated RS-485 circuitry on the board. As an additional safeguard, an external SVS

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device is added to the design to reset the host MCU when the supplied voltage to power the host MCU is not sufficient. In general, using an (optional) external supply voltage supervisor (SVS) provides more security than the internal SVS on a host microcontroller.

In this design, the test software specifically supports calculation of various metrology parameters for 3-phase energy measurement. These parameters can be viewed either from the calibration GUI or on an optional LCD display. The key parameters calculated during energy measurements are:

- Active, reactive, apparent power, and energy
- RMS current and voltage
- Power factor
- Line frequency

1.3 Power Quality Meter, Power Quality Analyzer

Except being used for electricity meters, this standalone ADC architecture applies also for power quality analyzers and power quality meters and EV chargers or wallboxes. This end equipment is used to monitor and control power quality by measuring certain power quality parameters, such as voltage harmonics, current harmonics, supply voltage dips, supply voltage swells, and other parameters as well. For all equipment, a lot of computation is required for calculating the power quality parameters. Also, accuracy is important to be able to meet the accuracy requirements for the different power quality parameters. The requirement for high accuracy and computation power is something well supported by having a standalone ADC and separate host MCU or processor, as is done in this design.

A couple of the parameters commonly measured by power quality meters and power quality analyzers are voltage and current harmonics. For the most accurate harmonic calculations, implement coherent sampling. One way of implementing coherent sampling is to vary the sampling clock based on the Mains frequency. The standalone ADC in this design has the ability to take in a varying clock so the ADC can support coherent sampling. Although the clock to the standalone ADC in this design can be varied, this design cannot support coherent sampling because the sampling clock from the host MCU to the standalone ADC cannot be varied with the proper resolution.

1.4 Key System Specifications

Table 1-1. Key System Specifications

FEATURES	DESCRIPTION
Number of phases	3 (each phase measures voltage and current through CT)
Accuracy class	Class 0.1
Current sensor	Current transformer
Tested current range	0.01 – 100 A
Tested voltage range	15 V – 240 V
ADS131M08 CLKIN frequency	8,192,000 Hz
ADS131M08 Delta-sigma modulation clock frequency	4,096,000 Hz (= CLKIN / 2)
SPI Clock	19,968,000 Hz
Oversampling ratio (OSR)	512
Digital filter output sample rate	8,000 samples per second
Phase compensation implementation	Software
Phase compensation resolution	0.0088° at 50 Hz or 0.0105° at 60 Hz
Selected CPU clock frequency	79.87 MHz
MCU External SVS *voltage*	*1.72 – 1.74 V*
System nominal frequency	50 or 60 Hz
Measured parameters	• Active, reactive, apparent power and energy • Root mean square (RMS) current and voltage • Power factor • Line frequency
Update rate for measured parameters	Approximately equal to 1 second

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Table 1-1. Key System Specifications (continued)

FEATURES	DESCRIPTION
Communication options	• LCD (Controlled by MSP430FR4131, not implemented in software yet) • PC GUI via 5 kV_{RMS} isolated RS-232 or 5 kV_{RMS} isolated RS-485
Utilized LEDs	Total active energy and total reactive energy
Board power supply	3.3 V directly to DVCC rail

2 System Overview

2.1 Block Diagram

TIDA-010243 Block Diagram, Three-Phase + Neutral Configuration depicts the block diagram of the high-level interface used for an ADS131M08-based three-phase energy measurement application. For each phase, the line-to-neutral voltage is directly measured, as well as the current for each line (3 phases) and the current thru the N (neutral) wire.

In the TIDA-010243 block diagram, a current transformer (CT) connects to each current channel and a simple voltage divider is used for dividing down the corresponding voltage of each channel. Each CT has an associated burden resistor that must be connected at all times to protect the measuring device. The selection of the CT and the burden resistor is made based on the manufacturer and current range required for energy measurements.

The choice of voltage divider resistors for the voltage channel is selected to make sure the Mains voltage is divided down to adhere to the normal input ranges of the ADS131M08 device. Since the ADS131M08 ADCs have a large dynamic range and a large dynamic range is not needed to measure voltage, the voltage front-end circuitry is purposely selected so that the maximum voltage seen at the inputs of the voltage channel ADCs are only a fraction of the full-scale voltage.

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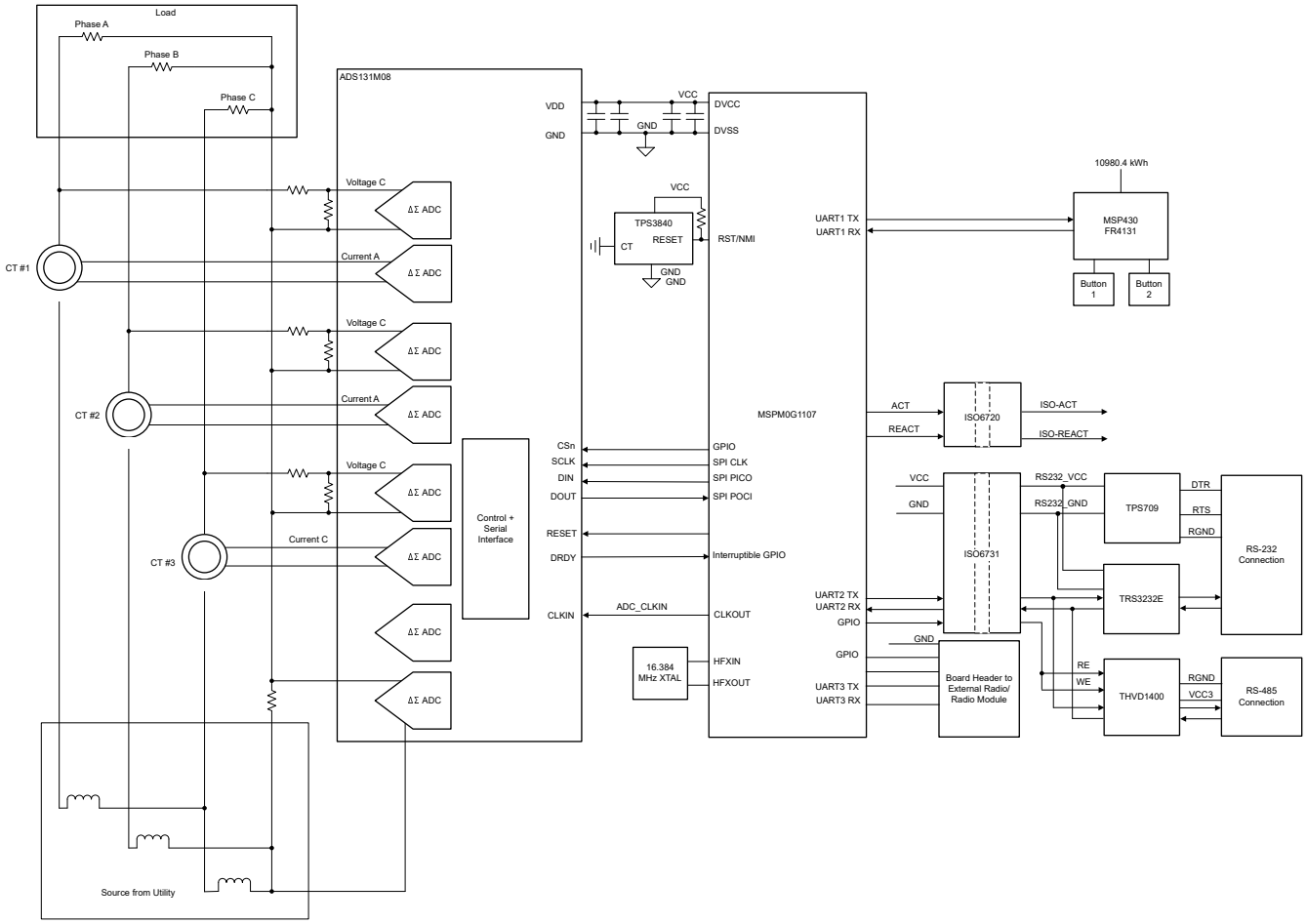

Figure 2-1. TIDA-010243 Block Diagram, Three-Phase + Neutral Configuration

By reducing the voltage fed to the three ADS131M08 voltage ADC channels, voltage to current crosstalk, which actually affects metrology accuracy more than voltage ADC accuracy, is reduced at the cost of voltage accuracy, thereby resulting in more accurate energy measurements at lower currents.

The ADS131M08 device interacts with the MSPM0+ MCU in the following manner:

1. The CLKIN clock used by the ADS131M08 device is provided from the M0_CLKOUT clock signal output of the MSPM0G3507 MCU.
2. The ADS131M08 device divides the clock provided on the CLKIN pin by two and uses this divided clock as the delta-sigma modulation clock.
3. When new ADC samples are ready, the ADS131M08 device asserts the $\overline{\text{DRDY}}$ pin, which alerts the MSPM0+ MCU that new samples are available.
4. After being alerted of new samples, the MSPM0+ MCU uses one of the SPIs and two of the DMA channels in the DMA module to get the voltage and current samples from the ADS131M08 device.

The optional TPS3840 device is used as an external SVS for the MSPM0+ MCU. Although the MSPM0+ MCU has internal Power-on reset (POR) and POR as well as a Brownout reset (BOR) supply monitor with four configurable threshold voltages, the external TPS3840 standalone SVS adds redundancy in case of a power failure.

Other signals of interest in Figure 2-1 are the active and reactive energy pulses used for accuracy measurement and calibration. The ISO6720 device provides an isolated connection for these pulses for connecting to non-isolated equipment. This design also supports isolated RS-232 communication through the use of the TPS70933, ISO6731B, and TRS3232E devices. The hardware uses a push switch to select between the RS-485 interface, with ISO6731 and THVD1400 devices, or the RS-232 interface with TRS3232E.

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The design can be powered either by applying 3.3 V at TP6 and GND at TP1 directly or by connecting 3.3 V and GND to the Application Board Connector J13. See Header Names and Jumper Settings for more details on the proper jumper connections for powering the board for both options.

2.2 Design Considerations

2.2.1 External Supply Voltage Supervisor (SVS) With TPS3840

The TPS3840 device is an external supply voltage supervisor (SVS) that is used to externally reset the MSPM0+ MCU. The TPS3840 maintains very low quiescent current, which enables this device to still be used if there is a power outage and the meter is running from a backup battery. The MSPM0+ MCU has internal POR and BOR supply monitors which cannot be disabled and suffices for this application; however, using the optional external SVS adds redundancy to SVS, in case some issue has affected the MCU itself.

In this design, the TPS3840DL20 device variant is specifically used, which has a negative-voltage threshold voltage of *1.72 ±1% V*. When the voltage rail that powers the MSPM0+ MCU drops below *1.74 V*, the TPS3840 device resets the MSPM0+ MCU. When the monitored voltage rises above the undervoltage threshold plus hysteresis voltage value (approximately equal to *1.85 V* total), the RESET pin of the TPS3840 is pulled back high after a user-defined reset delay time, t_D, elapses. The t_D is determined based on the value of the capacitor connected to the CT pin of the TPS3840 device.

The TPS3840 device is available with both push-pull and open-drain outputs. The open-drain output version TPS3840DL20 is specifically selected for this design since a 47-kΩ pullup resistor is recommended in the JTAG circuitry of the MSPM0+ MCU.

2.2.2 Magnetic Tamper Detection With TMAG5273 Linear 3D Hall-Effect Sensor

One common nonintrusive way to steal electricity is to apply a strong permanent magnet or an AC magnet near the electricity meter, thus tampering with the meter. A permanent magnet or an AC magnetic field can affect meter components like current transformer current sensors, shunt current sensors (shunts are only affected by AC magnets), or any power supply transformer. As a result of the weaknesses of these components to magnetic tampering, utility customers can be undercharged for their energy consumption, thereby allowing consumers to essentially steal electricity.

Due to the susceptibility of meters to magnetic tampering, magnetic sensors are often used in electricity meters to detect external magnetic fields to take appropriate action, such as disconnecting services to the meter or applying a penalty fee for magnetic tampering. In this design, magnetic tamper detection is done with the TMAG5273 linear 3D Hall-effect sensor, which has the following advantages compared to other magnetic sensing devices and designs:

- **Ease of assembly:** Hall sensors in general are not as fragile as reed switches, the latter of which can break during assembly.
- **Only one surface mount IC needed:** Sensing in three directions with the TMAG5273 requires only one surface mount IC for 3D linear Hall-effect sensors instead of the three ICs in the case of 1D Hall-effect sensors. 3D linear Hall-effect sensors therefore enable a more compact printed circuit board (PCB) layout. In addition, having a surface mount-only implementation can reduce PCB manufacturing costs compared to a 1D Hall-effect sensor implementation that can require through-hole sensors for detecting some of the directions.
- **Flexibility for defining magnetic tampering threshold:** Since 3D linear Hall-effect sensors provide information about the actual sensed magnetic flux density value, it is possible to select the magnetic tampering threshold of each axis to anything within the magnetic sensing range of the 3D linear Hall-effect sensor. This enables configuring how to define what is tampering, which can vary between designs since the magnetic flux density sensed depends on the distance from the magnet to the sensor as well as the characteristics of the external magnets to be detected. This type of flexibility is not possible for Hall-effect switches with fixed magnetic operating point (B_{OP}) thresholds. Finding the appropriate tamper threshold definition can be done by using a magnetic calculation tool to determine what is the resulting magnetic flux density seen for the different magnet-to-sensor distances and magnet types that must be detected. The magnetic threshold can be then set to something lower than the magnetic flux density seen by the sensor when exposed to the desired tamper conditions. Typically, it is desired to set the threshold to be small enough to detect tamper magnets but also large enough so that the system does not see any false positives from any nearby equipment that causes a magnetic field that does not affect the functionality of the meter. The

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magnet-to-sensor distance depends on where the sensor is placed on the PCB as well as the dimensions of the e-Meter case. For small-sized systems, the magnetic sensor can be placed near the center of the board for symmetrical sensing coverage across the meter case, or the sensor can be placed near any components that are affected by magnetic tampering. For large-sized systems like certain polyphase meters, sometimes it is not possible for one magnetic sensor to sense tampering across the entire meter surface, so multiple 3D Hall sensors can be used and placed spread out with respect to each other on the PCB to cover a large sensing area. The TMAG5273 has four sets of device orderables that are factory programmed with different I2C addresses, which enable multiple devices to share the same I2C bus.

- **Ability to change between multiple device power modes**: The TMAG5273 supports switching between multiple power modes, depending on if it is desired to reduce system current consumption. The TMAG5273 has an active mode for taking measurements, a sleep mode for minimizing current consumption, and a duty-cycle mode that automatically switches between active and sleep modes. Typical use-cases of the different power modes for electricity meters are described below:
  - Active mode is used for taking measurements and requires the most power out of the different power modes. An example scenario where active mode is typically used is when the Mains are available and the meter is running off the AC/DC power supply. When running off the AC/DC power supply, the relatively high active mode current consumption (2.3 mA) of the TMAG5273 is negligible.
  - In duty cycle mode, the device takes measurements and then automatically goes to sleep for a user-specified amount of time. Duty-cycle mode is good for minimizing current consumption while still detecting magnetic tampering, such as when low-speed magnetic tamper detection is necessary when running off a backup battery. To reduce average current consumption in duty cycle mode, select a long sleep time. When selecting the sleep time, set the sleep time to be less than the desired response time for magnetic measurements. As an example, to sense magnetic tampering every 2 ms using wakeup and sleep mode, set the sleep time to 1 ms instead of 1 second.
  - In sleep mode, the device does not take any magnetic measurements. An alternative to wakeup and sleep mode is to have the MCU manually set the sensor to sleep mode and then manually set the sensor to wake up after the desired sleep time has passed. This requires more overhead from the MCU; however, this option can reduce the system current consumption if the MCU is going to have its own wakeup and sleep mode that allows the MCU to reconfigure the TMAG5273 during each wakeup and sleep mode cycle. For systems that do not require detecting magnetic tampering when running off a backup battery, the TMA5273 can just be put in sleep mode to reduce system current consumption when running off a battery and then put back in active mode when the system is able to run off the AC/DC power supply again.
- **GPIO pin interrupts when magnetic tampering detected (depends on device)**: The TMAG5273 has the ability to set an interrupt pin when the sensed magnetic flux density of any axis goes beyond a user-defined magnetic switching threshold. To detect tampering, the user can set the magnetic switching point for interrupts to the desired magnetic tampering threshold. Since the interrupt pin of the Hall-effect sensor can wake up the microcontroller when the MCU is in low-power mode, and since the microcontroller does not have to read the Hall-effect sensor to determine magnetic tampering, the MCU can go to low-power mode when running off a backup power supply until woken up by the interrupt pin of the Hall-effect sensor. Used simultaneously, the general-purpose input/output (GPIO) pin interrupt feature and duty-cycle power mode can reduce system current consumption and extend the lifetime of the backup power supply. Once the GPIO pin of the Hall-effect sensor wakes up the microcontroller, the MCU can then retrieve the value of the sensed magnetic field reading that caused the interrupt and then enable wakeup and sleep mode with GPIO interrupts again.
- **Detection of AC magnets**: AC magnets do not only affect current transformers. AC magnets can also affect shunt and Rogowski coil current sensors. To detect AC magnets, a linear 3D Hall sensor can also be used. Detecting AC magnets requires a fast-enough effective sampling period and a small enough sleep time to properly capture enough samples along a cycle of the AC magnet waveform, as Figure 2-2 shows. The effective sampling period corresponds to the time needed to get one set of samples, which is dependent on the internal sampling rate of the device. Since linear Hall sensors provide information on the actual sensed magnetic flux densities, the sensors are better able to detect AC magnets than a low-sample rate Hall switch.

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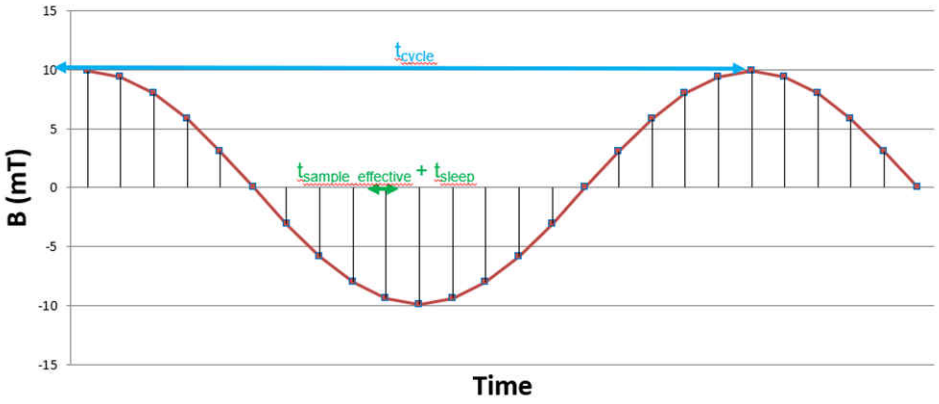

Figure 2-2. Detection AC Magnets

2.2.3 Analog Inputs

The analog front end in this design consists of the ADS131M08 delta-sigma standalone ADC. Each of the eight integrated channel converters is differential and requires that the input voltages at the pins does not exceed ±1.2 V (gain = 1). To meet this input voltage specification, the current and voltage inputs must be divided down. Because the ADS131M08 device can sense voltages down to −1.2 V, AC signals from Mains can be directly interfaced without the need for level shifters.

2.2.3.1 Voltage Measurement Analog Front End

The nominal voltage from the Mains is from 100 V – 240 V so the voltage needs to be scaled down to be sensed by an ADC. Figure 2-3 shows the analog front end used for this voltage scaling. J1 is where the voltage is applied for Phase A, similar circuitry is used for each of the Phases B and C.

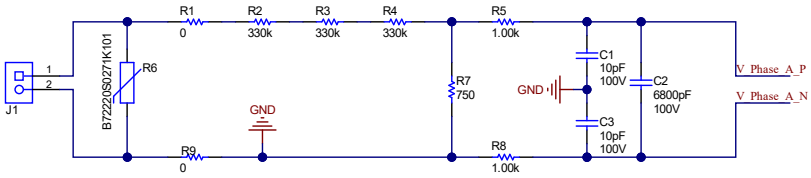

Figure 2-3. Analog Front End for Voltage Inputs

In the analog front end for voltage, there consists a spike protection varistor (R6), footprints for electromagnetic interference filter beads (resistor footprints R1 and R9), a voltage divider network (R2, R3, R4, and R7), and an RC low-pass filter (R5, R8, C1, C3, and C2).

At lower currents, voltage-to-current crosstalk affects active energy accuracy much more than voltage accuracy, if power offset calibration is not performed. To maximize the accuracy at these lower currents, in this design only a small part of the full ADC range is used for voltage channels. Since the ADCs of the ADS131M08 device are high-accuracy ADCs, using the reduced ADC range for the voltage channels in this design still provides more than enough accuracy for measuring voltage. Equation 1 shows how to calculate the range of differential voltages fed to the voltage ADC channel for a given Mains voltage and selected voltage divider resistor values.

$$V_{ADC\_Swing,\,Voltage} = \pm V_{RMS} \times \sqrt{2}\left(\frac{R_7}{R_2 + R_3 + R_4 + R_7}\right) \quad (1)$$

Based on this formula and the selected resistor values in Figure 2-3, for a mains voltage of 120 V (as measured between the line and neutral), the input signal to the voltage ADC has a voltage swing of ±128 mV (91 mV_{RMS}). For a mains voltage of 230 V (as measured between the line and neutral, the 230-V input to the front-end circuit produces a voltage swing of ±245.33 mV (173.48 mV_{RMS}). The ±128-mV and the ±245.33-mV voltage ranges are both well within the ±1.2-V input voltage that can be sensed by the ADS131M08 device for the selected PGA gain value of 1 that is used for the voltage channels.

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2.2.3.2 Current Measurement Analog Front End

The analog front end for current inputs is different from the analog front end for the voltage inputs. Figure 2-4 shows the analog front end used for a current channel, where the positive and negative leads from a CT for Phase A are connected to pins 1 and 3 of header J4. Again, similar circuitry is used for the CTs on each of the Phases B and C.

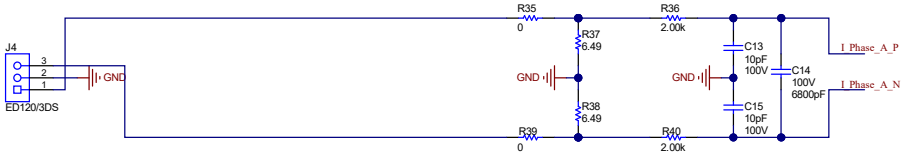

Figure 2-4. Analog Front End for Current Inputs

The analog front end for current consists of footprints for electromagnetic interference filter beads (R35 and R39), burden resistors for current transformers (R37 and R38), and an RC low-pass filter (R36, R40, C13, C15, and C14) that functions as an anti-alias filter.

As Figure 2-4 shows, resistors R37 and R38 are the burden resistors, which are in series with each other. For best THD performance, instead of using one burden resistor, two identical burden resistors in series are used with the common point being connected to GND. This split-burden resistor configuration makes sure that the waveforms fed to the positive and negative terminals of the ADC are 180 degrees out of phase with each other, which provides the best THD results with this ADC. The total burden resistance is selected based on the current range used and the turns ratio specification of the CT (this design uses CTs with a turns ratio of 2000). The total value of the burden resistor for this design is 12.98 Ω.

Equation 2 shows how to calculate the range of differential voltages fed to the current ADC channel for a given maximum current, CT turns ratio, and burden resistor value.

$$V_{ADC\_Swing,\,Current} = \pm \frac{\sqrt{2}(R_{37}+R_{38})I_{RMS,\,max}}{CT_{TURNS\_RATIO}} \quad (2)$$

Based on the maximum current of 100 A, CT turns ratio of 2000, and burden resistor of 12.98 Ω, of this design, the input signal to the current ADC has a voltage swing of ±918 mV maximum (649 mV_{RMS}) when the maximum current rating of the meter (100 A) is applied. This ±918-mV maximum input voltage is well within the ±1.2-V input range of the device for the selected PGA gain of 1 that is used for the current channels.

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2.3 Highlighted Products

2.3.1 ADS131M08

The ADS131M08 device is a eight-channel, simultaneously-sampling, 24-bit, 2nd order delta-sigma (ΔΣ), analog-to-digital converter (ADC) that offers wide dynamic range, and internal calibration features making the device an excellent choice for energy metering, power quality, and protection applications. The ADC inputs can be directly interfaced to a resistor-divider network, a transformer to measure voltage or current, or a Rogowski coil to measure current.

The individual ADC channels can be independently configured depending on the sensor input. A low noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 128 to amplify low-level signals. Additionally, these devices integrate channel to channel phase alignment and offset and gain calibration registers to help remove signal chain errors. A low-drift, 1.2-V reference is integrated into the device reducing printed circuit board (PCB) area. Cyclic redundancy check (CRC) options can be individually enabled on the data input, data output and register map to provide communication integrity. Figure 2-5 shows a block diagram of this device.

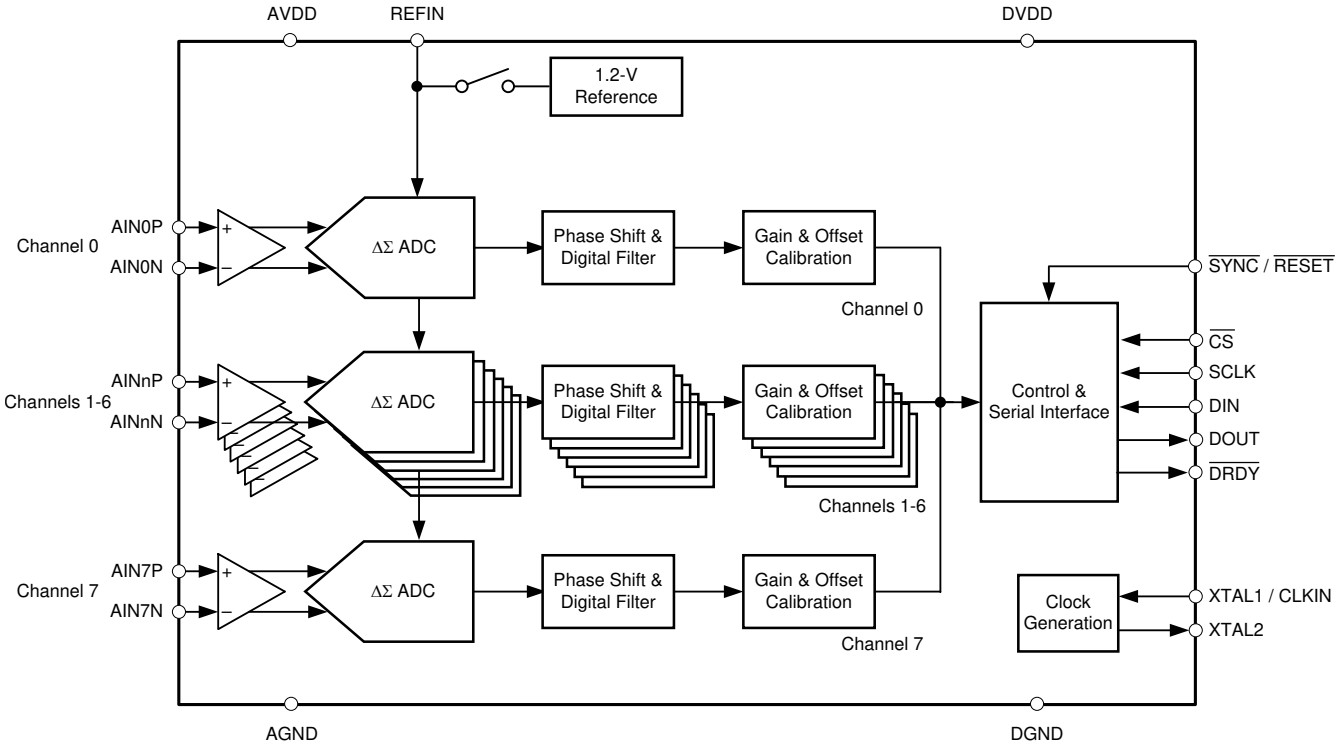

Figure 2-5. ADS131M08 Functional Block Diagram

2.3.2 MSPM0G3507

The MSPM0G device family integrates an Arm® 32-bit Cortex®-M0+ CPU with memory protection unit, clock frequency up to 80 MHz and two SPIs, one of those supporting up to 32Mbps. Other relevant peripherals for running Energy Calculations are the Real Time Clock (RTC) with calendar function, CRC-16 or CRC-32 HW module, four Universal Asynchronous Receiver Transmitters (UARTs), two I2Cs with 1Mbps and up to 60 GPIOs.

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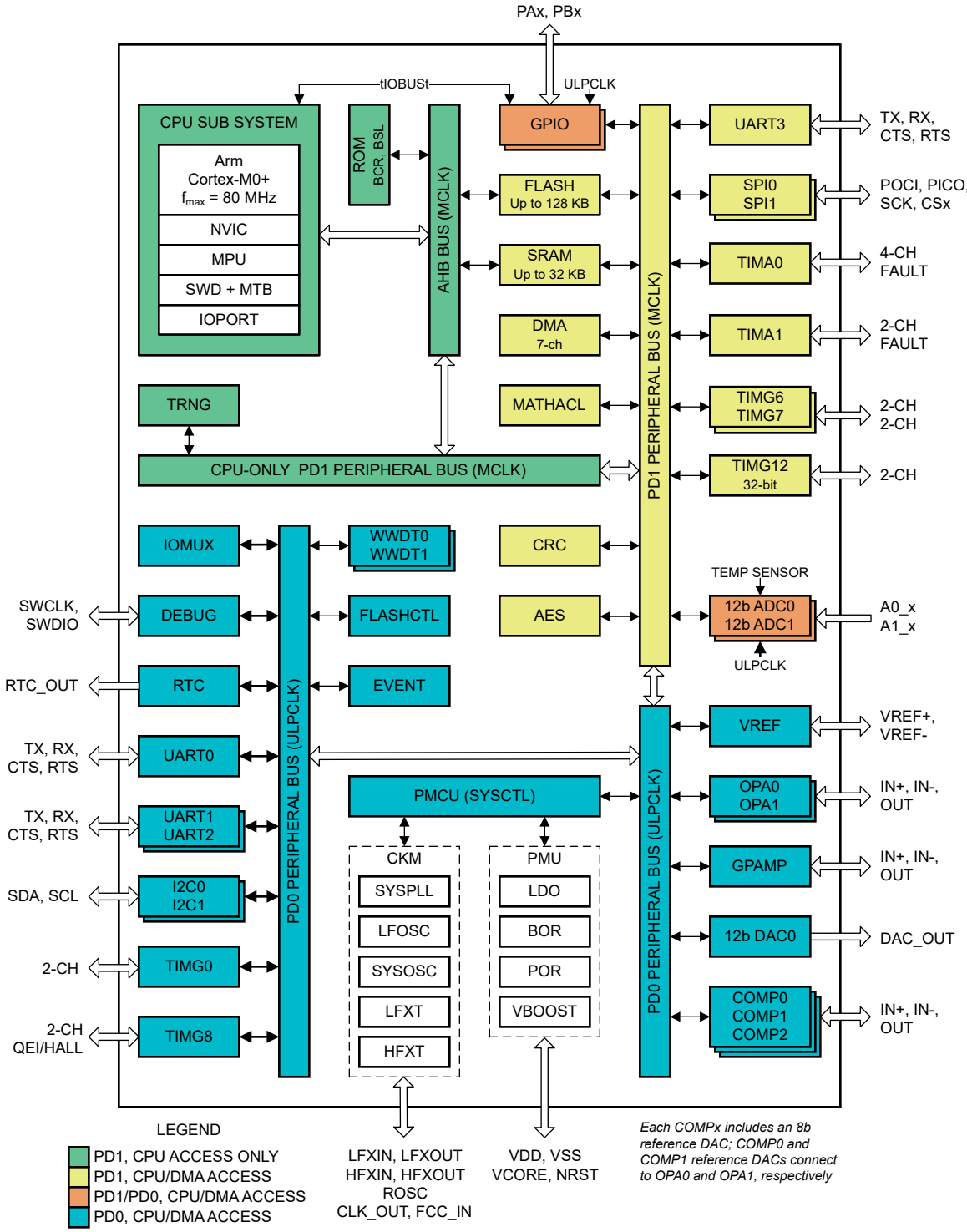

Figure 2-6. MSPM0G3507 Functional Block Diagram

The MSPM0+ MCU in this design retrieves voltage and current samples from the ADS131M08 device and calculates metrology parameters. In addition, the device also keeps track of time with the RTC module, and uses one of the UART interfaces to communicate to a PC GUI using either the isolated RS-232 or isolated RS-485 circuit of the board or sends the calculated parameters to be displayed on the LCD to an external MSP430FR4131 thru a 2nd UART link.

The CRC16 module of the MSPM0+ MCU is also used to accelerate the CRC calculations that are done to verify the integrity of the ADC packet sent by the ADS131M08 device.

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Main features of MSPM0G3507 are the extended temperature range: –40°C up to 125°C; the wide supply voltage range: 1.62 V to 3.6 V; and the integrated 128KB of flash memory with built-in error correction code (ECC) and 32KB of ECC protected SRAM with hardware parity.

The pin-compatible MSPM0G1107 device, featuring –40°C up to 105°C range and without the hardware math accelerator (MATHACL) and the AES modules can be used, if the application targets lower system cost and does not require these two peripherals.

2.3.3 MSP430FR4131 for Driving Segmented LCD Displays

The MSP430FR413x ultra-low power (ULP) microcontroller family supports low-cost LCD applications that benefit from an integrated 10-bit ADC such as remote controls, thermostats, smart meters, blood glucose monitors, and blood pressure monitors. The MCUs feature a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 10 µs. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The MSP430™ FRAM microcontroller platform combines uniquely embedded ferroelectric random access memory (FRAM) and a holistic ultra-low-power system architecture, allowing system designers to increase performance while lowering energy consumption. FRAM technology combines the low-energy fast writes, flexibility, and endurance of RAM with the nonvolatile behavior of flash.

The main features of this FRAM MCU are the temperature range: –40°C up to 85°C; the wide supply voltage range: 1.8 V to 3.6 V; and the integrated 4KB of program FRAM + 512B of information FRAM + 512B of RAM memory.

A key feature is the internal LCD driver module in the MSP430FR4131 supporting 4 × 36 or 8 × 32 segment LCD displays, which are quite popular in electricity meters.

2.3.4 TPS3840

The TPS3840 family of voltage supervisors or reset ICs can operate at high voltage levels while maintaining very low quiescent current across the whole VDD and temperature range. The TPS3840 device offers the best combination of low power consumption, high accuracy and low propagation delay.

The reset output signal of the device is asserted when the voltage at VDD drops below the negative voltage threshold (V_{IT-}) or when manual reset is pulled to a low logic ($V_{\overline{MR}\_L}$). The reset signal is cleared when VDD rises above V_{IT-} plus hysteresis (V_{IT+}) and manual reset ($\overline{MR}$) is floating or above $V_{\overline{MR}\_H}$ and the reset time delay (t_D) expires. Reset time delay can be programmed by connecting a capacitor to ground in the CT pin, because a fast reset CT pin can be left floating. Additional features include low power on reset voltage (V_{POR}), built-in glitch immunity protection for $\overline{MR}$ and VDD, built-in hysteresis and low open drain output leakage current ($I_{LKG(OD)}$).

For electricity meters, sometimes having external SVS devices to reset any microcontrollers in the system is beneficial, even if the microcontrollers already have an internal SVS. In this design the TPS3840 external SVS device is added for an additional level of security. External SVS devices can sometimes also be used for early detection of a Mains blackout condition by monitoring one of the rails of an AC/DC powered from Mains.

In this design, the TPS3840DL17 variant is specifically used, which has a 1.7-V threshold and an open drain, active low output.

2.3.5 THVD1400

The THVD1400 is a robust half-duplex RS-485 transceiver for industrial applications. The bus pins are immune to high levels of IEC Contact Discharge ESD events, eliminating the need for additional system-level protection components due to ±12-kV IEC 61000-4-2 contact discharge bus I/O protection. The device operates from a single 3- to 5.5-V supply and is available in industry standard, 8-pin SOIC package for drop-in compatibility as well as in the industry-leading, small SOT package.

The device is characterized for ambient temperatures from –40°C to 125°C and also meets or exceeds the requirements of the TIA/EIA-485A standard. The wide common-mode voltage range and low input leakage on bus pins make the devices an excellent choice for multi-point applications over long cable runs.

This device is specifically used in this design to convert from UART to RS-485 signals.

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2.3.6 ISO6731

To add isolation to the RS-232 and RS-485 connection to a PC, the isolated RS-232 and isolated RS-485 portion of this reference design uses capacitive galvanic isolation, which has an inherent life span advantage over an opto-isolator. In particular, industrial devices are usually pressed into service for much longer periods of time than consumer electronics; therefore, maintenance of effective isolation over a period of 15 years or longer is important.

The ISO6731 device is a high-performance, triple-channel digital isolator designed for cost-sensitive applications requiring up to 5000 V_{RMS} isolation ratings per UL 1577. This device is also certified by VDE, TUV, CSA, and CQC. The ISO6731 device provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications.

The ISO6731 device has two forward and one reverse-direction channels. In the event of input power or signal loss, the default output is high for the device without suffix F and low for the device with suffix F.

In this design, two isolation channels are used for the TX and RX in RS-485 communication mode, while the third isolation channel is used for the RE_DE control signal used to enable the receiver or driver. This chip supports a signaling rate of 50Mbps and operates from a 1.71-V to 1.89-V and 2.25-V to 5.5-V supply in the temperature range: –40°C to +125°C.

2.3.7 ISO6720

The ISO6720 device is a high-performance, dual-channel digital isolator designed for cost-sensitive applications requiring up to 3000 V_{RMS} (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO6720 device provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO2) insulation barrier. The ISO6720 device has 2 isolation channels with both channels in the same direction. Through remarkable chip design and layout techniques, the electromagnetic compatibility of the ISO6720 devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO6720 family of devices is available in a 8-pin SOIC narrow-body (D) package and is a pin-to-pin upgrade to the older generations.

To test the active energy and reactive energy accuracy of a meter, pulses are output at a rate proportional to the amount of energy consumed. A reference meter can then determine the accuracy of the electricity meter by calculating the error based on these pulses and how much energy is provided to the meter. In this reference design, pulses are output through headers for the cumulative active and reactive energy consumption. Using the ISO6720 device provides an isolated version of these headers for connection to non-isolated equipment. In this design, the D package of the ISO6720 device is used, which provides an isolation voltage of 3000 V_{RMS} for these signals. These isolated active and reactive signals can be set to have either a 3.3- or 5-V maximum voltage output by applying the selected maximum voltage output between the VCC (ISO_VCC) and GND (ISO_GND) of the isolated side.

This chip supports a signaling rate of 50Mbps and operates from a 1.71-V to 1.89-V and 2.25-V to 5.5-V supply in the temperature range: –40°C to +125°C.

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2.3.8 TRS3232E

To properly interface with the RS-232 standard, a voltage translation system is required to convert between the 3.3-V domain on the board and from the 12 V on the port itself. To facilitate the translation, the design uses a TRS3232E device. The TRS3232E device is capable of driving the higher voltage signals on the RS-232 port from only the 3.3-V DVCC through a charge pump system.

The TRS3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV electrostatic discharge (ESD) protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of the Telecommunications Industry Association and Electronic Industries Alliance TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250kbps and a maximum of 30-V/µs driver output slew rate.

2.3.9 TPS709

To power the data terminal equipment (DTE) side of the isolation boundary and the RS-232 charge pump, there are two choices. The interface can either implement an isolated power supply or harvest power from the RS-232 line. Integrating a power supply adds cost and complexity to the system, which is difficult to justify in low-cost sensing applications.

To implement the second option of harvesting power from the RS-232 port itself, this reference design uses the flow control lines that are ignored in most embedded applications. The RS-232 specification (when properly implemented on a host computer or adapter cable), keeps the request to send (RTS) and data terminal ready (DTR) lines high when the port is active. As long as the host has the COM port open, these two lines retain voltage on them. This voltage can vary from 5 V to 12 V, depending on the driver implementation. The 5 V to 12 V is sufficient for the use requirements in this design.

The voltage is put through a diode arrangement to block signals from entering back into the pins. The voltage charges a capacitor to store energy. The capacitor releases this energy when the barrier and charge pump pull more current than what is instantaneously allowed. The TPS70933 device is used to bring the line voltage down to a working voltage for the charge pump and isolation device.

In addition to being used in the RS-232 circuit, an additional TPS709 device is used to regulate the 5-V input voltage from the 5V_IN rail down to the 3.3 V used to power most of the components on the board.

The TPS70933 linear regulator is an ultra-low quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy overtemperature. A quiescent current of only 1 µA makes these devices an excellent design for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety. These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA (typical).

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2.3.10 TMAG5273

The TMAG5273 is a low-power linear 3D Hall-effect sensor designed for a wide range of industrial and personal electronics applications. This device integrates three independent Hall-effect sensors in the X, Y, and Z axes. A precision analog signal chain along with an integrated 12-bit ADC digitizes the measured analog magnetic field values. The I2C interface, while supporting multiple operating VCC ranges, provides seamless data communication with low-voltage microcontrollers. The device has an integrated temperature sensor available for multiple system functions, such as thermal budget check or temperature compensation calculation for a given magnetic field. The TMAG5273 can be configured through the I2C interface to enable any combination of magnetic axes and temperature measurements. Additionally, the device can be configured to various power options (including wake-up and sleep mode) allowing designers to optimize system power consumption based on their system-level needs. Multiple sensor conversion schemes and I2C read frames help optimize throughput and accuracy. A dedicated INT pin can act as a system interrupt during low power wake-up and sleep mode, and can also be used by a microcontroller to trigger a new sensor conversion. The ultra-low power consumption is defined by 2.3-mA active mode current, 1-µA wake-up current and just 5-nA sleep mode current.

TMAG5273 operates from 1.7-V to 3.6-V supply voltage in the –40°C to +125°C temperature range at a maximum 1-MHz I2C clock speed.

- The TMAG5273 is a linear 3D Hall-effect sensor that is designed for electricity meters.
- The TMAG5273 is offered in four different factory-programmed I2C addresses. The device also supports additional I2C addresses through the modification of a user-configurable I2C address register.
- Figure 2-7 shows how the TMAG5273 defines the X, Y, and Z directions:

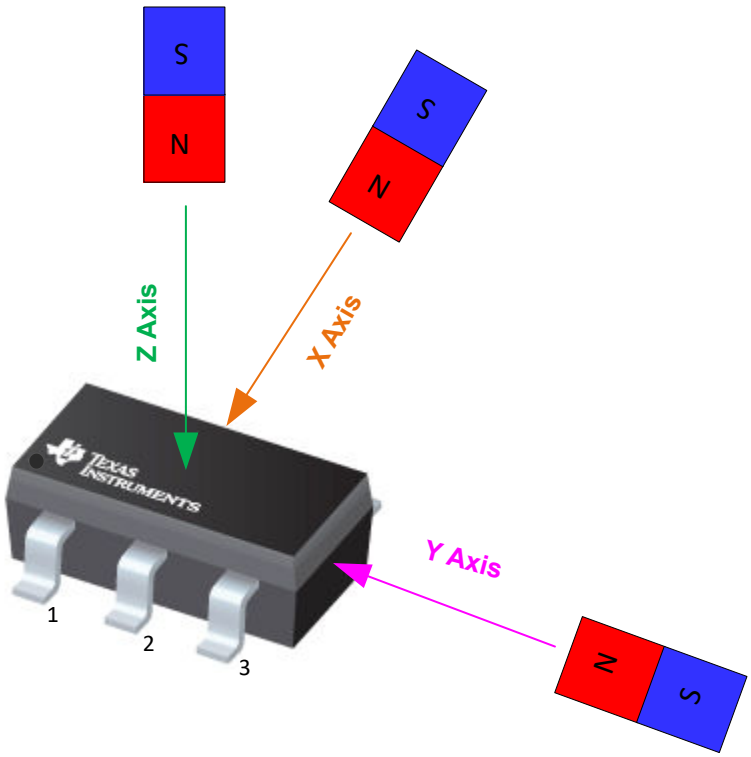

Figure 2-7. Field Direction Definition

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3 System Design Theory

This chapter explains the hardware architecture and the necessary software support for the MSPM0G3507 and ADS131M08 devices.

3.1 How to Implement Software for Metrology Testing

The MSPM0+ software used for evaluating this design is test software. This section discusses the features of the test software, which provides insight on how to implement custom software for metrology testing. This section discusses the setup of the ADS131M08 device and various peripherals on the MSPM0G3507 MCU. Subsequently, the metrology software is described as two major processes: the *foreground process* and *background process*.

The test data included in this reference design was taken using the generic test code written for the MSPM0G3507 MCU, which is a porting of the ADC Energy Metrology Library software to the TI MSPM0G-series of MCUs.

The original ADC Energy Metrology Library was developed and tested on an Arm Cortex-M4F MCU, which makes the software easily portable to popular Arm Cortex-M3, M4(F), and M33 microcontrollers, such as TI's wireless MCUs portfolio of Sub-1-GHz and 2.4-GHz devices.

The MSPM0+ software contains hardware abstraction layers which enable communication between the standalone ADC and an Arm Cortex-M0+ MCU and a library of metrology calculations for energy measurements. Also included in the software is a Microsoft Windows PC GUI to display metrology parameters from the TIDA-010243 reference design.

3.2 Clocking System

The MSPM0G3507 MCU is configured to have the CPU clock (MCLK) set at 79.87 MHz and the CLK_OUT clock signal to ADS131M08 is set to 8.192 MHz. The external 16.384 MHz XTAL, which is feeding the PLL module and is being multiplied and divided with specific factors, generates a MCLK frequency (the CPU clock speed) of 79.87 MHz.

The external 16.384-MHz crystal is divided by 2 to create the 8.192-MHz output frequency for CLK_OUT. An internal 32.768-kHz LFOSC is used as the clock source for the auxiliary clock (RTCCLK) of the device.

All these settings are configured in the TIDA-010243.syscfg file in the software deliverable, utilizing the graphical Clock Tree configuration inside the SYSCONFIG tool.

3.3 UART Setup for GUI Communication

The MSPM0+ MCU is configured to communicate to the PC GUI through either the RS-232 or RS-485 connection on this reference design. The MSPM0G3507 MCU communicates to the PC GUI using a UART module configured for 115,200 baud with 8N1.

3.4 Real-Time Clock (RTC)

The real-time clock module of the MSPM0G3507 MCU is configured to give precise two-second interrupts and update the calendar time and date, as necessary.

3.5 LCD Controller in MSP430FR4131

The LCD_E peripheral module on the MSP430FR4131 MCU can support up to 8-MUX displays with 256 segments or 4-MUX with 144 segment displays, as used in this design with the FH-1152P LCD. In the PCB layout-driven design process, LCD_E offers fully-software-configurable segment S and common COM signals which are connected to the respective MSP430 device pins. This enables an optimized routing of the PCB which avoids signal crossings and keeps signals on one side of the PCB only, here the top layer. If the internal charge pump of the LCD module is used, place the externally provided capacitor on the LCDCAP0 and LCDCAP1 pins as close as possible to the MCU. Connect the capacitor to the device using a short and direct trace. TI recommends using the VLO on-chip oscillator for the lowest system cost. The ultra-low power VLO has an accuracy of 10 kHz ±50% so calibrate the VLO against the ±1% accurate on-chip 16-MHz digitally-controlled oscillator (DCO) with frequency-locked loop (FLL).

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Alternatively, a 32.768-kHz clock output from MSPM0G3507 device can be provided to the MSP430FR4131 using a GPIO output.

3.6 Direct Memory Access (DMA)

The DMA module transfers packets between the MSPM0G3507 MCU and ADS131M08 device with minimal hardware resources and timing overhead. Two DMA channels are used for communicating to the ADS131M08. DMA Channel 0 is used to send data to the ADS131M08 and DMA Channel 1 is used simultaneously to receive the measurements data from the ADS131M08 over SPI bus. Once a complete packet has been received from the ADS131M08, an interrupt is generated to complete the (optional but strongly recommended) CRC16 verification of the data packet and finally the packet disassembly into voltage and current values per each phase line and the neutral line is done. Figure 3-5 shows the packets that are sent and received using the DMA of the MSPM0G3507 MCU.

3.7 ADC Setup

The ADS131M08 registers must be initialized to deliver measurement data from all 7 channels (the 8-th channel is unused but still has to be read out over SPI). This process is followed when the ADS131M08 is being first setup after the MSPM0G3507 MCU resets as well as each time calibration is performed.

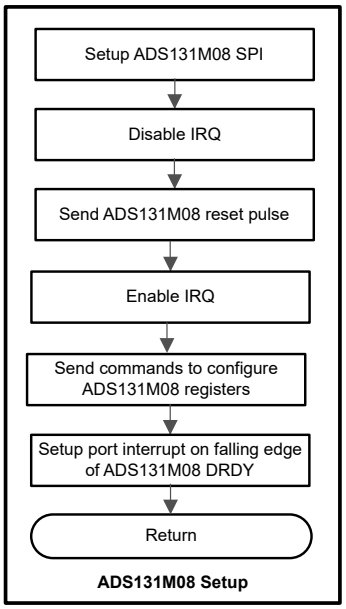

Figure 3-1. ADC Initialization and Synchronization Process

The SPI module of the MSPM0+ MCU is configured for communication to the ADS131M08 device as a controller device that uses 4-wire mode (the chip-select signal is automatically asserted high and low by the SPI hardware module) and has a 19.87-MHz SPI clock that is derived from the MCU MCLK clock, divided by 4. After the SPI is setup, all interrupts are disabled and a reset command is sent from the MSPM0+ MCU to the ADS131M08 via SPI. Interrupts are then re-enabled and the MSPM0+ MCU sends commands to the ADS131M08 to configure the registers.

By sending write commands to the ADS131M08 registers, the following configuration is done:

- MODE register settings: 16-bit CCITT CRC used, 24-bit length for each word in the ADS131M08 packet, $\overline{\text{DRDY}}$ signal asserted on most lagging enabled channel, $\overline{\text{DRDY}}$ asserted high when conversion value is not available, $\overline{\text{DRDY}}$ asserted low when conversion values are ready
- GAIN1 register settings: PGA gain of 1 used for all four ADC channels
- CFG register settings: Current detection mode disabled
- CHx_CNG register settings (where x is the channel number)
  - 3-phase mode: All seven ADC channel inputs connected to external ADC pins and channel phase delay set to 0 for each channel (note that software phase compensation is used instead of ADS131M08 hardware phase compensation).

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- CLOCK register settings: 512 OSR, all channels enabled, and high-resolution modulator power mode

After the ADS131M08 registers are properly initialized, the MSPM0+ MCU is configured to generate a port interrupt whenever a falling edge occurs on the $\overline{\text{DRDY}}$ pin, which indicates that the ADS131M08 has new measurement samples available.

The ADS131M08 modulator clock is derived from the clock fed to the CLKIN pin, which is output from the CLK_OUT output of the MSPM0+ MCU. The clock fed to the CLKIN pin of the ADS131M08 device is internally divided by two, to generate the ADS131M08 modulator clock. The sampling frequency of the ADS131M08 is therefore defined as shown in Equation 3.

$$f_S = \frac{f_M}{OSR} = \frac{f_{CLKIN}}{2 \times OSR} \tag{3}$$

where

- f_S is the sampling rate
- f_M is the modulator clock frequency
- f_{CLKIN} is the clock fed to the ADS131M08 CLKIN pin
- OSR is the selected oversampling ratio

In this design, the CLK_OUT signal of the MSPM0+ MCU that is fed to the ADS131M08 CLKIN pin has a frequency of 8.192 MHz. The oversampling ratio is selected to be 512 with the appropriate register setting. As a result, the ADS131M08 modulator clock is set to 4.096 MHz and the sample rate is set to 8000 samples per second.

For a 3-phase system where each line-to-neutral voltage is measured, at least six ADC channels are necessary to independently measure three voltages and three currents. In this design, the following ADS131M08 channel mappings are used in software for the 3-phase configuration:

- AIN0P and AIN0N ADS131M08 ADC channel pins → Voltage V1 (Phase A Line-to-Neutral Voltage)
- AIN1P and AIN1N ADS131M08 ADC channel pins → Voltage V2 (Phase B Line-to-Neutral Voltage)
- AIN2P and AIN2N ADS131M08 ADC channel pins → Voltage V3 (Phase C Line-to-Neutral Voltage)
- AIN3P and AIN3N ADS131M08 ADC channel pins → Current I1 (Phase A Current)
- AIN4P and AIN4N ADS131M08 ADC channel pins → Current I2 (Phase B Current)
- AIN5P and AIN5N ADS131M08 ADC channel pins → Current I3 (Phase C Current)
- AIN6P and AIN6N ADS131M08 ADC channel pins → Current N (Neutral Current)
- AIN7P and AIN7N ADS131M08 ADC channel pins → unconnected, channel 7 data is always reported as 0x00 00 00 over SPI when ADS131M08 is 24-bit mode with channel 7 disabled

3.8 Foreground Process

The foreground process includes the initial setup of the MSPM0+ MCU hardware and software and the ADS131M08 registers immediately after a device RESET. Figure 3-2 shows the flowchart for this process.

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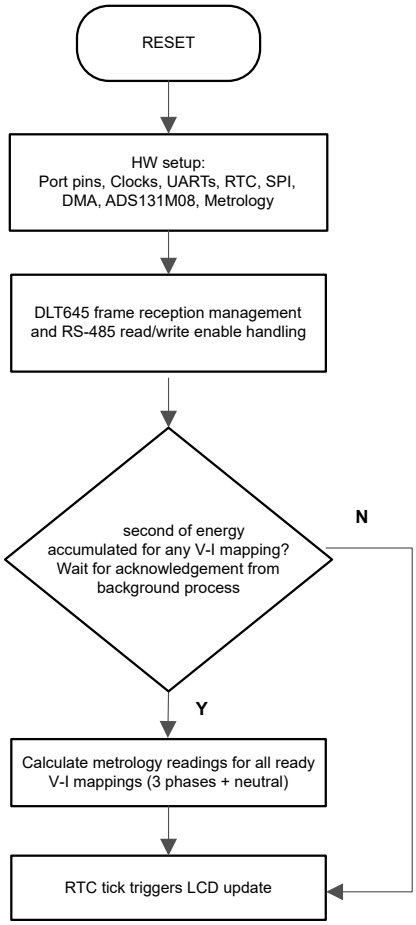

Figure 3-2. Foreground Process

The initialization routines involve the setup of the MSPM0G3507:

- General purpose input/output (GPIO) port pins
- Clock system (MCLK or CPU clock, RTC clock, SPI clock, I2C clock, CLK_OUT pin)
- 4 UART ports for UART functionality
- Two DMA channels, one per SPI receive and transmit
- ADS131M08 registers
- Metrology variables

After the hardware is setup, any received frames from the GUI are processed. If RS-485 is selected for communication to the PC GUI, the THVD1400 device must have the RE and DE pins driven to enable the receiver and driver during the proper points in time to receive packets from the PC GUI and send responses back to the GUI. After any packet is sent from the MSPM0+ MCU to the PC GUI, the foreground process is responsible for asserting the RE and DE pins after the packet has been completely sent out from the MSPM0+ MCU but before the GUI sends out the next packet.

Subsequently, the foreground process checks whether the background process has notified the foreground process to calculate new metering parameters for any voltage-current mappings. This notification is accomplished through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for approximately one second in the background process. This is equivalent to an accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps track of how many samples accumulate over this frame period. This count can vary as the software synchronizes with the incoming Mains frequency.

The processed dot products include the V_{RMS}, I_{RMS}, active power, and reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. Processed

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voltage dot products, current dot products, active energy dot products, and reactive energy dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the calculated values of active and reactive power of the foreground process, the apparent power is calculated. The frequency (in Hz) and power factor are also calculated using parameters calculated by the background process using the formulas in Section 3.8.1.

For the 3-phase configuration, there are three voltage-current mappings, where each voltage-to-current mapping has a different voltage and current channel. Specifically, the line-to-neutral voltage measurement for line A and the line A current measurement are associated with each other for one mapping and the line-to-neutral voltage measurement for line B and the line B current measurement are associated with each other for the other mapping and the same for Line C. For simplicity, note that each voltage-to-current mapping is referred to as a phase in the rest of this documentation as well as in the PC GUI.

The foreground process also updates the LCD. The LCD display item is changed every two seconds. See Section 4.2.4.1 for more information about the different items displayed on the LCD.

3.8.1 Formulas

This section describes the formulas used for the voltage, current, power, and energy calculations. As previously described, voltage and current samples are obtained at a sampling rate of 8000 Hz. All of the samples that are taken in approximately one second frames are kept and used to obtain the RMS values for voltage and current for each phase. The RMS values are obtained with the following formulas:

$$V_{RMS,\,ph} = K_{v,\,ph} \times \sqrt{\frac{\sum_{n=1}^{Sample\ Count} v_{ph}(n) \times v_{ph}(n)}{Sample\ Count}} - v_{offset,\,ph} \tag{4}$$

$$I_{RMS,\,ph} = K_{i,\,ph} \times \sqrt{\frac{\sum_{n=1}^{Sample\ Count} i_{ph}(n) \times i_{ph}(n)}{Sample\ Count}} - i_{offset,\,ph} \tag{5}$$

where

- ph = Phase parameters that are being calculated [that is, Phase A (= 1) or B (= 2)]
- $v_{ph}(n)$ = Voltage sample at a sample instant n
- $v_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter
- $i_{ph}(n)$ = Each current sample at a sample instant n
- $i_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the current converter
- Sample count = Number of samples within the present frame
- $K_{v,ph}$ = Scaling factor for voltage
- $K_{i,ph}$ = Scaling factor for current

Power and energy are calculated for active and reactive energy samples of one frame. These samples are phase-corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,\,ph} = K_{ACT,\,ph} \frac{\sum_{n=1}^{Sample\ Count} v(n) \times i_{ph}(n)}{Sample\ Count} - P_{ACT\_Offset,\,ph} \tag{6}$$

$$P_{REACT,\,ph} = K_{REACT,\,ph} \frac{\sum_{n=1}^{Sample\ Count} v_{90,\,ph}(n) \times i_{ph}(n)}{Sample\ Count} - P_{REACT\_Offset,\,ph} \tag{7}$$

$$P_{APP,\,ph} = \sqrt{P_{ACT,\,ph}{}^2 + P_{REACT,\,ph}{}^2} \tag{8}$$

where

- $v_{90}(n)$ = Voltage sample at a sample instant ‘n’ shifted by 90°
- $K_{ACT,ph}$ = Scaling factor for active power
- $K_{REACT,ph}$ = Scaling factor for reactive power
- $P_{ACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the active power measurements from other phases and the neutral

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- $P_{REACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the reactive power measurements from other phases and the neutral

Note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents
2. This approach conforms to the measurement method specified by IEC and ANSI standards

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, the mains frequency is first measured accurately to phase shift the voltage samples accordingly.

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90 degrees before the current sample and a voltage sample slightly less than 90 degrees before the current sample are used. The phase shift implementation of the application consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays.

In addition to calculating the per-phase active and reactive powers, the cumulative sum of these parameters are also calculated using Equation 9, Equation 10, and Equation 11.

$$P_{ACT,\,Cumulative} = \sum_{ph\,=\,1}^{2} P_{ACT,\,ph} \tag{9}$$

$$P_{REACT,\,Cumulative} = \sum_{ph\,=\,1}^{2} P_{REACT,\,ph} \tag{10}$$

$$P_{APP,\,Cumulative} = \sum_{ph\,=\,1}^{2} P_{APP,\,ph} \tag{11}$$

Using the calculated powers, energies are calculated with the following formulas in Equation 12.

$$\begin{aligned} E_{ACT,\,ph} &= P_{ACT,\,ph} \times \text{Sample Count} \\ E_{REACT,\,ph} &= P_{REACT,\,ph} \times \text{Sample Count} \\ E_{APP,\,ph} &= P_{APP,\,ph} \times \text{Sample Count} \end{aligned} \tag{12}$$

From there, the energies are also accumulated to calculate the cumulative energies, by the following Equation 13, Equation 14, and Equation 15.

$$E_{ACT,\ \ Cumulative} = \sum_{ph\,=\,1}^{2} E_{ACT,\,ph} \tag{13}$$

$$E_{REACT,\,Cumulative} = \sum_{ph\,=\,1}^{2} E_{REACT,\,ph} \tag{14}$$

$$E_{APP,\,Cumulative} = \sum_{ph\,=\,1}^{2} E_{APP,\,ph} \tag{15}$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since system reset. Note that these energies are different from the working variables used to accumulate energy for outputting energy pulses. There are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0; inductive generator)
6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

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The background process also calculates the frequency in terms of samples-per-mains cycle. The foreground process then converts this samples-per-mains cycle to Hertz with Equation 16.

$$\text{Frequency}\left(\text{Hz}\right) = \frac{\text{Sample Rate (samples / second)}}{\text{Frequency (samples / second)}} \tag{16}$$

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the internal representation of power factor of the system, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated with Equation 17.

$$\text{Internal Representation of Power Factor} = \begin{cases} \frac{\text{P}_{\text{ACT}}}{\text{P}_{\text{Apparent}}}, \textit{ if capacitive load} \\ \frac{\text{P}_{\text{ACT}}}{\text{P}_{\text{Apparent}}}, \textit{ if inductive load} \end{cases} \tag{17}$$

3.9 Background Process

Figure 3-3 shows the different events that occur when sampling voltage and current, where the items in gray are done by the hardware settings and not the test software.

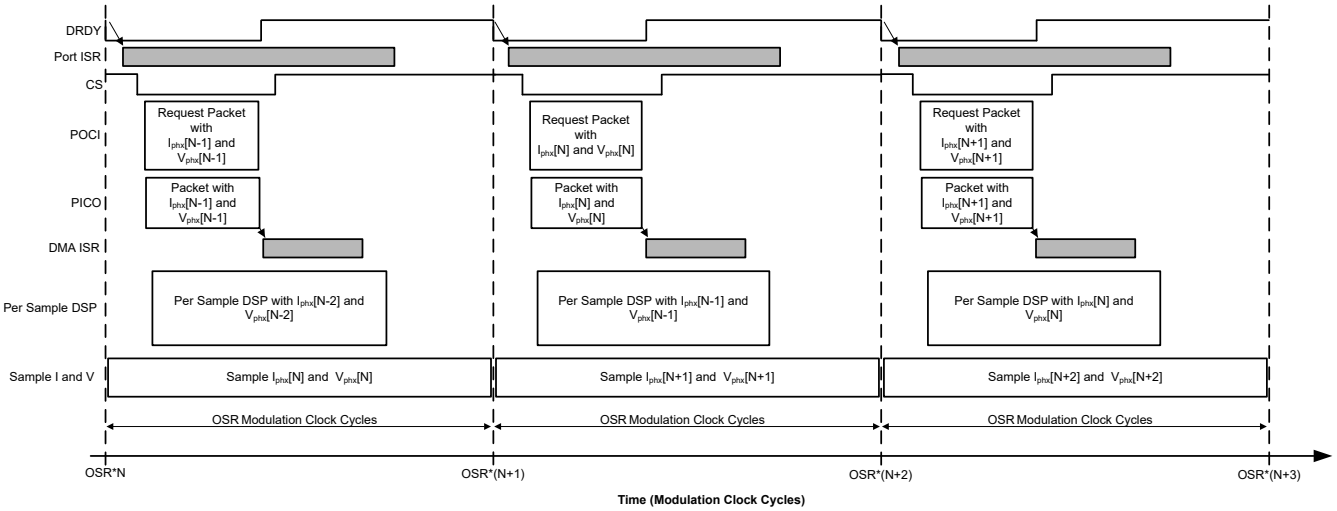

Figure 3-3. Voltage and Current Sampling Events

To go over the process mentioned in Figure 3-3, new current samples for each phase are ready every OSR, or 512 for this design, modulation clock cycles resulting 8000 samples per second over the SPI Bus to MSPM0+ MCU. Each sample contains 30 Bytes, with 3 Bytes data per ADC channel. Suppose the most recently ready phase current and voltage samples from the ADS131M08 device corresponds to the N^{th} – 1 current and voltage sample, or $I_{phx}[N - 1]$ and $V_{phx}[N - 1]$. Once new samples are ready, the $\overline{\text{DRDY}}$ pin is asserted low by the ADS131M08. The falling edge on the $\overline{\text{DRDY}}$ pin on the ADS131M08 causes a GPIO port interrupt on the MSPM0+ MCU, which triggers the Port ISR, and the background process is run within the Port ISR. Figure 3-4 shows the background process, which mainly deals with timing-critical events in the test software.

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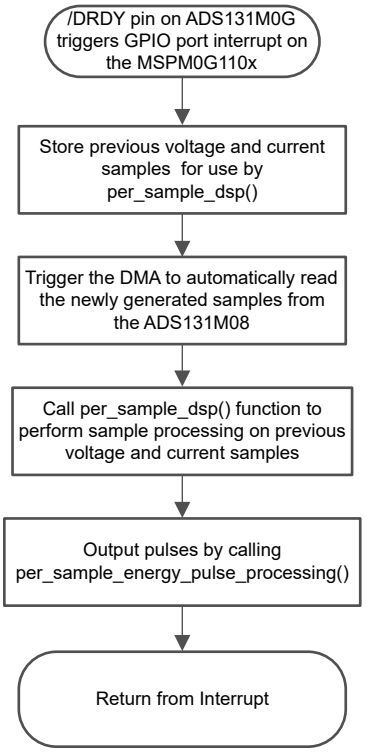

Figure 3-4. Background Process

In the background process, the previously-obtained voltage samples ($V_{phx}[N – 2]$) and previously obtained current samples ($I_{phx}[N – 2]$) are stored so that these samples can be used later by the per_sample_dsp function, which is responsible for updating the intermediate dot product quantities used to calculate metrology parameters.

After the previously-obtained voltage and current samples are stored, communication to the ADS131M08 is enabled by asserting the chip select signal low. The DMA is then configured to both send a request for the newest current and voltage samples ($I_{phx}[N – 1]$ and $V_{phx}[N – 1]$) of the ADS131M08 device and also to receive the data packet response from the ADS131M08. The request and reception of the current samples is done automatically by the DMA module.

Figure 3-5 shows the packet that is transmitted by the DMA of the MSPM0+ MCU and the response packet from the ADS131M08 that is received and assembled by the DMA as well. The transmission and reception packets contain 10 words, where each word is three bytes long, resulting in 30 Bytes DMA transaction over the SPI bus.

MSPM0+ Transmit	Command[N+1] / Dummy Write (3 bytes =0x00 00 00)	Dummy Write (3 bytes= 0x00 00 00)	Dummy Write (3 bytes= 0x00 00 00)	Dummy Write 5 x (3 bytes= 0x00 00 00)	Dummy Write (3 bytes= 0x00 00 00)	Dummy Write (3 bytes= 0x00 00 00)
MSPM0+ Receive	Response to Command[N]/Not used in design (3 bytes)	ADS131M08 Ch 0 Sample (3 bytes, MSB sent first)	ADS131M08 Ch 1 Sample (3 bytes, MSB sent first)	ADS131M08 Ch 2...Ch 6 Samples 5 x (3 bytes, MSB sent first)	ADS131M08 Ch 7 Sample (3 bytes, 0x00 00 00, MSB sent first)	ADS131M08 Packet CRC (3 bytes, MSB sent first)

Figure 3-5. ADS131M08 ADC Sample Request Packet

When requesting the ADC data from the ADS131M08 device, the first word that has to be sent to the ADS131M08 is the command word. Since the test software does not need to change the settings of the ADS131M08 or read any registers during typical ADC sample readouts, a NULL command is sent to the ADS131M08, which allows the designer to get the ADC samples from the ADS131M08 without changing the

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state of the device. The actual size of the null command is 16-bits; however, since 24-bit words are used, the 16-bit command must be padded with an extra value of 0x00 at the end of the command. The NULL command word sent; therefore, has a value of 0x00 00 00. While the MSPM0+ MCU is shifting out the command word, the MCU is simultaneously shifting in the response word to the command word of the previous packet. The response word to a NULL command is the contents of the STATUS register. The contents of the STATUS register is not used in this design so the first word received from the ADS131M08 is ignored (not processed in the software code).

After writing the command word, it is necessary for a dummy write to be performed for each byte that is to be read. The dummy byte write is necessary to enable the SPI clock, which is necessary to read a byte from the ADS131M08 device. For each dummy byte write, a value of 0x00 is written to the SPI transmit register. Immediately after writing the command byte, writing three dummy bytes allows the MSPM0+ MCU to receive the 3-byte ADC value from channel 0 of the ADS131M08. Writing the next 21 dummy bytes gets the ADC data for channel 1, channel 2, and so on up, to channel 7, respectively. Finally, writing the next three dummy bytes gets the CRC word. The CRC word is 24-bits; however, note that the actual CRC is only 16-bits, which are placed in the most significant bits of the 24-bit word. As a result, when parsing the CRC word, the last byte is not needed (note though that the dummy write for this zero-padded byte must still be sent though for proper ADS131M08 operation).

Figure 3-3 shows that whenever the DMA has received the entire $I_{phx}[N – 1]$ packet, the DMA ISR is automatically called. Within the ISR, the CRC is calculated over the nine command and ADC words (9 × 3 = 27 bytes in total). This CRC calculation can be done in two modes: either using the CRC module of the MSPM0G3507 MCU or using the memcpy() function to move the 27 Bytes ADC data to a special memory area where CRC16 is auto-calculated.

Both methods were successfully implemented in the test software, see the *verify_add_CRC()* routine. Here, the memcpy() implementation achieves almost 5 × faster calculation than using the CRC16 registers with bytewise feed and is used by default. The CRC module can be fed with 8- or 16-bit data, and since there are 27 bytes total, the CRC module is being updated byte for byte. Once the CRC has been calculated over the packet, the check is compared to the CRC obtained in the packet sent from the ADS131M08. The sent CRC is parsed from bytes 28 and 29 (byte 30 is the zero-padding for CRC16, so this byte value gets ignored).

If the calculated CRC and the parsed CRC are equal, then the CRC check passes and the ADC data is parsed to get the values of the voltage and current samples at time N – 1. The parsed voltage and current samples are put in temporary buffers so that this information is used the next time the per_sample_dsp function is called at the next interrupt. When the SPI transfer over DMA ends, the $\overline{CS}$ (chip select) line is automatically pulled back high again from the MSPM0+ MCU to properly reset the ADS131M08 communication before the next time current samples are ready for readout.

In parallel to transferring the latest current and voltage samples $I_{phx}[N – 1]$ and $V_{phx}[N – 1]$ to the MSPM0+ MCU using the DMA channels, the ADS131M08 is already sampling the next voltage ($V_{phx}[N]$) and current samples ($I_{phx}[N]$) while the test software performs per-sample processing on the earlier voltage ($V_{phx}[N – 2]$) and current samples ($I_{phx}[N – 2]$) obtained from the ADS131M08. This per-sample processing is used to update the intermediate dot product quantities that are used to calculate the metrology parameters. After sample processing, the background process uses the "per_sample_energy_pulse_processing" for the calculation and output of energy-proportional pulses. Once the *per_sample_energy_pulse_processing* is completed, the test software exits from the port ISR.

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3.10 Software Function per_sample_dsp()

Figure 3-6 shows the flowchart for the per_sample_dsp() function. The per_sample_dsp() function is used to calculate intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. Both voltage and current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power and reactive power are also accumulated in 64-bit registers.

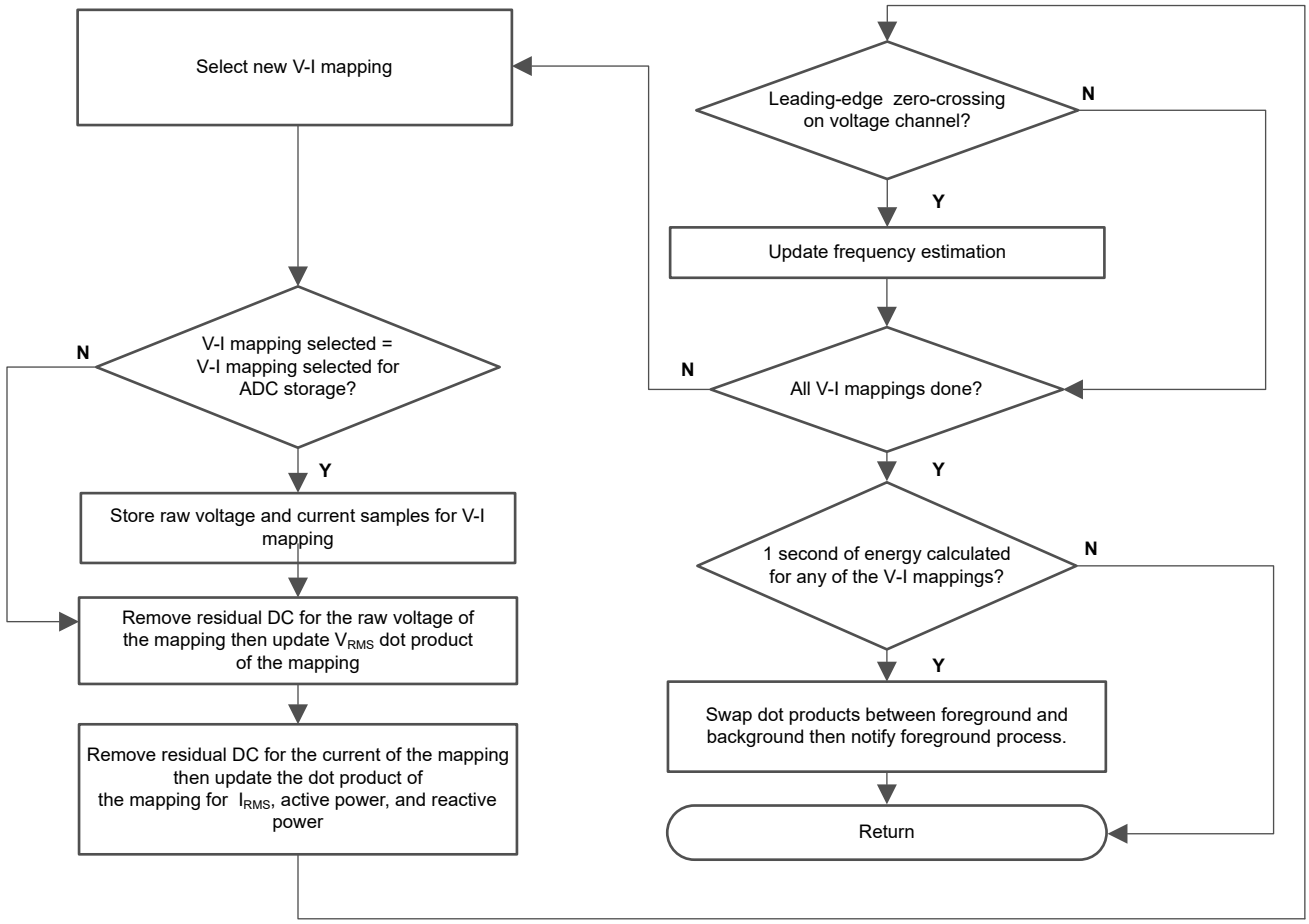

Figure 3-6. per_sample_dsp Function

After sufficient samples (of approximately one second) are accumulated, the foreground function is triggered to calculate the final values of V_{RMS}; I_{RMS}; active, reactive, and apparent powers; active, reactive, and apparent energy; frequency; and power factor. In the test software, there are two sets of dot products for a phase: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, the process swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products. Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel, the per_sample_dsp() function is also responsible for updating the corresponding frequency (in samples per cycle) of the phase.

The following sections describe the various elements of electricity measurement in the per_sample_dsp() function.

3.10.1 Voltage and Current Signals

The test software of the design has support for storing the raw voltage and current ADC values for phase A, B, and C. These raw ADS131M08 samples are signed integers and any stray DC or offset value on these converters are removed using a DC tracking filter. A separate DC estimate for all voltages and currents is obtained using the filter, voltage, and current samples, respectively. This estimate is then subtracted from each voltage and current raw ADC sample.

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The resulting instantaneous voltage and current samples are used to generate the following intermediate results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively
- Accumulated energy samples to calculate active energy
- Accumulated energy samples using current and 90° phase-shifted voltage to calculate reactive energy

The foreground process processes these accumulated values.

3.10.2 Frequency Measurement and Cycle Tracking

The instantaneous voltages, currents, active powers, and reactive powers are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When samples of approximately one second have been accumulated, the background process stores these accumulation registers and notifies the foreground process to produce the average results, such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. Figure 3-7 shows the samples near a zero cross and the process of linear interpolation.

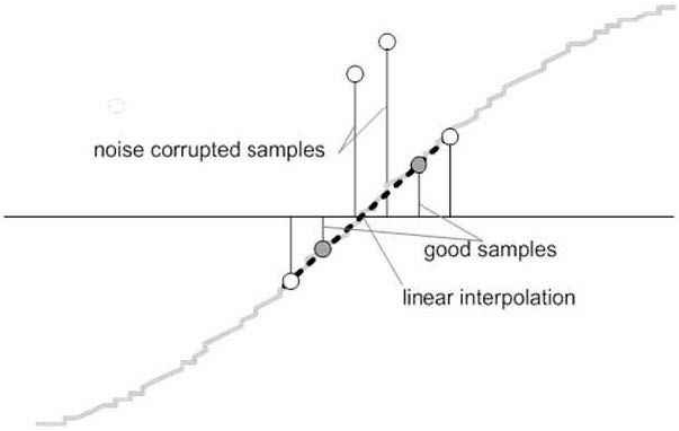

Figure 3-7. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate-of-change check to filter out the possible erroneous signals and make sure that the two points are interpolated from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair appear as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out any cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

3.11 LED Pulse Generation

In electricity meters, the energy consumption of the load is normally measured in a fraction of kilowatt-hour (kWh) pulses. This information can be used to accurately calibrate any meter for accuracy measurement. Typically, the measuring element (the MSPM0+ microcontroller) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, the pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, time jitters give a negative indication of the overall accuracy of the meter. The jitter must be averaged out due to this negative indication of accuracy.

This application uses average power to generate these energy pulses. The average power accumulates at every $\overline{\text{DRDY}}$ port ISR interrupt, thereby spreading the accumulated energy from the previous one-second time frame evenly for each interrupt in the current one-second time frame. This accumulation process is equivalent to converting power to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

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The threshold determines the energy *tick* specified by meter manufacturers and is a constant. The tick is usually defined in pulses-per-kWh or just in kWh. One pulse must be generated for every energy tick. For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy tick in this case is 1 kWh / 6400. Energy pulses are generated and available on a header and also through light-emitting diodes (LEDs) on the board. GPIO pins are used to produce the pulses.

In the reference design, the LED that is labeled "Active" corresponds to the active energy consumption for the 3-phase sum. "Reactive" corresponds to the cumulative 3-phase reactive energy sum.

Figure 3-8 shows the flow diagram for pulse generation.

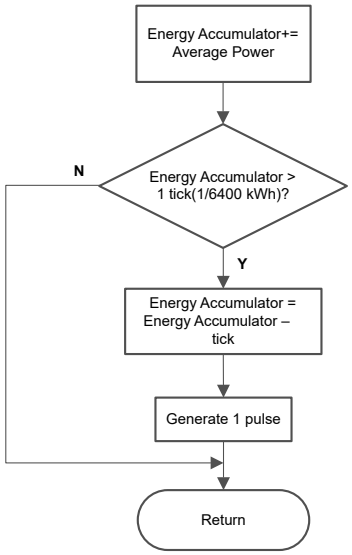

Figure 3-8. Pulse Generation for Energy Indication

The average power is in units of 0.001 W and a 1-kWh threshold is defined as:

$$1\text{−kWh threshold} = \frac{1}{0.001} \times 1\ \text{kW} \times \left(\text{Number of interrupts per second}\right) \times \left(\text{Number of seconds in one hour}\right)$$
$$= 1000000 \times 8000 \times 3600 = 0\text{x1A3185C50000} \quad (18)$$

3.12 Phase Compensation

When a current transformer (CT) is used as a sensor, the CT introduces additional phase shift on the current signals. Also, the passive components of the voltage and current input circuit can introduce another phase shift. The user must compensate the relative phase shift between voltage and current samples to provide accurate measurements. The implementation of the phase shift compensation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap finite impulse response (FIR) filter that interpolates between two samples, similar to the FIR filter used for providing 90°-shifted voltage samples for reactive energy measurements. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays. The lookup table provides fractional phase shifts as small as 1/256th of a sample. The 8000-Hz sample rate used in this application corresponds to a 0.0088° degree resolution at 50 Hz. In addition to the filter coefficients, the lookup table also has an associated gain variable for each set of filter coefficients. This gain variable is used to cancel out the resulting gain from using a certain set of filter coefficients.

An alternative option to the software phase compensation used in this design is to use the phase compensation feature on the ADS131M08 device. If this hardware phase compensation scheme is used, filter coefficients are not necessary so it is not necessary to divide by the gain of the filter coefficients.

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4 Hardware, Software, Testing Requirements, and Test Results

4.1 Required Hardware and Software

4.1.1 Hardware

Figure 4-1 shows the location of various pieces of the reference design based on functionality.

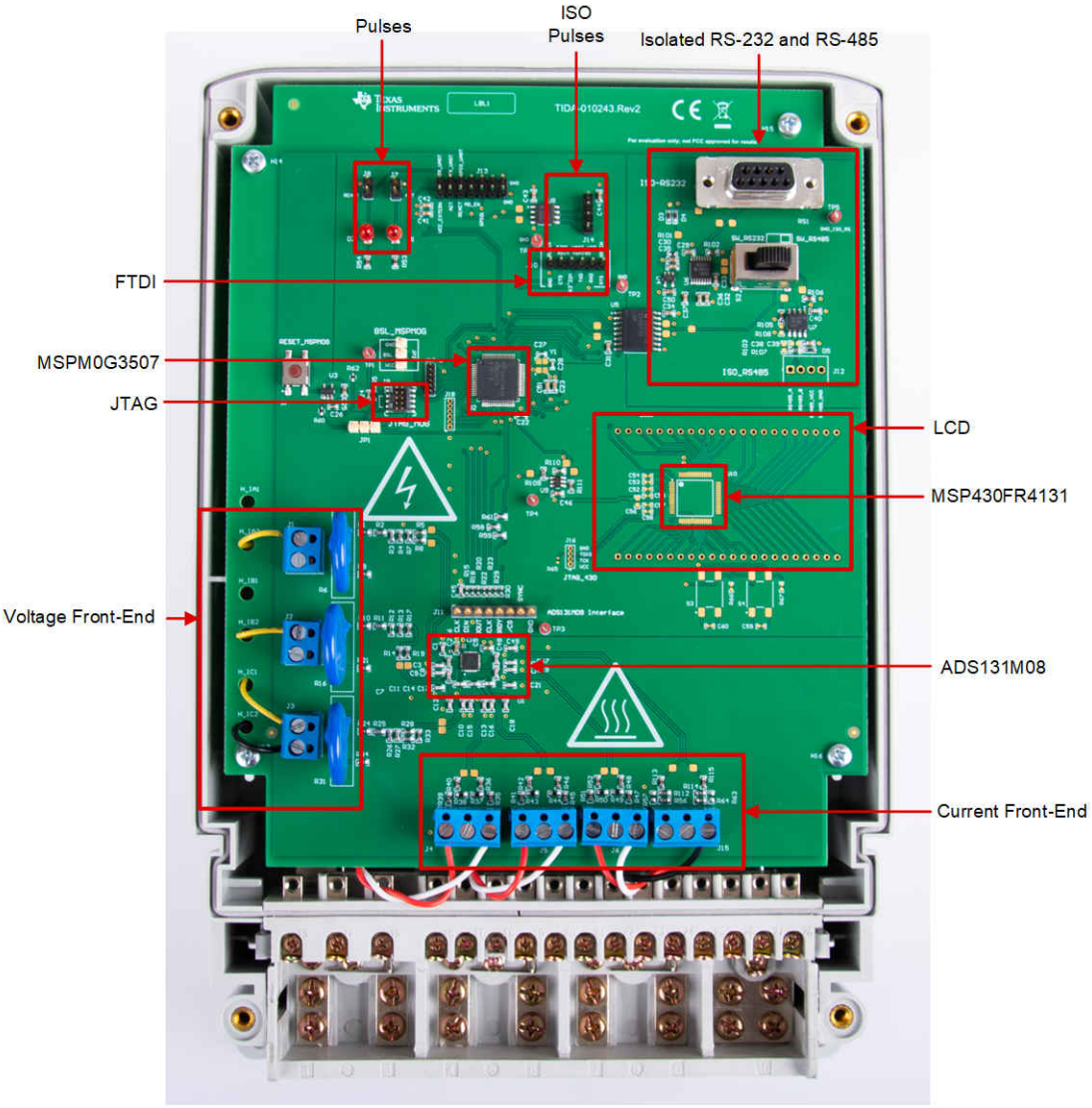

Figure 4-1. Top View of TIDA-010243 Design With Components Highlighted

4.1.2 Cautions and Warnings

At high currents, the terminal block can get warm. In addition, note that the phase voltages are fed to the board so take the proper precautions.

WARNING

Hot Surface! Contact can cause burns. Do not touch. Take the proper precautions when operating.

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CAUTION

High Voltage! Electric shocks are possible when connecting the board to live wires. The board must be handled with care by a professional. For safety, use of isolated test equipment with overvoltage or overcurrent protection is highly recommended.

4.2 Test Setup

4.2.1 Connecting the TIDA-010243 to the Metering Test Equipment

The design has support for 3-phase + Neutral configuration with current transformers (CT). AC voltages and currents can be applied to the board for testing purposes at these points:

- Terminal blocks "J1", "J2", and "J3", correspond to the line voltage connections for Phases A, B, and C, respectively. These terminal blocks have two positions.
- Terminal blocks "J4", "J5", and "J6" correspond to the current inputs after the sensors for Phases A, B, and C, respectively. These are three-position terminal blocks but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. Select the applied current to the input of the CT so that the current does not exceed 100 A. *In addition, before performing any test, verify that this terminal block is securely connected to both output leads of the CT.*
- Terminal block "J15" corresponds to the current input after the sensor for the Neutral line. This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. Select the applied current to the input of the CT so that the current does not exceed 100 A. *In addition, before performing any test, verify that this terminal block is securely connected to both output leads of the CT.*

Figure 4-2 and Figure 4-3 show the various test setup connections required for the reference design to function properly for the one-voltage configuration.

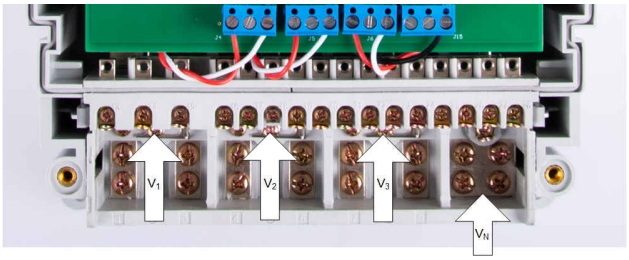

Figure 4-2. Test Setup Configuration

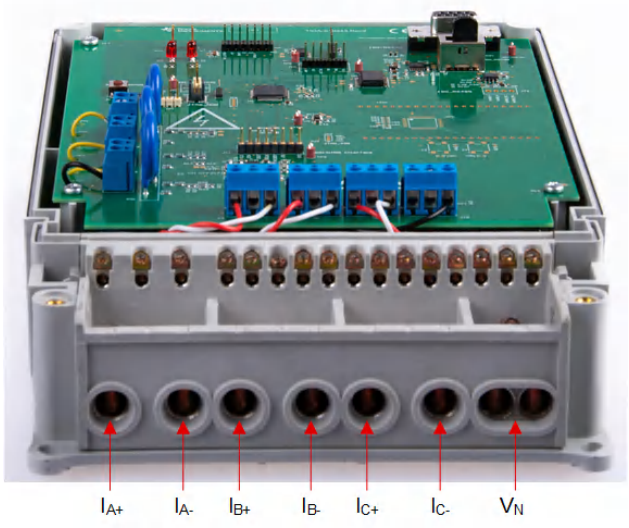

Figure 4-3. Port Image

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4.2.2 Power Supply Options and Jumper Settings

The MSPM0+ MCU and ADS131M08 portion of this design is powered from a single voltage rail (DVCC), which is by connecting a 3.3-V external power supply at the DVCC header J13.P1 and J13.P13 or J13.P14 (GND).

Various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for the board to correctly function. Table 4-1 indicates the functionality of each jumper on the board.

Note

The headers with **(WARNING)** text in the *MAIN FUNCTIONALITY* column are not isolated, so do not use measuring equipment there when running off the Mains. This applies, unless either isolators external to the board of this design are used to connect at the headers, if the equipment is battery powered and does not connect to Mains, or if AC mains is isolated.

Table 4-1. Header Names and Jumper Settings

HEADER OR HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J1, J2, J3	2-pin terminal blocks	Phases A, B, and C voltages **(WARNING)**	Voltage inputs for line A, B, and C	Each of these terminal blocks connect with one terminal to the Neutral voltage, while the second terminal is wired to either phase A, B, and C respectively.
J4, J5, J6	3-pin terminal blocks	Connect CT (Current Transformers) for line A, B, and C **(WARNING)**	Current inputs after the CT sensors for line A, B, and C	This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. Before performing any test, verify that this terminal block is securely connected to both output leads of the CT.
J7	2-pin header	Active energy pulses **(WARNING)**	Probe here for cumulative active energy pulses. This header has two pins: GND and ACT, which is where the active energy pulses are actually output.	This header is not isolated from AC mains, so do not connect measuring equipment here. See the "ISO_ACT" pin of J14 instead, which is isolated. If testing the active power pulses is desired, use the "ISO_ACT" pin of J14 instead since is isolated.
J8	4-pin header	Reactive energy pulses **(WARNING)**	Probe here for cumulative reactive energy pulses. This header has two pins: GND and REACT, which is where the reactive energy pulses are actually output.	This header is not isolated from AC mains, so do not connect measuring equipment here. If testing the reactive power pulses is desired, use the "ISO_REACT" pin of J14 instead since it is isolated.
J9	10-pin, 2-row connector	Neutral Connection **(WARNING)**	Connect the XDS110 Debug Probe to this connector to power the MSPM0G3507 MCU.	The XDS110 Debug Probe is used to program the MSPM0G3507 device. Note that the MSPM0 MCU has to be powered externally to program it. Since this header and the XDS110 are not isolated, do not connect to this header when running off Mains and Mains is not isolated.
J10	6-pin header	FTDI UART to USB header **(WARNING)**	Use FTDI cable and UART link while debugging with *no Mains* connected.	Provides UART link through a PC USB port. Since this header is not isolated, do not connect to this header when running off Mains and Mains is not isolated.
J11	8-pin header	ADS131M08 MSPM0G3507 communication header **(WARNING)**	Probe here for connections to the 4-wire SPI signals, $\overline{\text{RST}}$ signal, CLKIN signal, and $\overline{\text{DRDY}}$ signal of the ADS131M08 device.	The $\overline{\text{RST}}$ pin resets the ADS131M08. When initializing the ADS131M08, the MSPM0G3507 drives this pin to reset the ADS131M08. The DRDY pin of the ADS131M08 device is used to alert the MSPM0+ MCU that new current samples are available. The CLKIN pin is fed from the CLK_OUT clock output of the MSPM0+ MCU to the ADS131M08 device, which divides the clock down to produce the used modulator clock. **(WARNING)**This header is NOT isolated from AC mains, so do NOT connect measuring equipment when running from Mains unless isolators external to the reference design are available. The pin mappings on this header are as follows: ● Pin 1: ADS131M08 CLKIN pin ● Pin 2: SPI DIN, ADS131M08 DOUT/ pin POCI ● Pin 3: SPI DOUT, ADS131M08 DIN pin/PICO ● Pin 4: SPI CLK (ADS131M08 SCLK pin) ● Pin 5: ADS131M08 $\overline{\text{DRDY}}$ pin ● Pin 6: ADS131M08 $\overline{\text{CS}}$ pin ● Pin 7: ADS131M08 $\overline{\text{SYNC}}$/ $\overline{\text{RESET}}$ pin). Pin 8: NC
J12	4-pin terminal block	Isolated RS-485 connection		To view the GUI using RS-485, connect the USB to RS-485 adapter here. 5 V must be provided externally on pin 3 of this header. Pin 4 is the RS-485 ground, pin 2 is the B bus I/O line, and pin 1 is the A bus I/O line.
J13	14-pin 2-row header	Application connector **(WARNING)**	Probe here for various non-isolated signals.	Provides access to another UART link and ACT and REACT lines. Since this header is not isolated, do not connect to this header when running off Mains and Mains is not isolated.

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Table 4-1. Header Names and Jumper Settings (continued)

HEADER OR HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J14	4-pin header	Isolated pulses header	Probe here for the isolated cumulative active energy pulses and the isolated cumulative three-phase reactive energy pulses.	This header has four pins: GND_ISO, REACT_ISO, ACT_ISO, and DVDD_ISO. GND_ISO is the isolated ground for the energy pulses. DVDD_ISO is the VDD connection for the isolated active and reactive energy pulses. ACT_ISO is where the isolated active energy pulses are output. REACT_ISO is where the isolated reactive energy pulses are output. This header is isolated from AC mains so it is safe to connect to a scope or other measuring equipment because isolators are already present. However, either 3.3 V or 5 V must be applied between GND_ISO and DVDD_ISO to produce both the active and the reactive energy pulses at this header. The produced pulses have a logical high voltage that is equal to the voltage applied between GND_ISO and DVDD_ISO.
J15	3-pin terminal block	Neutral Connection **(WARNING)**	Current input after the CT for Neutral line (if Neutral current monitoring is desired).	This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. Before performing any test, verify that this terminal block is securely connected to both output leads of the CT.
J17	6-pin header	GPIO lines from MSPM0G3507	Access to 6 unused GPIOs	Connect to 6 GPIOs for experimenting and debugging
S2	12-pin dual switch	RS-232 or RS-485 serial Interface selection switch	Set S2 to either the left or right position to select if serial interface RS-232 or RS-485 is used. Both Interfaces are isolated through the U5 (ISO6731).	The PCB silkscreen marking indicates the position for RS-232 and RS-485.
JP1	3-pin jumper header	Reset selection	Place a jumper at either 1-2 or 2-3 positions depending on which RESET line is active. TVS3840 and Push Button S1 are used in Position 1-2, otherwise in 2-3 the nRST_debug line from J9 (ARM debug connector) is active.	Useful during board debugging and code development
JP2	3-pin jumper header	Pullup or Pulldown for BSL_invoke line on MSPM0G3507	Place a jumper at either 1-2 or 2-3 positions depending on if BSL_INVOKE is VDD_3V3 or GND respectively.	Was used on 1st silicon revision, not needed anymore.

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4.2.3 Electricity Meter Metrology Accuracy Testing

To test for metrology accuracy in the electricity meter configuration, a source generator is used to provide the voltages and currents to the system at the proper locations mentioned in Test Setup. In this design, a nominal voltage of 230 V between the line and neutral, calibration current of 10 A, and nominal frequency of 50 Hz are used for each of the three phases.

When the voltages and currents are applied to the system, the system outputs the cumulative active energy pulses and cumulative reactive energy pulses at a rate of 6400 pulses/kWh. This pulse output is fed into a reference meter (in the test equipment for this reference design, this pulse output is integrated in the same equipment used for the source generator) that determines the energy % error based on the actual energy provided to the system and the measured energy as determined by the active and reactive energy output pulse of the system. For the 3-phases configuration, cumulative active energy error testing, cumulative reactive energy error testing, individual phase active energy testing, and frequency variation testing are performed after performing the energy gain calibration and phase compensation as described in Section 4.2.5. In addition to the energy error tests, the RMS voltage % error and RMS current % error are measured as well for the two-voltage configuration. For the one-voltage configuration, cumulative active energy error testing and voltage variation tests are also performed.

For cumulative active energy error, cumulative reactive energy error testing, and individual phase active energy testing, current is varied from 50 mA to 100 A. For cumulative active energy and individual phase error testing, a phase shift of 0°, 60°, and −60° is applied between the voltage and current waveforms fed to the reference design. Based on the error from the active energy output pulse, a plot of active energy % error versus current is created for 0°, 60°, and –60° phase shifts. For cumulative reactive energy error testing, a similar process is followed except that 30°, 60°, –30°, and –60° phase shifts are used, and cumulative reactive energy error is plotted instead of cumulative active energy error. In the cumulative active and reactive energy testing, the sum of the energy reading of each phase is tested for accuracy. In contrast, the individual phase energy readings (Phase A, Phase B, and Phase C) are tested for the individual phase active energy testing. When testing the individual energy accuracy of a phase, the other phase is disabled by providing 0-A input for the current of this other phase so that the cumulative active energy reading is ideally equal to the individual phase voltage, which allows the cumulative energy pulse output to be used for testing individual phase accuracy.

In addition to testing active energy by varying current, active energy was also tested by varying the RMS voltage from 240 V – 15 V and measuring the active energy % error. Another set of energy tests performed were frequency variation tests. For this test, the frequency is varied by ±2 Hz from the 60-Hz nominal frequency. This test is conducted at 0.5 A and 10 A at phase shifts of 0°, 60°, and −60°. The resulting active energy error under these conditions are logged.

To test RMS accuracy, the RMS readings were used from the GUI since the pulse output that was used for the energy accuracy tests cannot be used for RMS voltage and current. For the voltage testing, 10-A current is applied for each phase and the voltage is varied from 9 V – 270 V on each phase simultaneously. The voltage was not varied beyond 270 V because of the 275-V varistor present on the board, which can be removed for testing at voltages beyond 275 V. After applying each voltage, the resulting RMS voltage reading from the GUI is logged for each phase after the readings stabilize. Once the measured RMS voltage readings are obtained from the GUI, the actual RMS voltage readings are obtained from the reference meter, which is necessary because the source generator may not generate the requested values for voltage, especially at small voltages. With the reference meter measured RMS voltage and the RMS voltage value of the GUI, the RMS voltage % error is calculated. A similar process is used to calculate the RMS current % error by using 120 V for each phase and varying current from 50 mA to 100 A.

All these tests have been run using the 8 kSPS sample rate setting of the ADS131M08.

4.2.4 Viewing Metrology Readings and Calibration

This section describes the methods used to verify the results of this design with the test software.

4.2.4.1 Viewing Results From LCD

The software for displaying the metrology parameters on the LCD is not implemented yet. For each metering parameter that gets displayed on the LCD, three items are usually required: (1) a symbol used to denote the phase of the parameter, (2) text to denote which parameter is being displayed, and (3) the actual value of

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the parameter. The phase symbol is displayed at the top of the LCD and denoted by a triangle shape. The orientation of the symbol determines the corresponding phase.

If running, the LCD typically scrolls between metering parameters every two seconds.

4.2.4.2 Calibrating and Viewing Results From PC

To view the metrology parameter values from the GUI, perform the following steps:

1. Select whether to use the RS-485 or RS-232 connection for communication to the PC GUI. This selection is done by moving right or to the PCB edge for the RS-485 communication option, and moving the S2 switch left for the RS-232 communication option.
2. Connect the reference design to a PC:
   - RS-232 option: Connect the reference design to a PC using an RS-232 cable. If the PC does not have an RS-232 adapter, use a serial RS-232 adapter. The RS-232 adapter creates a COM port on the PC when the adapter is plugged in.
   - RS-485 option: A USB to RS-485 adapter can be used to communicate between the PC GUI and the RS-485 port on this design. The USB to RS-485 adapter creates a COM port on the PC when the adapter is plugged in. The other end of the adapter has wires for the RS-485 Data A and Data B connections as well as a GND connection and a 5-V power connection, which are all connected to the J12 screw terminal block of the design according to the connection labels next to the terminal block pins. For testing this circuit, the following USB to RS-485 adapter is specifically used: http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_USB_RS485_CABLES.pdf. For this specific adapter, the Data A connection is orange, the Data B connection wire is yellow, the GND connection is black, and the 5-V power connection is red.
3. Open the GUI folder and open *calibration-config.xml* in a text editor.
4. Change the *port name* field within the *meter* tag to the COM port connected to the system. As Figure 4-4 shows, this field is changed to *COM7*.

```
260        </correction>
261      </phase>
262      <temperature/>
263      <rtc/>
264    </cal-defaults>
265    <meter position="1">
266      <port name="com7" speed="9600"/>
267    </meter>
268    <reference-meter>
269      <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270      <type id="chroma-66202"/>
271      <log requests="on" responses="on"/>
272      <scaling voltage="1.0" current="1.0"/>
273    </reference-meter>
```

Figure 4-4. GUI Configuration File Changed to Communicate With Energy Measurement System

5. Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the reference design, the GUI opens (see Figure 4-5). If the GUI connects to the design properly, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

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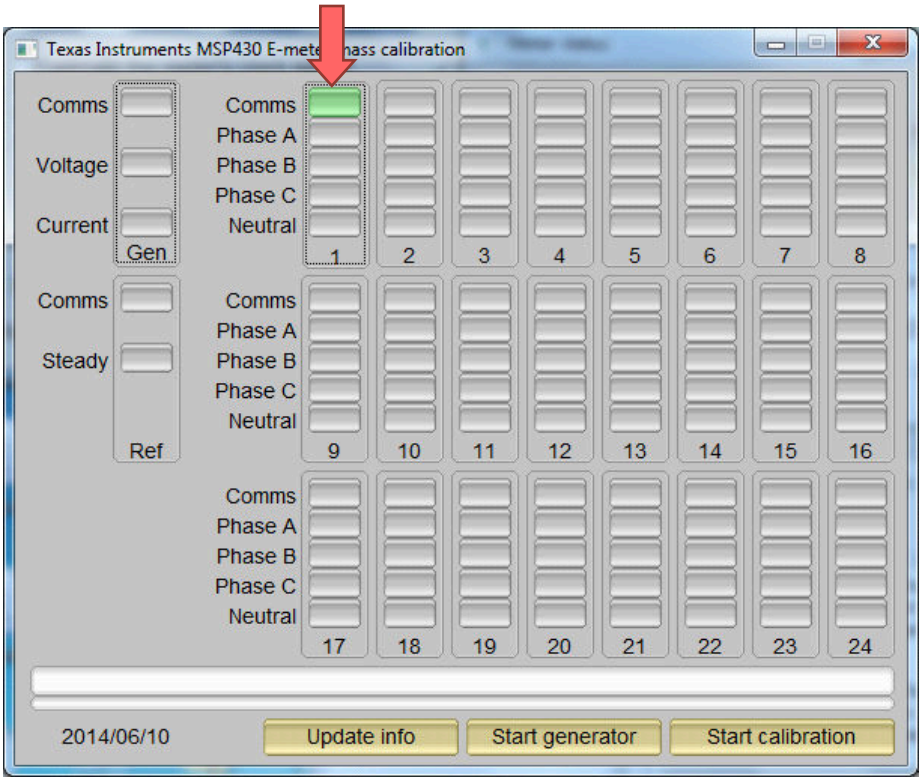

Figure 4-5. GUI Start-Up Window

Upon clicking on the green button, the results window opens (see Figure 4-6). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively.

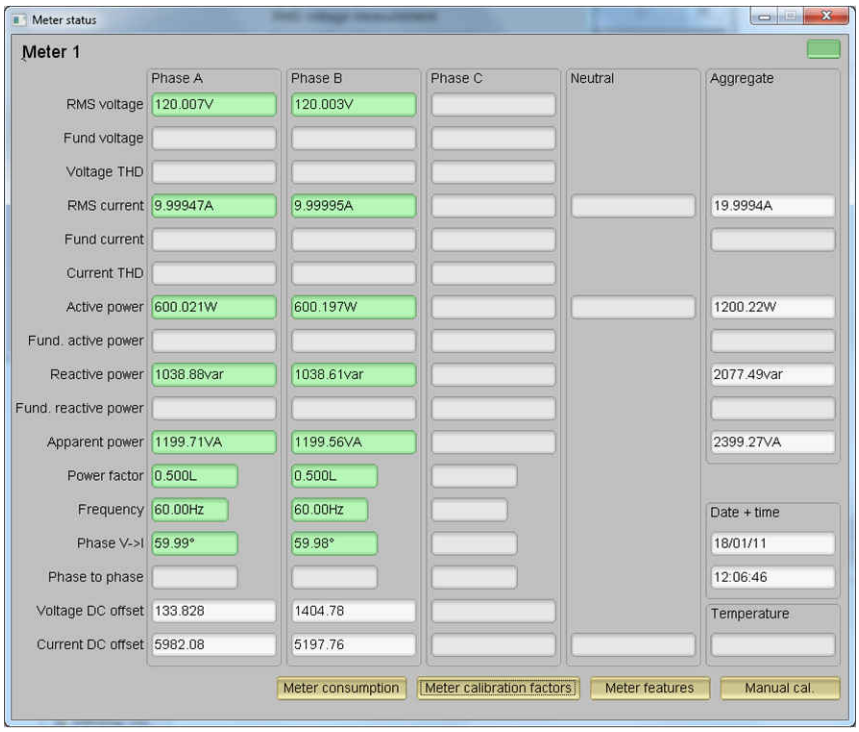

Figure 4-6. GUI Results Window

From the results window, view the total-energy consumption readings by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as Figure 4-7 shows.

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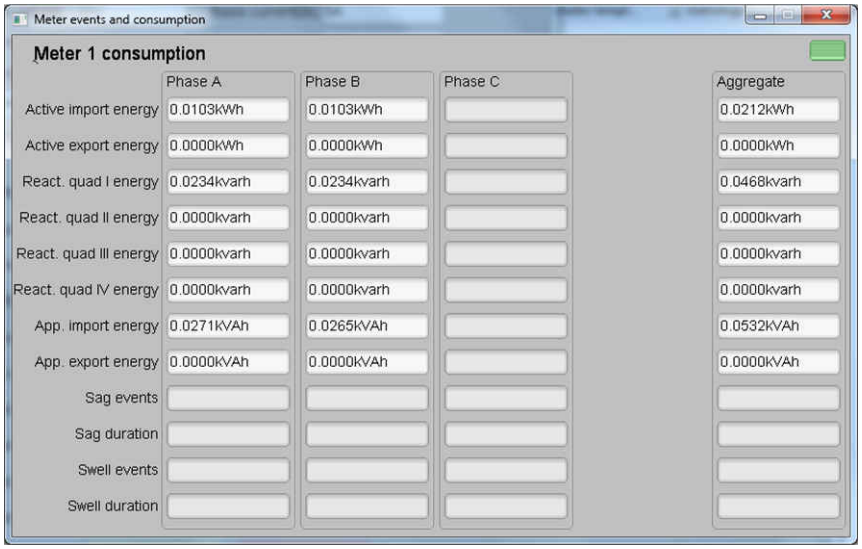

Figure 4-7. Meter Events and Consumption Window

From the results window, the user can also view the meter settings by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

4.2.5 Calibration and FLASH Settings for MSPM0+ MCU

Calibration is key to any meter performance, and calibration is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify their effects, every meter must be calibrated. To perform calibration accurately, there must be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this 3-phase electricity meter design.

The GUI used for viewing measurement results can also easily be used to calibrate the design. During calibration, parameters called calibration factors are modified in the test software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, active power offset (erroneously called voltage AC offset in the GUI), current scaling factor, reactive power offset (erroneously called current AC offset in the GUI), power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The power offset is used to subtract voltage to current crosstalk, which appears as a constant power offset and causes greater inaccuracies at lower currents. Note that offset calibration was not used for testing this specific design. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter software is flashed on the MSPM0G3507 device for the first time, default calibration factors are loaded into these calibration factors. Calibration factors or values are modified through the GUI during calibration. The calibration factors are also stored in the last MSPM0+ MCU FLASH sector and therefore, remain the same if the meter is restarted.

The settings are defined in the mspm0g3507.cmd file using one of the following:

- `#define CALIBRATION_START_ADDR (TOTAL_FLASH_SIZE - TOTAL_FLASH_SIZE)`
- 0x1FC00 being the start address of the last FLASH area sector, when TOTAL_FLASH_SIZE =0x20000 and FLASH_SECTOR_SIZE = 0x400

In addition, all 5 FLASH access routines must be placed into the RAM area because when calibration takes place, multiple read and write operations to the last FLASH sector are executed.

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This is achieved using a compiler directive in the "flash_M0G.h" file, for example:

```
void __attribute__((section(".ramfunc"))) flash_clr_calibration(void);
```

Because MSPM0+ MCUs FLASH memory is 64-bit aligned, all alignments for data in the FLASH memory are 64-bit or palign(8), as seen in the "mspm0g3507.cmd" file.

```
.rodata : palign(8) {} > FLASH

.caldata : palign(8) {} > CALIBRATION
```

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with Figure 4-2, and the energy pulses connected to the reference meter.

4.2.6 Gain Calibration

Usually, gain correction for voltage and current can be done simultaneously for all phases. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction for active power. Also, when performing active power calibration for any given phase, the other phases must be turned OFF by turning off the current but leaving the other voltages still enabled.

4.2.7 Voltage and Current Gain Calibration

To calibrate the voltage and current readings, perform the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
2. Configure the test source to supply the desired voltage and current for all phases. Make sure that these are the voltage and current calibration points with a zero-degree phase shift between each phase voltage and current. For example, for 120 V, 10 A, 0° (PF = 1). Typically, these values are the same for every phase.
3. Click on the *Manual cal.* button in Figure 4-6. The screen in Figure 4-8 pops up:

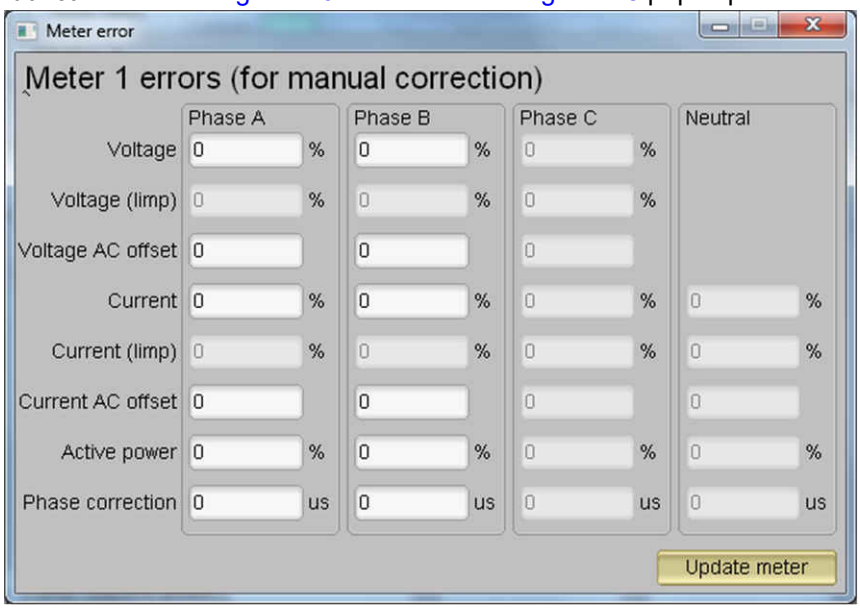

Figure 4-8. Manual Calibration Window

4. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated using Equation 19:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \tag{19}$$

where

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source

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5. After calculating for all voltages and currents, input these values as is (±) for the fields *Voltage and Current* for the corresponding phases.
6. Click on the *Update meter* button and the observed values for the voltages and currents on the GUI settle immediately to the desired voltages and currents.

4.2.8 Active Power Gain Calibration

Note

This section is an example for one phase. Repeat these steps for the other two phases.

After performing gain correction for voltage and current, complete *gain correction* for active power. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating the active energy % error as is done with voltage and power can be done, avoid using this method because it is not the most accurate.

The best option to get the *Correction (%)* is directly from the reference meters measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, complete the following steps:

1. Turn off the system and connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
2. Turn on the AC test source.
3. Repeat step 1 to step 3 from Voltage and Current Gain Calibration with the identical voltages, currents, and 0° phase shift that were used in the same section.
4. Obtain the % error in measurement from the reference meter. A negative value is possible here.
5. Enter the error obtained in step 4 into the *Active Power* field under the corresponding phase in the GUI window. This error is already the value and does not require calculation.
6. Click the *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

4.2.9 Offset Calibration

After performing gain calibration, if the accuracy at low currents is not acceptable, perform offset calibration. Offset calibration removes any crosstalk, such as the crosstalk to the current channels of a phase from the line voltages.

To perform active power offset calibration for a phase, simply add the offset to be subtracted from the active power reading (in units of mW) to the current value of the active power offset (labeled "Voltage AC off" in Figure 4-9) and then enter this new value in the *Voltage AC offset* field in the Manual Calibration window. As an example, if the *Voltage AC off* has a value of 200 (0.2 W) in Figure 4-9, and it is desired to subtract an additional 0.300 mW, then enter a value of 500 in the *Voltage AC offset* field in the Manual Calibration window. After entering the value in the *Voltage AC offset* field in the Manual Calibration window, press the *Update meter* button.

To perform reactive power offset calibration for a phase, a similar process is followed as the process used to perform active power offset calibration. Add the offset to be subtracted from the reactive power reading (in units of mvar) to the current value of the reactive power offset (labeled "Current AC offset" in Figure 4-9) and then enter the value in the *Current AC offset* field in the Manual Calibration window. After entering the value in the *Current AC offset* field in the Manual Calibration window, press the *Update meter* button.

4.2.10 Phase Calibration

After performing power gain correction, perform the phase calibration. Similar to active power gain calibration, to perform phase correction on one phase, the other two phases must be disabled. To perform phase correction calibration, complete the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform step 1 to step 3 from Voltage and Current Gain Calibration using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0 A.
3. Modify only the phase-shift to a non-zero value; typically, +60° is chosen. The reference meter now displays a different % error for active power measurement. This value can be negative.

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4. If the error from step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
   a. Enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60°), a positive (negative) error requires a positive (negative) number as correction.
   b. Click on the *Update meter* button and monitor the error values on the reference meter.
   c. If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on Step 4a and Step 4b. Note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
   d. Change the phase to −60° now, and check if this error is still acceptable. Ideally, errors must be symmetric for same phase shift on lag and lead conditions.

After performing phase calibration, calibration is complete for one phase. Gain calibration, offset calibration, and phase calibration must be performed for the other phases.

This completes calibration of voltage, current, and power for both phases. View the new calibration factors (see Figure 4-9) by clicking the *Meter calibration factors* button of the GUI metering results window in Figure 4-6. For these displayed calibration factors, note that the *Voltage AC off* parameter actually represents the active power offset (in units of mW) subtracted from each measurement and the *Current AC offset* parameter actually represents the reactive power offset subtracted (in units of mvar) from reactive power readings. Also, this shows example calibration factors for a meter that uses the two-voltage configuration. If the same meter is set for one-voltage configuration, the voltage and active power scaling factors are approximately half of what it is in Figure 4-6, since the line-to-line voltage measurement is used for the voltage readings of both phases instead of measuring the two line-to-neutral voltages. Under the best conditions for a split-phase system, the line-to-line voltage measurement has an RMS value that is twice each of the two line-to-neutral RMS measurements, which means that the voltage fed to the ADC is also twice as much when measuring line-to-line voltage compared to when measuring line-to-neutral voltage. As a result, for one-voltage configurations, the voltage and power readings have to be divided by an additional factor of two, which is automatically done by following the active power and voltage gain calibration steps.

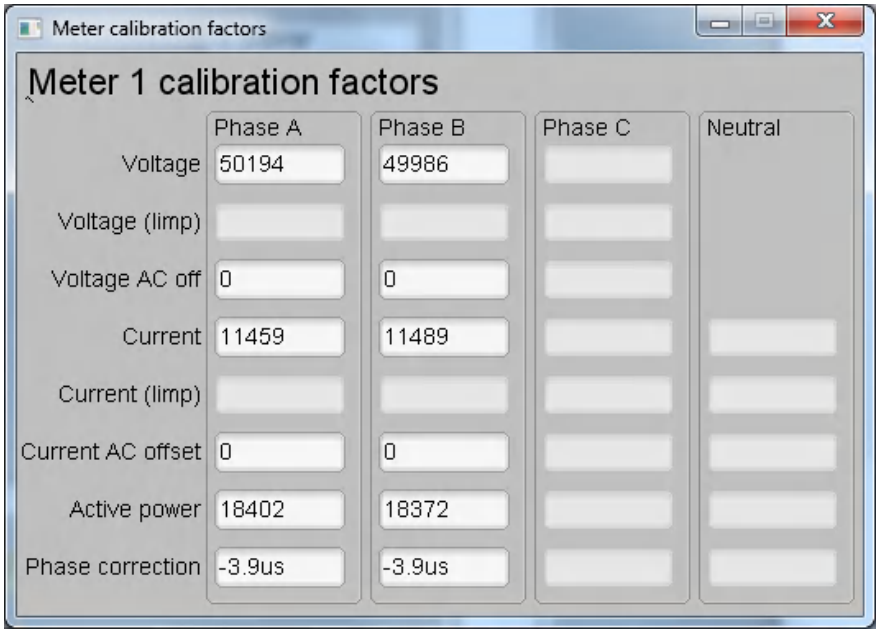

Figure 4-9. Calibration Factors Window

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View the configuration of the system by clicking on the *Meter features* button (illustrated in Figure 4-6) to get to the window that Figure 4-10 shows.

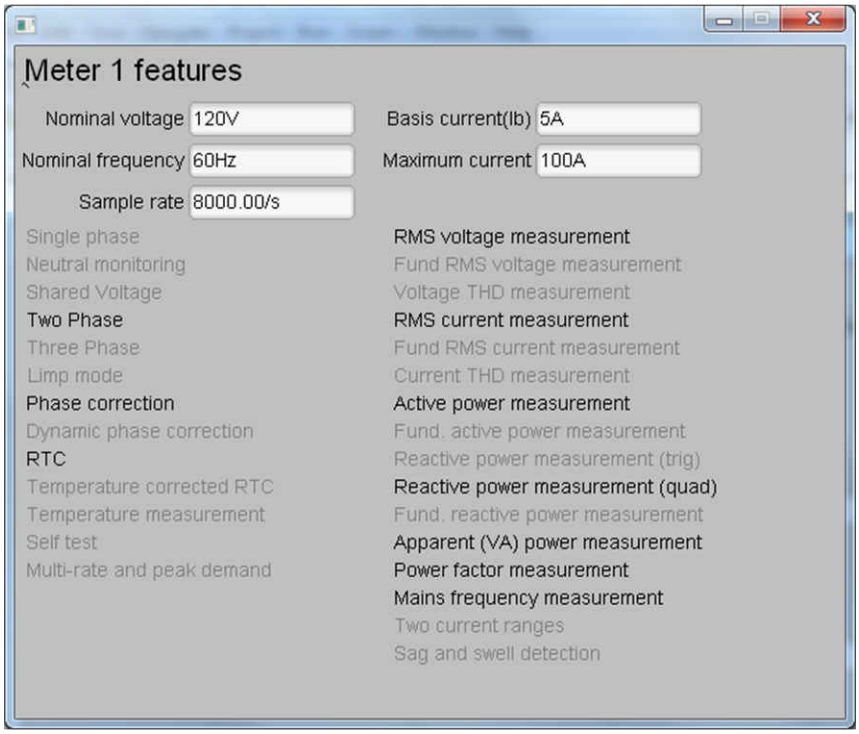

Figure 4-10. Meter Features Window

4.2.11 Software Code Example

The MSPM0+ software used for evaluating this design is test software and the features are discussed in the *How to Implement Software for Metrology Testing* section.

4.3 Test Results

4.3.1 SVS Functionality Testing

In addition to metrology accuracy testing, functionality testing is done on the TPS3840 SVS device. For this purpose, the board is powered by connecting an external power supply directly to DVCC and the output voltage of the external power supply is slowly varied from 3.3 V down to 1.6 V. The threshold voltage at which the MSPM0G3507 MCU is reset by the TPS3840 device, which is referred to as the negative voltage threshold, is logged. After the negative voltage threshold is reached, the power supply output voltage is slowly increased from 1.6 V back to 3.3 V. The voltage at which the reset is released, which is equal to the negative voltage threshold plus hysteresis voltage, is logged as well.

Table 4-2. Table Title

CONDITION	MEASURED VOLTAGE (V)	Data Sheet Typical Value (V)
Negative voltage threshold, VIT–	1.74	1.72 ±1%
Positive voltage threshold, VIT+ = VIT– + Vhys	1.85	1.82
Hysteresis Voltage, Vhys = VIT+ - VIT–	1.85 –1.74 = 0.11	1.82 –1.72 = 0.10

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4.3.2 Electricity Meter Metrology Accuracy Results

For the following test results, gain and phase calibration are applied to the meter. In the following results, the active energy results are within 0.1% at 0° phase shift. Additionally, the active energy versus voltage results and the RMS voltage results show that good accuracy results are able to be obtained despite using only a fraction of the ADC range for the voltage channels.

The "% Error" columns in the following 6 tables and plots are calculated as the difference between the multiple reference input values to TIDA-010243 and the measured values, shown on the PC GUI. The reference input values to TIDA-010243 are generated by a PTS3.3C Source Generator/Reference Meter from the company MTE, while the measured values calculated by the TIDA-010243 Energy Library are reported in the PC GUI.

Table 4-3. Phase A RMS Voltage % Error Versus Voltage, 3-Phase Mode

VOLTAGE (V)	% ERROR
270	0.00555
260	0.00384
240	0.00375
230	0.01086
220	0.00863
200	0.00700
180	0.01055
160	0.00250
140	0.00214
120	0.00666
100	0.00300
90	0.01300
70	0.01571
50	0.00240
30	0.01200
10	0.00299
9	0.02733

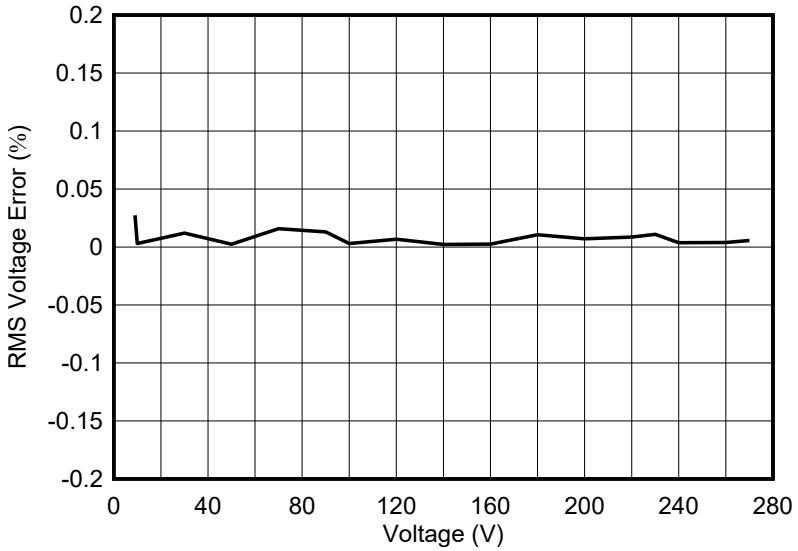

Figure 4-11. Phase A RMS Voltage % Error Versus Voltage, 3-Phase Mode

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Table 4-4. Phase A RMS Current % Error Versus Current, 3-Phase Mode

CURRENT (A)	% ERROR
0.01	0.50383
0.03	0.20413
0.05	0.07749
0.1	0.00399
0.25	0.02239
0.50	0.00179
1.00	0.01999
2.00	0.01649
5.00	0.00539
10.00	0.00999
20.00	0.01449
30.00	0.03366
40.00	0.01124
50.00	0.01398
60.00	0.01566
70.00	0.00642
80.00	0.00749
90.00	0.02321
100.00	0.02099

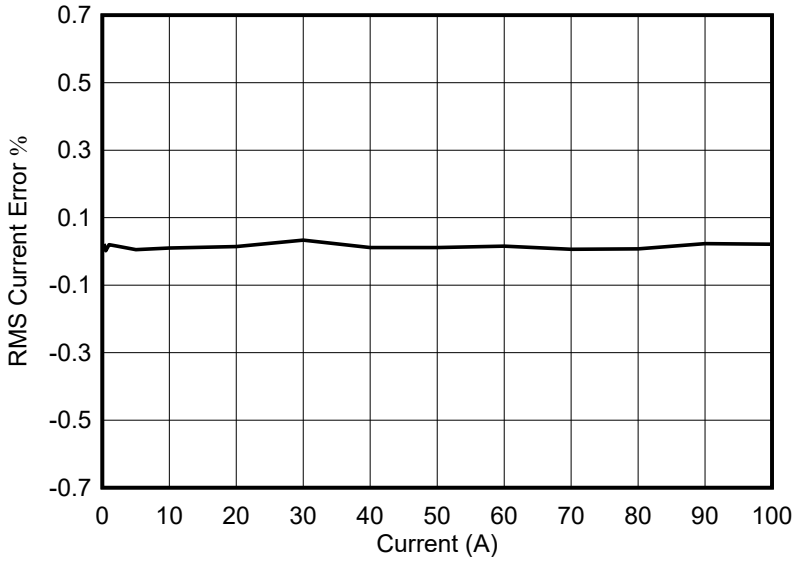

Figure 4-12. Phase A RMS Current % Error Versus Current, 3-Phase Mode

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Table 4-5. Phase B RMS Voltage % Error Versus Voltage, 3-Phase Mode

VOLTAGE (V)	% ERROR
270	0.01444
260	0.01307
240	0.00500
230	0.00304
220	0.01090
200	0.00500
180	0.00111
160	0.00687
140	0.00428
120	0.01916
100	0.00900
90	0.00922
70	0.02771
50	0.02240
30	0.02500
10	0.03400
9	0.02133

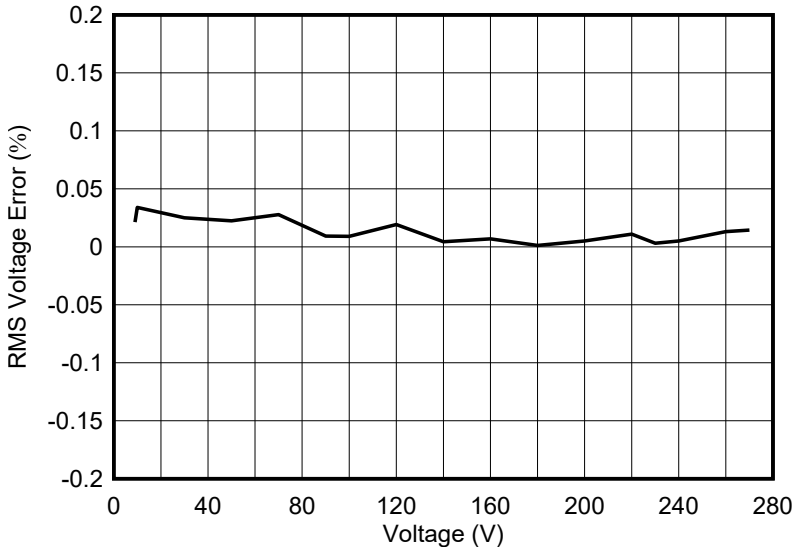

Figure 4-13. Phase B RMS Voltage % Error Versus Voltage, 3-Phase Mode

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Table 4-6. Phase B RMS Current % Error Versus Current, 3-Phase Mode

CURRENT (A)	% ERROR
0.01	0.63311
0.03	0.26816
0.05	0.07893
0.10	0.04498
0.25	0.01159
0.50	0.01220
1.00	0.01499
2.00	0.00449
5.00	0.01339
10.00	0.00100
20.00	0.01449
30.00	0.02666
40.00	0.02825
50.00	0.01019
60.00	0.01683
70.00	0.00414
80.00.	0.00475
90.00	0.01988
100.00	0.03199

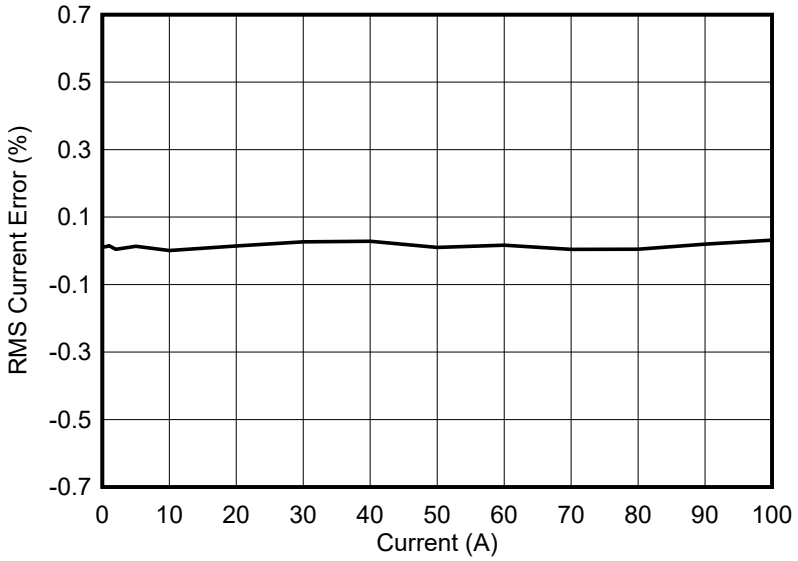

Figure 4-14. Phase B RMS Current % Error Versus Current, 3-Phase Mode

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Table 4-7. Phase C RMS Voltage % Error Versus Voltage, 3-Phase Mode

VOLTAGE (V)	% ERROR
9	0.02077
10	0.00699
30	0.00566
50	0.00960
70	0.00528
90	0.00988
100	0.00200
120	0.00999
140	0.00071
160	0.01874
180	0.00388
200	0.00650
220	0.00090
230	0.01652
240.	0.01124
260	0.02461
270	0.02444

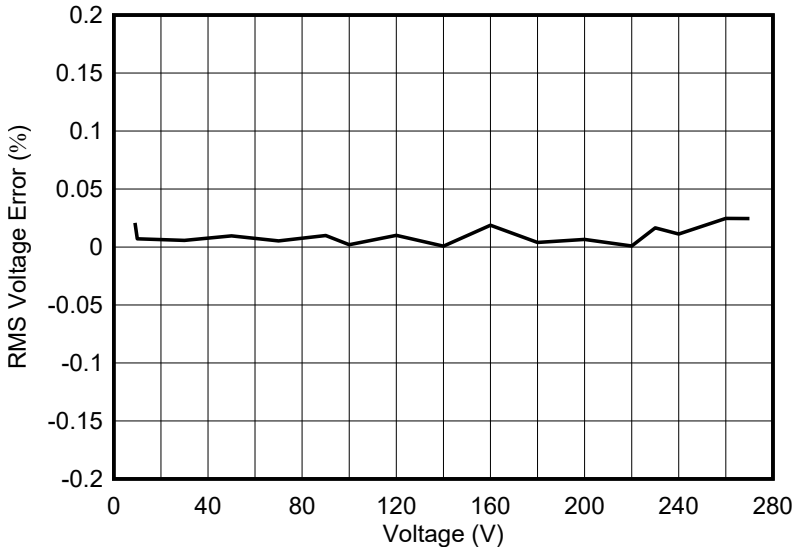

Figure 4-15. Phase C RMS Voltage % Error Versus Voltage, 3-Phase Mode

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Table 4-8. Phase C RMS Current % Error Versus Current, 3-Phase Mode

CURRENT (A)	% ERROR
0.01	0.32617
0.03	0.15916
0.05	0.09126
0.10	0.00499
0.25	0.00200
0.50	0.01940
1.00	0.00500
2.00	0.00699
5.00	0.01139
10.00	0.09506
20.00	0.05700
30.00	0.02899
40.00	0.03625
50.00	0.01720
60.00	0.01166
70.00	0.01842
80.00.	0.01062
90.00	0.00100
100.00	0.00120

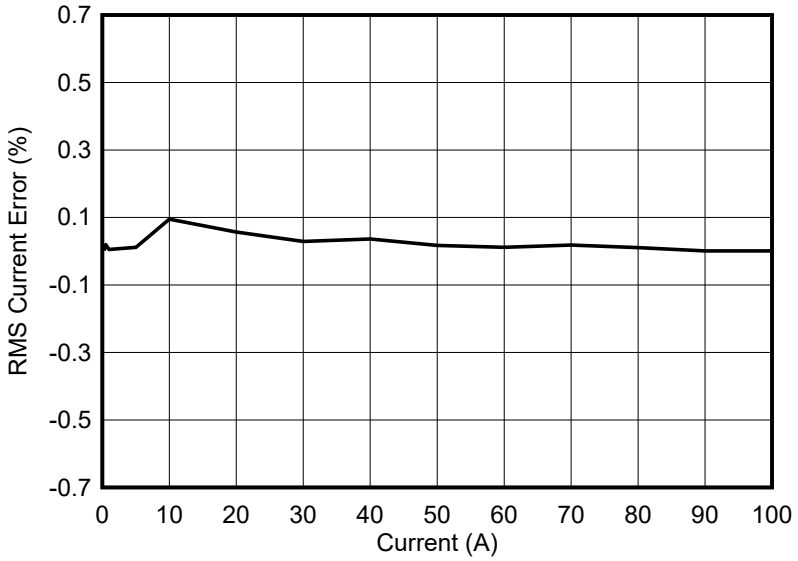

Figure 4-16. Phase C RMS Current % Error Versus Current, 3-Phase Mode

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5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010243.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010243.

5.1.3 PCB Layout Recommendations

For this design, the following general guidelines must be followed:

- Place decoupling capacitors close to their associated pins.
- Use ground planes instead of ground traces and minimize the cuts in the ground plane, especially near the ADS131M08. In this design, there is a ground plane on both the top and bottom layer; for this situation, make sure that there is good stitching between the planes through the liberal use of vias.
- Keep the two traces to the inputs of an ADC channel symmetrical and as close as possible to each other.
- Crosstalk from the voltage to current channels can reduce accuracy at lower currents if power offset is not performed. To minimize voltage to current crosstalk on the PCB, assign ADC channels 0, 1, and 2 to the current channels and channels 3, 4, and 5 to the voltage channels or vice versa: ADC channels 0, 1, and 2 are the voltage channels and channels 3, 4, and 5 are the current channels.
- For the ADS131M08 device, place the 0.1-µF capacitor closest to the AVDD pin than the 1-µF capacitor. Do the same thing also for the 0.1-µF and 1-µF capacitors connected to DVDD.
- Note that the order of the AINxP and AINxN pins on the ADS131M08 switches when going from one converter channel to another. This swapped order is dealt with in this design by routing the connections at J4 and J6 on the PCB accordingly.
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there must be clean ground underneath the 16.384-MHz crystal and placing any traces underneath the crystal must be avoided. Also, keep high-frequency signals away from the crystal.
- Use wide traces for power-supply connections.
- Use a different ground plane for the isolated RS-232 and RS-485. This other ground plane is at the potential of the RS-232 and RS-485 ground and not the GND used elsewhere in the board.
- Make sure that the recommended clearance and creepage spacing are met for the ISO6731 and ISO6720 isolation devices in this design.

5.1.4 Layout Prints

To download the layer plots, see the design files at TIDA-010243.

5.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010243.

5.2 Tools and Software

Tools

CCSTUDIO	Code Composer Studio™ integrated development environment (IDE)
MSPM0-SDK	MSPM0 software development kit (SDK)
SYSCONFIG	System configuration tool with an intuitive graphical user interface for configuring pins, peripherals, radios, software stacks, RTOS, clock tree, and other components.
ADC-ENERGY-METROLOGY-LIB-SW	ADC energy metrology library software package implements various metrology parameters for energy measurement typical of electricity meters, power-distribution units (PDUs), and circuit breakers using high-performance, multichannel analog-to-digital converters (ADCs).

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Software

TIDA-010243 Energy Library	Source code of Energy Library for TIDA-010243

5.3 Documentation Support

1. Texas Instruments, *ADS131M08 8-Channel, Simultaneously-Sampling, 24-Bit, Delta-Sigma ADC* Data Sheet
2. Texas Instruments, *MSPM0G110x Mixed-Signal Microcontrollers* Data Sheet
3. Texas Instruments, *TPS3840 Nano Power, High Input Voltage Supervisor With MR and Programmable Delay* Data Sheet
4. Texas Instruments, *THVD1400, THVD1420 3.3-V to 5-V RS-485 Transceivers in Small Package with ±12-kV IEC ESD Protection* Data Sheet
5. Texas Instruments, *ISO6731 General-Purpose Triple-Channel Digital Isolator with Robust EMC* Data Sheet
6. Texas Instruments, *TPS709 150-mA, 30-V, 1-µA I_Q Voltage Regulators With Enable* Data Sheet
7. Texas Instruments, *TRS3232E 3- to 5.5-V Multichannel RS-232 Line Driver/Receiver With ±15-kV ESD Protection* Data Sheet
8. Texas Instruments, Magnetic Tampering Detection video

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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