

CD4094B Types

CMOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

■ CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- 3-state parallel outputs for connection to common bus
- Separate serial outputs synchronous to both positive and negative clock edges for cascading
- Medium speed operation - 5 MHz at 10 V (typ.)
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range):
1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V
2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial-to-parallel data conversion
- Remote control holding register
- Dual-rank shift, hold, and bus applications

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|---|-------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) | -0.5V to +20V |
| Voltages referenced to V _{SS} Terminal) | |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to V _{DD} + 0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | ±10mA |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -55°C to +100°C | 500mW |
| For T _A = +100°C to +125°C | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | +265°C |

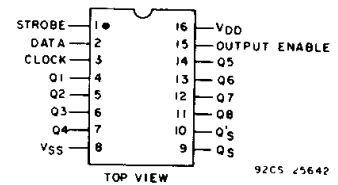
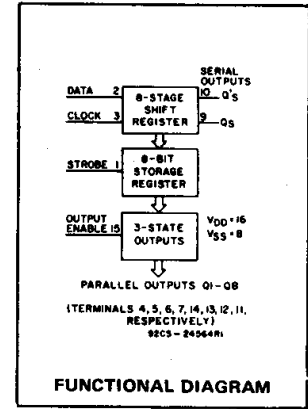


Fig. 1 - Terminal assignment.

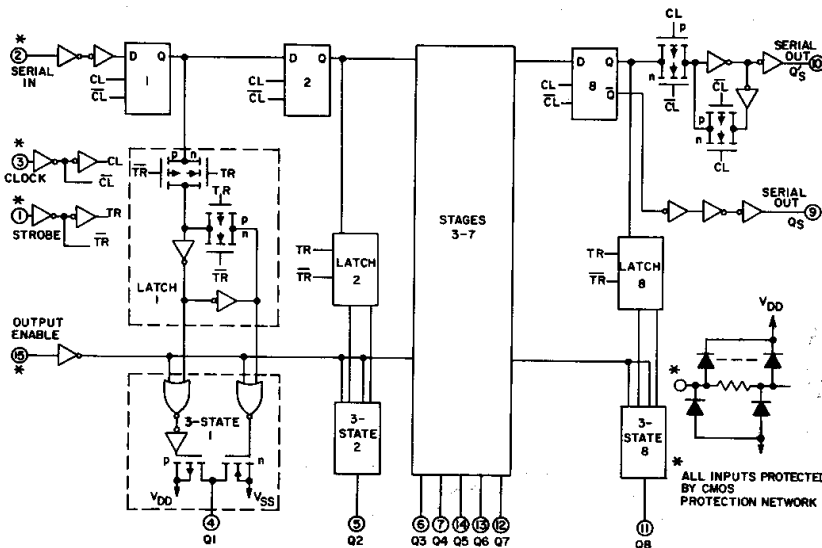


Fig. 2 - CD4094B Logic diagram.

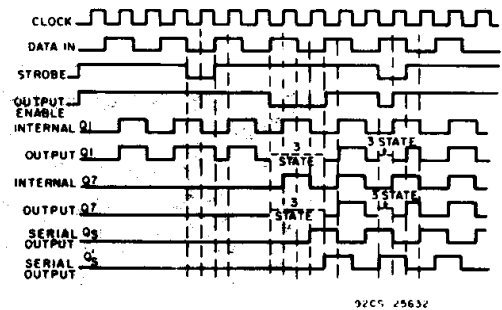


Fig. 3 - Timing diagram.

CD4094B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | VDD (V) | LIMITS | | UNITS |
|--|---------|--------|------|---------------|
| | | MIN. | MAX. | |
| Supply-Voltage Range (For T_A =Full Package-Temperature Range) | | 3 | 18 | V |
| Data Setup Time, t_S | 5 | 125 | — | ns |
| | 10 | 55 | — | |
| | 15 | 35 | — | |
| Clock Pulse Width, t_W | 5 | 200 | — | ns |
| | 10 | 100 | — | |
| | 15 | 83 | — | |
| Clock Input Frequency, f_{CL} | 5 | | 1.25 | MHz |
| | 10 | dc | 2.5 | |
| | 15 | | 3 | |
| Clock Input Rise or Fall time, t_{rCL}, t_{fCL} * | 5 | | 15 | μs |
| | 10 | — | 5 | |
| | 15 | | 5 | |
| Strobe Pulse Width, t_W | 5 | 200 | — | ns |
| | 10 | 80 | — | |
| | 15 | 70 | — | |

*If more than one unit is cascaded t_{fCL} (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.

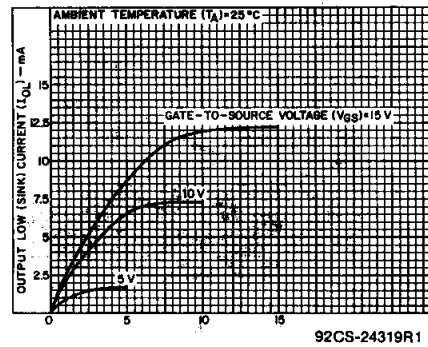


Fig. 5 - Minimum output low (sink) current characteristics.

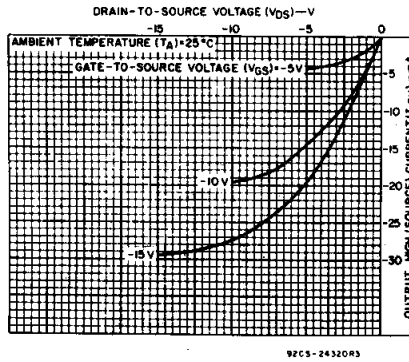


Fig. 6 - Typical output high (source) current characteristics.

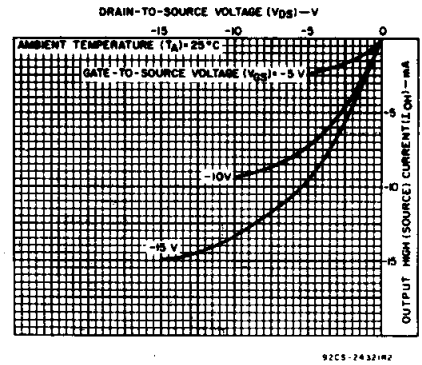


Fig. 7 - Minimum output high (source) current characteristics.

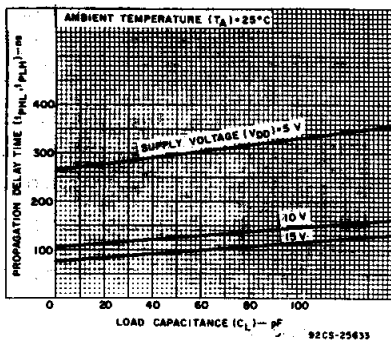


Fig. 8 - Clock-to-serial output Q_S propagation delay vs C_L .

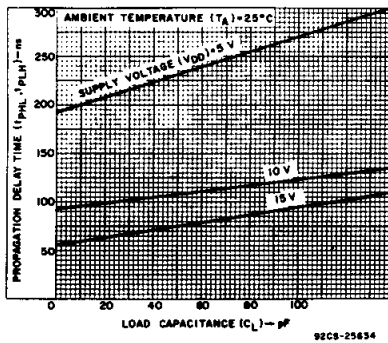


Fig. 9 - Clock-to-serial output Q'_S propagation delay vs C_L .

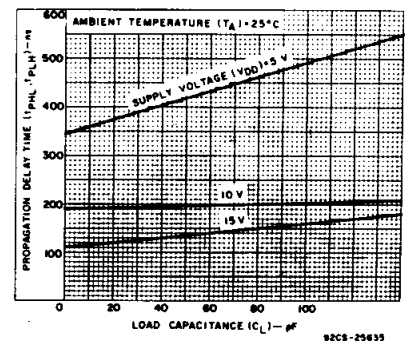


Fig. 10 - Clock-to-parallel output propagation delay vs C_L .

TRUTH TABLE

| CL [▲] | Output Enable | Strobe | Data | Parallel Outputs | | Serial Outputs | |
|-----------------|---------------|--------|------|------------------|------|----------------|----|
| | | | | Q1 | Q2 | Q3* | Q4 |
| [Symbol] | 0 | X | X | OC | OC | Q7 | NC |
| | 0 | X | X | OC | OC | NC | Q7 |
| [Symbol] | 1 | 0 | X | NC | NC | Q7 | NC |
| | 1 | 1 | 0 | 0 | QN-1 | Q7 | NC |
| [Symbol] | 1 | 1 | 1 | 1 | QN-1 | Q7 | NC |
| | 1 | 1 | 1 | 1 | NC | NC | Q7 |

▲ = Level Change
 X = Don't Care
 NC = No Change
 OC = Open Circuit

Logic 1 \equiv High
 Logic 0 \equiv Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

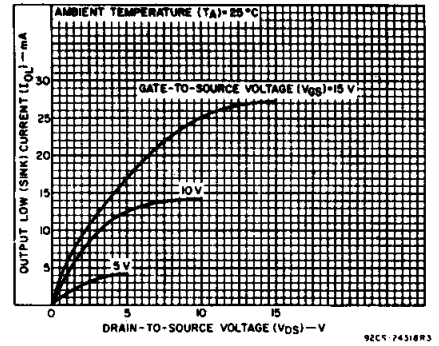


Fig. 4 - Typical output low (sink) current characteristics.

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STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | - | 0.5 | 5 | 5 | 5 | 150 | 150 | - | 0.04 | 5 | μA |
| | - | 0.10 | 10 | 10 | 10 | 300 | 300 | - | 0.04 | 10 | |
| | - | 0.15 | 15 | 20 | 20 | 600 | 600 | - | 0.04 | 20 | |
| | - | 0.20 | 20 | 100 | 100 | 3000 | 3000 | - | 0.08 | 100 | |
| Output Low (Sink) Current, I _{OL} Min. | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | - | mA |
| | 0.5 | 0.10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | - | |
| | 1.5 | 0.15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0.5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | - | mA |
| | 2.5 | 0.5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | - | |
| | 9.5 | 0.10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | - | |
| | 13.5 | 0.15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0.5 | 5 | 0.05 | | | | - | 0 | 0.05 | V |
| | - | 0.10 | 10 | 0.05 | | | | - | 0 | 0.05 | |
| | - | 0.15 | 15 | 0.05 | | | | - | 0 | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0.5 | 5 | 4.95 | | | | 4.95 | 5 | - | V |
| | - | 0.10 | 10 | 9.95 | | | | 9.95 | 10 | - | |
| | - | 0.15 | 15 | 14.95 | | | | 14.95 | 15 | - | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | - | 5 | 1.5 | | | | - | - | 1.5 | V |
| | 1.9 | - | 10 | 3 | | | | - | - | 3 | |
| | 1.5, 13.5 | - | 15 | 4 | | | | - | - | 4 | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | - | 5 | 3.5 | | | | 3.5 | - | - | V |
| | 1.9 | - | 10 | 7 | | | | 7 | - | - | |
| | 1.5, 13.5 | - | 15 | 11 | | | | 11 | - | - | |
| Input Current I _{IN} Max. | - | 0.18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA |
| 3-State Output Leakage Current I _{OUT} Max. | 0.18 | 0.18 | 18 | ±0.4 | ±0.4 | ±12 | ±12 | - | ±10 ⁻⁴ | ±0.4 | μA |

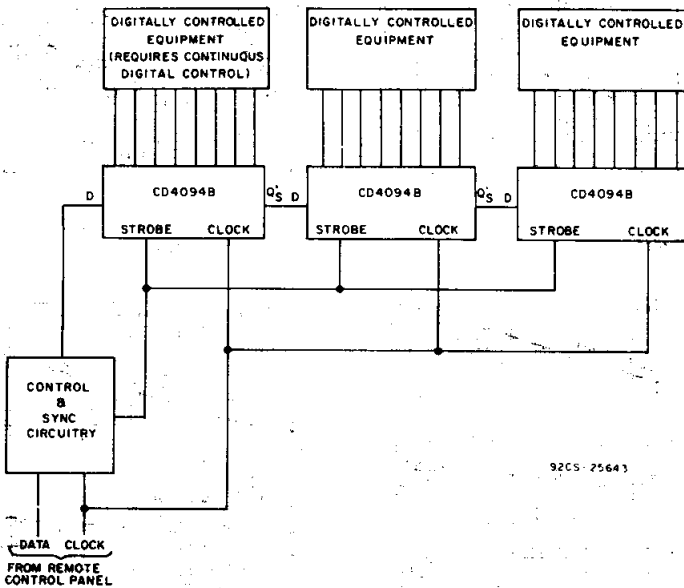


Fig. 14 - Remote control holding register.

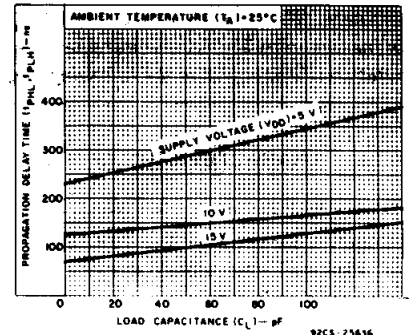


Fig. 11 - Strobe-to-parallel output propagation delay vs. C_L.

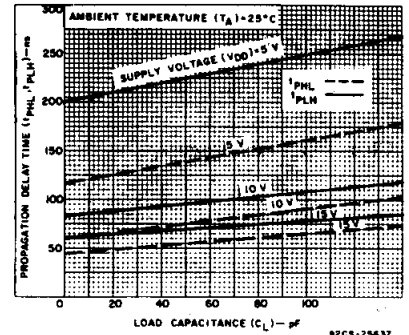


Fig. 12 - Output enable-to-parallel output propagation delay vs. C_L.

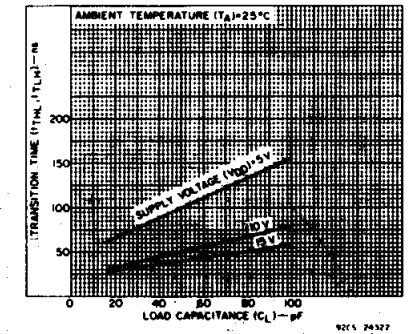


Fig. 13 - Typical transition time vs. load capacitance.

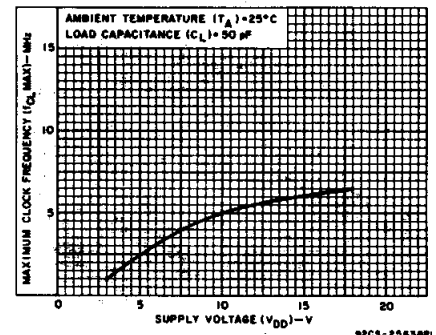


Fig. 15 - Typical maximum-clock-frequency vs. supply voltage.

CD4094B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A=25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | VDD (V) | LIMITS | | | UNITS |
|--|---------|--------|------|------|---------------|
| | | MIN. | TYP. | MAX. | |
| Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Serial Output Q_S | 5 | — | 300 | 600 | ns |
| | 10 | — | 125 | 250 | |
| | 15 | — | 95 | 190 | |
| Clock to Serial Output Q'_S | 5 | — | 230 | 460 | ns |
| | 10 | — | 110 | 220 | |
| | 15 | — | 75 | 150 | |
| Clock to Parallel Output | 5 | — | 420 | 840 | ns |
| | 10 | — | 195 | 390 | |
| | 15 | — | 135 | 270 | |
| Strobe to Parallel Output | 5 | — | 290 | 580 | ns |
| | 10 | — | 145 | 290 | |
| | 15 | — | 100 | 200 | |
| Output Enable to Parallel Output: t_{PHZ}, t_{PZH} | 5 | — | 140 | 280 | ns |
| | 10 | — | 60 | 120 | |
| | 15 | — | 45 | 90 | |
| t_{PLZ}, t_{PZL} | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Minimum Strobe Pulse Width, t_W | 5 | — | 100 | 200 | ns |
| | 10 | — | 40 | 80 | |
| | 15 | — | 35 | 70 | |
| Minimum Clock Pulse Width, t_W | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 83 | |
| Minimum Data Setup Time, t_S | 5 | — | 60 | 125 | ns |
| | 10 | — | 30 | 55 | |
| | 15 | — | 20 | 35 | |
| Transition Time; t_{THL}, t_{TLH} | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Maximum Clock Input Rise or Fall Time, t_{rCL}, t_{fCL} | 5 | 15 | — | — | μs |
| | 10 | 5 | — | — | |
| | 15 | 5 | — | — | |
| Maximum Clock Input Frequency, f_{CL} | 5 | 1.25 | 2.5 | — | MHz |
| | 10 | 2.5 | 5 | — | |
| | 15 | 3 | 6 | — | |
| Input Capacitance C_{iN} (Any Input) | — | — | 5 | 7.5 | pF |

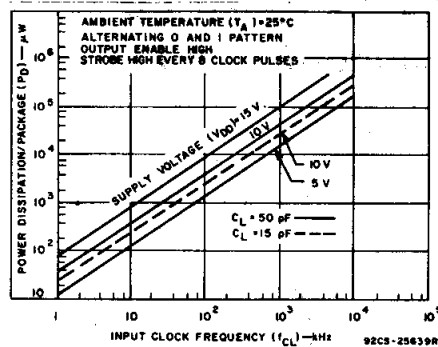


Fig. 16 — Dynamic power dissipation vs input clock frequency.

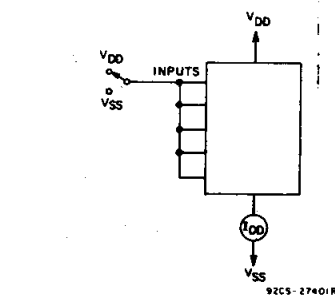


Fig. 17 — Quiescent device current test circuit.

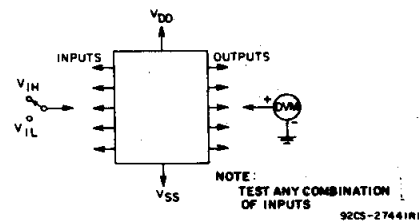


Fig. 18 — Input voltage test circuit.

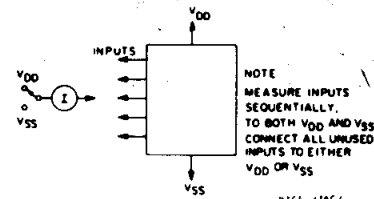
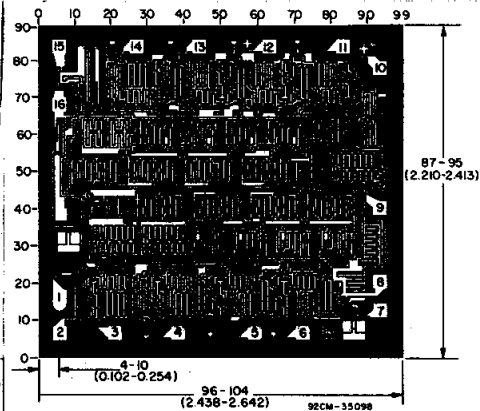


Fig. 19 — Input current test circuit.



Dimensions and Pad Layout for CD4094B Chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| 7702501EA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7702501EA CD4094BF3A | Samples |
| CD4094BE | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD4094BE | Samples |
| CD4094BEE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD4094BE | Samples |
| CD4094BF | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD4094BF | Samples |
| CD4094BF3A | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7702501EA CD4094BF3A | Samples |
| CD4094BNSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4094B | Samples |
| CD4094BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM094B | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4094B, CD4094B-MIL :

- Catalog : [CD4094B](#)
- Military : [CD4094B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4094BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4094BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4094BNSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| CD4094BPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE

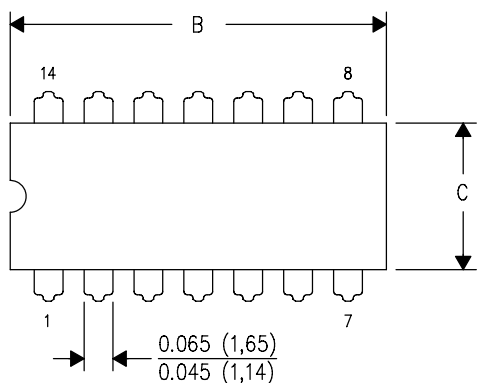

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD4094BE | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4094BE | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4094BEE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4094BEE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

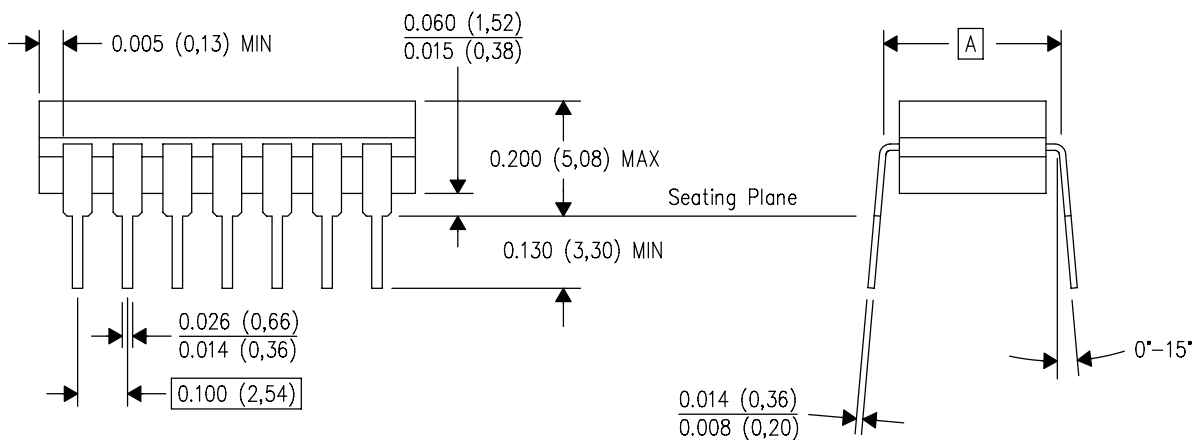
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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