

### Features

- FCT-C speed at 5.5 ns (FCT16841T Com'l)
- $I_{off}$  supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

#### CY74FCT16841T Features:

- 64 mA sink current, 32 mA source current
- Typical  $V_{OLP}$  (ground bounce) < 1.0V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

#### CY74FCT162841T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) < 0.6V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

### Functional Description

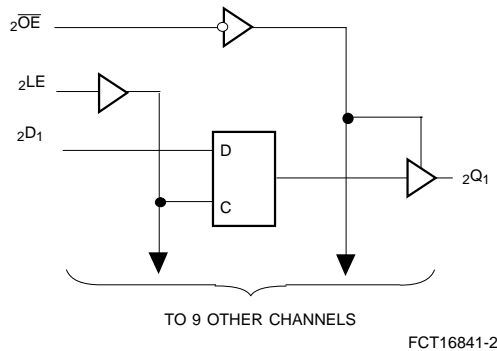
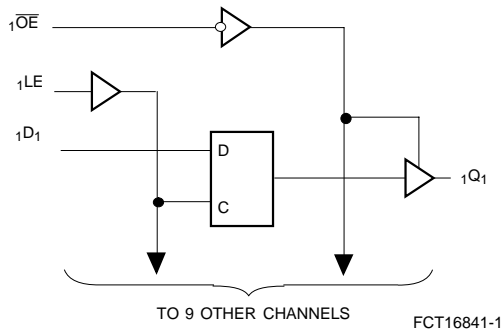
The CY74FCT16841T and CY74FCT162841T are 20-bit D-type latches designed for use in bus applications requiring high speed and low power. These devices can be used as two independent 10-bit latches, or as a single 10-bit latch, or as a single 20-bit latch by connecting the Output Enable ( $\overline{OE}$ ) and Latch (LE) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16841T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162841T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162841T is ideal for driving transmission lines.

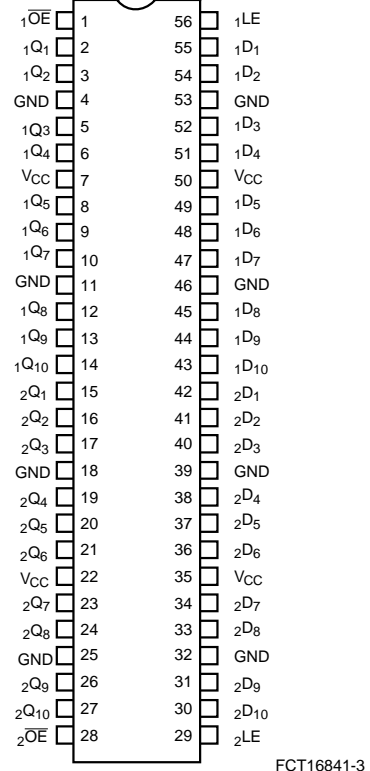
### Logic Block Diagrams



### Pin Configuration

#### SSOP/TSSOP

#### Top View



**Pin Description**

Name	Description
D	Data Inputs
LE	Latch Enable Input (Active HIGH)
OE	Output Enable Input (Active LOW)
O	Three-State Outputs

**Function Table<sup>[1]</sup>**

Inputs			Outputs
D	LE	OE	Q
H	H	L	H
L	H	L	L
X	L	L	Q <sup>[2]</sup>
X	X	H	Z

**Maximum Ratings<sup>[3, 4]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -55°C to +125°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

DC Input Voltage ..... -0.5V to +7.0V

DC Output Voltage ..... -0.5V to +7.0V

DC Output Current  
(Maximum Sink Current/Pin) ..... -60 to +120 mA

Power Dissipation ..... 1.0W

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	Logic HIGH Level	2.0			V
V <sub>IL</sub>	Input LOW Voltage	Logic LOW Level			0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[6]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>			±1	µA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>I</sub> =GND			±1	µA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	µA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	µA
I <sub>OS</sub>	Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[8]</sup>			±1	µA

**Notes:**

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance.
- Output level before LE HIGH-to-LOW Transition.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- Typical values are at V<sub>CC</sub>= 5.0V, T<sub>A</sub>= +25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Tested at +25°C.

**Output Drive Characteristics for CY74FCT16841T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

**Output Drive Characteristics for CY74FCT162841T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[7]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[7]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA		0.3	0.55	V

**Capacitance<sup>[6]</sup> (T<sub>A</sub> = +25°C, f = 1.0 MHz)**

Symbol	Description	Conditions	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit	
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max., V <sub>IN</sub> ≤0.2V V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	—	5	500	μA	
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max., V <sub>IN</sub> =3.4V <sup>[9]</sup>	—	0.5	1.5	mA	
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[10]</sup>	V <sub>CC</sub> =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND	—	60	100	μA/MHz	
I <sub>C</sub>	Total Power Supply Current <sup>[11]</sup>	V <sub>CC</sub> =Max., f <sub>1</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OE=GND LE = V <sub>CC</sub>	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	—	0.6	1.5	mA
			V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	—	0.9	2.3	
		V <sub>CC</sub> =Max., f <sub>1</sub> =2.5 MHz, 50% Duty Cycle, Outputs Open, Twenty Bits Toggling, OE=GND	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	—	3.0	5.5 <sup>[12]</sup>	
			V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	—	8.0	20.5 <sup>[12]</sup>	

**Notes:**

9. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub>D<sub>H</sub>N<sub>T</sub> + I<sub>CCD</sub>(f<sub>0</sub>/2 + f<sub>1</sub>N<sub>1</sub>)  
 I<sub>CC</sub> = Quiescent Current with CMOS input levels  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL inputs HIGH  
 N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)  
 f<sub>0</sub> = Clock frequency for registered devices, otherwise zero  
 f<sub>1</sub> = Input signal frequency  
 N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>  
 All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[13]</sup>

Parameter	Description	Condition <sup>[14]</sup>	74FCT16841AT		74FCT16841CT 74FCT162841CT		Unit	Fig. No. <sup>[15]</sup>
			Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D to Q (LE=HIGH)	C <sub>L</sub> =50 pF R <sub>L</sub> =500Ω	1.5	9.0	1.5	5.5	ns	1, 5
		C <sub>L</sub> =300 pF <sup>[16]</sup> R <sub>L</sub> =500Ω	1.5	13.0	1.5	13.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to Q	C <sub>L</sub> =50 pF R <sub>L</sub> =500Ω	1.5	12.0	1.5	6.4	ns	1, 5
		C <sub>L</sub> =300 pF <sup>[16]</sup> R <sub>L</sub> =500Ω	1.5	16.0	1.5	15.0		
t <sub>PHZ</sub> t <sub>PZL</sub>	Output Enable Time OE to Q	C <sub>L</sub> =50 pF R <sub>L</sub> =500Ω	1.5	11.5	1.5	6.5	ns	1, 7, 8
		C <sub>L</sub> =300 pF <sup>[16]</sup> R <sub>L</sub> =500Ω	1.5	23.0	1.5	12.0		
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE to Q	C <sub>L</sub> =5 pF <sup>[16]</sup> R <sub>L</sub> =500Ω	1.5	7.0	1.5	5.7	ns	1, 7, 8
		C <sub>L</sub> =50 pF R <sub>L</sub> =500Ω	1.5	8.0	1.5	6.0		
t <sub>SU</sub>	Set-Up Time HIGH or LOW, D to LE	C <sub>L</sub> =50 pF R <sub>L</sub> =500Ω	2.5	—	2.0	—	ns	9
t <sub>H</sub>	Hold Time HIGH or LOW, D to LE		2.5	—	1.5	—	ns	9
t <sub>W</sub>	LE Pulse Width HIGH		4.0 <sup>[17]</sup>	—	4.0 <sup>[17]</sup>	—	ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[18]</sup>		—	0.5	—	0.5	ns	—

**Notes:**

13. Minimum limits are specified but not tested on Propagation Delays.
14. See test circuit and waveform.
15. See "Parameter Measurement Information" in the General Information section.
16. These conditions are specified but not tested.
17. These limits are specified but not tested.
18. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Ordering Information for CY74FCT16841T**

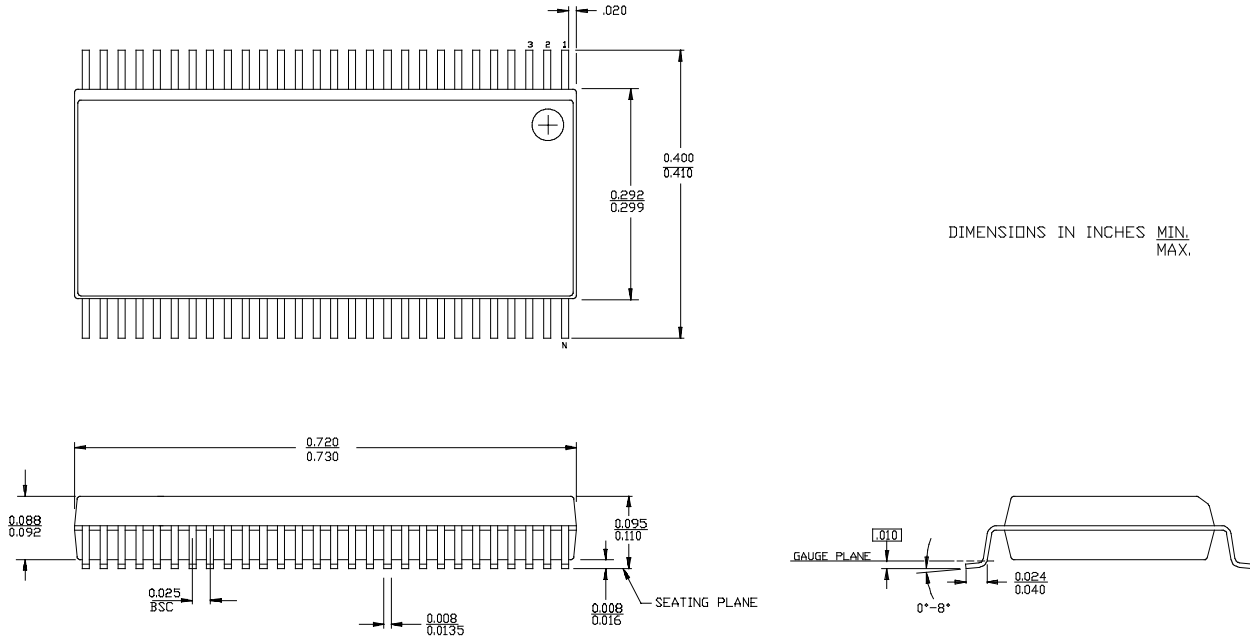
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	CY74FCT16841CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
6.5	CY74FCT16841ATPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

**Ordering Information CY74FCT162841T**

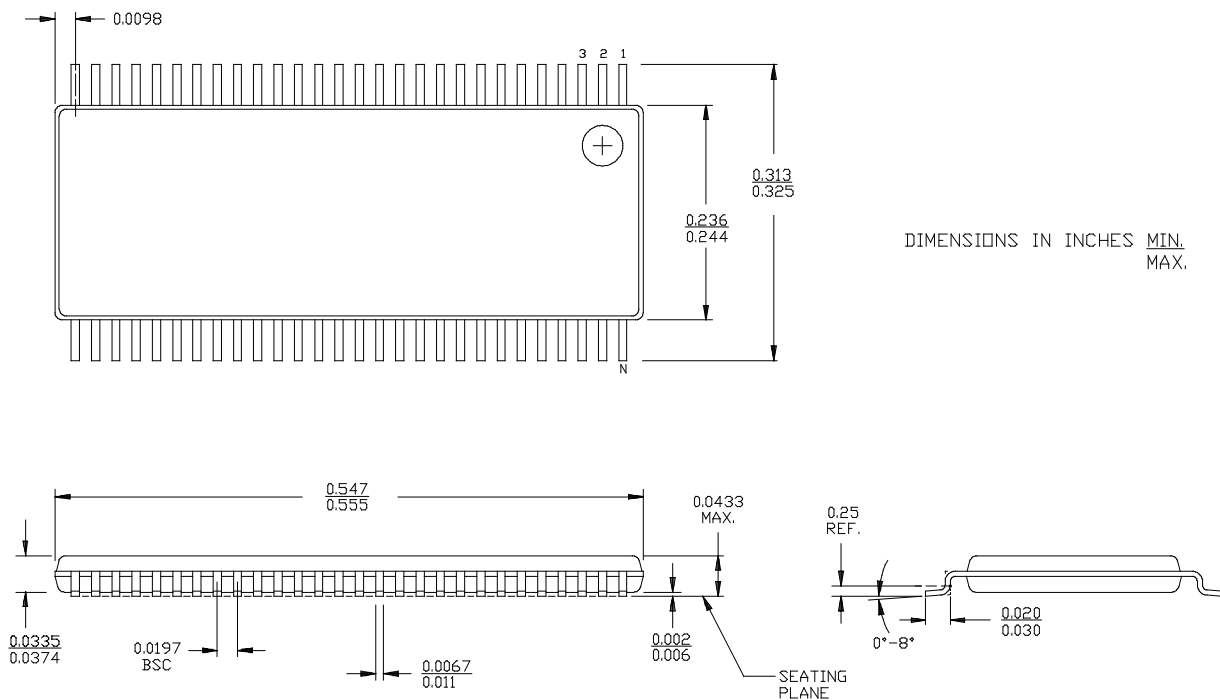
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	74FCT162841CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162841CTPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162841CTPVCT	O56	56-Lead (300-Mil) SSOP	

**Package Diagrams**

**56-Lead Shrunk Small Outline Package O56**



**56-Lead Thin Shrunk Small Outline Package Z56**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74FCT162841CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162841CTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162841CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162841ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
74FCT16841ATPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16841CTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16841CTPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162841CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162841ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT16841ATPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16841CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16841CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162841CTPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162841CTPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162841CTPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is

provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162841CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
74FCT162841CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
CY74FCT16841CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162841CTPACT	TSSOP	DGG	56	2000	346.0	346.0	41.0
74FCT162841CTPVCT	SSOP	DL	56	1000	346.0	346.0	49.0
CY74FCT16841CTPVCT	SSOP	DL	56	1000	346.0	346.0	49.0

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT16841CTPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85	FCT16841C	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated