LM4936 Boomer™ Audio Power Amplifier Series Stereo 2W Audio Power Amplifiers with Volume Control and Selectable Control Interface (SPI or I²C)

Check for Samples: LM4936

FEATURES

- **Selectable SPI or I²C Control Interface**
- **System Beep Detect**
- **Stereo Switchable Bridged/Single-Ended Power Amplifiers**
- **Selectable Internal/External Gain and Bass Boost**
- **"Click and Pop" Suppression Circuitry**
- **Thermal Shutdown Protection Circuitry**
- **Headphone Sense**

APPLICATIONS

- **Portable and Desktop Computers**
- **Multimedia Monitors**
- **Portable Radios, PDAs, and Portable TVs**

KEY SPECIFICATIONS

- **P_O at 1% THD+N**
  - **into 3Ω, 2.2W (Typ)**
  - **into 4Ω, 2.0W (Typ)**
  - **into 8Ω, 1.25W (Typ)**
- **Single-ended mode - THD+N at 90mW into 32Ω, 1% (Typ)**
- **Shutdown current, 0.7µA (Typ)**

DESCRIPTION

The LM4936 is a monolithic integrated circuit that provides volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω (1) with less than 1% THD or 2.2W into 3Ω (2) with less than 1% THD.

Boomer audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4936 incorporates a SPI or I²C Control Interface that runs the volume control, stereo bridged audio power amplifiers and a selectable gain or bass boost. All of the LM4936's features (i.e. SD, Mode, Mute, Gain Sel) make it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4936 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

(1) When properly mounted to the circuit board, LM4936MH will deliver 2W into 4Ω. See Application Information section HTSSOP PACKAGE PCB MOUNTING CONSIDERATIONS for more information.
(2) An LM4936MH that has been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Connection Diagram

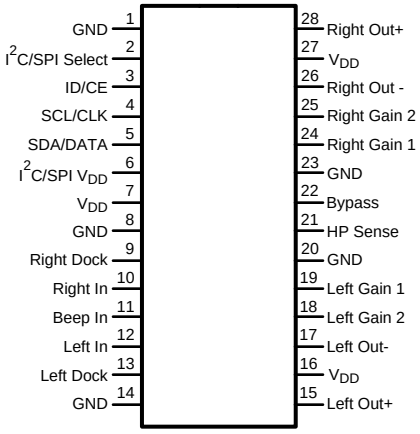


Figure 1. HTSSOP Package
(Top View)
See Package Number PWP0028A for HTSSOP

Block Diagram

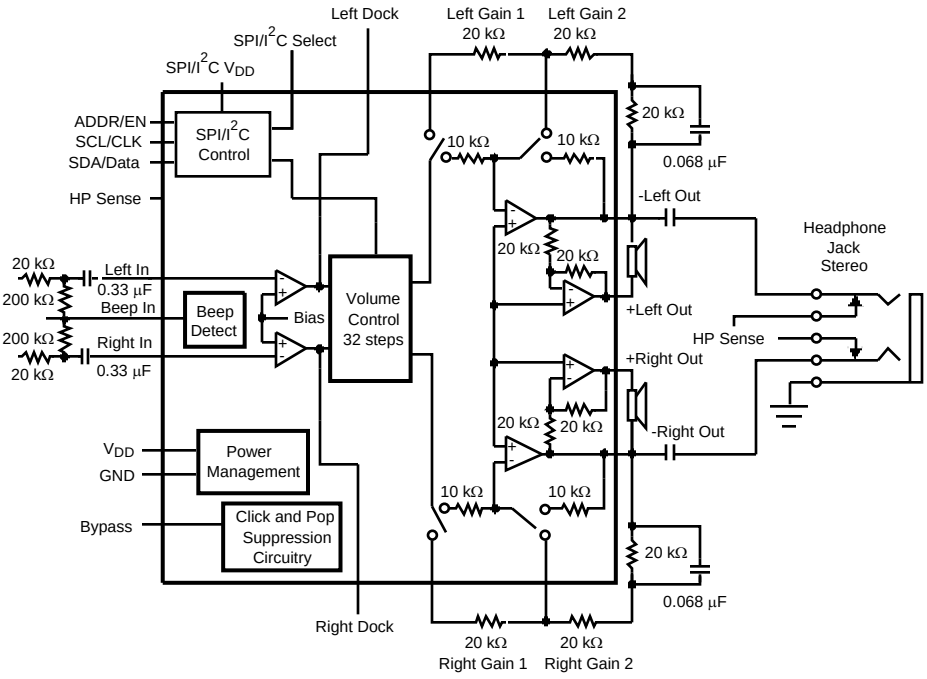


Figure 2. LM4936 Block Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage			6.0V
Storage Temperature			-65°C to +150°C
Input Voltage			−0.3V to V_{DD} +0.3V
Power Dissipation(3)			Internally limited
ESD Susceptibility(4)			2000V
ESD Susceptibility(5)			200V
Junction Temperature			150°C
Soldering Information	Small Outline Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
θ_{JC} (typ) - PWP0028A			2°C/W
θ_{JA} (typ) - PWP0028A (HTSSOP)(6)			41°C/W
θ_{JA} (typ) - PWP0028A (HTSSOP)(7)			54°C/W
θ_{JA} (typ) - PWP0028A (HTSSOP)(8)			59°C/W
θ_{JA} (typ) - PWP0028A (HTSSOP)(9)			93°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4936, T_{JMAX} = 150°C, and the typical junction-to-ambient thermal resistance for each package can be found in the **Absolute Maximum Ratings** section above.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model, 220pF – 240pF discharged through all pins.
(6) The θ_{JA} given is for an PWP0028A package whose HTSSOP is soldered to a 2in^2 piece of 1 ounce printed circuit board copper on a bottom side layer through 21 8mil vias.
(7) The θ_{JA} given is for an PWP0028A package whose HTSSOP is soldered to an exposed 2in^2 piece of 1 ounce printed circuit board copper.
(8) The θ_{JA} given is for an PWP0028A package whose HTSSOP is soldered to an exposed 1in^2 piece of 1 ounce printed circuit board copper.
(9) The θ_{JA} given is for an PWP0028A package whose HTSSOP is not soldered to any copper.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ TA ≤ 85°C
Supply Voltage(1)		2.7V ≤ V_{DD} ≤ 5.5V
		I^2C/SPI V_{DD} ≤ V_{DD}
		2.4V ≤ I^2C/SPI V_{DD} ≤ 5.5V

(1) I^2C/SPI V_{DD} must not be larger than V_{DD} at any time or damage to the IC may occur. During power up and power down, I^2C/SPI V_{DD} must remain equal to V_{DD} or lower.

Electrical Characteristics for Entire IC[1][2]

The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4936		Units (Limits)
			Typical[3]	Limit[4]	
V_{DD}	Supply Voltage			2.7	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	10	25	mA (max)
I_{SD}	Shutdown Current	$V_{shutdown}$ = V_{DD}	0.7	2.0	µA (max)
V_{IH}	Headphone Sense High Input Voltage			4	V (min)
V_{IL}	Headphone Sense Low Input Voltage			0.8	V (max)

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 2.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Electrical Characteristics for Volume Control[1][2]

The following specifications apply for V_{DD} = 5V. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4936		Units (Limits)
			Typical[3]	Limit[4]	
C_{RANGE}	Volume Control Range	Maximum gain setting	0	±0.75	dB (max)
		Minimum gain setting	-91	-75	dB (min)
A_{Ch-Ch}	Channel to Channel Gain Mismatch	f_{IN} = 1kHz	0.35		dB
A_M	Mute Attenuation	Mute Mode		-78	dB (min)

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 2.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Electrical Characteristics for Control Interface (1) (2)

The following specifications apply for V_{DD} = 5V, V_{DD} = 3V and 2.4V ≤ I^2C/SPI V_{DD} ≤ 5.5V. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4936		Units (Limits)
			Typical (3)	Limit (4)	
t_1	SCL period			2.5	µs (min)
t_2	SDA Set-up Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
V_{IH}	Digital Input High Voltage			0.7 X $I^2C/SPIV_{DD}$	V (min)
V_{IL}	Digital Input Low Voltage			0.3 X $I^2C/SPIV_{DD}$	V (max)
t_{ES}	SPI ENABLE Setup Time			50	ns (min)
t_{EH}	SPI ENABLE Hold Time			50	ns (min)
t_{EL}	SPI ENABLE High Time			50	ns (min)
t_{DS}	SPI DATA Setup Time			50	ns (min)
t_{DH}	SPI DATA HOLD Time			50	ns (min)
t_{CS}	SPI CLOCK Setup Time			50	ns (min)
t_{CH}	SPI CLOCK High Pulse Width			100	ns (min)
t_{CL}	SPI CLOCK Low Pulse Width			100	ns (min)
f_{CLK}	SPI CLOCK Frequency			5	MHz (max)

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 2.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Electrical Characteristics for Single-Ended Mode Operation (1) (2)

The following specifications apply for V_{DD} = 5V. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4936		Units (Limits)
			Typical (3)	Limit (4)	
P_O	Output Power	THD = 1%; f = 1kHz; R_L = 32Ω	90		mW
		THD = 10%; f = 1 kHz; R_L = 32Ω	110		mW
THD+N	Total Harmonic Distortion+Noise	P_{OUT} = 20mW, f = 1kHz, R_L = 32Ω, A_{VD} = 1, 80kHz BW	0.02		%
PSRR	Power Supply Rejection Ratio	C_B = 1µF, f = 120Hz, Input Terminated V_{RIPPLE} = 200mVp-p	57		dB
N_{OUT}	Output Noise	A-Wtd Filter	18		µV
X_{talk}	Channel Separation (5)	f = 1kHz, C_B = 1µF	63		dB

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 2.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) PCB design will affect Crosstalk performance.

Electrical Characteristics for Bridged Mode Operation(1)(2)

The following specifications apply for V_{DD} = 5V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4936		Units (Limits)
			Typical(3)	Limit(4)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V, No Load	10	50	mV (max)
P_O	Output Power	THD + N = 1%; f = 1kHz; R_L = 3Ω(5)	2.2		W
		THD + N = 1%; f = 1kHz; R_L = 4Ω(6)	2		W
		THD+N = 1% (max); f = 1kHz; R_L = 8Ω	1.25	1.0	W (min)
		THD+N = 10%; f = 1kHz; R_L = 8Ω	1.6		W
THD+N	Total Harmonic Distortion+Noise	P_O = 0.4W, f = 1kHz R_L = 8Ω, A_{VD} = 2, 80kHz BW	0.06		%
PSRR	Power Supply Rejection Ratio	C_B = 1µF, f = 120Hz, Input Terminated V_{RIPPLE} = 200mVp-p; R_L = 8Ω	55		dB
N_{OUT}	Output Noise	A-Wtd Filter	36		µV
X_{talk}	Channel Separation(7)	f = 1kHz, C_B = 1µF	63		dB

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 2.

(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.

(3) Typicals are measured at 25°C and represent the parametric norm.

(4) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

(5) When driving 3Ω loads from a 5V supply the LM4936MH must be mounted to the circuit board and forced-air cooled. The demo board shown in the datasheet has planes for heat sinking. The top layer plane is 1.05 in^2 (675mm^2), the inner two layers each have a 1.03 in^2 (667mm^2) plane and the bottom layer has a 3.32 in^2 (2143mm^2) plane. The planes are electrically GND and interconnected through six 15 mil vias directly under the package and eight 28 mil vias in various locations.

(6) When driving 4Ω loads from a 5V supply the LM4936MH must be mounted to the circuit board. The demo board shown in the datasheet has planes for heat sinking. The top layer plane is 1.05 in^2 (675mm^2), the inner two layers each have a 1.03 in^2 (667mm^2) plane and the bottom layer has a 3.32 in^2 (2143mm^2) plane. The planes are electrically GND and interconnected through six 15 mil vias directly under the package and eight 28 mil vias in various locations.

(7) PCB design will affect Crosstalk performance.

Typical Application

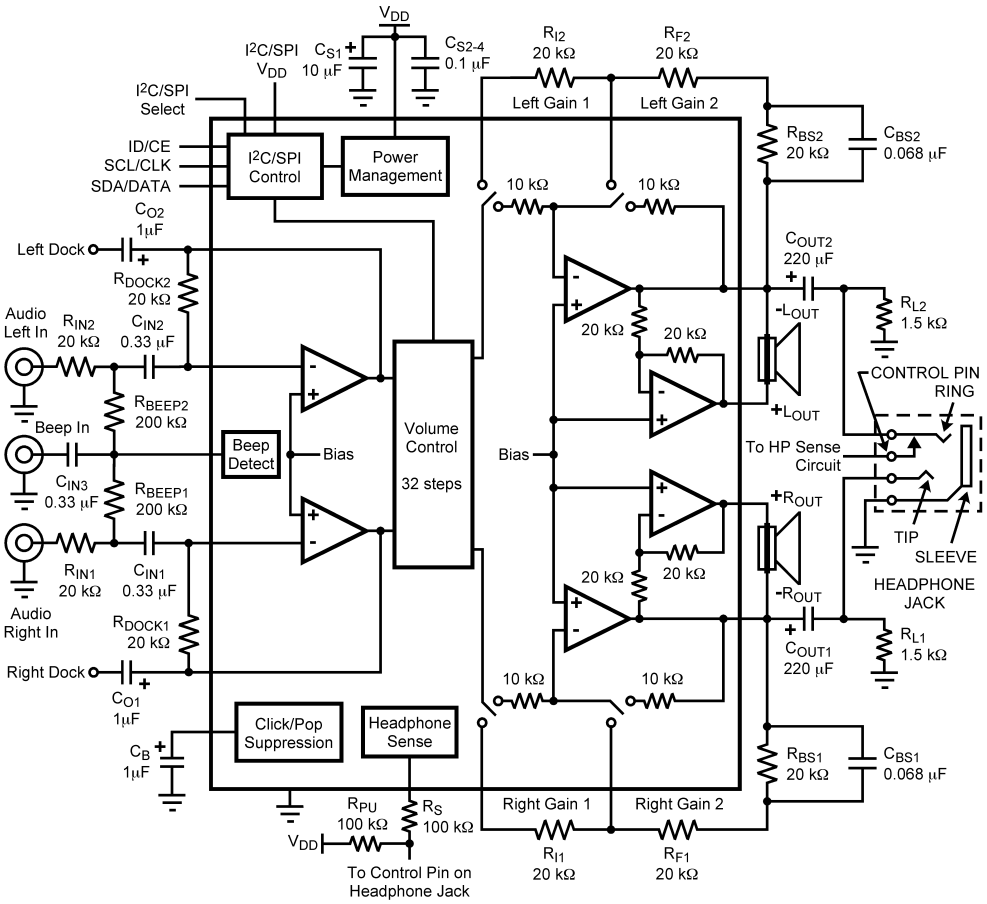


Figure 3. Typical Application Circuit

Table 1. I²C/SPI Interface Controls(1)

	B7	B6	B5	B4	B3	B2	B1	B0
I²C Address	1	1	0	1	1	0	ID	0
Mode Control Register	0	0	0	HP Control	Gain Sel	Mode	Mute	Shutdown
Volume Control Register (See Table 4)	1	0	0	V4	V3	V2	V1	V0

(1) If system beep is detected on the Beep In pin, the system beep will be passed through the bridged amplifier regardless of the logic of the Mute and HP Control bits (B1, B4) and HP Sense pin.

Table 2. Headphone Control

HP Sense Pin	I²C/SPI HP Control (B4)	Output Stage Configuration
0	0	BTL
0	1	SE
1 (V_{DD})	0	SE
1 (V_{DD})	1	SE

Table 3. Logic Controls

Logic Level	B3 (Gain Sel)	B2 (Mode)	B1 (Mute)	B0 (Shutdown)	I²C/SPI Select
0	Internal Gain	Fixed Volume, 0dB	Mute Off (Play)	Device Shutdown	I²C mode
1	External Gain	Adjustable Volume	Mute On	Device Active	SPI mode

Typical Performance Characteristics

THD+N vs Output Power/Channel
V_{DD} = 5V, R_L = 3Ω, A_{V-BTL} = 2V/V
f = 1kHz, 80kHz BW

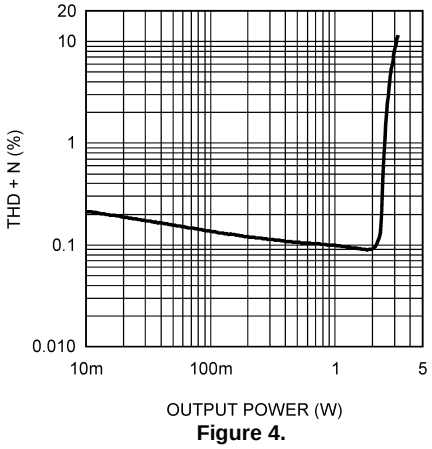


Figure 4.

THD+N vs Frequency
V_{DD} = 5V, R_L = 3Ω, A_{V-BTL} = 2V/V
P_{OUT} = 1.5W/Channel, 80kHz BW

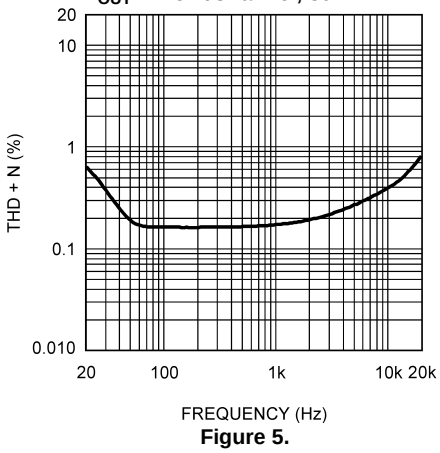


Figure 5.

THD+N vs Output Power/Channel
V_{DD} = 5V, R_L = 4Ω, A_{V-BTL} = 2V/V
f = 1kHz, 80kHz BW

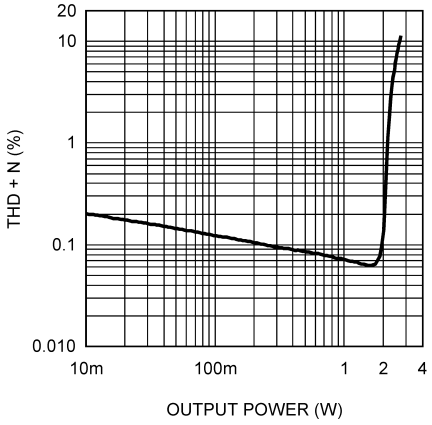


Figure 6.

THD+N vs Frequency
V_{DD} = 5V, R_L = 4Ω, A_{V-BTL} = 2V/V
P_{OUT} = 1.5W/Channel, 80kHz BW

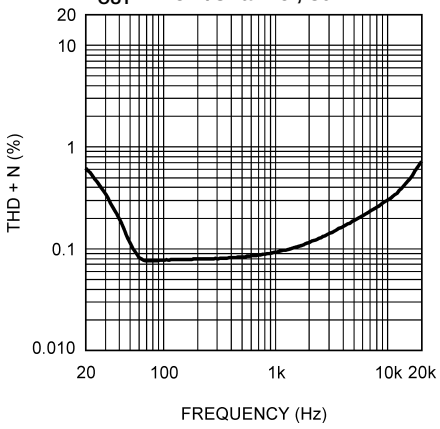


Figure 7.

THD+N vs Output Power/Channel
V_{DD} = 5V, R_L = 8Ω, A_{V-BTL} = 2V/V
f = 1kHz, 80kHz BW

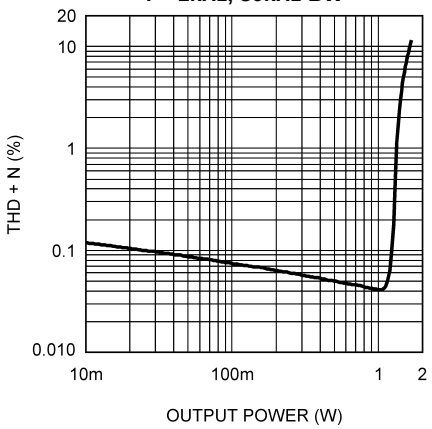


Figure 8.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, A_{V-BTL} = 2V/V
P_{OUT} = 1W/Channel, 80kHz BW

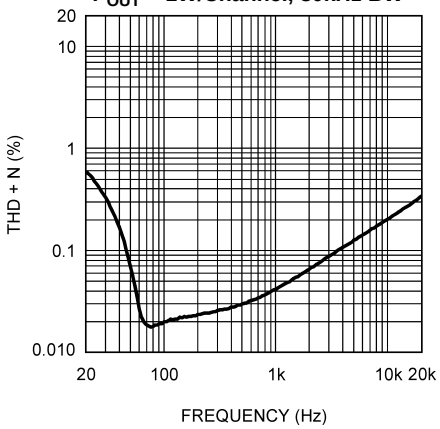


Figure 9.

Typical Performance Characteristics (continued)

THD+N vs Output Power/Channel
V_{DD} = 5V, R_L = 8Ω, A_{V-SE} = 1V/V
f = 1kHz, C_{OUT} = 220µF, 80kHz BW

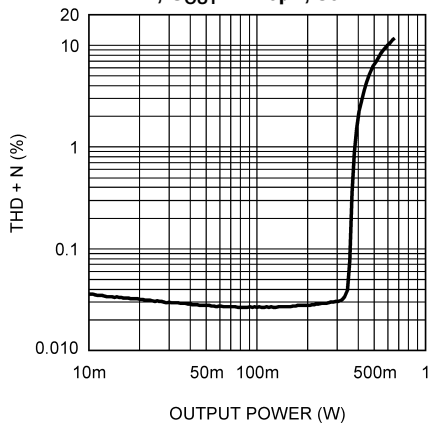


Figure 10.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, A_{V-SE} = 1V/V
P_{OUT} = 100mW/Channel, 80kHz BW

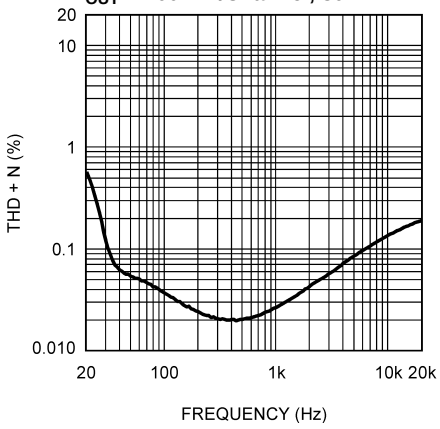


Figure 11.

THD+N vs Output Power/Channel
V_{DD} = 5V, R_L = 32Ω, A_{V-SE} = 1V/V
f = 1kHz, C_{OUT} = 220µF, 80kHz BW

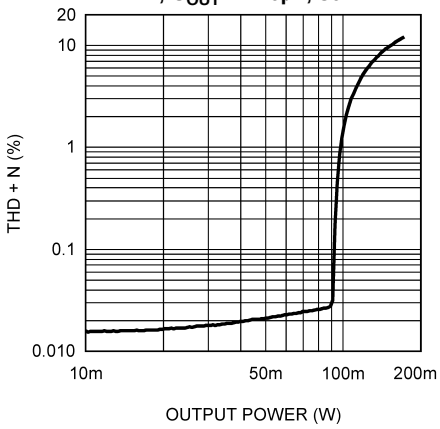


Figure 12.

THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, A_{V-SE} = 1V/V
P_{OUT} = 40mW/Channel, 80kHz BW

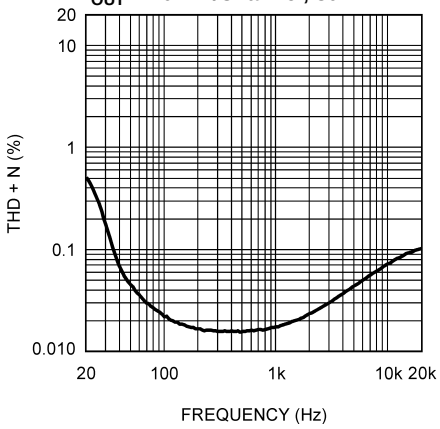


Figure 13.

THD+N vs Output Power/Channel
V_{DD} = 3V, R_L = 3Ω, A_{V-BTL} = 2V/V
f = 1kHz, 80kHz BW

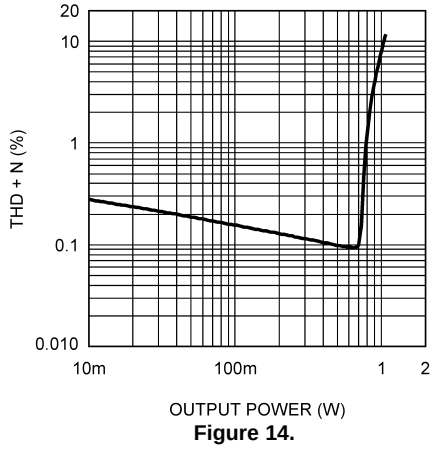


Figure 14.

THD+N vs Frequency
V_{DD} = 3V, R_L = 3Ω, A_{V-SE} = 2V/V
P_{OUT} = 500mW/Channel, 80kHz BW

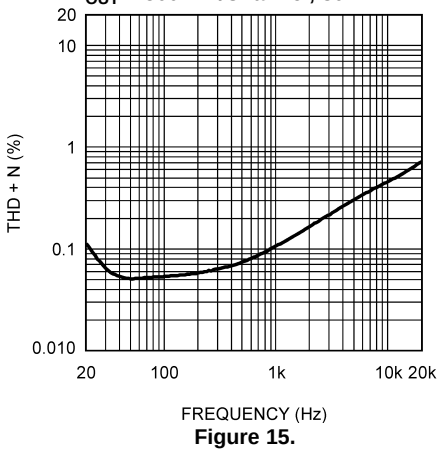


Figure 15.

Typical Performance Characteristics (continued)

THD+N vs Output Power/Channel
V_{DD} = 3V, R_L = 4Ω, A_{V-BTL} = 2V/V
f = 1kHz, 80kHz BW

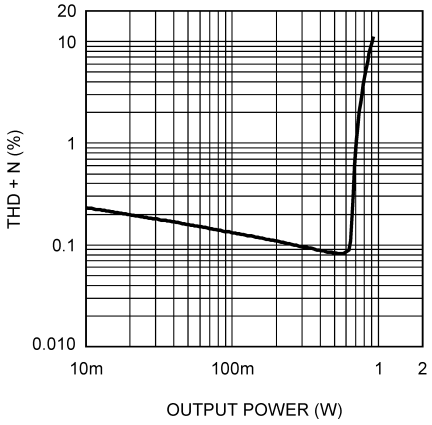


Figure 16.

THD+N vs Frequency
V_{DD} = 3V, R_L = 4Ω, A_{V-BTL} = 2V/V
P_{OUT} = 450mW/Channel, 80kHz BW

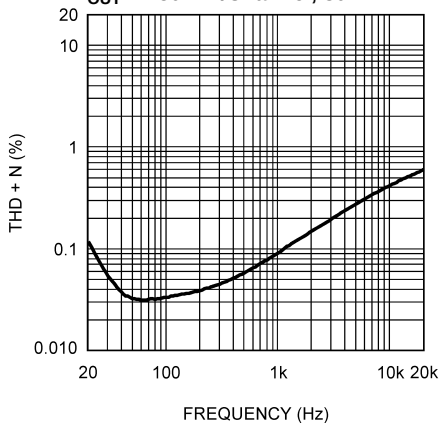


Figure 17.

THD+N vs Output Power/Channel
V_{DD} = 3V, R_L = 8Ω, A_{V-BTL} = 2V/V
f = 1kHz, 80kHz BW

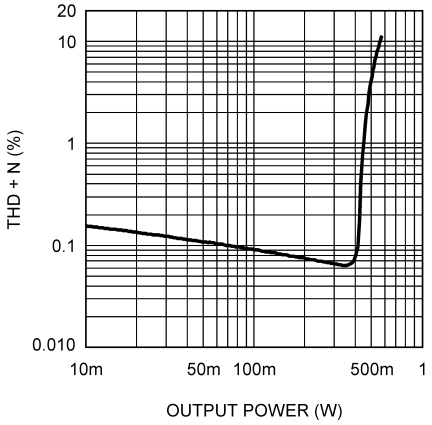


Figure 18.

THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, A_{V-BTL} = 2V/V
P_{OUT} = 250mW/Channel, 80kHz BW

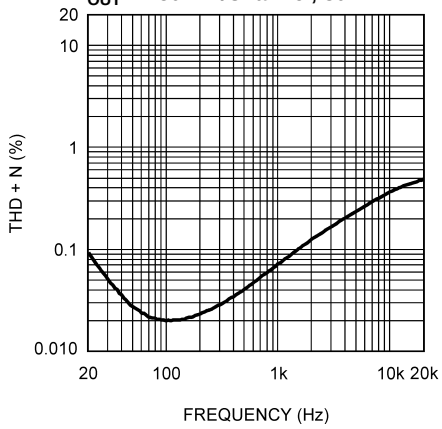


Figure 19.

THD+N vs Output Power/Channel
V_{DD} = 3V, R_L = 8Ω, A_{V-SE} = 1V/V
f = 1kHz, C_{OUT} = 220µF, 80kHz BW

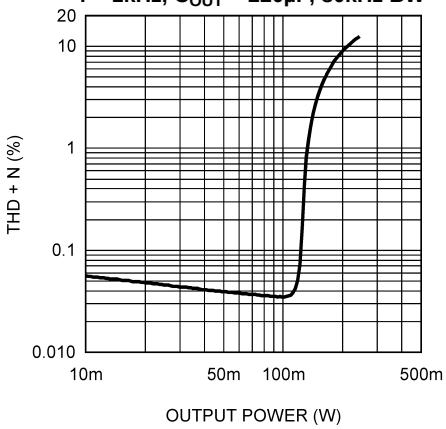


Figure 20.

THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, A_{V-SE} = 1V/V
P_{OUT} = 50mW/Channel, 80kHz BW

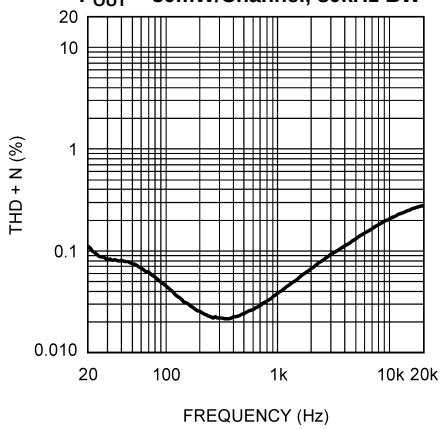


Figure 21.

Typical Performance Characteristics (continued)

THD+N vs Output Power/Channel
V_{DD} = 3V, R_L = 32Ω, A_{V-SE} = 1V/V
f = 1kHz, C_{OUT} = 220µF, 80kHz BW

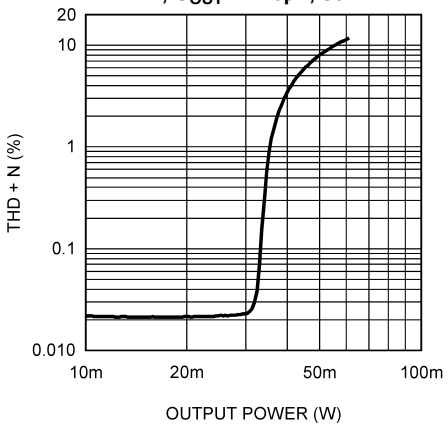


Figure 22.

THD+N vs Frequency
V_{DD} = 3V, R_L = 32Ω, A_{V-SE} = 1V/V
P_{OUT} = 20mW/Channel, 80kHz BW

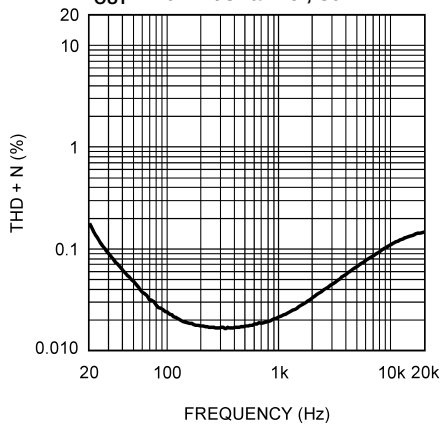


Figure 23.

THD+N vs Output Voltage
V_{DD} = 5V, R_{LDOCK} = 10kΩ, Dock Pins
f = 1kHz, C_O = 1µF, 80kHz BW

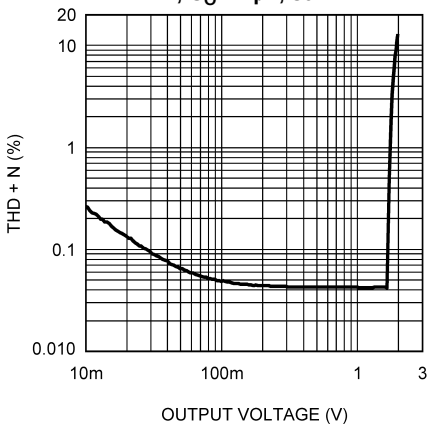


Figure 24.

THD+N vs Frequency
V_{DD} = 5V, R_{LDOCK} = 10kΩ, Dock Pins
V_{IN} = 1Vp-p, C_O = 1µF, 80kHz BW

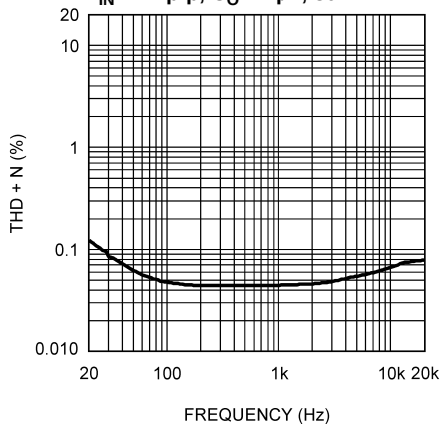


Figure 25.

THD+N vs Output Voltage
V_{DD} = 3V, R_{LDOCK} = 10kΩ, Dock Pins
f = 1kHz, C_O = 1µF, 80kHz BW

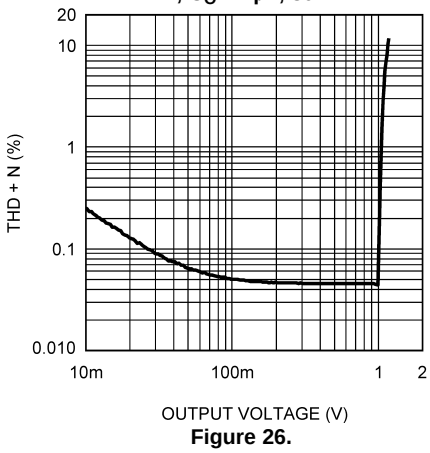


Figure 26.

THD+N vs Frequency
V_{DD} = 3V, R_{LDOCK}= 10kΩ, Dock Pins
V_{IN} = 1Vp-p, C_O = 1µF, 80kHz BW

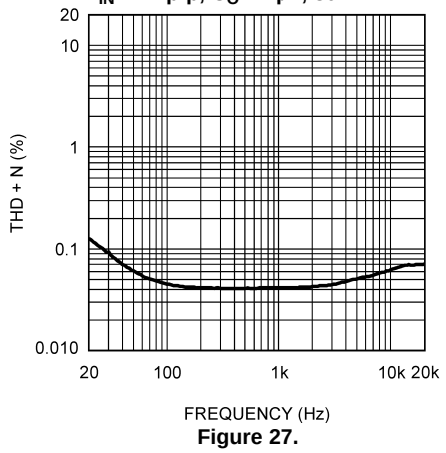


Figure 27.

Typical Performance Characteristics (continued)

PSRR vs Frequency
V_{DD} = 5V, V_{RIPPLE} = 200mVp-p
Inputs Terminated, 80kHz BW

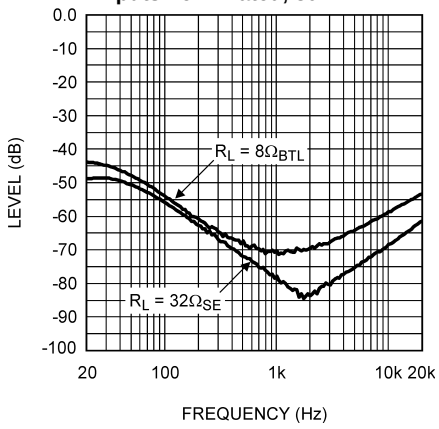


Figure 28.

PSRR vs Frequency
V_{DD} = 3V, V_{RIPPLE} = 200mVp-p
Inputs Terminated, 80kHz BW

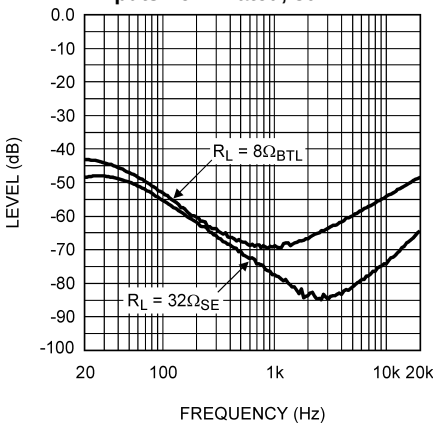


Figure 29.

Crosstalk vs Frequency
V_{DD} = 5V, R_L = 8Ω, A_{V-BTL} = 2V/V
P_{OUT} = 1W, 80kHz BW

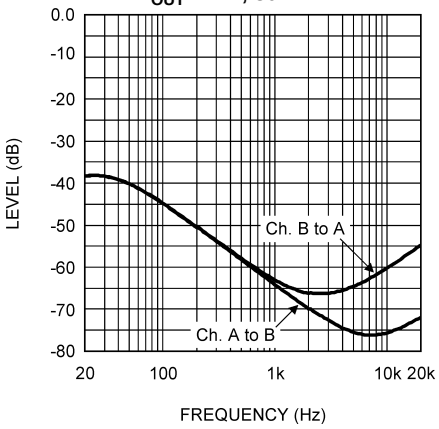


Figure 30.

Crosstalk vs Frequency
V_{DD} = 3V, R_L = 8Ω, A_{V-BTL} = 2V/V
P_{OUT} = 250mW, 80kHz BW

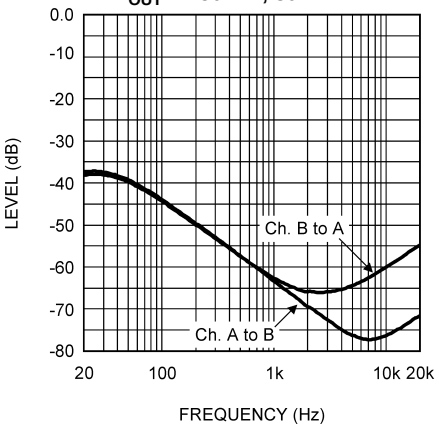


Figure 31.

Crosstalk vs Frequency
V_{DD} = 5V, R_L = 32Ω, A_{V-SE} = 1V/V
P_{OUT} = 40mW, 80kHz BW

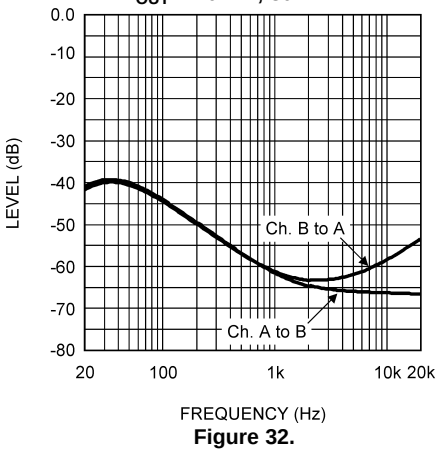


Figure 32.

Crosstalk vs Frequency
V_{DD} = 3V, R_L = 32Ω, A_{V-SE} = 1V/V
P_{OUT} = 20mW, 80kHz BW

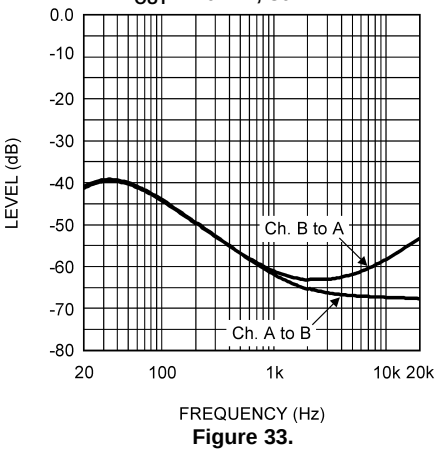


Figure 33.

Typical Performance Characteristics (continued)

Headphone Sense Threshold vs Supply Voltage
R_L = 8Ω, A_{V-SE} = 1V/V
C_{OUT} = 220µF, 80kHz BW

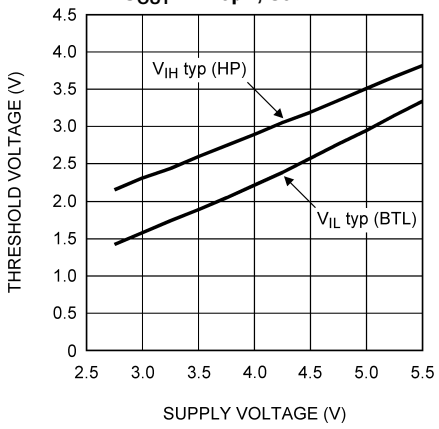


Figure 34.

Output Level vs Frequency
External Gain with Bass Boost

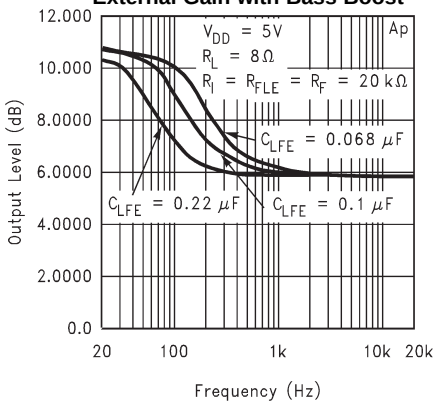


Figure 35.

Output Power/Channel vs Supply Voltage
R_L = 3Ω, A_{V-BTL} = 2V/V, 80kHz BW

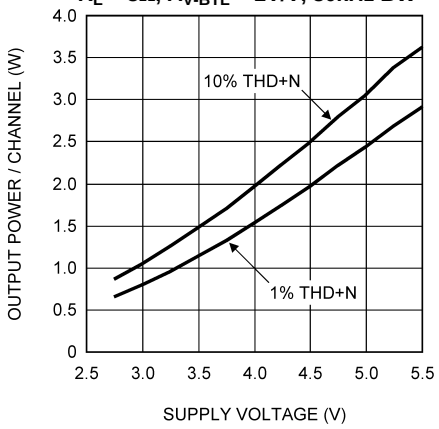


Figure 36.

Output Power/Channel vs Supply Voltage
R_L = 4Ω, A_{V-BTL} = 2V/V, 80kHz BW

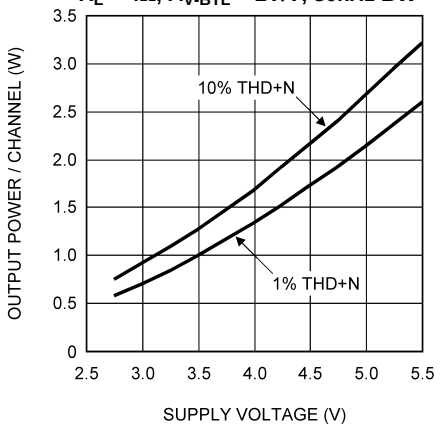


Figure 37.

Output Power/Channel vs Supply Voltage
R_L = 8Ω, A_{V-BTL} = 2V/V, 80kHz BW

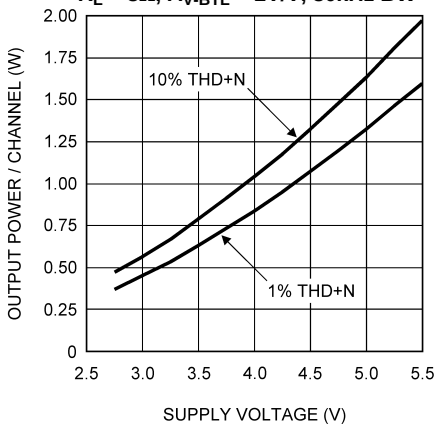


Figure 38.

Output Power/Channel vs Supply Voltage
R_L = 8Ω, A_{V-SE} = 1V/V, 80kHz BW

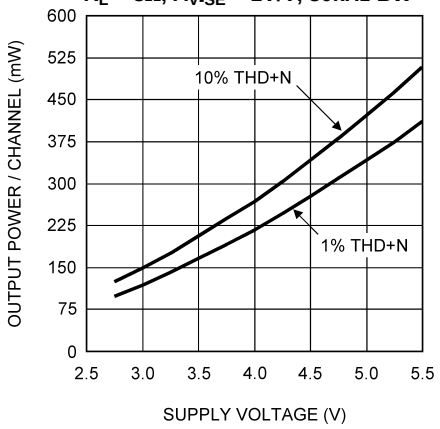


Figure 39.

Typical Performance Characteristics (continued)

Output Power/Channel vs Supply Voltage
R_L = 32Ω, A_{V-SE} = 1V/V, 80kHz BW

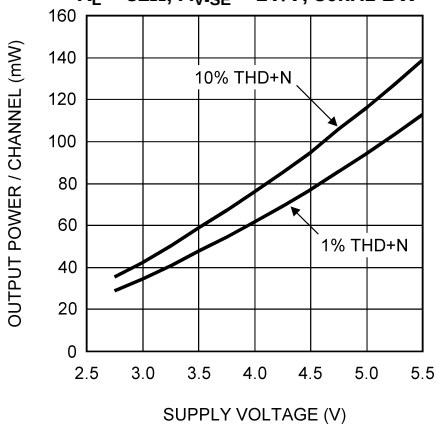
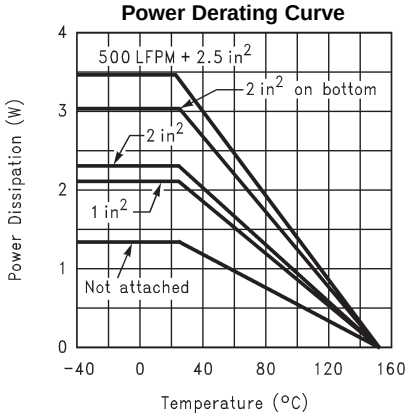


Figure 40.

Power Derating Curve



These curves show the thermal dissipation ability of the LM4936MH at different ambient temperatures given these conditions:
500LFPM + 2in^2: The part is soldered to a 2in^2, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it.
2in^{2}on bottom: The part is soldered to a 2in^2, 1oz. copper plane that is on the bottom side of the PC board through 21 8 mil vias.
2in^2: The part is soldered to a 2in^2, 1oz. copper plane.
1in^2: The part is soldered to a 1in^2, 1oz. copper plane.
Not Attached: The part is not soldered down and is not forced-air cooled.

Figure 41.

Power Dissipation vs Output Power/Channel
V_{DD} = 5V, A_{V-BTL} = 2V/V, THD+N ≤ 1%, 80kHz BW

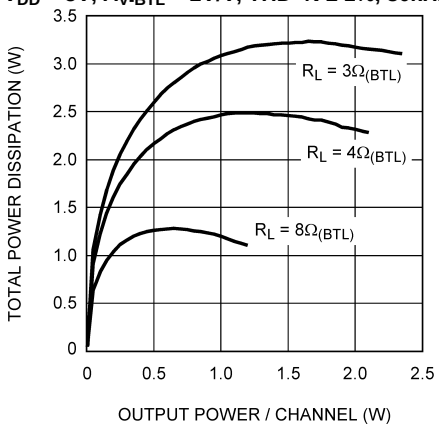


Figure 42.

Power Dissipation vs Output Power/Channel
V_{DD} = 3V, A_{V-BTL} = 2V/V, THD+N ≤ 1%, 80kHz BW

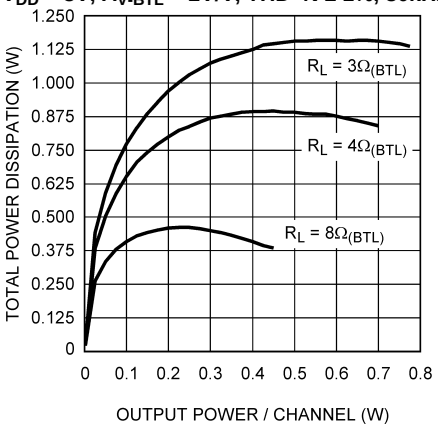


Figure 43.

Typical Performance Characteristics (continued)

Power Dissipation vs Output Power/Channel
V_{DD} = 5V, A_{V-SE} = 1V/V, THD+N ≤ 1%, 80kHz BW

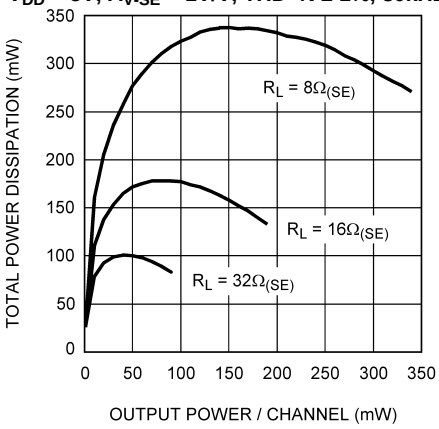


Figure 44.

Power Dissipation vs Output Power/Channel
V_{DD} = 3V, A_{V-SE} = 1V/V, THD+N ≤ 1%, 80kHz BW

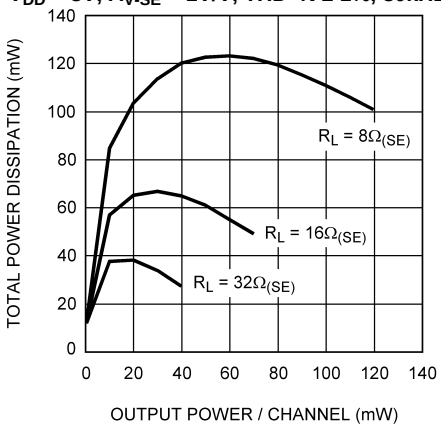


Figure 45.

Supply Current vs Supply Voltage
R_L = 8Ω

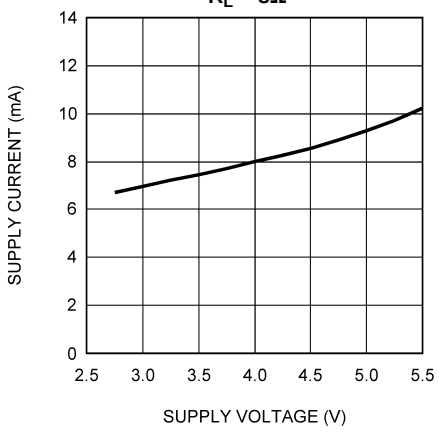


Figure 46.

Dropout Voltage

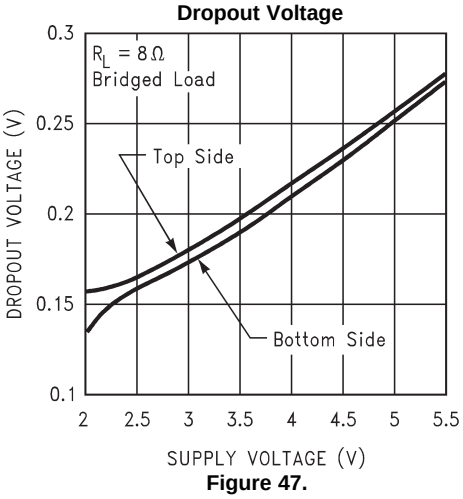


Figure 47.

Output Power/Channel vs Load Resistance

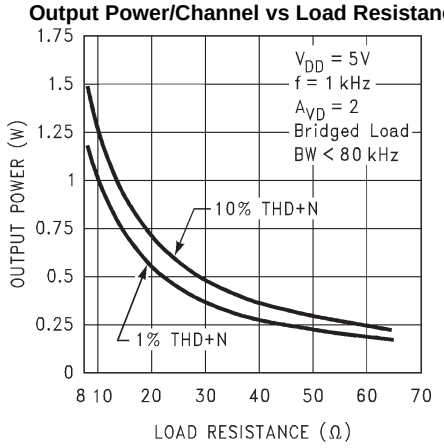


Figure 48.

Output Power/Channel vs Load Resistance

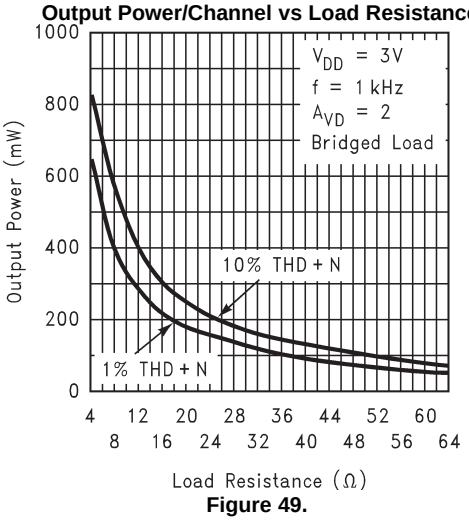


Figure 49.

Typical Performance Characteristics (continued)

Output Power/Channel vs Load Resistance

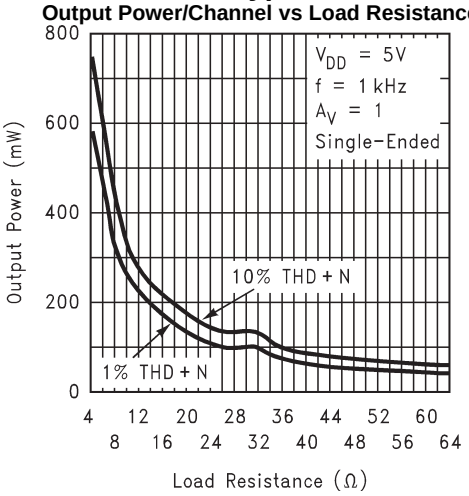


Figure 50.

Output Power/Channel vs Load Resistance

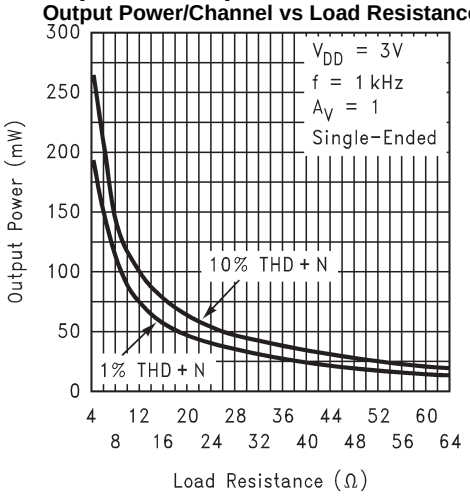


Figure 51.

APPLICATION INFORMATION

I²C COMPATIBLE INTERFACE

The LM4936 uses a serial bus, which conforms to the I²C protocol, to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I²C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4936.

The I²C address for the LM4936 is determined using the ID/CE pin. The LM4936's two possible I²C chip addresses are of the form 110110$X_1$0 (binary), where X_1 = 0, if ID/CE is logic low; and X_1 = 1, if ID/CE is logic high. If the I²C interface is used to address a number of chips in a system, the LM4936's chip address can be changed to avoid any possible address conflicts.

The bus format for the I²C interface is shown in Figure 53. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is high.

After the last bit of the address bit is sent, the master releases the data line high (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4936 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not held low during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4936.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must check for another acknowledge to see if the LM4936 received the data.

If the master has more data bytes to send to the LM4936, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes high while the clock signal is high. The data line should be held high when not in use.

I²C/SPI INTERFACE POWER SUPPLY PIN (I²C/SPI V_{DD})

The LM4936's I²C/SPI interface is powered up through the I²C/SPI V_{DD} pin. The LM4936's I²C/SPI interface operates at a voltage level set by the I²C/SPI V_{DD} pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I²C/SPI interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

HTSSOP PACKAGE PCB MOUNTING CONSIDERATIONS

HTSSOP (die attach paddle) packages provide a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2.1W at ≤ 1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4936's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The packages must have their exposed DAPs soldered to a grounded copper pad on the PCB. The DAP's PCB copper pad is connected to a large grounded plane of continuous unbroken copper. This plane forms a thermal mass heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with vias. The via diameter should be 0.012in–0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4936 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. In systems using cooling fans, the LM4936MH can take advantage of forced air cooling. With an air flow rate of 450 linear-feet per minute and a 2.5in^2 exposed copper or 5.0in^2 inner layer copper plane heatsink, the LM4936MH can continuously drive a 3Ω load to full power. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the LM4936's thermal shutdown protection. The LM4936's power de-rating curve in the Typical Performance Characteristics shows the maximum power dissipation versus temperature. Example PCB layouts are shown in the LM4936 MH HTSSOP Board Artwork section. Further detailed and specific information concerning PCB layout, fabrication, and mounting is available in Texas Instruments' AN1187.

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 3, the LM4936 output stage consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.)

Figure 3 shows that the first amplifier's negative (-) output serves as the second amplifier's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between −OUTA and +OUTA and driven differentially (commonly referred to as “bridge mode”). This results in a differential gain of

$$A_{VD} = 2 * (R_f/R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: **its differential output doubles the voltage swing across the load.** This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the AUDIO POWER AMPLIFIER DESIGN section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended} \tag{2}$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4936 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation 3, assuming a 5V power supply and a 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$$P_{DMAX} = 4 * (V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge Mode} \tag{3}$$

The LM4936's power dissipation is twice that given by Equation 2 or Equation 3 when operating in the single-ended mode or bridge mode, respectively due to stereo operation. Twice the maximum power dissipation point given by Equation 3 must not exceed the power dissipation given by Equation 4:

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \tag{4}$$

The LM4936's T_{JMAX} = 150°C. In the MH package soldered to a DAP pad that expands to a copper area of 2in^2 on a PCB, the LM4936MH's θ_{JA} is 41°C/W. At any given ambient temperature T_A, use Equation 4 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 4 and substituting P_{DMAX} for P_{DMAX}' results in Equation 5. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4936's maximum junction temperature.

$$T_A = T_{JMAX} - 2*P_{DMAX}\,\theta_{JA} \tag{5}$$

For a typical application with a 5V power supply and an 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 45°C for the MH package.

$$T_{JMAX} = P_{DMAX}\,\theta_{JA} + T_A \tag{6}$$

Equation 6 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4936's 150°C T_{JMAX}, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point.

If the result of Equation 3 multiplied by 2 for stereo operation is greater than that of Equation 4, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1µF tantalum bypass capacitance connected between the LM4936's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4936's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and the amplifier's PSRR. The PSRR improvements increase as the BYPASS pin capacitor value increases. Too large a capacitor, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the following section, SELECTING PROPER EXTERNAL COMPONENTS), system cost, and size constraints.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4936's performance requires properly selecting external components. Though the LM4936 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4936 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain circuits demand input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the AUDIO POWER AMPLIFIER DESIGN section for more information on selecting the proper gain.

INPUT CAPACITOR VALUE SELECTION

Amplifying the lowest audio frequencies requires a high value input coupling capacitor (0.33µF in Figure 3), but high value capacitors can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. Applications using speakers with this limited frequency response reap little improvement by using a large input capacitor.

Besides affecting system cost and size, the input coupling capacitor has an effect on the LM4936's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage ($V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_f. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −6dB frequency.

As shown in Figure 3, the input resistor (R_{IR}, R_{IL} = 20kΩ) and the input capacitor (C_{IR}, C_{IL} = 0.33µF) produce a −6dB high pass filter cutoff frequency that is found using Equation 7.

$$f_{-6\,dB} = \frac{1}{2\pi R_{IN} C_I} \tag{7}$$

As an example when using a speaker with a low frequency limit of 150Hz, the input coupling capacitor, using Equation 7, is 0.053µF. The 0.33µF input coupling capacitor shown in Figure 3 allows the LM4936 to drive a high efficiency, full range speaker whose response extends below 30Hz.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4936 contains circuitry that minimizes turn-on and shutdown transients or “clicks and pops”. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4936's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the BYPASS pin reaches 1/2 V_{DD} . As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C_B alters the device's turn-on time and the magnitude of “clicks and pops”. Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of C_B and the turn-on time. Below are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.01µF	2ms
0.1µF	20ms
0.22µF	44ms
0.47µF	94ms
1.0µF	200ms

DOCKING STATION INTERFACE

Applications such as notebook computers can take advantage of a docking station to connect to external devices such as monitors or audio/visual equipment that sends or receives line level signals. The LM4936 has two outputs, Right Dock and Left Dock, which connect to outputs of the internal input amplifiers that drive the volume control inputs. These input amplifiers can drive loads of >1kΩ (such as powered speakers) with a rail-to-rail signal. Since the output signal present on the RIGHT DOCK and LEFT DOCK pins is biased to $V_{DD}/2$, coupling capacitors should be connected in series with the load when using these outputs. Typical values for the output coupling capacitors are 0.33µF to 1.0µF. If polarized coupling capacitors are used, connect their "+" terminals to the respective output pin, see Figure 3.

Since the DOCK outputs precede the internal volume control, the signal amplitude will be equal to the input signal's magnitude and cannot be adjusted. However, the input amplifier's closed-loop gain can be adjusted using external resistors. These 20kΩ (R_{DOCK1}, R_{DOCK2}) are shown in Figure 3 and they set each input amplifier's gain to -1. Use Equation 8 to determine the input and feedback resistor values for a desired gain.

$$- A_{VR} = R_{DOCK1}/R_{IN1} \text{ and } - A_{VL} = R_{DOCK2}/R_{IN2} \quad (8)$$

Adjusting the input amplifier's gain sets the minimum gain for that channel. Although the single ended output of the Bridge Output Amplifiers can be used to drive line level outputs, it is recommended that the R & L Dock Outputs simpler signal path be used for better performance.

BEEP DETECT FUNCTION

Computers and notebooks produce a system “beep“ signal that drives a small speaker. The speaker's auditory output signifies that the system requires user attention or input. To accommodate this system alert signal, the LM4936's beep input pin is a mono input that accepts the beep signal. Internal level detection circuitry at this input monitors the beep signal's magnitude. When a signal level greater than $V_{DD}/2$ is detected on the BEEP IN pin, the bridge output amplifiers are enabled. The beep signal is amplified and applied to the load connected to the output amplifiers. A valid beep signal will be applied to the load even when MUTE is active. Use the input resistors connected between the BEEP IN pin and the stereo input pins to accommodate different beep signal amplitudes. These resistors (R_{BEEP}) are shown as 200kΩ values in Figure 3. Use higher value resistors to reduce the gain applied to the beep signal. The resistors must be used to pass the beep signal to the stereo inputs. The BEEP IN pin is used only to detect the beep signal's magnitude: it does not pass the signal to the output amplifiers. The LM4936's shutdown mode must be deactivated before a system alert signal is applied to BEEP IN pin.

MICRO-POWER SHUTDOWN

Shutdown mode is activated when a digital 0 is loaded into the Shutdown bit, B0. When active, the LM4936's micro-power shutdown feature turns off the amplifier's bias circuitry reducing supply current to a typical 0.7µA. Loading a digital 1 into B0 disables shutdown mode. When the LM4936 has power applied, all register bits will have a default value of 0. Because of this, the LM4936 will be in shutdown mode when power is applied.

MODE FUNCTION

The LM4936's Mode function has two states controlled by bit B2. A digital 0 in bit B2 disables the volume control and forces the LM4936 to function as a fixed gain amplifier. The gain selection is determined by the GAIN SEL bit (B3) While in the fixed gain mode the volume setting has no effect on the output. When a digital 1 is loaded into B2 the output level is determined by the volume control bits. See Table 4 for volume settings.

MUTE FUNCTION

The LM4936 mutes the amplifier and DOCK outputs when a digital 1 is loaded in bit B1. Even while muted, the LM4936 will amplify a system alert (beep) signal whose magnitude satisfies the BEEP DETECT circuitry. Loading a digital 0 into B1 returns the LM4936 to normal operation.

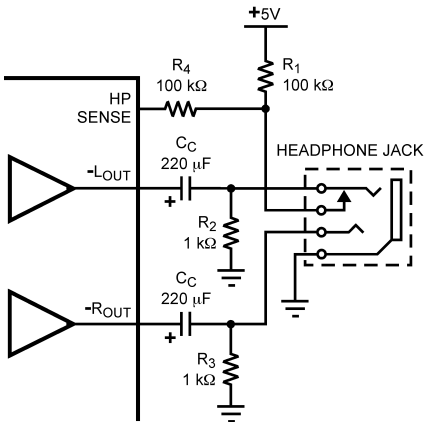


Figure 52. Headphone Sensing Circuit

HP SENSE FUNCTION (Headphone In)

Applying a voltage between the V_{IH} threshold shown in the graph found in the Typical Performance Characteristics and V_{DD} to the LM4936's HP SENSE control pin or loading a digital 1 into the HP Control bit (B4) will change the output mode. The '+' outputs will change to be in phase with the '-' outputs instead of 180 degrees out of phase. This action mutes a bridged-connected load since the differential voltage across the load is now close to 0V. The HP SENSE pin over rides the HP Control bit. See Table 2 for more info. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 52 shows the implementation of the LM4936's headphone control function. With no headphones connected to the headphone jack, the R1-R2 voltage divider sets the voltage applied to the HP SENSE pin at approximately 50mV. This 50mV puts the LM4936 into bridged mode operation. The output coupling capacitor blocks the amplifier's half supply DC voltage, protecting the headphones.

The HP SENSE threshold is set so the output signal cannot cause an output mode change. While the LM4936 operates in bridge mode, the DC potential across the load is essentially 0V. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from R2 and allows R1 to pull the HP SENSE pin up to V_{DD} through R4. This enables the headphone function and mutes the bridged speaker. The single-ended '-' outputs then drive the headphones, whose impedance is in parallel with resistors R2 and R3. These resistors have negligible effect on the LM4936's output drive capability since the typical impedance of headphones is 32Ω.

Figure 52 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three-wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP-IN pin when connecting headphones.

GAIN SELECT FUNCTION (Bass Boost)

The LM4936 features selectable gain, using either internal or external feedback resistors. The GAIN SEL bit (B3) controls which gain is selected. Loading a digital 0 into the GAIN SEL bit sets the gain to internal resulting in a gain of 6dB for BTL mode or unity for singled-ended mode. Loading a digital 1 into the GAIN SEL bit sets the gain to be determined by the external resistors, R_I and R_F.

In some cases a designer may want to improve the low frequency response of the bridged amplifier or incorporate a bass boost feature. This bass boost can be useful in systems where speakers are housed in small enclosures. A resistor, R_{BS}, and a capacitor, C_{BS}, in parallel, can be placed in series with the feedback resistor of the bridged amplifier as seen in Figure 3.

At low, frequencies C_{BS} is a virtual open circuit and at high frequencies, its nearly zero ohm impedance shorts R_{BS}. The result is increased bridge-amplifier gain at low frequencies. The combination of R_{BS} and C_{BS} form a -6dB corner frequency at

$$f_C = 1/(2\pi R_{BS} C_{BS}) \quad (9)$$

The bridged-amplifier low frequency differential gain is:

$$A_{VD} = 2(R_F + R_{BS}) / R_i \quad (10)$$

Using the component values shown in Figure 3 (R_F = 20kΩ, R_{BS} = 20kΩ, and C_{BS} = 0.068µF), a first-order, -6dB pole is created at 120Hz. Assuming R_i = 20kΩ, the low frequency differential gain is 4V/V or 12dB. The input (C_i) and output (C_{OUT}) capacitor values must be selected for a low frequency response that covers the range of frequencies affected by the desired bass-boost operation.

VOLUME CONTROL

The LM4936 has an internal stereo volume control whose setting is a function of the digital values in the V4 – V0 bits. See Table 4.

The LM4936 volume control consists of 31 steps that are individually selected. The range of the steps, are from 0dB - 78dB. The gain levels are 1dB/step from 0dB to -6dB, 2dB/step from -6dB to -36dB, 3dB/step from -36dB to -47dB, 4dB/step from -47dB to -51dB, 5dB/step from -51dB to -66dB, and 12dB to the last step at -78dB.

Table 4. Volume Control Table

Serial Number	V4	V3	V2	V1	V0	Gain (dB)
0	0	0	0	0	0	–90
1	0	0	0	0	1	–90
2	0	0	0	1	0	–68
3	0	0	0	1	1	–63
4	0	0	1	0	0	–57
5	0	0	1	0	1	–51
6	0	0	1	1	0	–47
7	0	0	1	1	1	–45
8	0	1	0	0	0	–42
9	0	1	0	0	1	–39
10	0	1	0	1	0	–36
11	0	1	0	1	1	–34
12	0	1	1	0	0	–32
13	0	1	1	0	1	–30
14	0	1	1	1	0	–28
15	0	1	1	1	1	–26
16	1	0	0	0	0	–24
17	1	0	0	0	1	–22
18	1	0	0	1	0	–20
19	1	0	0	1	1	–18
20	1	0	1	0	0	–16
21	1	0	1	0	1	–14
22	1	0	1	1	0	–12
23	1	0	1	1	1	–10
24	1	1	0	0	0	–8
25	1	1	0	0	1	–6
26	1	1	0	1	0	–5
27	1	1	0	1	1	–4
28	1	1	1	0	0	–3
29	1	1	1	0	1	–2
30	1	1	1	1	0	–1
31	1	1	1	1	1	0

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	1 W_{RMS}
Load Impedance:	8Ω
Input Level:	1 V_{RMS}
Input Impedance:	20 kΩ
Bandwidth:	100 Hz−20 kHz ± 0.25 dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the Typical Performance Characteristics section. Another way, using Equation 10, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the Typical Performance Characteristics curves, must be added to the result obtained by Equation 10. The result is Equation 11.

$$V_{outpeak} = \sqrt{(2R_L P_O)} \quad (11)$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (12)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4936 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the POWER DISSIPATION section.

After satisfying the LM4936's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation 12.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (13)$$

Thus, a minimum overall gain of 2.83 allows the LM4936's to reach full output swing and maintain low noise and THD+N performance.

The last step in this design example is setting the amplifier's −6dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \quad (14)$$

and an

$$f_H = 20kHz \times 5 = 100kHz \quad (15)$$

As mentioned in the SELECTING PROPER EXTERNAL COMPONENTS section, R_i (Right & Left) and C_i (Right & Left) create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the input coupling capacitor's value using Equation 14.

$$C_i \geq 1/(2\pi R_i f_L) \quad (16)$$

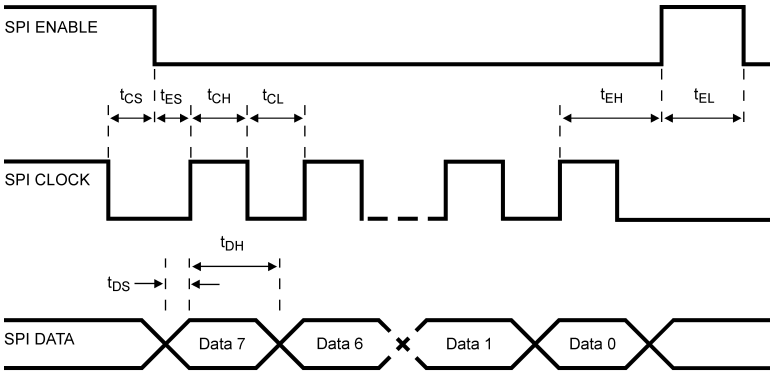
The result is

$$1/(2\pi * 20k\Omega * 20Hz) = 0.397\mu F \quad (17)$$

Use a 0.39µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain A_{VD}, determines the upper passband response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4936's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance,restricting bandwidth limitations.

SPI TIMING DIAGRAM



SPI OPERATIONAL REQUIREMENTS

1. The maximum clock rate is 5MHz for the CLK pin.
2. CLK must remain logic-high for at least 100ns (t_{CH}) after the rising edge of CLK, and CLK must remain logic-low for at least 100ns (t_{CL}) after the falling edge of CLK.
3. Data bits are written to the DATA pin with the most significant bit (MSB) first.
4. The serial data bits are sampled at the rising edge of CLK. Any transition on DATA must occur at least 50ns (t_{DS}) before the rising edge of CLK. Also, any transition on DATA must occur at least 50ns (t_{DH}) after the rising edge of CLK and stabilize before the next rising edge of CLK.
5. ENABLE should be logic-low only during serial data transmission.
6. ENABLE must be logic-low at least 50ns (t_{ES}) before the first rising edge of CLK, and ENABLE has to remain logic-low at least 50ns (t_{EH}) after the eighth rising edge of CLK.
7. If ENABLE remains logic-high for more than 50ns before all 8 bits are transmitted then the data latch will be aborted.
8. If ENABLE is logic-low for more than 8 CLK pulses then only the first 8 data bits will be latched and activated at rising edge of eighth CLK.
9. ENABLE must remain logic-high for at least 50ns (t_{EL}).
10. Coincidental rising or falling edges of CLK and ENABLE are not allowed. If CLK is to be held logic-high after the data transmission, the falling edge of CLK must occur at least 50ns (t_{CS}) before ENABLE transitions to logic-low for the next set of data.

I²C TIMING DIAGRAMS

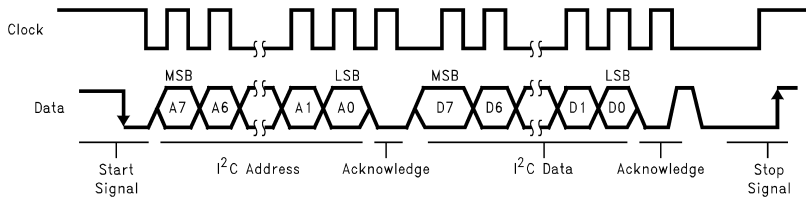


Figure 53. I²C Bus Format

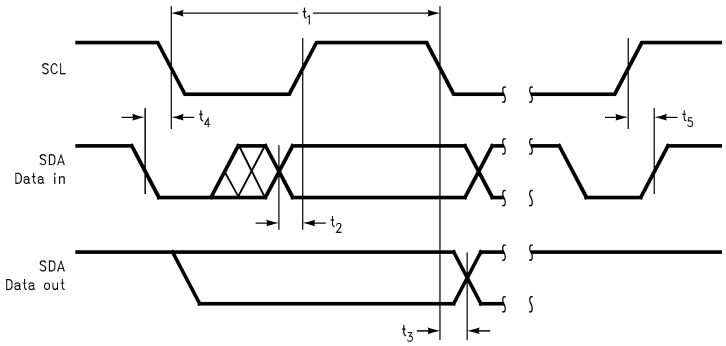
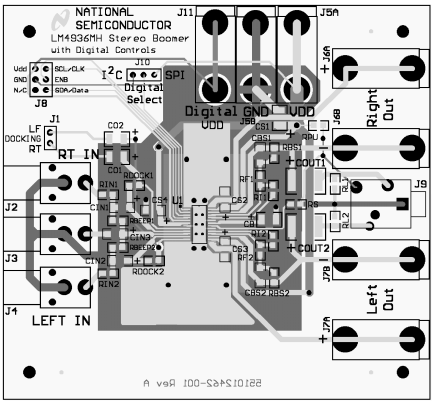


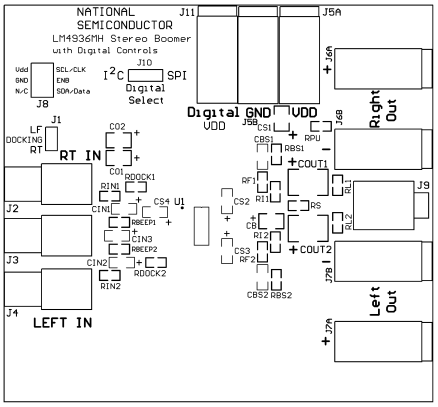
Figure 54. I²C Timing Diagram

LM4936 MH HTSSOP Board Artwork(1)(2)

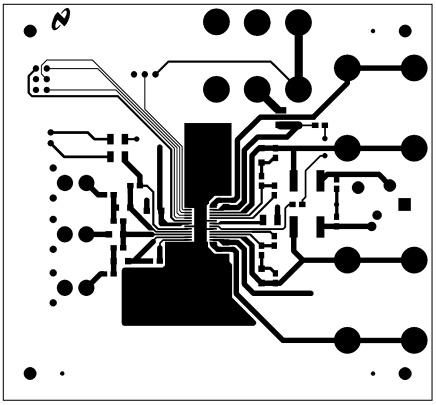
Composite View



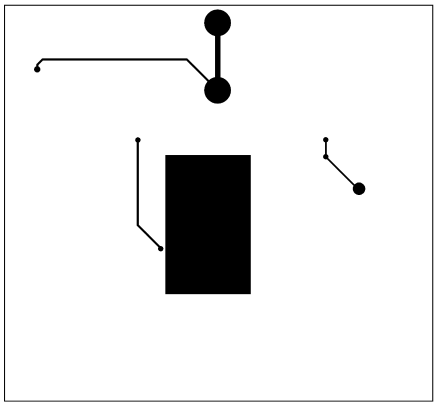
Silk Screen



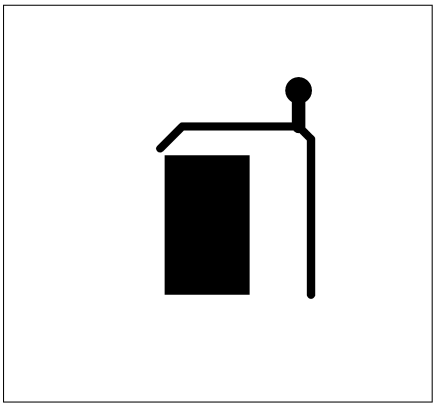
Top Layer



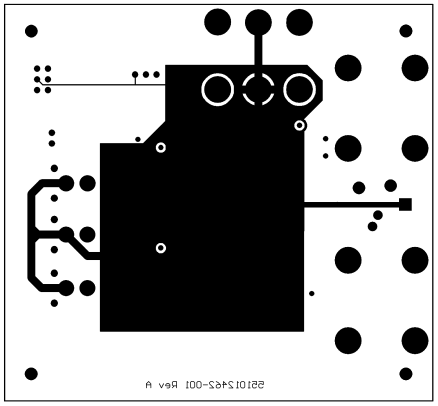
Internal Layer 1



Internal Layer 2



Bottom Layer



(1) When driving 3Ω loads from a 5V supply the LM4936MH must be mounted to the circuit board and forced-air cooled. The demo board shown in the datasheet has planes for heat sinking. The top layer plane is 1.05 in^2 (675mm^2), the inner two layers each have a 1.03 in^2 (667mm^2) plane and the bottom layer has a 3.32 in^2 (2143mm^2) plane. The planes are electrically GND and interconnected through six 15 mil vias directly under the package and eight 28 mil vias in various locations.

(2) When driving 4Ω loads from a 5V supply the LM4936MH must be mounted to the circuit board. The demo board shown in the datasheet has planes for heat sinking. The top layer plane is 1.05 in^2 (675mm^2), the inner two layers each have a 1.03 in^2 (667mm^2) plane and the bottom layer has a 3.32 in^2 (2143mm^2) plane. The planes are electrically GND and interconnected through six 15 mil vias directly under the package and eight 28 mil vias in various locations.

Table 5. LM4936 Board Bill of Materials

Designator	Value	Tolerance	Part Description	Comment
R_{IN1}, R_{IN2}	20kΩ	1%	1/10W, 0805 Resistor	
R_{I1}, R_{I2}	20kΩ	1%	1/10W, 0805 Resistor	
R_{F1}, R_{F2}	20kΩ	1%	1/10W, 0805 Resistor	
R_{DOCK1}, R_{DOCK2}	20kΩ	1%	1/10W, 0805 Resistor	
R_{BS1}, R_{BS2}	20kΩ	1%	1/10W, 0805 Resistor	
R_{BEEP1}, R_{BEEP2}	200kΩ	1%	1/10W, 0805 Resistor	
R_{L1}, R_{L2}	1.5kΩ	1%	1/10W, 0805 Resistor	
R_S, R_{PU}	100kΩ	1%	1/10W, 0805 Resistor	
C_{IN1}, C_{IN2}, C_{IN3}	0.33µF	10%	10V, Ceramic 1206 Capacitor	
C_{BS1}, C_{BS2}	0.068µF	10%	10V, Ceramic 1206 Capacitor	
C_{S1}	10µF	10%	10V, Tantalum 1210 Capacitor	
C_{S2}, C_{S3}, C_{S4}	0.1µF	10%	10V, Tantalum 1206 Capacitor	
C_{O1}, C_{O2}	1µF	10%	10V, Electrolytic 1210 Capacitor	
C_B	1µF	10%	10V, Tantalum 1210 Capacitor	
C_{OUT1}, C_{OUT2}	220µF	10%	16V, Electrolytic 2220 Capacitor	
J_1			0.100 1x2 header, vertical mount	Docking Outputs
J_2, J_3, J_4			RCA Input Jack, PCB Mount	Mouser: 16PJ097
J_{5A}			Banana-Jack Red, Analog V_{DD}	Mouser: 164–6219
J_{5B}			Banana-Jack Blck, GND	Mouser: 164–6218
J_{6A}			Banana-Jack Red, Right Out +	Mouser: 164–6219
J_{6B}			Banana-Jack Black, Right Out -	Mouser: 164–6218
J_{7A}			Banana-Jack Red, Left Out +	Mouser: 164–6219
J_{7B}			Banana-Jack Black, Left Out -	Mouser: 164–6218
J_8			0.100” 2x3 header, vertical mount	I^2C/SPI Inputs
J_9			3.5mm Stereo Headphone Jack	Shogyo: SJS–0354–5P
J_{10}			0.100” 1x3 header, vertical mount	Digital Select
J_{11}			Banana Jack — Red, Digital V_{DD}	Mouser: 164–6219

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	29

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4936MH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM4936MH	Samples
LM4936MHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM4936MH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

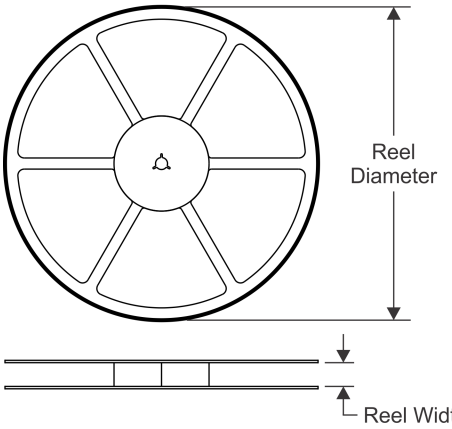
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

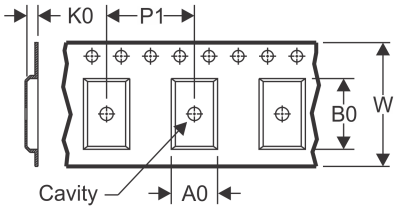
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

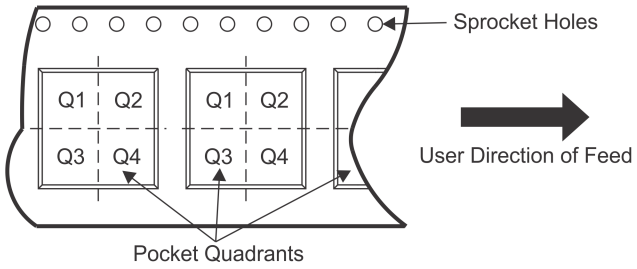


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

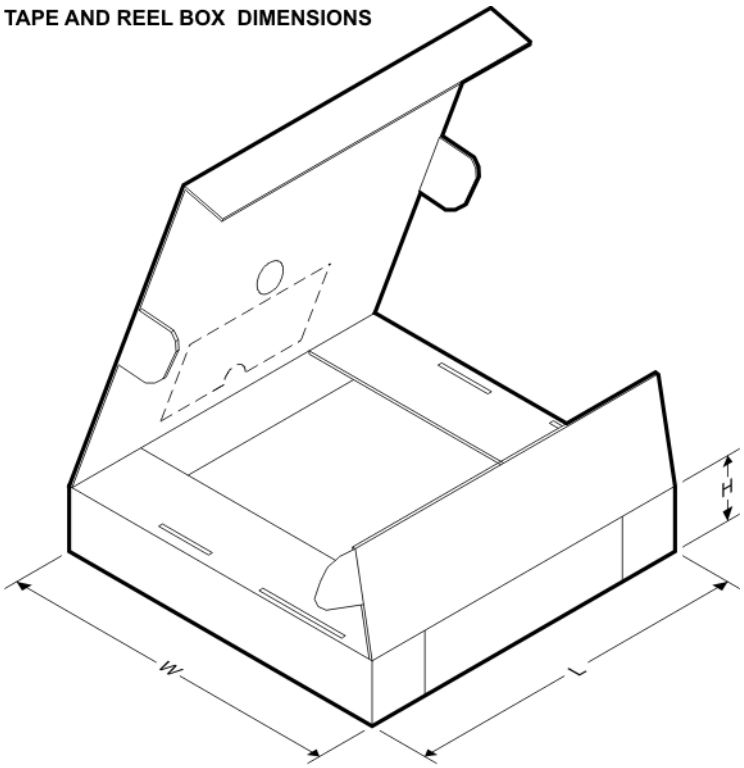
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4936MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

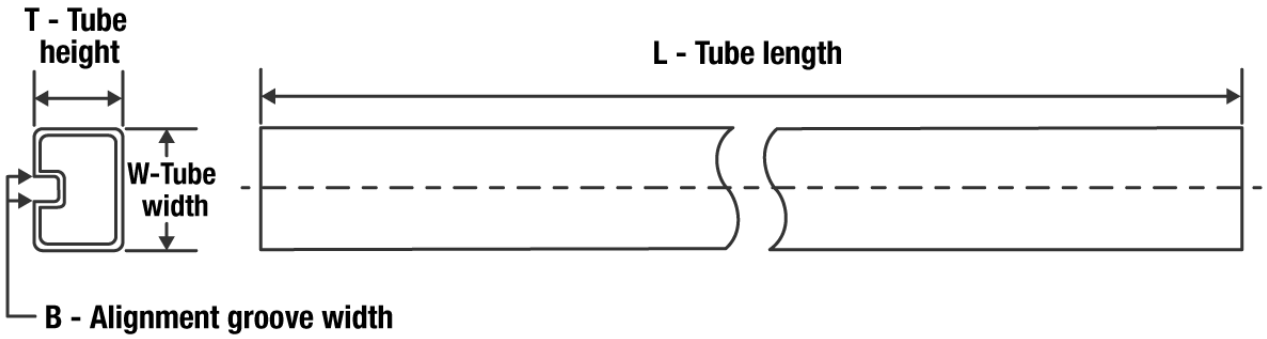
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4936MHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

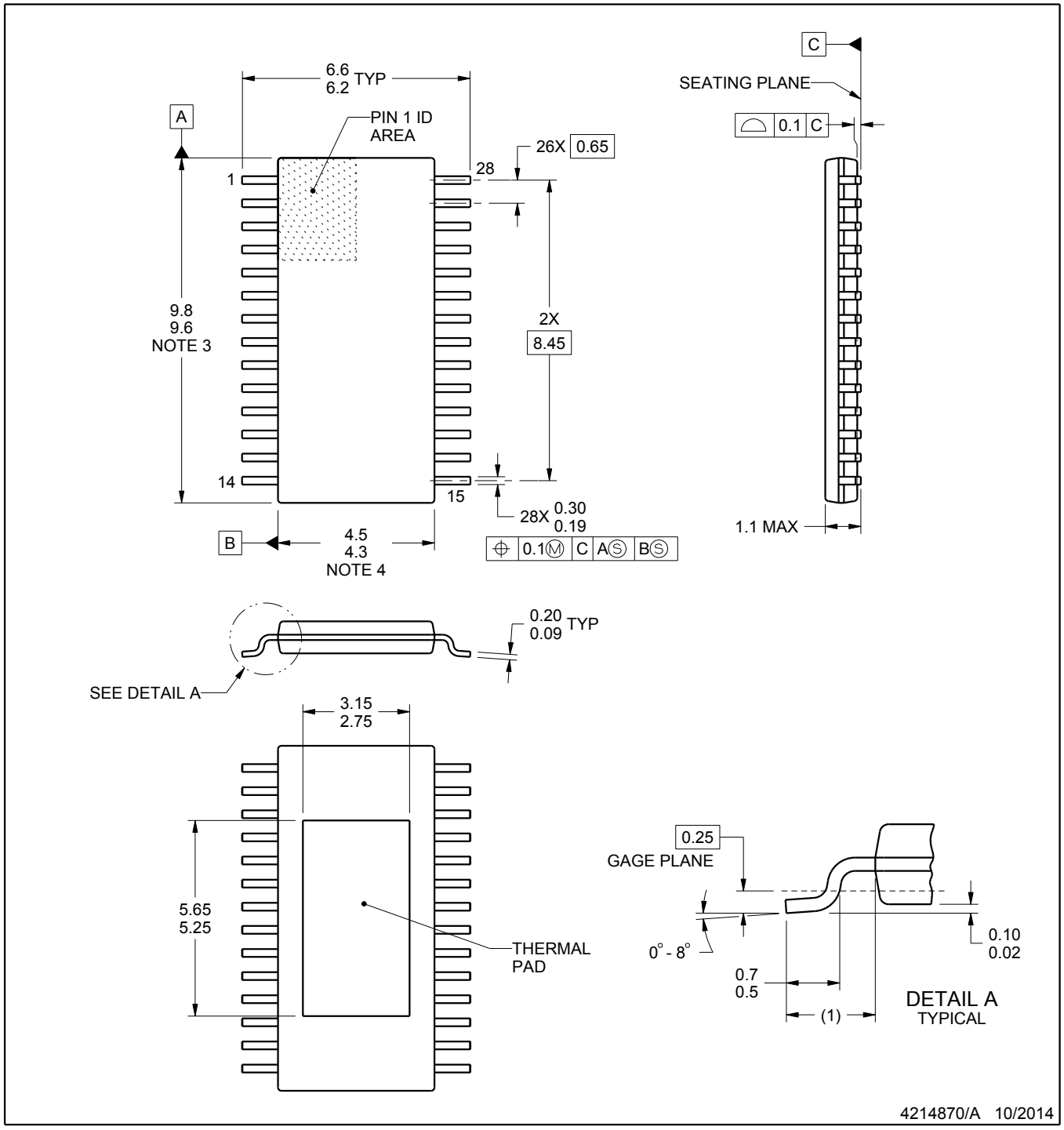
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4936MH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06

PACKAGE OUTLINE

PWP0028A

PowerPAD™ - 1.1 mm max height

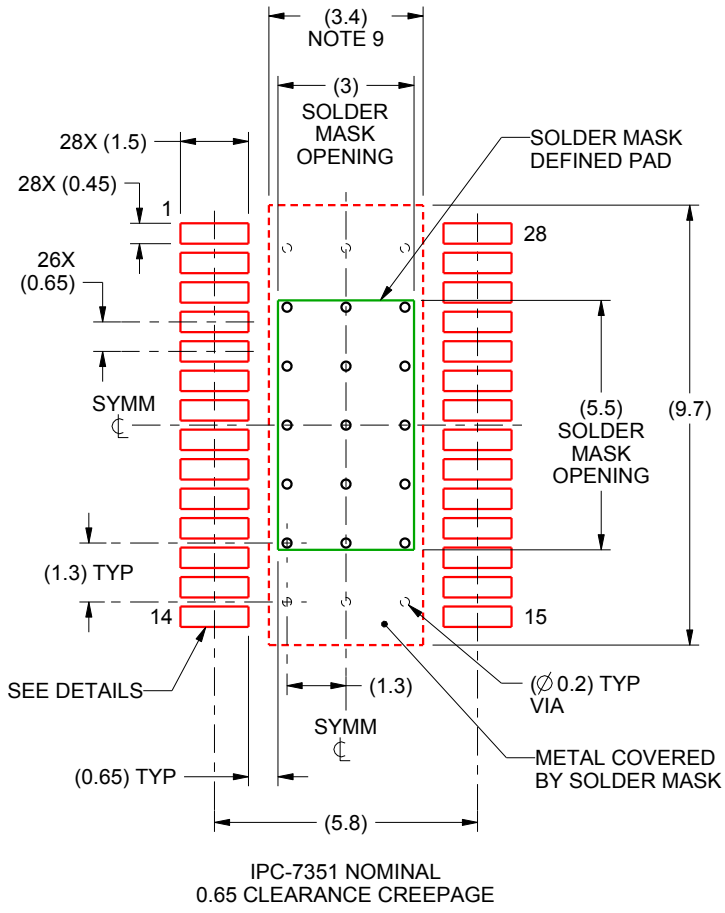
PLASTIC SMALL OUTLINE



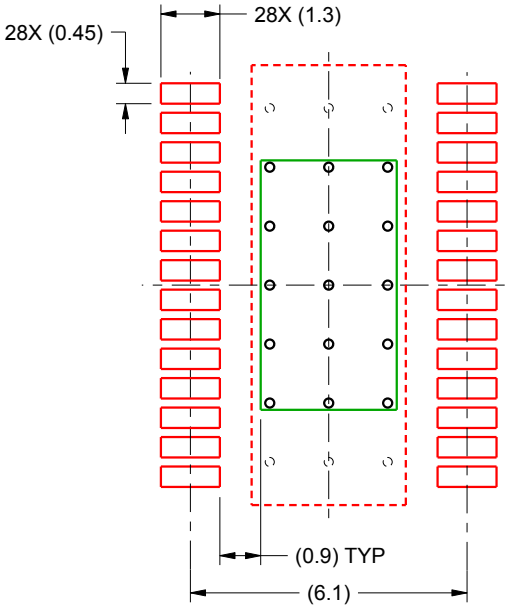
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

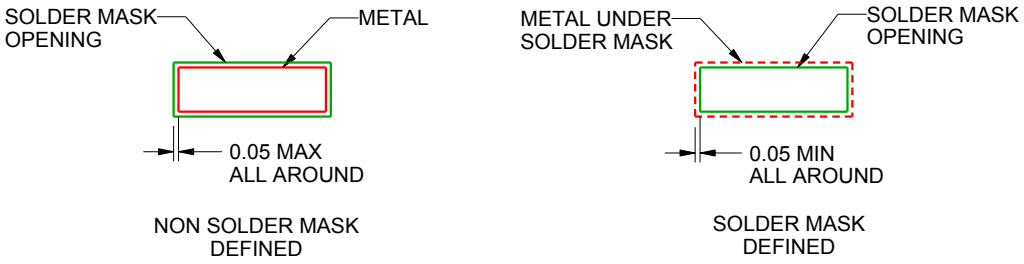


IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

LAND PATTERN EXAMPLE
SCALE:6X

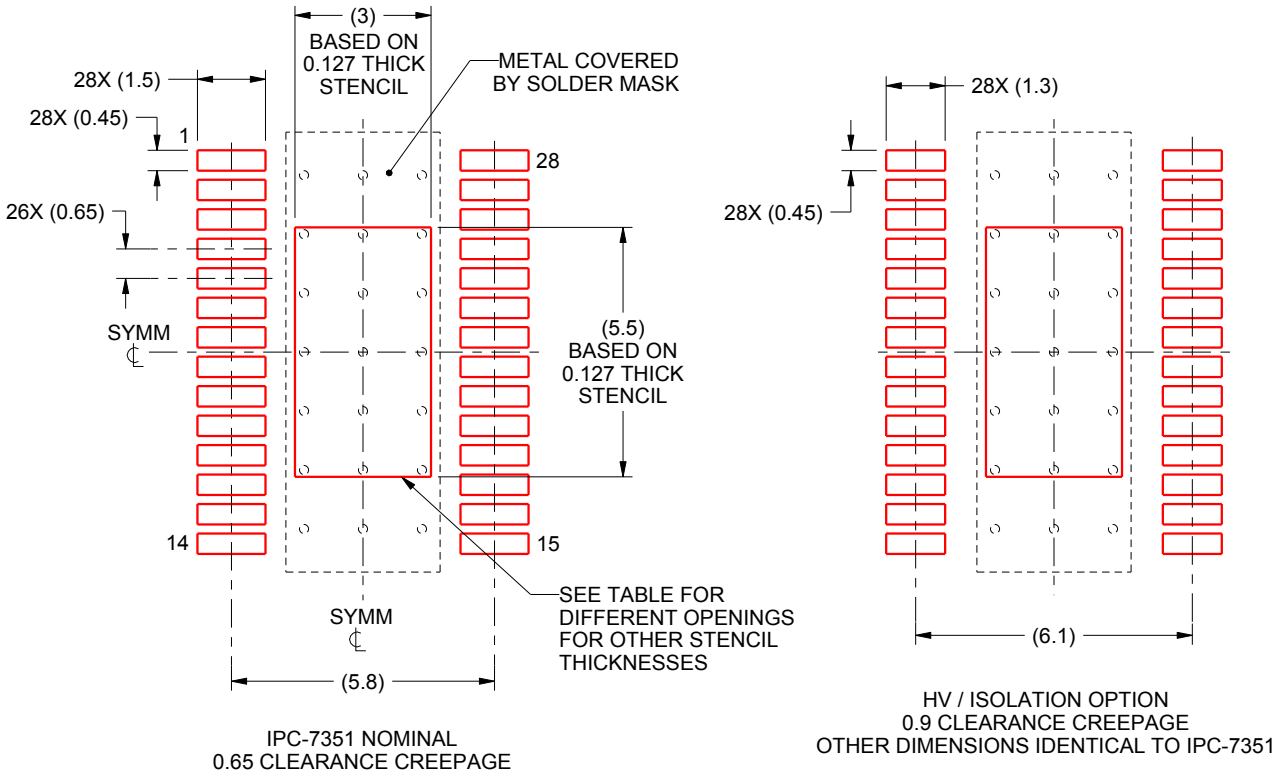


SOLDER MASK DETAILS

4214870/A 10/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

4214870/A 10/2014

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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