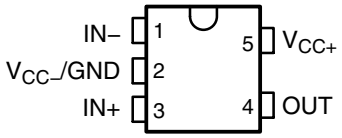
- **Low-Voltage and Single-Supply Operation V_{CC} = 2 V to 7 V**
- **Common-Mode Voltage Range Includes Ground**
- **Fast Response Time . . . 0.7 μs Typ**
- **Low Supply Current . . . 80 μA Typ and 150 μA Max**
- **Fully Specified at 3-V and 5-V Supply Voltages**

DBV PACKAGE
(TOP VIEW)



description/ordering informaton

The TLV1391 is a differential comparator built using a Texas Instruments low-voltage, high-speed bipolar process. These devices have been developed specifically for low-voltage, single-supply applications. Their enhanced performance makes them excellent replacements for the LM393 in the improved 3-V and 5-V system designs.

The TLV1391, with its typical supply current of only 80 μA, is ideal for low-power systems. Response time also has been improved to 0.7 μs.

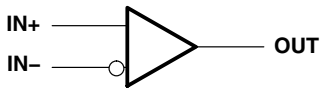
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–0°C to 70°C	SOT-23-5 (DBV)	Reel of 3000	TLV1391CDBVR	Y3D_
		Reel of 250	TLV1391CDBVT	
–40°C to 85°C	SOT-23-5 (DBV)	Reel of 3000	TLV1391IDBVR	Y3E_
		Reel of 250	TLV1391IDBVT	

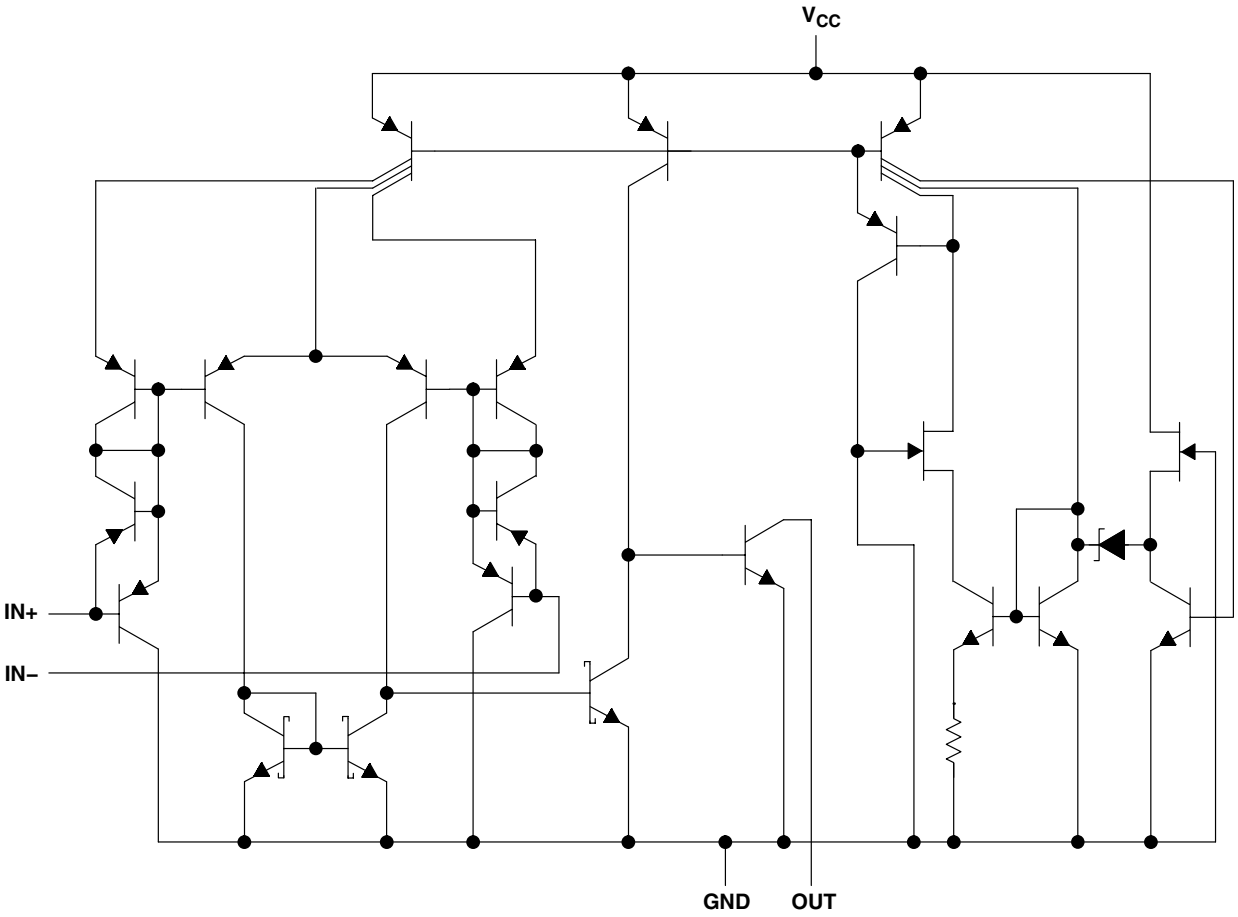
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ The actual top-side marking has one additional character that designates the wafer fab/assembly site.

symbol (each comparator)



equivalent schematic



COMPONENT COUNT	
Transistors	26
Resistors	1
Diodes	4
Epi-FET	1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±7 V
Input voltage range, V_I (any input) . . . . . –0.3 V to V_{CC}
Output voltage, V_O . . . . . 7 V
Output current, I_O (each output) . . . . . 20 mA
Duration of short-circuit current to GND (see Note 3) . . . . . Unlimited
Package thermal impedance, θ_{JA} (see Note 4 and 5) . . . . . 206°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network GND.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. Short circuits from the outputs to V_{CC} can cause excessive heating and eventual destruction of the chip.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	7	V
T_A	Operating free-air temperature	TLV1391C	0	70	°C
		TLV1391I	–40	85	

electrical characteristics, V_{CC} = 3 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, $V_{IC} = V_{ICR}$(min)	25°C		1.5	5	mV
			Full range			9	
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{CC}–1.5	0 to V_{CC}–1.2		V
			Full range	0 to V_{CC}–2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 500 µA	Full range		120	300	mV
I_{IO}	Input offset current	V_O = 1.4 V	25°C		5	50	nA
			Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		–40	–250	nA
			Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V, V_{OH} = 5 V	Full range			100	
I_{OL}	Low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	25°C	500			µA
$I_{CC(H)}$	High-level supply current	$V_O = V_{OH}$	25°C		80	125	µA
			Full range			150	
$I_{CC(L)}$	Low-level supply current	$V_O = V_{OL}$	25°C		80	125	µA
			Full range			150	

switching characteristics, V_{CC} = 3 V, C_L = 15 pF†, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	100-mV input step with 5-mV overdrive,	R_L = 5.1 kΩ	0.7	µs

† C_L includes the probe and jig capacitance.

electrical characteristics, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, $V_{IC} = V_{ICR}$(min)	25°C		1.5	5	mV
			Full range			9	
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{CC}–1.5	0 to V_{CC}–1.2		V
			Full range	0 to V_{CC}–2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 500 µA	Full range		120	300	mV
I_{IO}	Input offset current	V_O = 1.4 V	25°C		5	50	nA
			Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		–40	–250	nA
			Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V, V_{OH} = 5 V	Full range			100	
I_{OL}	Low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	25°C	600			µA
$I_{CC(H)}$	High-level supply current	$V_O = V_{OH}$	25°C		100	150	µA
			Full range			175	
$I_{CC(L)}$	Low-level supply current	$V_O = V_{OL}$	25°C		100	150	µA
			Full range			175	

switching characteristics, V_{CC} = 5 V, C_L = 15 pF†, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	100-mV input step with 5-mV overdrive,	R_L = 5.1 kΩ	0.65	µs
	TTL-level input step,	R_L = 5.1 kΩ	0.18	

† C_L includes the probe and jig capacitance.

TYPICAL CHARACTERISTICS

LOW-TO HIGH-LEVEL OUTPUT
RESPONSE FOR VARIOUS INPUT OVERDRIVES

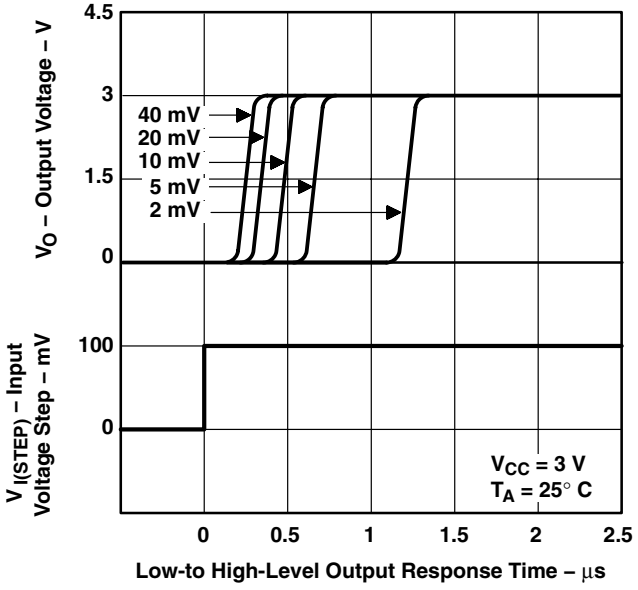


Figure 1

HIGH-TO LOW-LEVEL OUTPUT
RESPONSE FOR VARIOUS INPUT OVERDRIVES

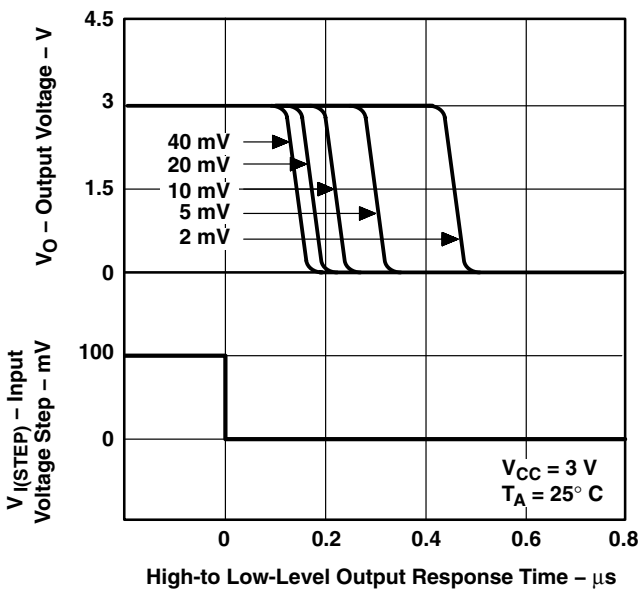


Figure 2

LOW-TO HIGH-LEVEL OUTPUT
RESPONSE FOR VARIOUS INPUT OVERDRIVES

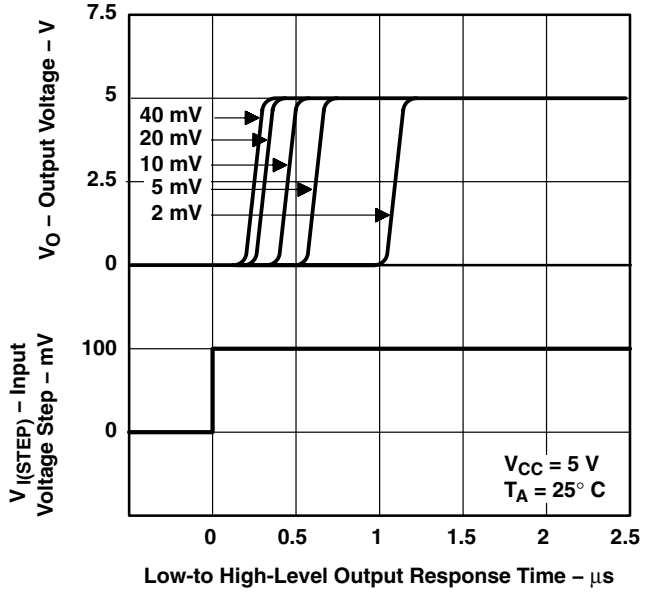


Figure 3

HIGH-TO LOW-LEVEL OUTPUT
RESPONSE FOR VARIOUS INPUT OVERDRIVES

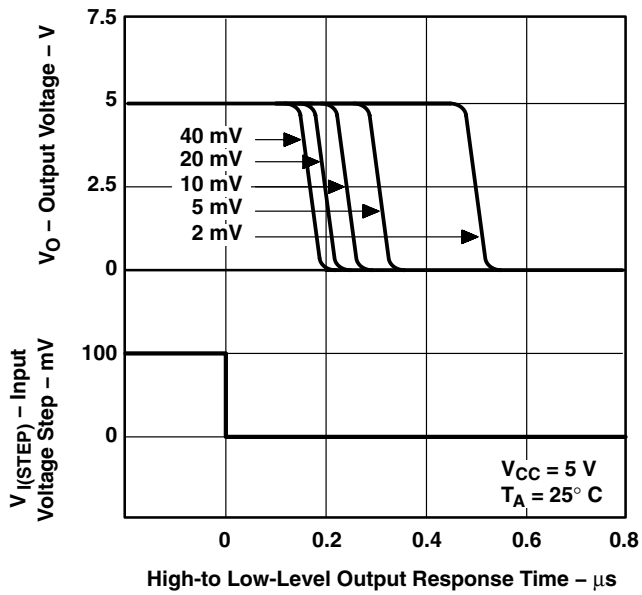


Figure 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1391CDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3D6, Y3DG, Y3DJ)	Samples
TLV1391CDBVRG4	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	0 to 70	Y3DG	
TLV1391IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3E6, Y3EB, Y3EJ)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

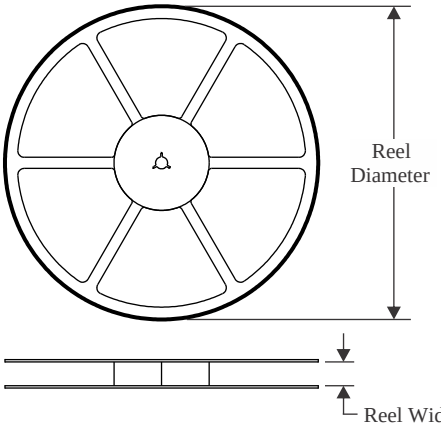
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

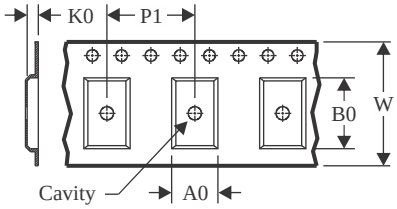
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

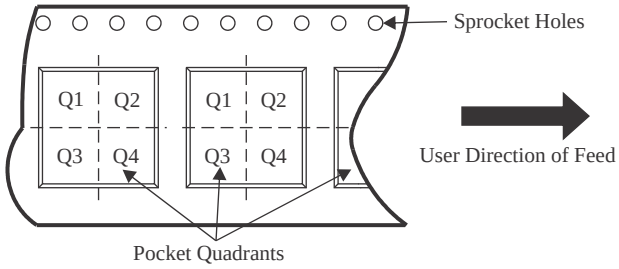


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

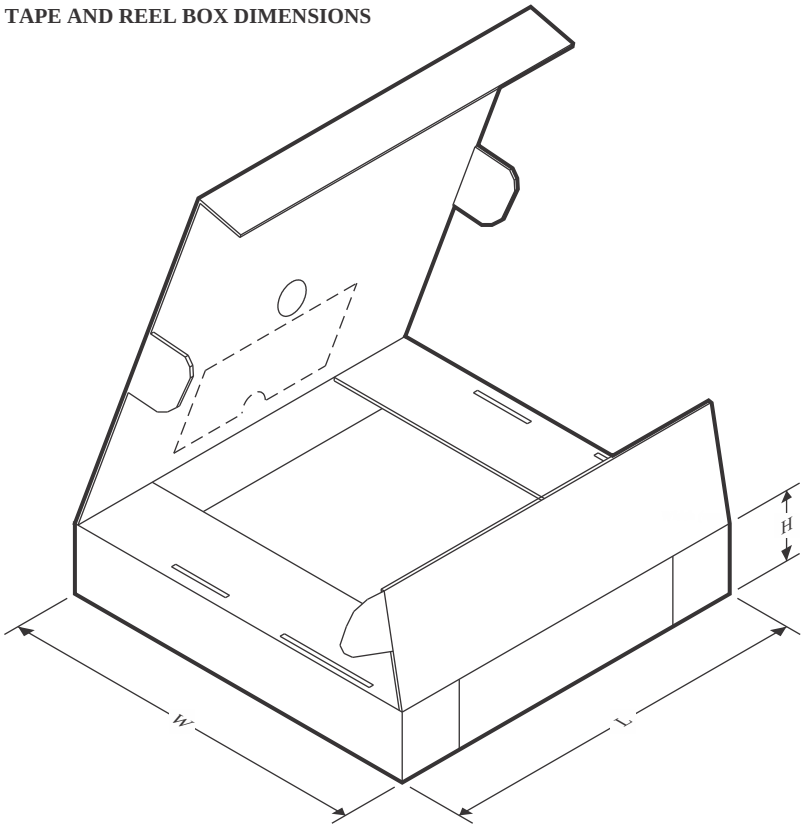
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1391CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV1391IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

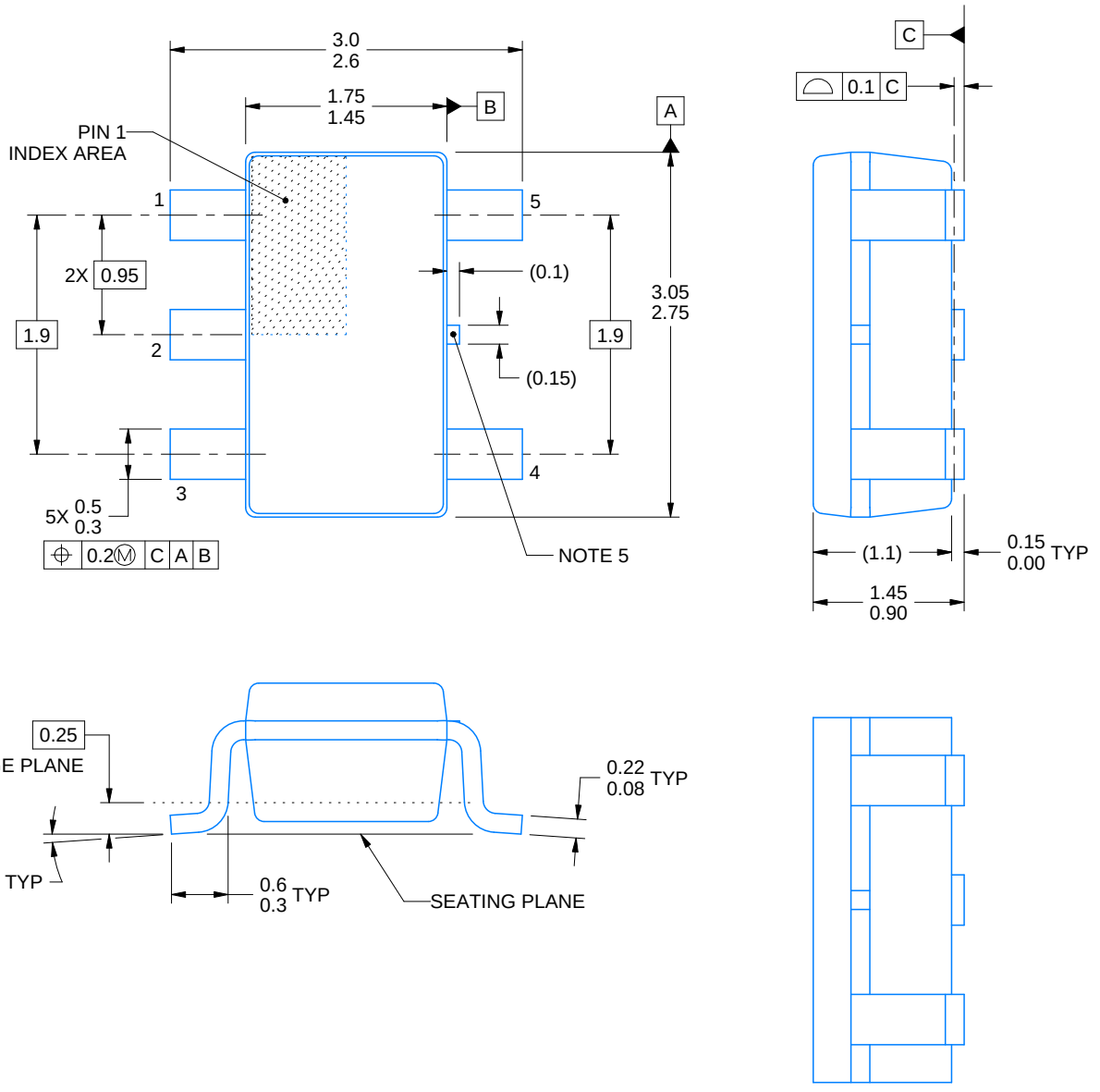
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1391CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1391IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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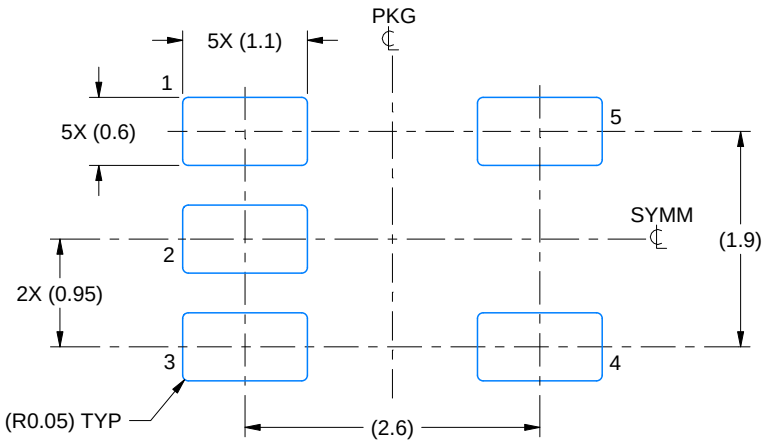
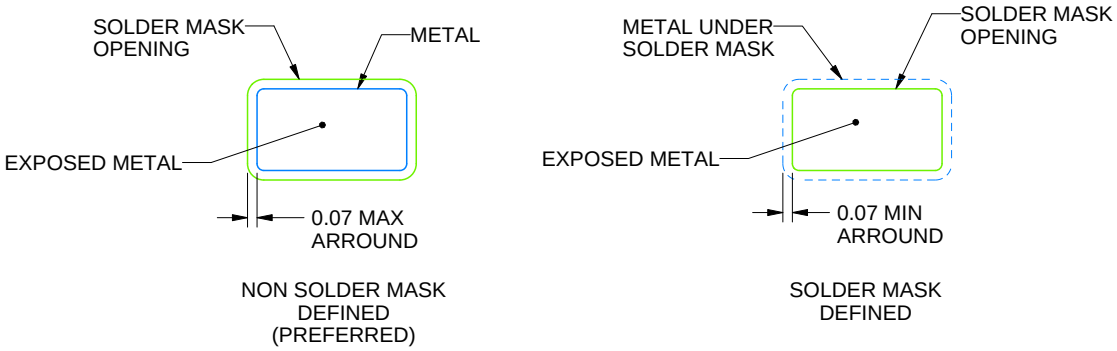
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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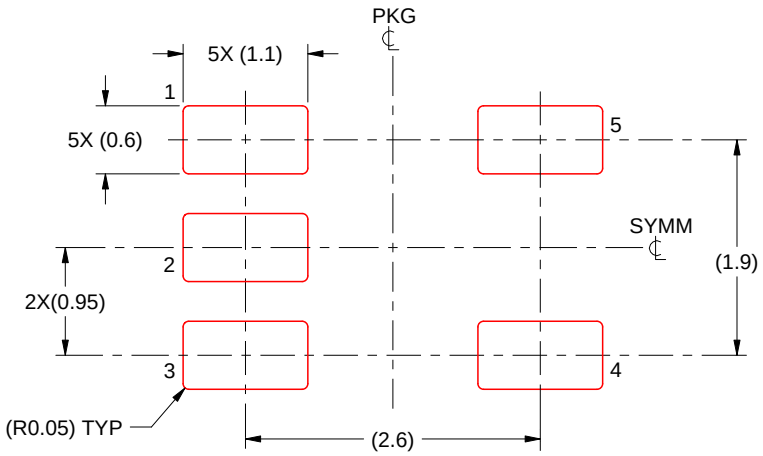
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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