DLP550HE 0.55 SVGA Digital Micromirror Device

1 Features

- 0.55-inch diagonal micromirror array
  - SVGA (800 x 600) array
  - 13.68-µm micromirror pitch
  - ±12° micromirror tilt angle (relative to flat state)
  - Designed for corner illumination
- LVDS input data bus
- The DLP550HE chipset includes:
  - DLP550HE DMD
  - DLPC4430 controller
  - DLPA100 controller power management and motor driver IC
  - DLPA200 DMD power management IC

2 Applications

- Smart lighting
- Business projector
- Education projector

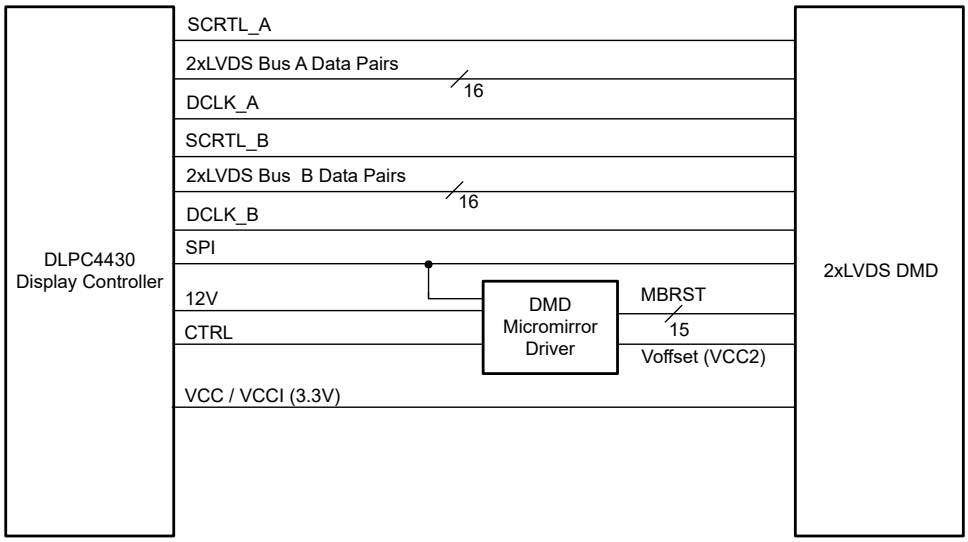
3 Description

The TI DLP550HE digital micromirror device (DMD) is a digitally controlled micro-electro-mechanical system (MEMS) spatial light modulator (SLM) that enables bright, affordable SVGA display solutions. The DLP550HE DMD, together with the DLPC4430 display controller, the DLPA100 power and motor driver, and DLPA200 DMD micromirror driver provides the capability to achieve high performance systems and is a great fit for display applications that require 4:3 aspect ratio, high brightness, and system simplicity.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DLP550HE	FYA (149)	32.20 mm × 22.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DLP550HE Simplified Application

Table of Contents

4 Revision History

Date	Revision	Note
April 2023	*	Initial Release

5 Pin Configuration and Functions

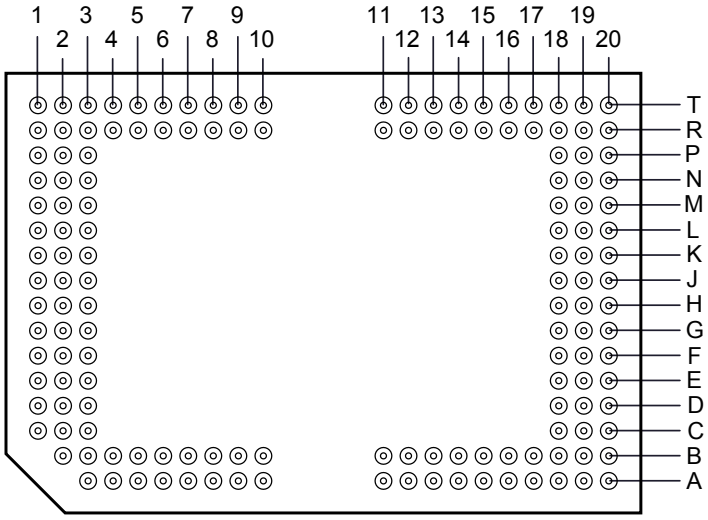


Figure 5-1. FYA Package 149-Pin Bottom View

Table 5-1. Pin Functions

PIN		NET LENGTH (mils)	SIGNAL	TYPE[1]	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(1)	G20	760.78	LVDS	I	LVDS pair for Data Bus A
D_AN(3)	H19	760.73			
D_AN(5)	F18	760.73			
D_AN(7)	E18	760.77			
D_AN(9)	C20	760.67			
D_AN(11)	B18	760.68			
D_AN(13)	A20	760.77			
D_AN(15)	B19	760.79			
D_AP(1)	H20	760.86			
D_AP(3)	G19	760.76			
D_AP(5)	G18	760.81			
D_AP(7)	D18	760.81			
D_AP(9)	D20	760.74			
D_AP(11)	A18	760.77			
D_AP(13)	B20	760.77			
D_AP(15)	A19	760.75			

Table 5-1. Pin Functions (continued)

PIN		NET LENGTH (mils)	SIGNAL	TYPE[1]	DESCRIPTION
NAME	NO.				
D_BN(1)	K20	760.72	LVDS	I	LVDS pair for Data Bus B
D_BN(3)	J19	760.79			
D_BN(5)	L18	760.77			
D_BN(7)	M18	760.78			
D_BN(9)	P20	760.76			
D_BN(11)	R18	760.78			
D_BN(13)	T20	760.78			
D_BN(15)	R19	760.77			
D_BP(1)	J20	760.8			
D_BP(3)	K19	760.82			
D_BP(5)	K18	760.85			
D_BP(7)	N18	760.81			
D_BP(9)	N20	760.83			
D_BP(11)	T18	760.8			
D_BP(13)	R20	760.72			
D_BP(15)	T19	760.77			
DCLK_AN	D19	760.73		I	LVDS pair for Data Clock A
DCLK_AP	E19	760.8			
DCLK_BN	N19	760.72		I	LVDS pair for Data Clock B
DCLK_BP	M19	760.8			
DATA CONTROL INPUTS					
SCTRL_AN	F20	760.78		I	LVDS pair for Serial Control (Sync) A
SCTRL_AP	E20	760.7			
SCTRL_BN	L20	760.83		I	LVDS pair for Serial Control (Sync) B
SCTRL_BP	M20	760.78			

Table 5-1. Pin Functions (continued)

PIN		NET LENGTH (mils)	SIGNAL	TYPE[1]	DESCRIPTION
NAME	NO.				
MICROMIRROR BIAS RESET INPUTS					
MBRST(0)	C3			I	Nonlogic compatible Micromirror Bias Reset signals. Connected directly to the array of pixel micromirrors. Used to hold or release the micromirrors. Bond Pads connect to an internal pulldown resistor.
MBRST(1)	D2				
MBRST(2)	D3				
MBRST(3)	E2				
MBRST(4)	G3				
MBRST(5)	E1				
MBRST(6)	G2				
MBRST(7)	G1				
MBRST(8)	N3				
MBRST(9)	M2				
MBRST(10)	M3				
MBRST(11)	L2				
MBRST(12)	J3				
MBRST(13)	L1				
MBRST(14)	J2				
MBRST(15)	J1			NC	Unused extra pin. Bond Pad connects to an internal pulldown resistor. Do not connect on DLP® system board.
SCP CONTROL					
SCPCLK	A8			I	Serial Communications Port Clock. Bond Pad connects to an internal pulldown circuit.
SCPDI	A5			I	Serial Communications Port Data. Bond Pad connects to an internal pulldown circuit.
SCPENZ	B7			I	Active low serial communications port enable. Bond pad connects to an internal pulldown circuit.
SCPDO	A9			O	Serial communications port output
OTHER SIGNALS					
EVCC	A3			P	Do not connect on the DLP® system board.
MODE_A	A4			I	Data Bandwidth Mode Select. Bond Pad connects to an internal pulldown circuit. Refer to Table 5-2 for DLP® system board connection information.
PWRDNZ	B9			I	Active Low Device Reset. Bond Pad connects to an internal pulldown circuit.
POWER					
V_{CC} [2]	B11, B12, B13, B16, R12, R13, R16, R17			P	Power supply for low voltage CMOS logic. Power supply for normal high voltage at micromirror address electrodes
V_{CCI} [2]	A12, A14, A16, T12, T14, T16			P	Power supply for low voltage CMOS LVDS interface
V_{CC2} [2]	C1, D1, M1, N1			P	Power supply for high voltage CMOS logic. Power supply for stepped high voltage at micromirror address electrodes

Table 5-1. Pin Functions (continued)

PIN		NET LENGTH (mils)	SIGNAL	TYPE[1]	DESCRIPTION
NAME	NO.				
V_{SS} (Ground)[3]	A6, A11, A13, A15, A17, B4, B5, B8, B14, B15, B17, C2, C18, C19, F1, F2, F19, H1, H2, H3, H18, J18, K1, K2, L19, N2, P18, P19, R4, R9, R14, R15, T7, T13, T15, T17			P	Common Return for all power
RESERVED SIGNALS					
RESERVED_FC	R7			I	Connect to GND on the DLP® system board. Bond Pad connects to an internal pulldown circuit.
RESERVED_FD	R8			I	Connect to GND on the DLP® system board. Bond Pad connects to an internal pulldown circuit.
RESERVED_PFE	T8			I	Connect to ground on the DLP® system board. Bond Pad connects to an internal pulldown circuit.
RESERVED_STM	B6			I	Connect to GND on the DLP® system board. Bond Pad connects to an internal pulldown circuit.
RESERVED_TP0	R10			I	Do not connect on the DLP® system board.
RESERVED_TP1	T11			I	Do not connect on the DLP® system board.
RESERVED_TP2	R11			I	Do not connect on the DLP® system board.
RESERVED_BA	T10			O	Do not connect on the DLP® system board.
RESERVED_BB	A10			O	Do not connect on the DLP® system board.
RESERVED_RA1	T9			O	Do not connect on the DLP® system board.
RESERVED_RB1	A7			O	Do not connect on the DLP® system board.
RESERVED_TS	B10			O	Do not connect on the DLP® system board.
RESERVED_A(0)	T2			NC	Do not connect on the DLP® system board.
RESERVED_A(1)	T3				
RESERVED_A(2)	R3				
RESERVED_A(3)	T4				
RESERVED_M(0)	R2			NC	Do not connect on the DLP® system board.
RESERVED_M(1)	P1			NC	Do not connect on the DLP® system board.
RESERVED_S(0)	T1			NC	Do not connect on the DLP® system board.
RESERVED_S(1)	R1			NC	Do not connect on the DLP® system board.
RESERVED_IRQZ	T6			NC	Do not connect on the DLP® system board.
RESERVED_OEZ	R5			NC	Do not connect on the DLP® system board.
RESERVED_RSTZ	R6			NC	Do not connect on the DLP® system board.
RESERVED_STR	T5			NC	Do not connect on the DLP® system board.
RESERVED_STR	T5			NC	Do not connect on the DLP® system board.

Table 5-1. Pin Functions (continued)

PIN		NET LENGTH (mils)	SIGNAL	TYPE(1)	DESCRIPTION
NAME	NO.				
RESERVED_VB	E3, F3, K3, L3			NC	Do not connect on the DLP® system board.
RESERVED_VR	B2, B3, P2, P3			NC	Do not connect on the DLP® system board.

(1) I = Input, O = Output, G = Ground, A = Analog, P = Power, NC = No Connect.
(2) Power supply pins required for all DMD operating modes are V_{SS}, V_{CC}, V_{CCI} , and V_{CC2}.
(3) V_{SS} must be connected for proper DMD operation.

Table 5-2. Data Bus LVDS Pairs versus MODE_A

MODE_A	D_A & D_B
GND	(1, 3, 5, 7, 9, 11, 13, 15)
VCC	(3, 7, 11, 15)

1. DLP® ASICs that drive data to the DMD typically do not support every mode shown in Table 5-2.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MON	MAX	UNIT
SUPPLY VOLTAGES					
V_{CC}	Supply voltage for LVCMOS core logic(2)	–0.5		4	V
V_{CCI}	Supply voltage for LVDS Interface(2)	–0.5		4	V
V_{CC2}	Micromirror Electrode and HVCMOS voltage(2)	–0.5		8	V
V_{MBRST}	Input voltage for MBRST(14:0)(2)	–28		28	V
$\lvert V_{CCI} - V_{CC} \rvert$	Supply voltage delta (absolute value)(3)			0.3	V
Input Voltage	Input voltage for all other input pins(2)	–0.5		V_{CC} + 0.3	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(4)			700	mV
CLOCKS					
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_A			230	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_B			230	MHz
ENVIRONMENTAL					
T_{ARRAY} and T_{WINDOW}	Temperature, operating(5)	0		90	°C
	Temperature, non-operating(5)	–40		90	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1(6)			30	°C
T_{DP}	Dew point nominal condition outside of desiccant sealed bag			81	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are referenced to common ground V_{SS}. V_{CC}, V_{CCI}, V_{CC2}, and V_{SS} (GND) power supplies are all required for all DMD operating modes.
(3) Exceeding the recommended allowable voltage difference between V_{CC} and V_{CCI} may result in excessive current draw.
(4) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS differential inputs must not exceed $\lvert V_{ID} \rvert$ = 700 mV or damage may result to the internal termination resistors.
(5) The highest temperature of the active array (as calculated using Section 7.6) or of any point along the window edge as defined in Figure 7-1. The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, then that point needs to be used.
(6) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 7-1. The window test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to result in the worst-case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, then that point needs to be used.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	80	°C
T_{DP-AVG}	Average dew point temperature (non-condensing)(1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation needs to be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except MBRST(15:0)	±2000	V
			Pins MBRST(15:0)	< 250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	Supply voltage for LVCMOS core logic(1)	3.0	3.3	3.6	V
V_{CCI}	Supply voltage for LVDS interface(1) (2)	3.0	3.3	3.6	V
V_{CC2}	Micromirror electrode and HVCMOS voltage(1)	7.25	7.5	7.75	V
V_{MBRST}	Micromirror bias / reset voltage	–27		26.5	V
LVCMOS INTERFACE					
V_{IH}	Input high voltage(3)	1.7	2.5	V_{CC} + 0.3	V
V_{IL}	Input low voltage(3)	–0.3		0.7	V
I_{OH}	High level output current			–30	mA
I_{OL}	Low level output current			25	mA
t_{PWRDNZ}	PWRDNZ pulse width(4)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency(5)	50		500	kHz
t_{SCP_SKEW}	Time between valid SCPDI and rising-edge of SCPCLK(6)	-300		300	ns
t_{SCP_DELAY}	Time between valid SCPDO and rising-edge of SCPCLK(6)			960	ns
$t_{SCP\_NEG\_ENZ}$	Time between falling-edge of SCPENZ and the rising-edge of SCPCLK.(5)	$6/f_{DCLK}$			s
$t_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tristate)			$192/f_{DCLK}$	s
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)	1			$1/f_{scpclk}$
t_r	Rise Time (20% to 80%)(6)			200	ns
t_f	Fall time (80% to 20%)(6)			200	ns
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_A and DCLK_B(7)		200	230	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value)(7)	100	400	600	mV
V_{CM}	Common mode voltage(7)		1200		mV

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
V_{LVDS}	LVDS voltage(7)	0		1900	mV
t_r	Rise Time (20% to 80%)(8)	100		400	ns
t_f	Fall time (80% to 20%)(8)	100		400	ns
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			10	ns
Z_{IN}	Internal differential termination resistance	95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	85	90	95	Ω
ENVIRONMENT					
T_{ARRAY}	Array temperature, long-term operational(9) (10) (11) (12) (13)	10		40 to 70	°C
	Array temperature, short-term operational, 500-hr max(10) (14)	0		10	°C
T_{WINDOW}	Window temperature, operational(15)			85	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1(16)			14	°C
$T_{DP\text{-}AVG}$	Average dew point temperature (non-condensing)(17)			28	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range (non-condensing)(18)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	months
LAMP ILLUMINATION					
ILL_{UV}	Illumination Wavelengths < 395 nm(9)		0.68	2	mW/cm^2
ILL_{VIS}	Illumination Wavelengths between 395 nm and 800 nm(13)		Thermally limited		W/cm^2
ILL_{IR}	Illumination Wavelengths > 800 nm			10	mW/cm^2
SOLID STATE ILLUMINATION					
ILL_{UV}	Illumination Wavelengths < 410 nm(9)			3	mW/cm^2
ILL_{VIS}	Illumination Wavelengths between 410 nm and 800 nm(13)		Thermally limited		W/cm^2
ILL_{IR}	Illumination Wavelengths > 800 nm			10	mW/cm^2

(1) All voltages are referenced to common ground V_{SS}. V_{CC}, V_{CCI}, and V_{CC2} power supplies are all required for proper DMD operation. V_{SS} (GND) must also be connected.
(2) To prevent excess current, the supply voltage delta $|V_{CCI} – V_{CC}|$ must be less than the specified limit. See Section 9, Figure 9-1, and Figure 9-1.
(3) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, “Low-Power Double Data Rate (LPDDR)” JESD209B. Tester Conditions for V_{IH} and V_{IL}.
- Frequency = 60 MHz. Maximum Rise Time = 2.5 ns @ (20% to 80%).
- Frequency = 60 MHz. Maximum Fall Time = 2.5 ns @ (80% to 20%).

(4) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
(5) The SCP clock is a gated clock. Duty cycle must be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(6) See Figure 6-2.
(7) See LVDS Timing Requirements in Section 6.8 and Figure 6-6.
(8) See Figure 6-5 LVDS Waveform Requirements.
(9) Simultaneous exposure of the DMD to the maximum Section 6.4 for temperature and UV illumination reduces device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measure at test point (TP1) shown in Figure 7-1 and the Thermal Table using the Section 7.6.
(11) Per Figure 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to Section 7.7 for a definition of micromirror landed duty cycle.
(12) Long-term is defined as the usable life of the device.
(13) The maximum optical power that can be incident on the DMD is limited by the maximum optical power density and the micromirror array temperature.
(14) Short-term is the total cumulative time over the useful life of the device.
(15) The locations of thermal test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.

(16) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 7-1. The window test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point should be used.
(17) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(18) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

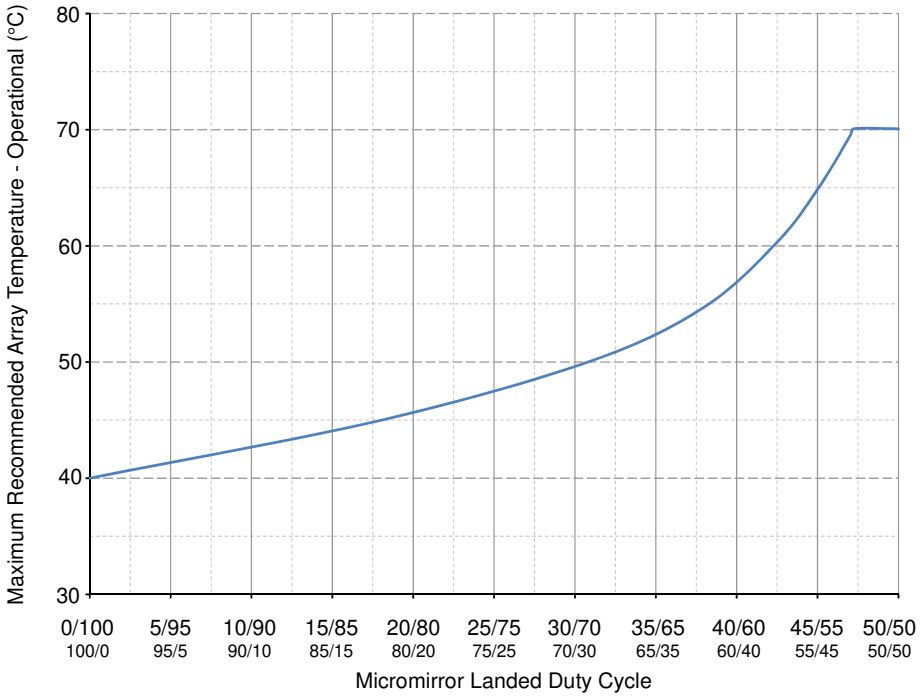


Figure 6-1. Max Recommended Array Temperature—Derating Curve

6.5 Thermal Information

THERMAL METRIC	DLP550HE FYA PACKAGE 149 PINS	Unit
Thermal Resistance, active area to test point 1 (TP1)(1)	0.6	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the Section 6.4.
The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.
It's recommended that an optical system be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 3 V, I_{OH} = –15 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 3.6 V, I_{OL} = 10 mA			0.4	V
I_{OZ}	High-impedance output current	V_{CC} = 3.6 V			10	µA
I_{IL}	Low-level input current	V_{CC} = 3.6 V, VI = 0			–5	µA
I_{IH}	High-level input current (1)	V_{CC} = 3.6 V, VI = V_{CC}			200	µA
I_{CC}	Supply current VCC (2)	V_{CC} = 3.6 V			280	mA
I_{CCI}	Supply current VCCI (2)	V_{CCI} = 3.6 V			235	mA

6.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC2}	Supply current VCC2	V_{CC2} = 7.8 V			25	mA
	Supply input power total				2.28	W

(1) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins.
(2) To prevent excess current, the supply voltage delta $|V_{CCI} – V_{CC}|$ must be less than the specified limit in Section 6.4.

6.7 Capacitance at Recommended Operating Conditions

over operating free-air temperature range, f = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_I	Input capacitance			10	pF
C_O	Output capacitance			10	pF
C_{IM}	MBRST(14:0) input capacitance	800 x 600 array all inputs interconnected	160	200	pF

6.8 Timing Requirements

Over Section 6.4 (unless otherwise noted).

PARAMETER DESCRIPTION			SIGNAL	MIN	TYP	MAX	UNIT
LVDS (1)							
t_C	Clock Cycle	DCLK_A	LVDS	4.34	5		ns
t_C	Clock Cycle	DCLK_B	LVDS	4.34	5		ns
t_W	Pulse Width	DCLK_A	LVDS	2.17	2.5		ns
t_W	Pulse Width	DCLK_B	LVDS	2.17	2.5		ns
t_{SU}	Setup Time	D_A(15:0) before DCLK_A	LVDS	0.35			ns
t_{SU}	Setup Time	D_A(15:0) before DCLK_B	LVDS	0.35			ns
t_{SU}	Setup Time	SCTRL_A before DCLK_A	LVDS	0.35			ns
t_{SU}	Setup Time	SCTRL_B before DCLK_B	LVDS	0.35			ns
t_H	Hold Time	D_A(15:0) after DCLK_A	LVDS	0.65			ns
t_H	Hold Time	D_B(15:0) after DCLK_B	LVDS	0.65			ns
t_H	Hold Time	SCTRL_A after DCLK_A	LVDS	0.65			ns
t_H	Hold Time	SCTRL_B after DCLK_B	LVDS	0.65			ns
t_{SKEW}	Skew Time	Channel B relative to Channel A(2) (3)	LVDS	–1.25		1.25	ns

(1) See Figure 6-6 for timing requirements for LVDS.
(2) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0) and D_AP(15:0).
(3) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0) and D_BP(15:0).

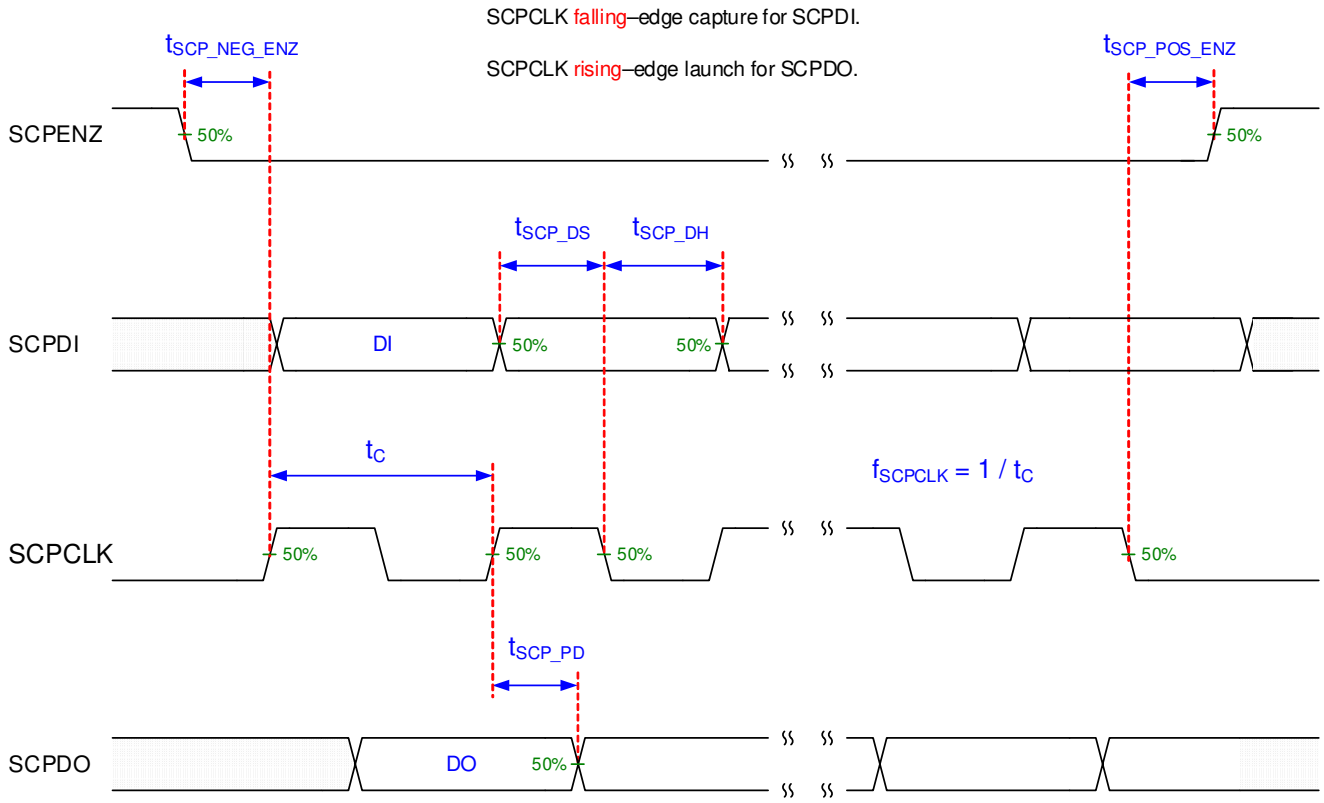
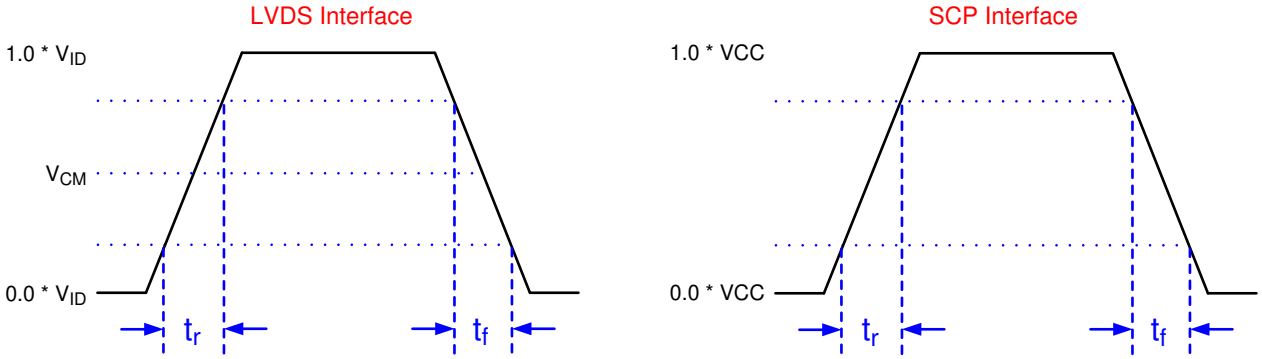


Figure 6-2. SCP Timing Requirements

See Section 6.4 for f_{SCPCLK}, t_{SCP_DS}, t_{SCP_DH}, and t_{SCP_PD} specifications.

See Section 6.4 for t_r and t_f specifications and conditions.



Not to scale.

Refer to the Section 6.8.

Refer to Section 5 for list of LVDS pins and SCP pins.

Figure 6-3. Rise Time and Fall Time

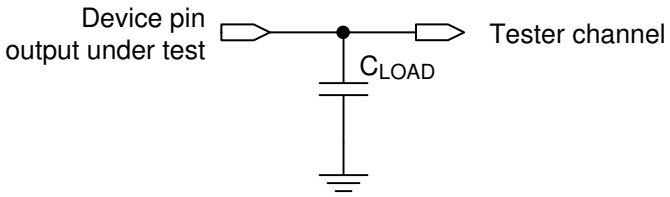


Figure 6-4. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be considered. System designers must use IBIS or other simulation tools to correlate the timing reference load to a system environment. See Figure 6-4.

Not to Scale

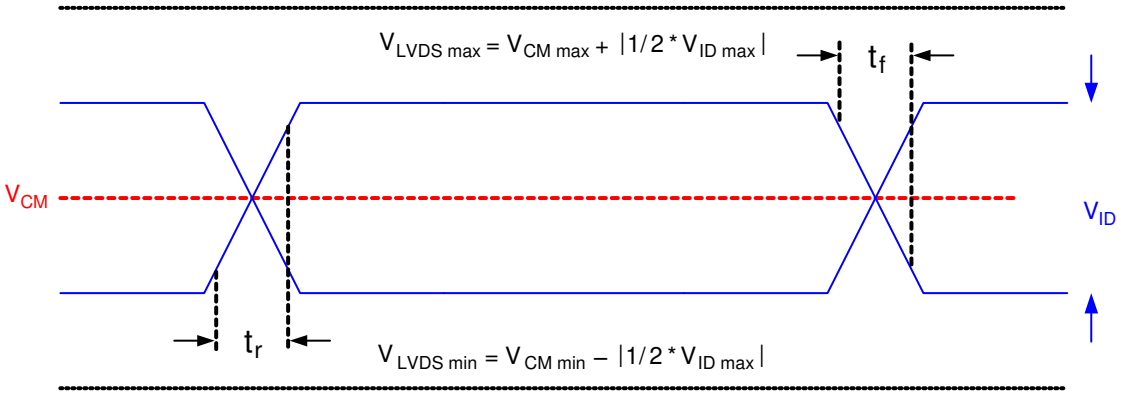


Figure 6-5. LVDS Waveform Requirements

See Section 6.4 for V_{CM}, V_{ID}, and V_{LVDS} specifications and conditions.

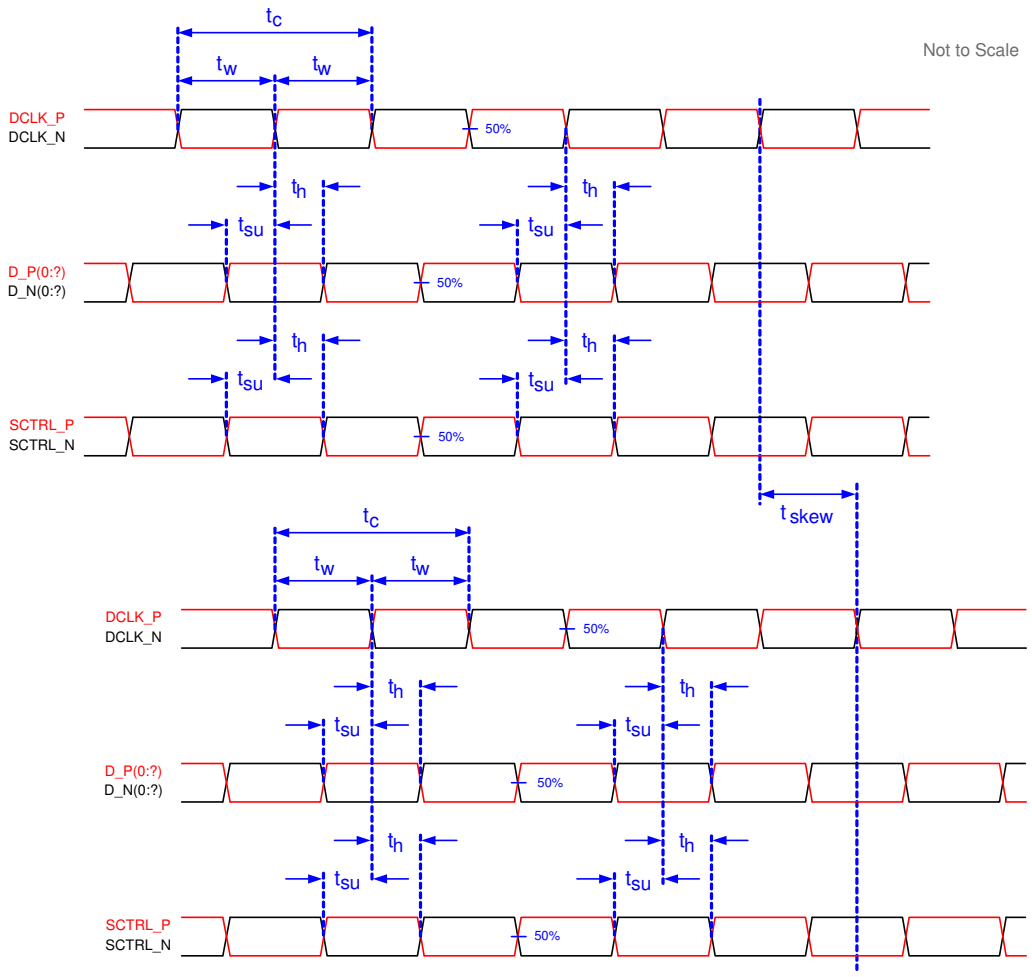


Figure 6-6. Timing Requirements

See Section 6.8 for timing requirements and LVDS pairs per channel (bus) defining D_P(0:x) and D_N(0:x).

6.9 System Mounting Interface Loads

PARAMETER	MIN	TYP	MAX	UNIT
When loads are applied to the electrical and thermal interface areas				
Maximum load to be applied to the electrical interface area(1)			111	N
Maximum load to be applied to the thermal interface area(1)			111	N
When a load is applied to only the electrical interface area				
Maximum load to be applied to the electrical interface area(1)			222	N
Maximum load to be applied to the thermal interface area(1)			0	N

(1) Uniformly distributed within area shown in Figure 6-7

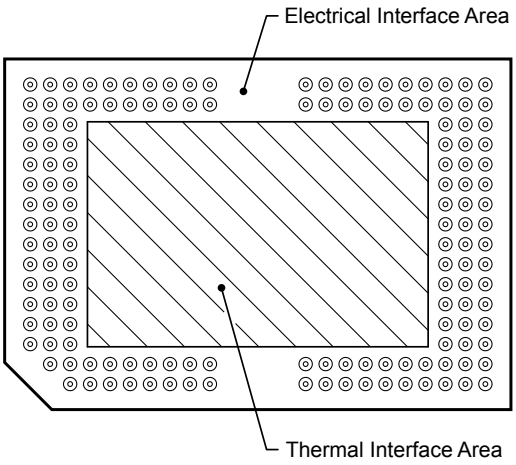


Figure 6-7. System Mounting Interface Loads

6.10 Micromirror Array Physical Characteristics

Table 6-1. Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns(1)	M	800	micromirrors
Number of active rows(1)	N	600	
Micromirror (pixel) pitch (1)	P	13.68	µm
Micromirror active array width(1)	Micromirror pitch × number of active columns	10.944	mm
Micromirror active array height(1)	Micromirror pitch × number of active rows	8.208	mm
Micromirror active border size(2)	Pond of Micromirror (POM)	6	micromirrors / side

(1) See Figure 6-8.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the *Pond Of Mirrors* (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or "on" state but still require an electrical bias to tilt toward "off."

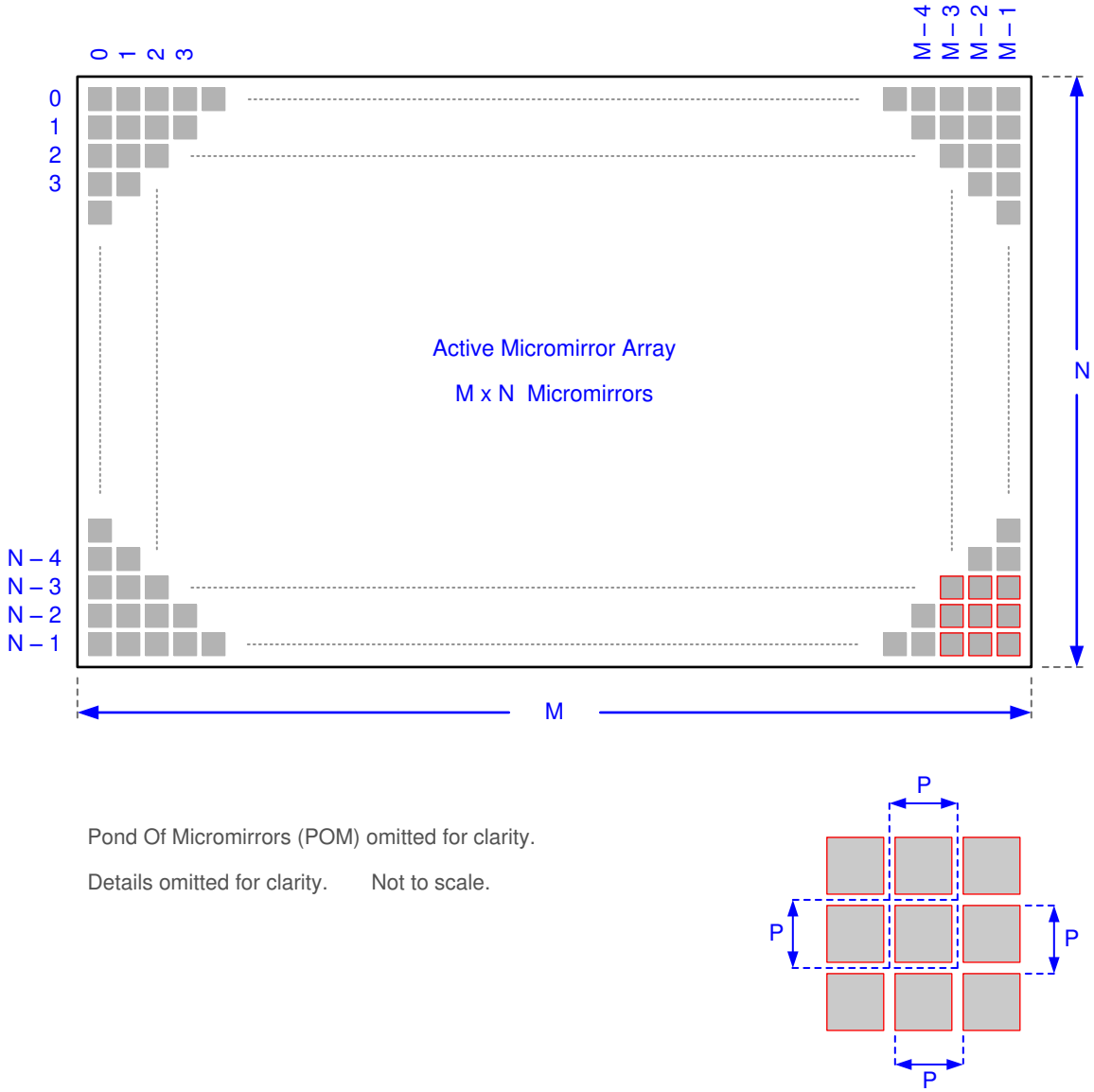


Figure 6-8. Micromirror Array Physical Characteristics

Refer to Section 6.10 table for M, N, and P specifications.

6.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Mirror Tilt angle, variation device to device (1) (2) (3) (4)		Landed state	11	12	13	°
Micromirror crossover time(5)		Typical performance		4		µs
Micromirror switching time(6)		Typical performance	11			
Image performance(7)	Bright pixels(s) in active area(8)	Gray 10 Screen(9)			0	micromirrors
	Bright pixes(s) in POM(10)	Gray 10 Screen(9)			1	micromirrors
	Dark pixel(s) in active area(11)	White Screen			4	micromirrors
	Adjacent pixels(12)	Any Screen			0	micromirrors
	Unstable pixel(s) in active area(13)	Any Screen			0	micromirrors

(1) Measured relative to the plane formed by the overall micromirror array
(2) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(3) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(4) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction. See Figure 6-9.
(5) The time required for a micromirror to nominally transition from one landed state to the opposite landed state
(6) The minimum time between successive transitions of a micromirror
(7) Conditions of Acceptance: All DMD image performance returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear
Test set brightness and contrast shall be set to nominal
The diagonal size of the projected image shall be a minimum of 60 inches
The projection screen shall be 1x gain
The projected image shall be inspected from an 8 foot minimum viewing distance
The image shall be in focus during all image performance tests
(8) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter that the surrounding pixels
(9) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(10) POM definition: Rectangular border of off-state mirror surrounding the active area.
(11) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
(12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
(13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with the parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

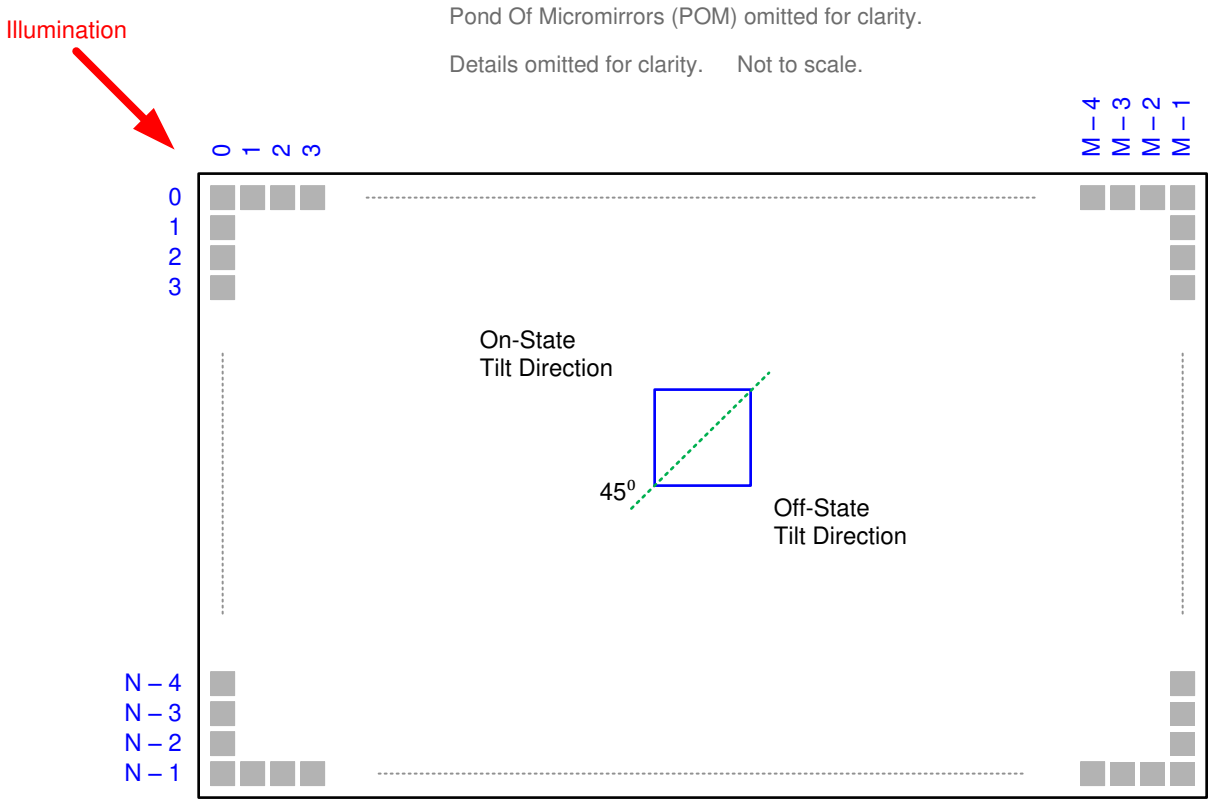


Figure 6-9. Micromirror Landed Orientation and Tilt

Refer to Section 6.10 table for M, N, and P specifications.

6.12 Window Characteristics

Table 6-2. DMD Window Characteristics

PARAMETER	MIN	NOM
Window material		Corning Eagle XG
Window Refractive Index at 546.1 nm		1.5119
Window Transmittance, minimum within the wavelength range 420–680 nm. Applies to all angles 0°–30° AOI. (1) (2)	97%	
Window Transmittance, average over the wavelength range 420–680 nm. Applies to all angles 30°–45° AOI. (1) (2)	97%	

(1) Single-pass through both surfaces and glass
(2) AOI—Angle of incidence is the angle between an incident ray and the normal to a reflecting or refracting surface.

6.13 Chipset Component Usage Specification

Reliable function and operation of the DLP550HE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

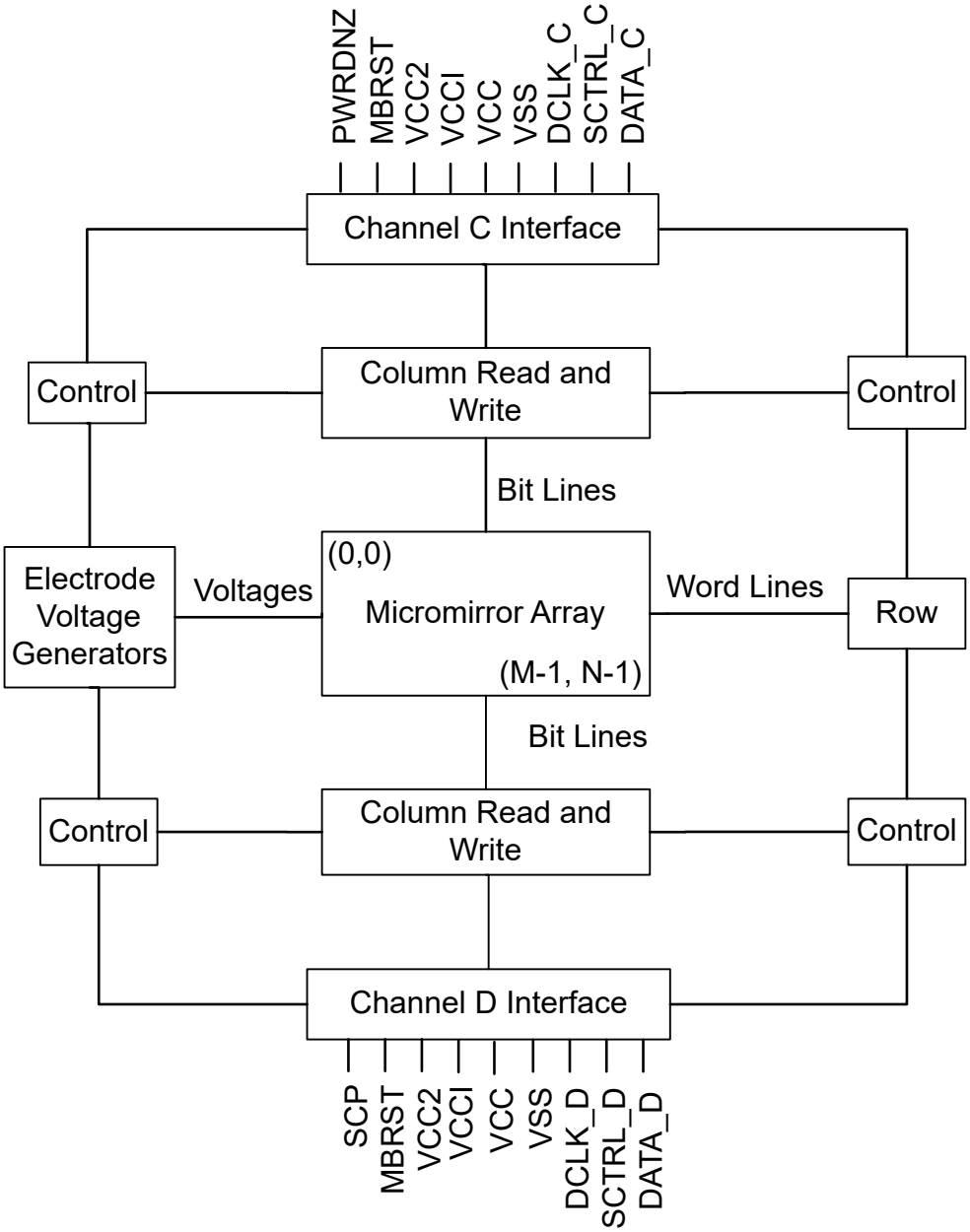
7 Detailed Description

7.1 Overview

The DMD is a 0.55-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to Section 7.2. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP550HE DMD is part of the chipset comprising of the DLP550HE DMD, the DLPC4430 display controller, the DLPA100 power and motor driver and the DLPA200 micromirror driver. To ensure reliable operation, the DLP550HE DMD must always be used with the DLPC4430 display controller, the DLPA100 power and motor driver and the DLPA200 micromirror driver.

7.2 Functional Block Diagram



For pin details on Channels A, B refer to Section 5 and LVDS Interface section of Section 6.8.

7.3 Feature Description

7.3.1 Power Interface

The DMD requires 3 DC voltages: DMD_P3P3V, V_{OFFSET}, and MBRST. DMD_P3P3V is created by the DLPA100 power and motor driver and the DLPA200 DMD micromirror driver. Both the DLPA100 and DLPA200 create the main DMD voltages, as well as powering various peripherals (TMP411, I^2C, and TI level translators). DMD_P3P3V provides the VCC voltage required by the DMD. V_{CC2} (8.5V) and MBRST are made by the DLPA200 and are supplied to the DMD to control the micromirrors.

7.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Figure 6-4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers need to use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4430 display controller. See the *DLPC4430 Display Controller Data Sheet* or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trade offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area could occur.

7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. It's recommended the illumination optical system be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's

optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

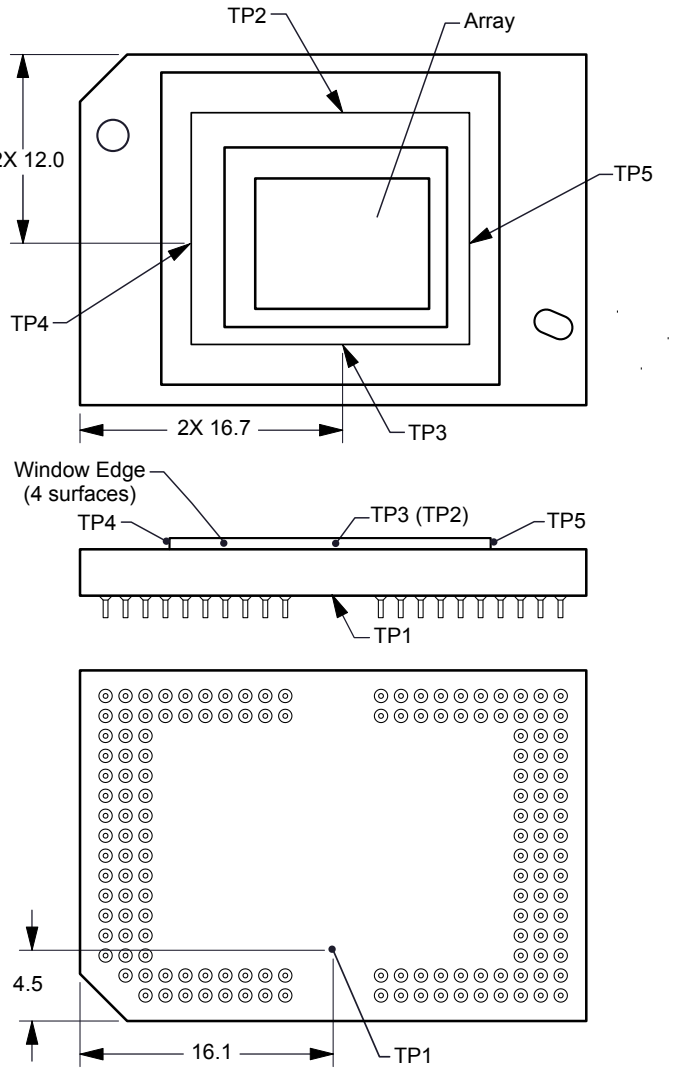


Figure 7-1. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in Figure 7-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in *Thermal Information* from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.42

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.8 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 25 \text{ W (measured)} \quad (3)$$

$$T_{CERAMIC} = 55.0°C \text{ (measured)} \quad (4)$$

$$Q_{ELECTRICAL} = 0.8 \text{ W} \quad (5)$$

$$Q_{ARRAY} = 0.8 \text{ W} + (0.42 \times 25 \text{ W}) = 11.3 \text{ W} \quad (6)$$

$$T_{ARRAY} = 55.0°C + (11.3 \text{ W} \times 0.6°C/W) = 61.8°C \quad (7)$$

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time); whereas 0/100 indicate that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the derating curve. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature at a given long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 7-1.

Table 7-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

- Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

Where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point. (1)

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, and blue color intensities will be as shown in Table 7-2 and Table 7-3.

Table 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage

RED CYCLE	GREEN CYCLE	BLUE CYCLE
50%	20%	30%

Table 7-3. Example Landed Duty Cycle for Full-Color

RED SCALE	GREEN SCALE	BLUE SCALE	LANDED DUTY CYCLE
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Texas Instruments DLP technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, either towards the projection optics, or the collection optics. The large micromirror array size and ceramic package provides great thermal performance for bright display applications. Typical applications using the DLP550HE include smart lighting, education projectors, and business projectors.

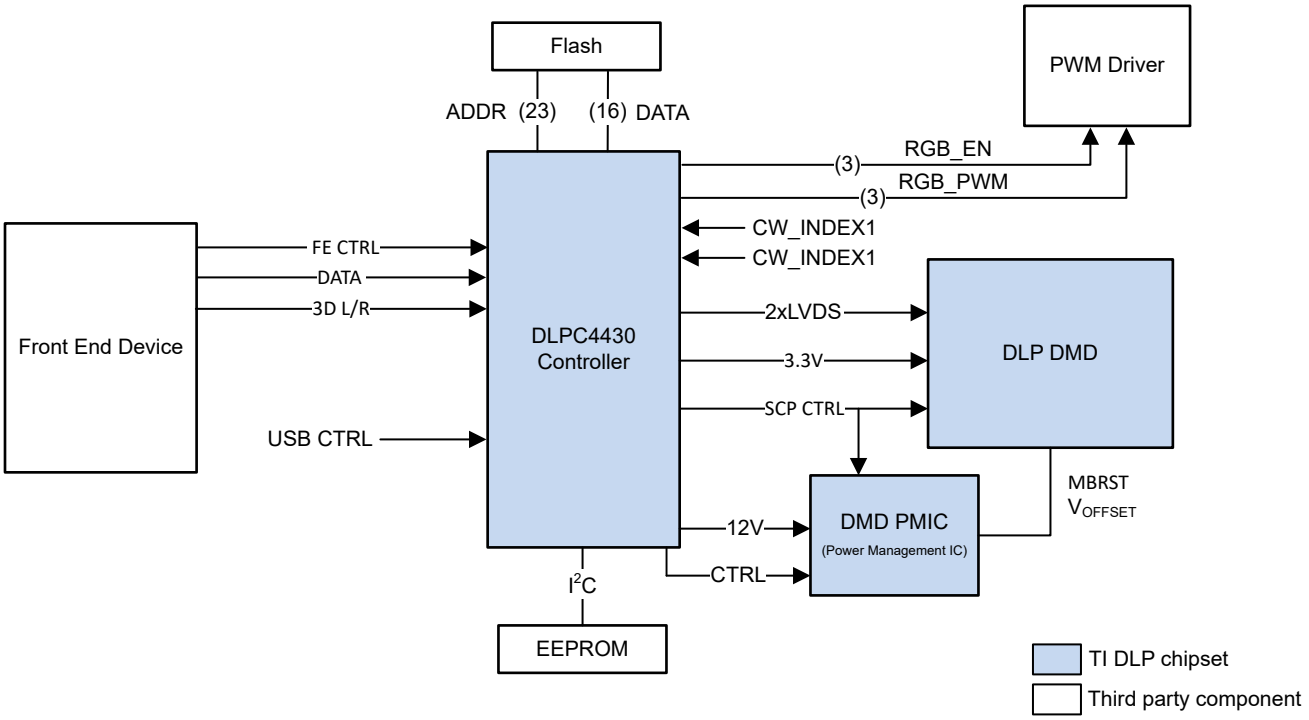
The following orderables have been replaced by the DLP550HE:

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)	MECHANICAL ICD
DLP550HET	FYA (149)	32.20 mm × 22.30 mm	2512649
8060-643AB	FYA (149)	32.20 mm × 22.30 mm	2512649

8.2 Typical Application

The DLP550HE DMD combined with a DLPC4430 digital controller, DLPA100 power management device, and DLPA200 micromirror driver provides SVGA resolution for bright, colorful display applications. A typical display system using the DLP550HE and additional system components are shown in Figure 8-1.



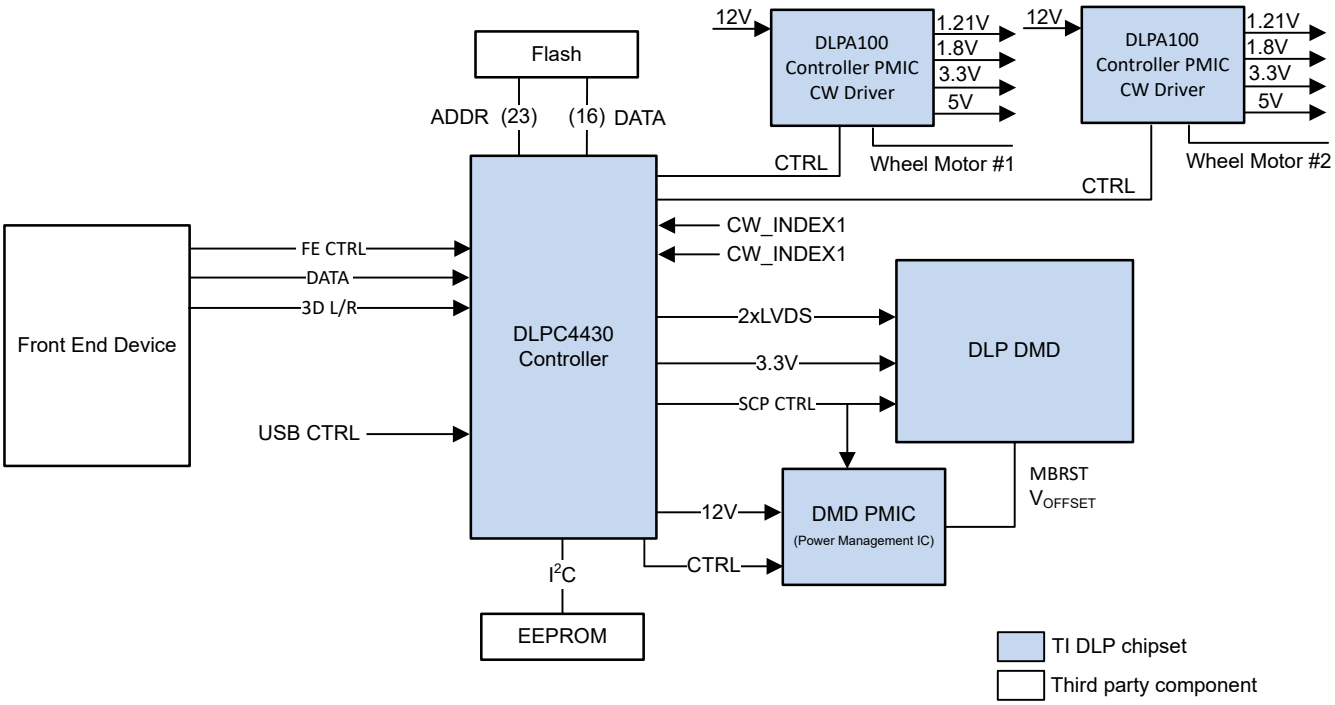


Figure 8-1. Typical DLPC4430 Application (LED - top, LPCW - bottom)

8.2.1 Design Requirements

The DLP 0.55-inch SVGA chipset creates a powerful projection system. This chipset includes the DLP550HE, DLPC4430, DLPA100, and the DLPA200. The DLP550HE is used as the core imaging device in the display system and contains a 0.55-inch array of micromirrors. The DLPC4430 controller is the digital interface between the DMD and the rest of the system. The controller drives the DMD by taking the converted source data from the front end receiver and transmitting it to the DMD over a high speed interface. The DLPA100 power management device provides voltage regulators for the controller and colorwheel motor control. The DLPA200 provides the power and sequencing to drive the DLP550HE. To ensure reliable operation, the DLP550HE DMD must always be used with the DLPC4430 display controller, a DLPA100 PMIC driver, and a DLPA200 DMD micromirror driver.

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include lamp, LED, laser, or laser phosphor. The type of illumination used and desired brightness will have a major effect on the overall system design and size.

8.2.2 Detailed Design Procedure

For help connecting the DLPC4430 display controller and the DLP550HE DMD, see the reference design schematic. For a complete DLP system, an optical module or light engine is required that contains the DLP550HE DMD, associated illumination sources, optical elements, and necessary mechanical components. The optical module is typically supplied by an optical OMM (optical module manufacturer) who specializes in designing optics for DLP projectors.

8.2.3 Application Curve

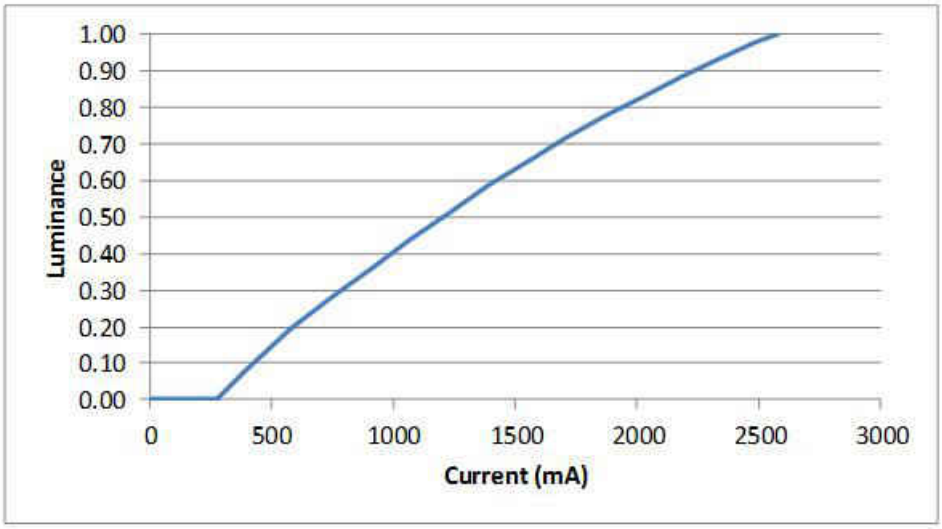


Figure 8-2. Luminance vs Current

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: V_{CC}, V_{CCI}, and V_{CC2}. V_{SS} must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC4430 display controller.

Note

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. V_{CC}, V_{CCI} and V_{CC2} power supplies have to be coordinated during power-up and power-down operations. V_{SS} must also be connected. Failure to meet any of the below requirements results in a significant reduction in the reliability and lifetime of the DMD. Refer to Figure 9-1.

9.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{CC} and V_{CCI} must always start and settle before V_{CC2} is applied to the DMD.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed in Section 6.1 and in Section 6.4.
- During power-up, LVCMOS input pins must not be driven high until after V_{CC} and V_{CCI} have settled at operating voltages listed in Section 6.4 table.

9.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{CC} and V_{CCI} must be supplied until after V_{CC2} is discharged to within the specified limit of ground. Refer to Section 6.4.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in Section 6.1 and in Section 6.4. During power-down, LVCMOS input pins must be less than specified in Section 6.4.

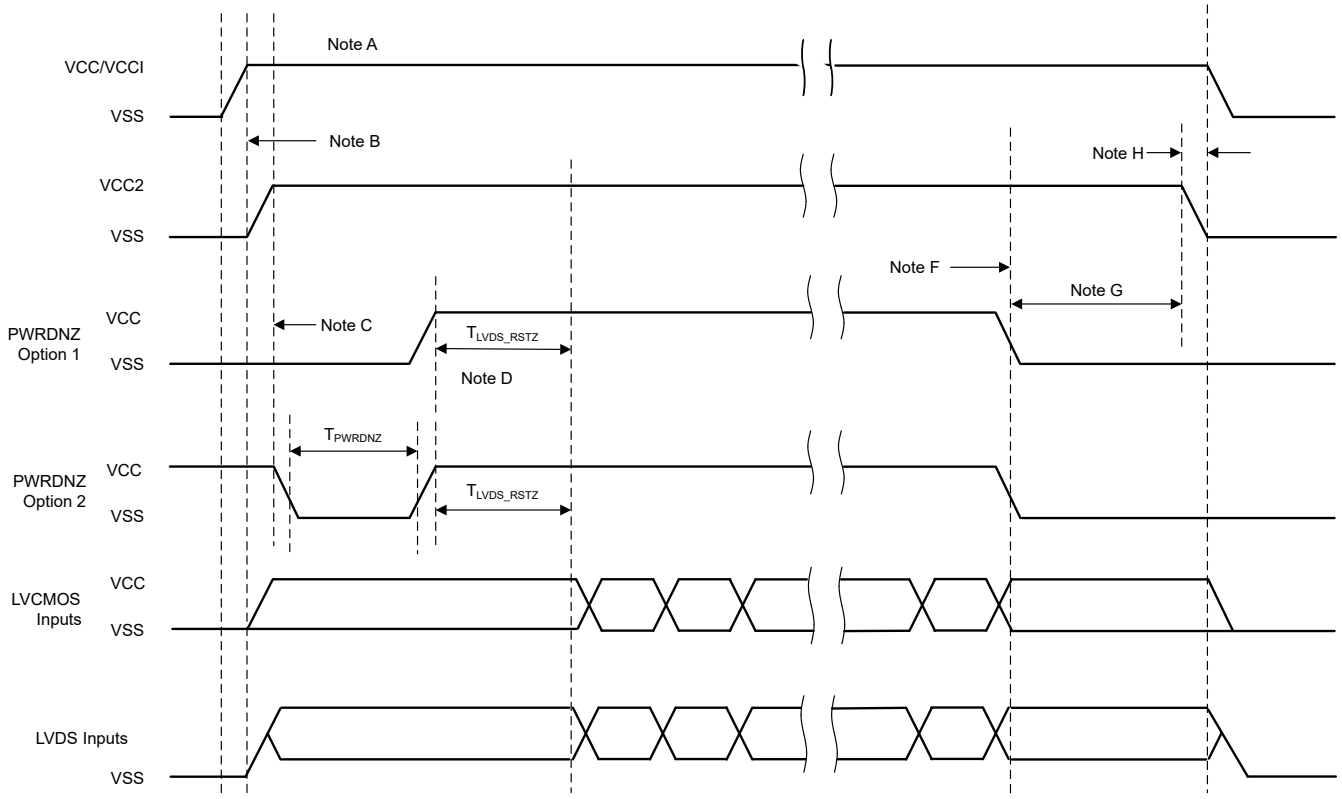


Figure 9-1. Power Supply Timing

A. See *Pin Configuration and Functions* for pin functions.
B. V_{CC} must be up and stable prior to V_{CC2} powering up.

C. PWRDNZ has two turn on options. Option 1: PWRDNZ does not go high until V_{CC} and V_{CC2} are up and stable, or Option 2: PWRDNZ must be pulsed low for a minimum of T_{PWRDNZ}, or 10 ns after V_{CC} and V_{CC2} are up and stable.
D. There is a minimum of T_{LVDS_ARSTZ}, or 2 µs, wait time from PWRDNZ going high for the LVDS receiver to recover.
E. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates the PWRDNZ and disables V_{CC2}.
F. Under power-loss conditions, where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, PWRDNZ goes low.
G. V_{CC} must remain high until after V_{CC2} goes low.
H. To prevent excess current, the supply voltage delta $|V_{CCI} – V_{CC}|$ must be less than specified limit in Section 6.4.

10 Layout

10.1 Layout Guidelines

The DLP550HE DMD is part of a chipset that is controlled by the DLPC4430 display controller in conjunction with the DLPA100 power and motor driver. These guidelines are targeted at designing a PCB board with the DLP550HE DMD. The DLP550HE DMD board is a high-speed multilayer PCB, with primarily high-speed digital logic utilizing dual edge clock rates up to ~400 MHz for DMD LVDS signals. The remaining traces are comprised of low speed digital LVTTL signals. TI recommends that mini power planes are used for VOFFSET and MBRST[0:15]. Solid planes are required for DMD_P3P3V(3.3 V) and Ground. The target impedance for the PCB is 50 Ω ±10% with the LVDS traces being 100 Ω ±10% differential. TI recommends using an 8 layer stack-up as described in Table 10-1.

10.2 Layout Example

10.2.1 Layers

The layer stack-up and copper weight for each layer is shown in Table 10-1. Small subplanes are allowed on signal routing layers to connect components to major sub-planes on top/bottom layers if necessary.

Table 10-1. Layer Stack-Up

LAYER NUMBER	LAYER NAME	COPPER WEIGHT	COMMENTS
1	Side A - DMD only	1.5 oz.	DMD, escapes, low frequency signals, power subplanes
2	Ground	1 oz.	Solid ground plane (net GND)
3	Signal	0.5 oz.	50-Ω and 100-Ω differential signals
4	Ground	1 oz.	Solid ground plane (net GND)
5	DMD_P3P3V	1 oz.	+3.3-V power plane (net DMD_P3P3V)
6	Signal	0.5 oz.	50-Ω and 100-Ω differential signals
7	Ground	1 oz.	Solid ground plane (net GND)
8	Side B—All other Components	1.5 oz.	Discrete components, low frequency signals, power subplanes

10.2.2 Impedance Requirements

TI recommends the board have matched impedance of 50 Ω ±10% for all signals.Special Impedance Requirements lists the exceptions.

Table 10-2. Special Impedance Requirements

SIGNAL TYPE	SIGNAL NAME	IMPEDANCE (Ω)
A channel LVDS differential pairs	D_AP(0:15), D_AN(0:15)	100 ±10% differential across each pair
	DCLK_AP, DCLK_AN	
	SCTRL_AP, SCTRL_AN	
B channel LVDS differential pairs	D_BP(0:15), D_BN(0:15)	100 ±10% differential across each pair
	DCLK_BP, DCLK_BN	
	SCTRL_BP, SCTRL_BN	

10.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends all signals follow the 0.005-inch/0.005-inch design rule. Minimum trace clearance from the ground ring around the PWB has a 0.10-inch minimum. Actual trace widths and clearances will be determined based on an analysis of impedance and stack-up requirements.

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Device Support

11.2.1 Device Nomenclature

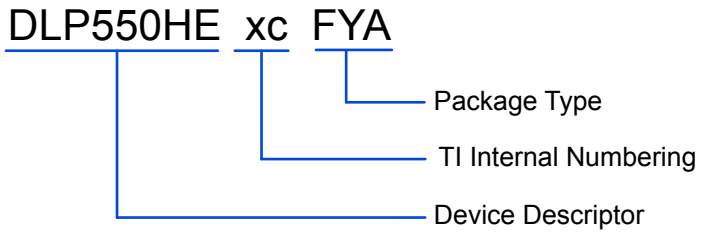

Figure 11-1. Part Number Description

11.2.2 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 11-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number.

Example: DLP550HEA0FYA

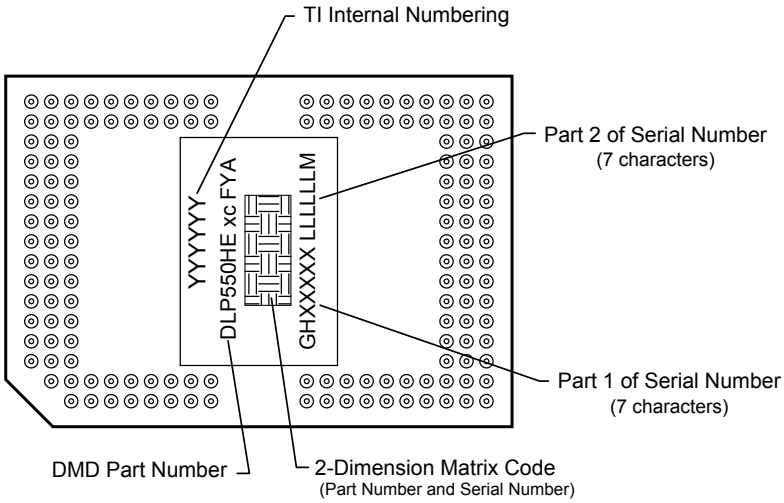

Figure 11-2. DMD Marking Locations

11.3 Documentation Support

11.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP550HE:

- *DLPC4430 Display Controller Data Sheet*
- *DLPA100 Power and Motor Driver Data Sheet*

- *DLPA200 Micromirror Driver Data Sheet*

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

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11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

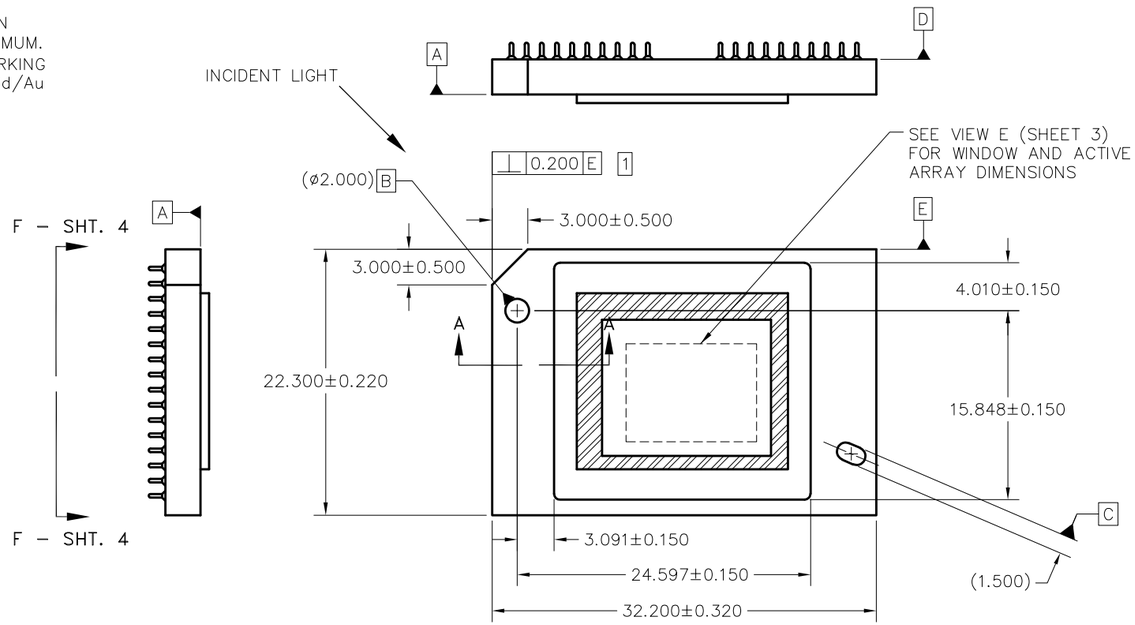
12 Mechanical, Packaging, and Orderable Information

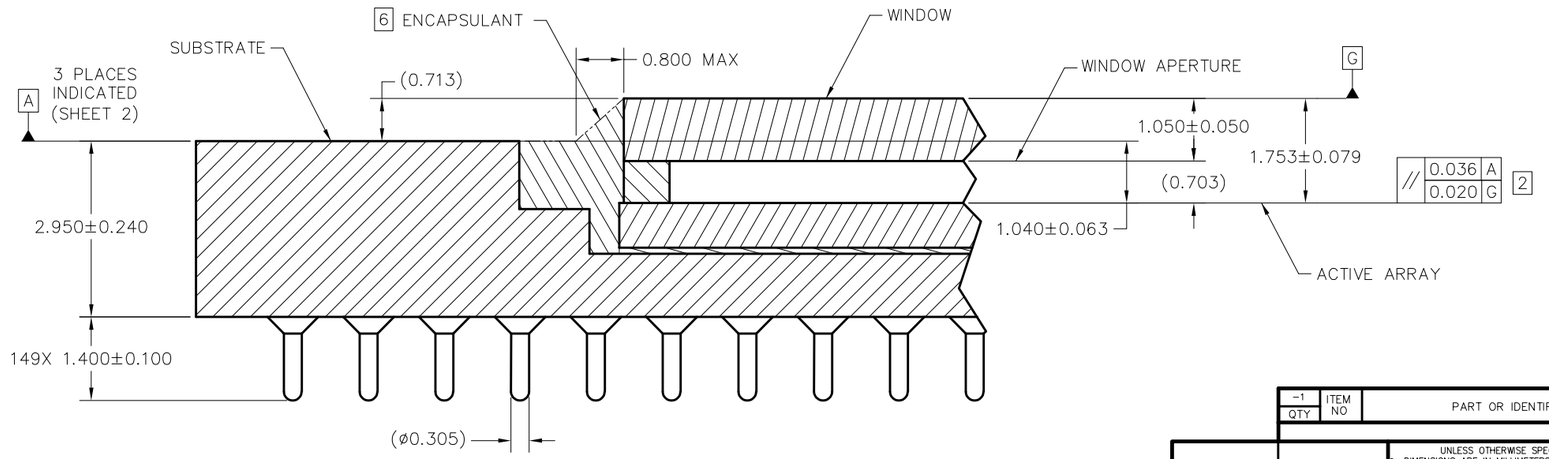
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2126839, INITIAL RELEASE	01/30/2013	F. ARMSTRONG
B	ECO 2135222, ADD NOTE 8 TO SHEETS 1 & 4	08/02/2013	F. ARMSTRONG

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.





SECTION A–A
SCALE 20/1

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

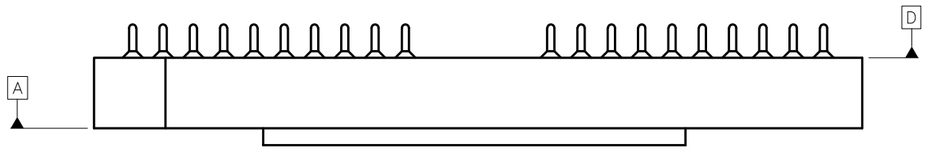
DWN	F. ARMSTRONG	DATE 01/30/13
ENGR	F. ARMSTRONG	01/30/13
QA	P. KONRAD	01/30/13
CQE	M. DORAK	01/30/13

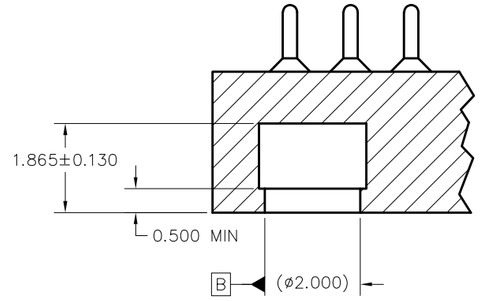
TEXAS INSTRUMENTS
Dallas, Texas

ICD, MECHANICAL, DMD
.55" SVGA LVDS V2 SERIES 450

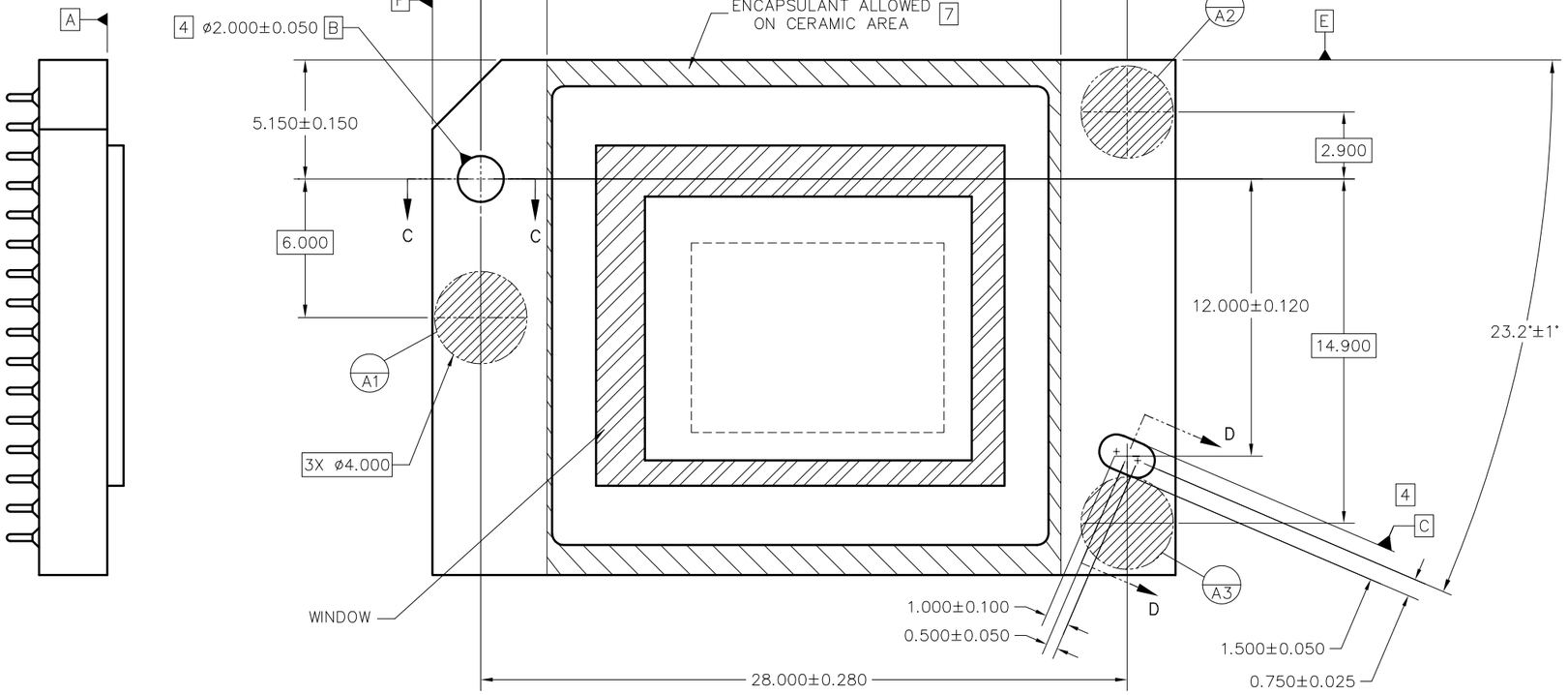
SIZE D | DRAWING NO 2512649 | REV B | SCALE 4/1 | SHEET 1 OF 4

ACED1g

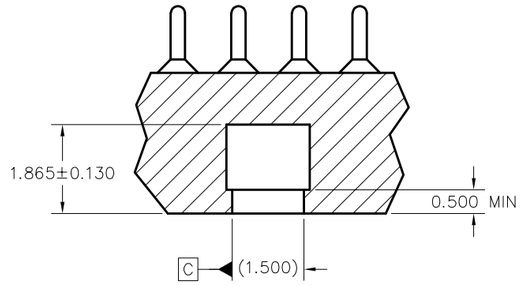




SECTION C–C
DATUM B
SCALE 16/1



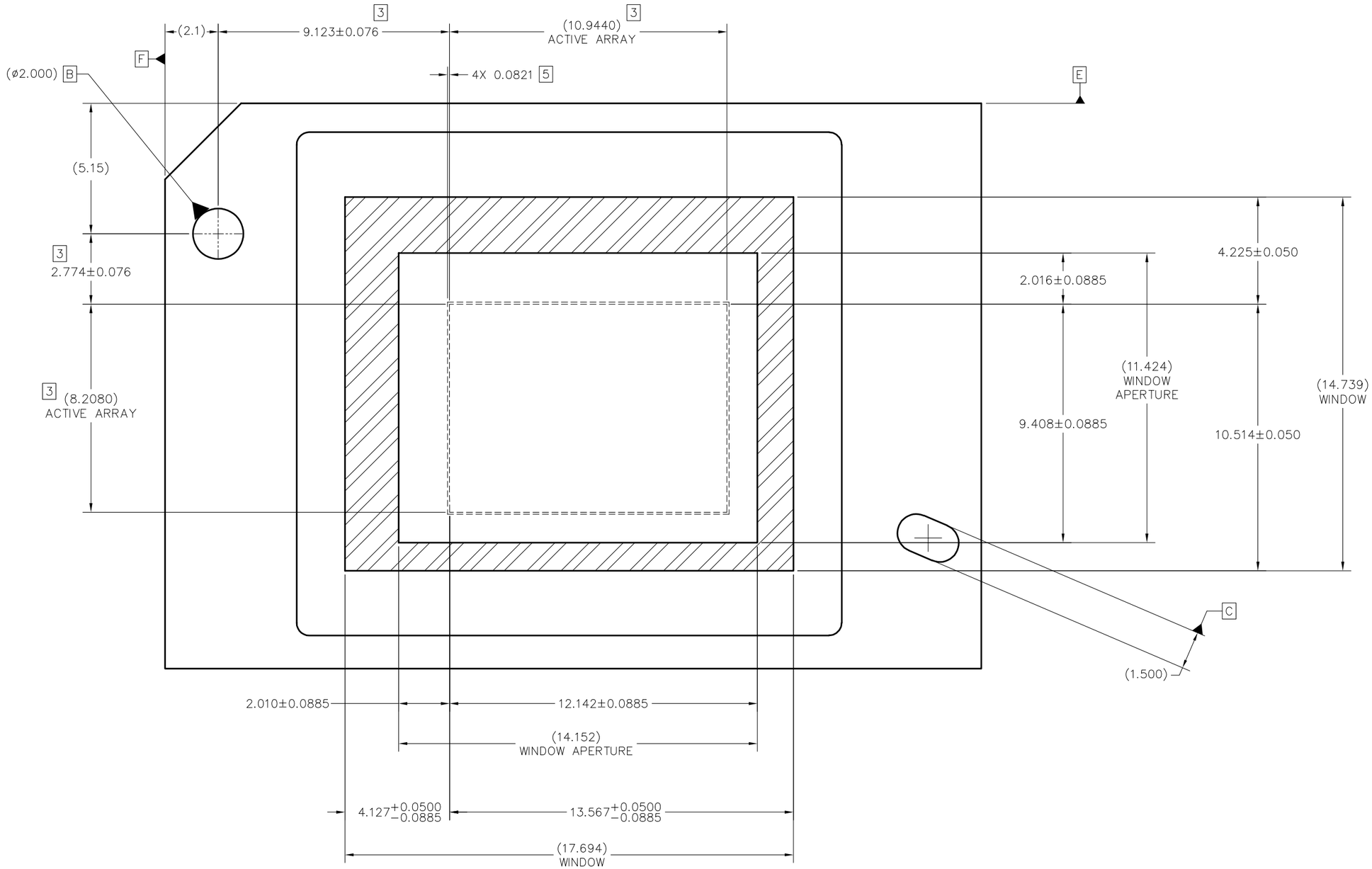
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

Texas Instruments, Dallas, Texas	DWN / DATE	SIZE D	DRAWING NO 2512649	REV B
	ISSUE DATE	SCALE 4/1	SHEET 2	

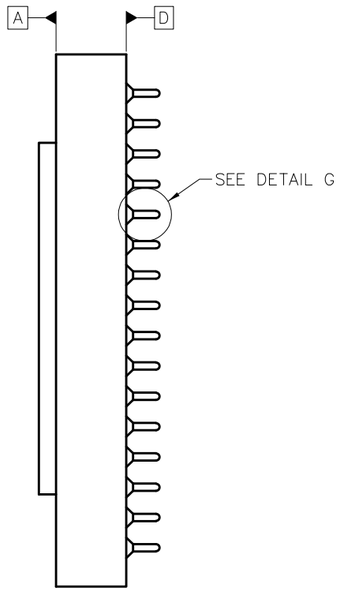
ACED2c

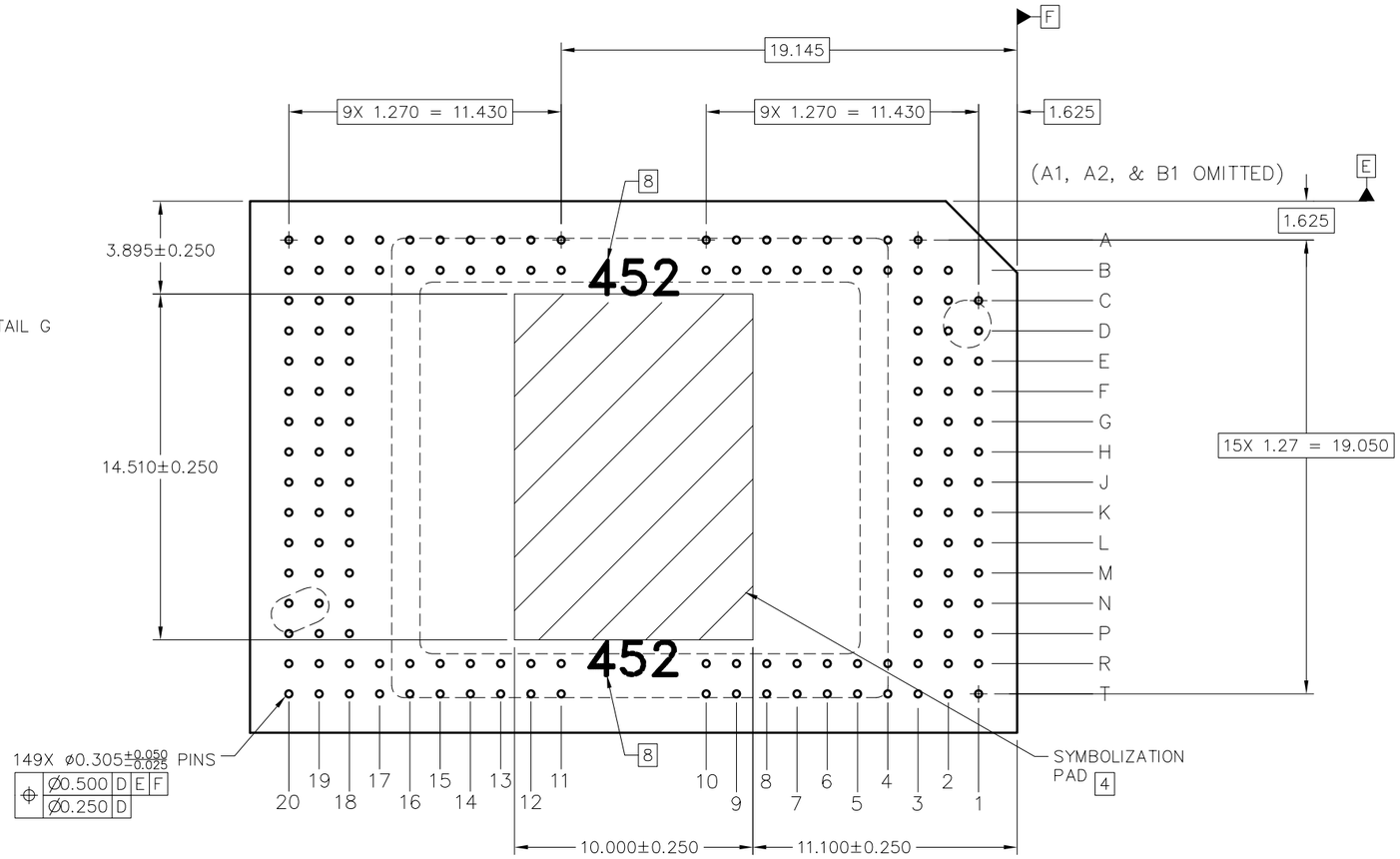


VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

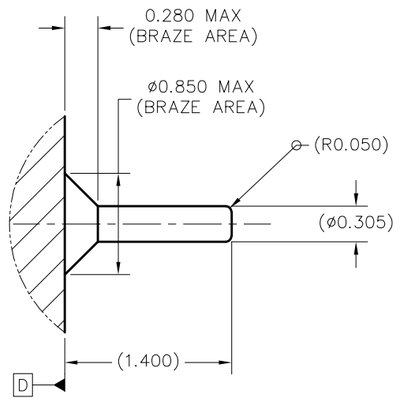
TEXAS INSTRUMENTS Dallas, Texas	DWN	DATE	SIZE D	DRAWING NO 2512649	REV B
	ISSUE DATE		SCALE 4/1	SHEET 3	

ACED2c





VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1



DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2512649	REV B
		SCALE 4/1	SHEET 4	

ACED2c

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP550HEA0FYA	ACTIVE	CPGA	FYA	149	33	RoHS & Green	NI-PD-AU	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

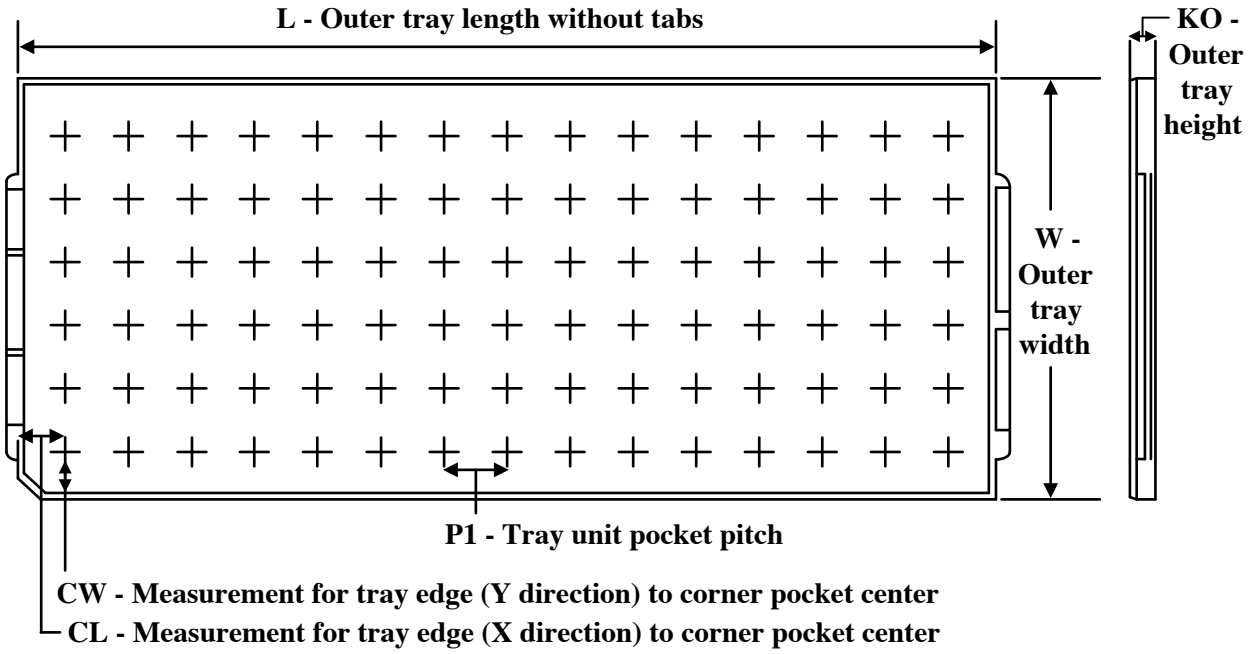
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP550HEA0FYA	FYA	CPGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45

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