

SN74LVC1G08 単一 2 入力の正論理 AND ゲート

1 特長

- 0.64mm²、0.5mm ピッチの超小型パッケージ (DPW) で供給
- 5V V_{CC} 動作をサポート
- 5.5V までの入力電圧に対応
- V_{CC} への降圧変換をサポート
- 最大 t_{pd} : 3.6ns (3.3V 時)
- 低消費電力、最大 I_{CC} 10μA
- 3.3V において ±24mA の出力駆動能力
- I_{off} により活線挿抜、部分的パワーダウン・モード、バック・ドライブ保護をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
 - 2000V、人体モデル (A114-A)
 - 200V、マシン・モデル (A115-A)
 - 1000V、荷電デバイス・モデル (C101)

2 アプリケーション

- ATCA ソリューション
- アクティブ・ノイズ・キャンセレーション (ANC)
- バーコード・スキャナ
- 血圧計
- CPAP マシン
- ケーブル・ソリューション
- DLP 3D マシン・ビジョン、ハイパースペクトル画像処理、光ネットワーク、分光法
- eBook (電子書籍)
- 組み込み PC
- フィールド・トランスミッタ：温度または圧力センサ
- 指紋認証
- HVAC：暖房、換気、空調
- ネットワーク接続ストレージ (NAS)
- サーバーのマザーボードおよび PSU
- ソフトウェア定義無線 (SDR)
- テレビ：高解像度 (HDTV)、LCD、デジタル
- ビデオ通信システム
- ワイヤレス・データ・アクセス・カード、ヘッドセット、キーボード、マウス、LAN カード
- X 線：手荷物スキャナ、医療用、歯科用

3 概要

この単一 2 入力の正 AND ゲートは、1.65V～5.5V の V_{CC} で動作するように設計されています。

SN74LVC1G08 デバイスは、ブール関数 $Y = A \cdot B$ or $Y = \overline{A + B}$ を正論理で実行します。

CMOS デバイスは出力駆動能力が大きく、広い V_{CC} 動作範囲にわたって、静止電力消費が低く保たれます。

SN74LVC1G08 は、本体サイズ 0.8mm × 0.8mm の超小型 DPW パッケージなど、各種のパッケージで供給されます。

製品情報⁽¹⁾

| 型番 | パッケージ | 本体サイズ |
|-------------|------------|----------------|
| SN74LVC1G08 | SOT-23 (5) | 2.9mm × 1.6mm |
| | SC70 (5) | 2.0mm × 1.25mm |
| | X2SON (4) | 0.8mm × 0.8mm |
| | SON (6) | 1.45mm × 1.0mm |
| | SON (6) | 1.0mm × 1.0mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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4 改訂履歴

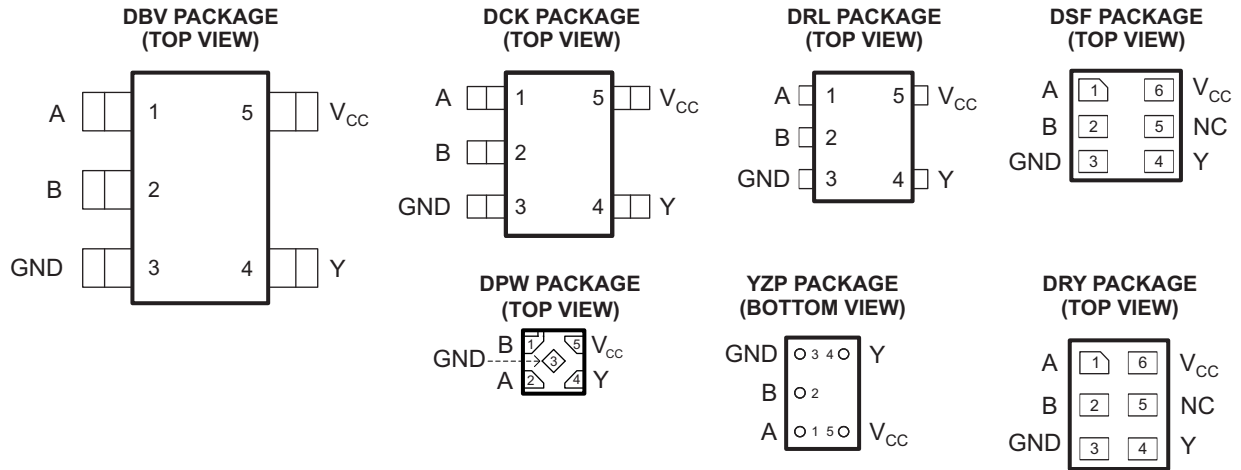
| Revision Y (April 2014) から Revision Z に変更 | Page |
|---|-------------|
| • Added $T_J(\text{max})$ spec to Absolute Maximum Ratings table | 4 |
| • Moved T_{stg} spec from Handling Ratings table to Absolute Maximum Ratings table. | 4 |
| • Renamed Handling Ratings table to ESD Ratings table | 4 |

| Revision X (March 2014) から Revision Y に変更 | Page |
|--|-------------|
| • Updated Handling Ratings table. | 4 |
| • Added Thermal Information table. | 5 |
| • Added Typical Characteristics. | 7 |
| • Added Detailed Description section. | 10 |
| • Added Application and Implementation section. | 11 |
| • Added Power Supply Recommendations section. | 12 |
| • Added Layout section. | 12 |

| Revision W (July 2013) から Revision X に変更 | Page |
|--|-------------|
| • 「アプリケーション」を追加 | 1 |
| • 「製品情報」表追加 | 1 |
| • Moved T_{stg} to Handling Ratings table. | 4 |

| Revision V (November 2012) から Revision W に変更 | Page |
|---|-------------|
| • Added parameter values for -40 to 125°C temperature ratings | 6 |

5 Pin Configuration and Functions



NC – No internal connection

See mechanical drawings for dimensions.

Pin Functions

| NAME | PIN | | | DESCRIPTION |
|-----------------|--------------------|----------|-----|---------------|
| | DBV, DCK, DRL, YZP | DRY, DSF | DPW | |
| A | 1 | 1 | 2 | Input |
| B | 2 | 2 | 1 | Input |
| GND | 3 | 3 | 3 | Ground |
| Y | 4 | 4 | 4 | Output |
| V _{CC} | 5 | 6 | 5 | Power pin |
| NC | | 5 | | Not connected |

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------------|---|--------------------|-----------------------|------|
| V _{CC} | Supply voltage range | –0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | –0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | –0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | –0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | –50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | –50 | mA |
| I _O | Continuous output current | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| T _{J(max)} | Junction temperature | | 150 | °C |
| T _{stg} | Storage temperature | –65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

| | | MIN | MAX | UNIT | |
|--------------------|-------------------------|--|-----|------|---|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|---|------------------------|------------------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 3 V to 3.6 V | 2 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | |
| | | V _{CC} = 3 V to 3.6 V | | 0.8 | |
| | | V _{CC} = 4.5 V to 5.5 V | | 0.3 × V _{CC} | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | V _{CC} | V | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | mA |
| | | V _{CC} = 2.3 V | | –8 | |
| | | V _{CC} = 3 V | | –16 | |
| | | V _{CC} = 4.5 V | | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 3 V | | 16 | |
| | | V _{CC} = 4.5 V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | V _{CC} = 3.3 V ± 0.3 V | | 10 | |
| | | V _{CC} = 5 V ± 0.5 V | | 5 | |
| T _A | Operating free-air temperature | –40 | 125 | °C | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74LVC1G08 | | | | | | UNIT | |
|-------------------------------|--|--------|--------|--------|--------|--------|------|------|
| | DBV | DCK | DRL | DRY | YZP | DPW | | |
| | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 5 PINS | 4 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 207.6 | 283.1 | 242.9 | 438.8 | 130 | 340 | °C/W |
| R _{θJctop} | Junction-to-case (top) thermal resistance | 145.2 | 92.3 | 77.5 | 276.8 | 54 | 215 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 53.5 | 60.9 | 77.5 | 271.7 | 51 | 294 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 37.5 | 1.7 | 9.6 | 83.8 | 1 | 41 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 53.1 | 60.1 | 77.3 | 271.4 | 50 | 294 | °C/W |
| R _{θJcbot} | Junction-to-case (bottom) thermal resistance | – | – | – | – | – | 250 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#)

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | –40°C to 85°C | | | –40°C to 125°C RECOMMENDED | | | UNIT |
|------------------|---------------------------|--|-----------------------|--------------------|-----|----------------------------|-----|-----|------|
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP | MAX | |
| V _{OH} | I _{OH} = –100 μA | 1.65 V to 5.5 V | V _{CC} – 0.1 | | | V _{CC} – 0.15 | | | V |
| | I _{OH} = –4 mA | 1.65 V | 1.2 | | | 1.2 | | | |
| | I _{OH} = –8 mA | 2.3 V | 1.9 | | | 1.9 | | | |
| | I _{OH} = –16 mA | 3 V | 2.4 | | | 2.4 | | | |
| | I _{OH} = –24 mA | | 2.3 | | | 2.3 | | | |
| | I _{OH} = –32 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 5.5 V | 0.1 | | | 0.1 | | | V |
| | I _{OL} = 4 mA | 1.65 V | 0.45 | | | 0.45 | | | |
| | I _{OL} = 8 mA | 2.3 V | 0.3 | | | 0.3 | | | |
| | I _{OL} = 16 mA | 3 V | 0.4 | | | 0.4 | | | |
| | I _{OL} = 24 mA | | 0.55 | | | 0.55 | | | |
| | I _{OL} = 32 mA | 4.5 V | 0.55 | | | 0.55 | | | |
| I _I | A or B inputs | V _I = 5.5 V or GND | 0 to 5.5 V | | | ±5 | | | μA |
| I _{off} | | V _I or V _O = 5.5 V | 0 | | | ±10 | | | μA |
| I _{CC} | | V _I = 5.5 V or GND, I _O = 0 | 1.65 V to 5.5 V | | | 10 | | | μA |
| ΔI _{CC} | | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 3 V to 5.5 V | | | 500 | | | μA |
| C _i | | V _I = V _{CC} or GND | 3.3 V | | | 4 | | | pF |

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to 85°C | | | | | | | | UNIT |
|-----------------|--------------|-------------|----------------------------------|-----|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|------|
| | | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | 1.5 | 7.2 | 0.7 | 4.4 | 0.8 | 3.6 | 0.8 | 3.4 | ns |

6.7 Switching Characteristics, 1.8 V and 2.5 V⁽¹⁾

over recommended operating free-air temperature range, (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to 85°C | | –40°C to 125°C | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|-----------------|--------------|-------------|----------------------------------|-----|----------------------------------|-----|---------------------------------|-----|---------------------------------|-----|------|
| | | | RECOMMENDED | | RECOMMENDED | | RECOMMENDED | | RECOMMENDED | | |
| | | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.5 V ± 0.2 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | 2.4 | 8 | 2.4 | 10 | 1.1 | 5.5 | 1.1 | 7 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, 3.3 V and 5 V⁽¹⁾

over recommended operating free-air temperature range, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 85°C | | -40°C to 125°C | | -40°C to 85°C | | -40°C to 125°C | | UNIT |
|-----------|--------------|-------------|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|-------------------------------|---|------|
| | | | | | RECOMMENDED | | | | RECOMMENDED | | |
| | | | $V_{CC} = 3.3$ V ± 0.3 V | | $V_{CC} = 3.3$ V ± 0.3 V | | $V_{CC} = 5$ V ± 0.5 V | | $V_{CC} = 5$ V ± 0.5 V | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t_{pd} | A or B | Y | 1 | 4.5 | 1 | 6 | 1 | 4 | 1 | 5 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CC} = 1.8$ V | $V_{CC} = 2.5$ V | $V_{CC} = 3.3$ V | $V_{CC} = 5$ V | UNIT |
|--|-----------------|------------------|------------------|------------------|----------------|------|
| | | TYP | TYP | TYP | TYP | |
| C_{pd} Power dissipation capacitance | $f = 10$ MHz | 21 | 24 | 26 | 31 | pF |

6.10 Typical Characteristics

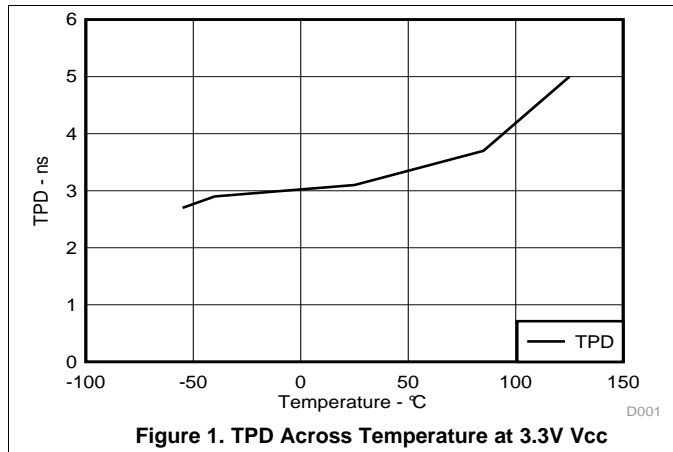


Figure 1. TPD Across Temperature at 3.3V Vcc

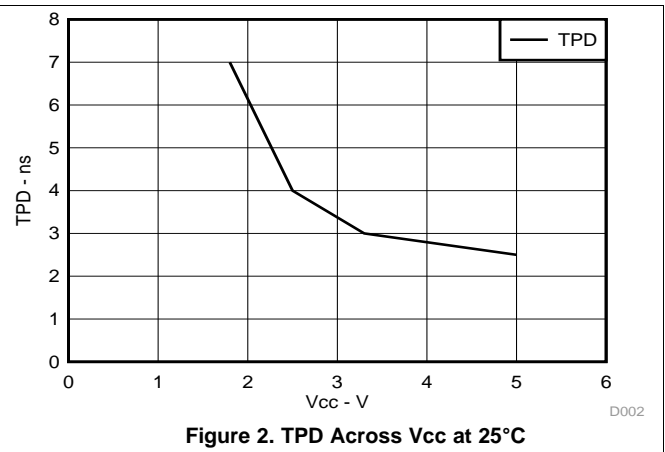
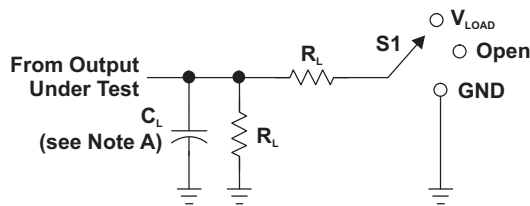


Figure 2. TPD Across Vcc at 25°C

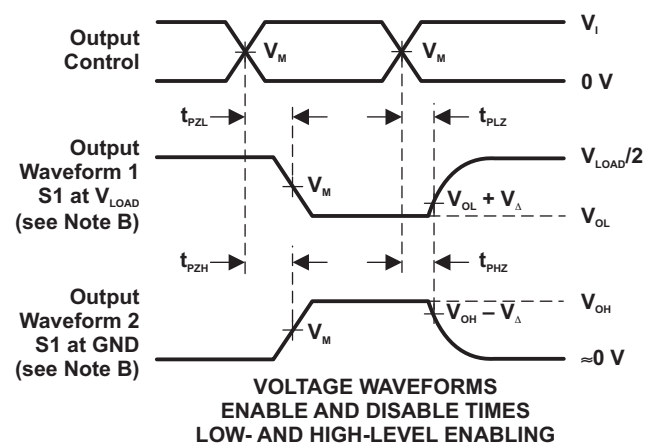
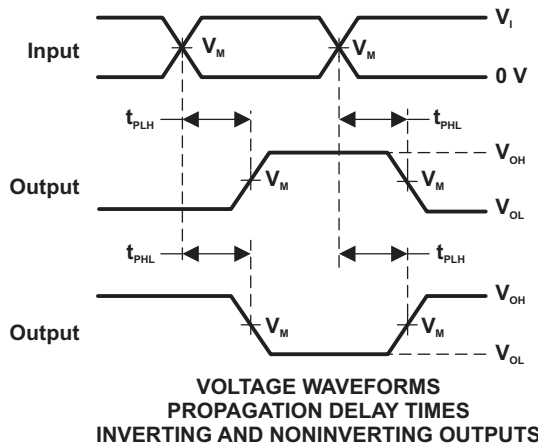
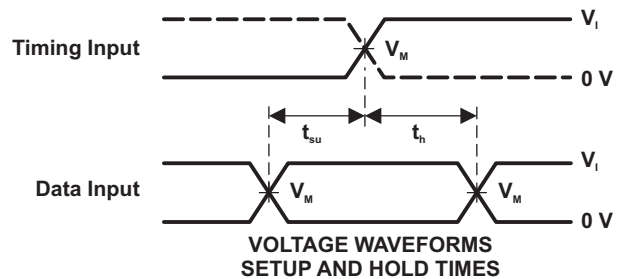
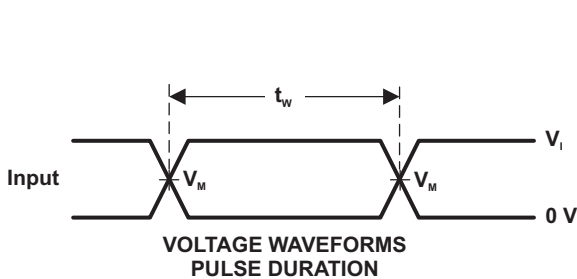
7 Parameter Measurement Information



LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

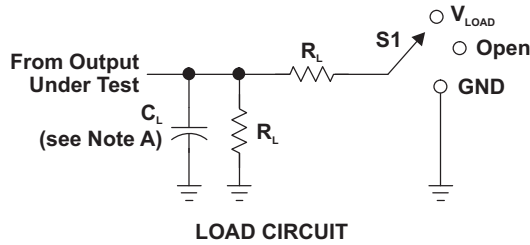
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_Δ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|------------|
| | V_i | t_i/t_r | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 1 M Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.3 V |



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

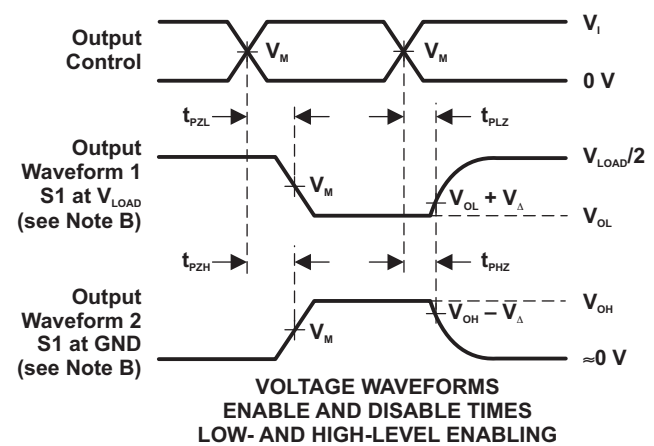
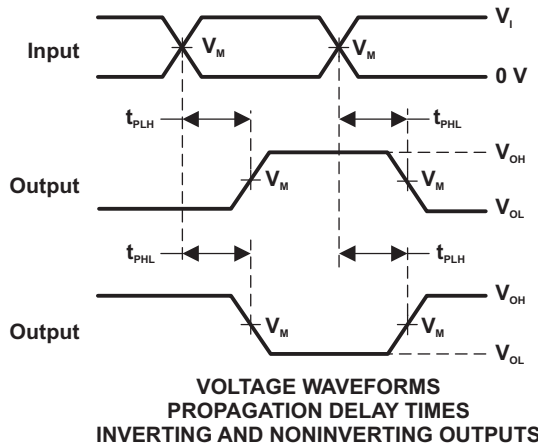
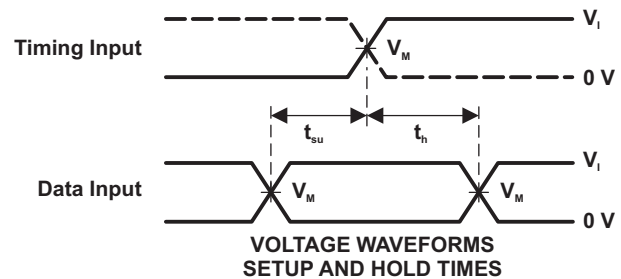
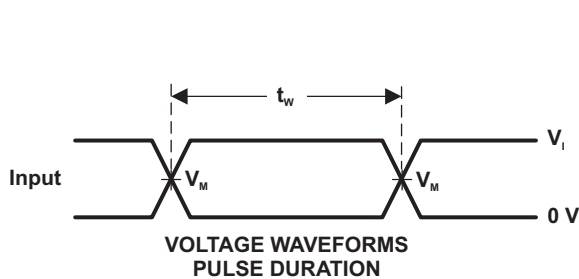
Figure 3. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{on} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G08 device contains one 2-input positive AND gate device and performs the Boolean function $Y = A \cdot B$ or $Y = \overline{A + B}$. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V.

8.4 Device Functional Modes

Table 1. Function Table

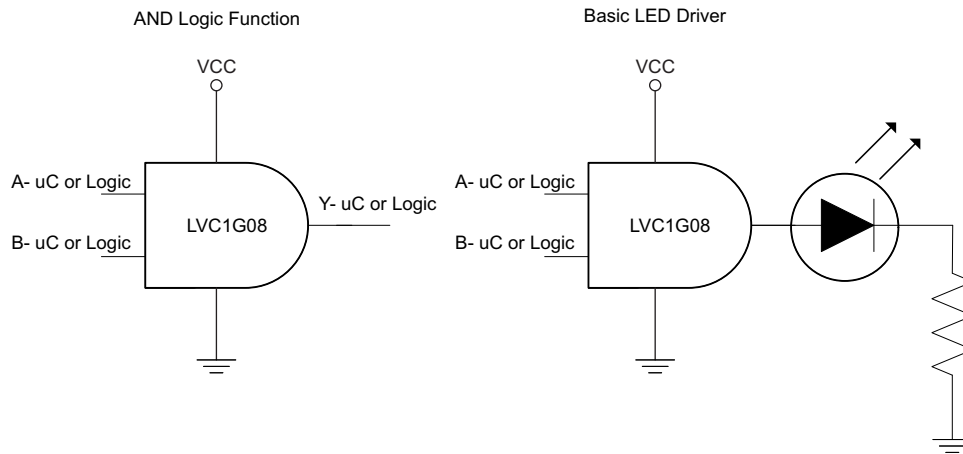
| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | H | H |
| L | X | L |
| X | L | L |

9 Application and Implementation

9.1 Application Information

The SN74LVC1G08 is a high drive CMOS device that can be used for implementing AND logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC} .

9.2 Typical Application



9.2.1 Design Requirements

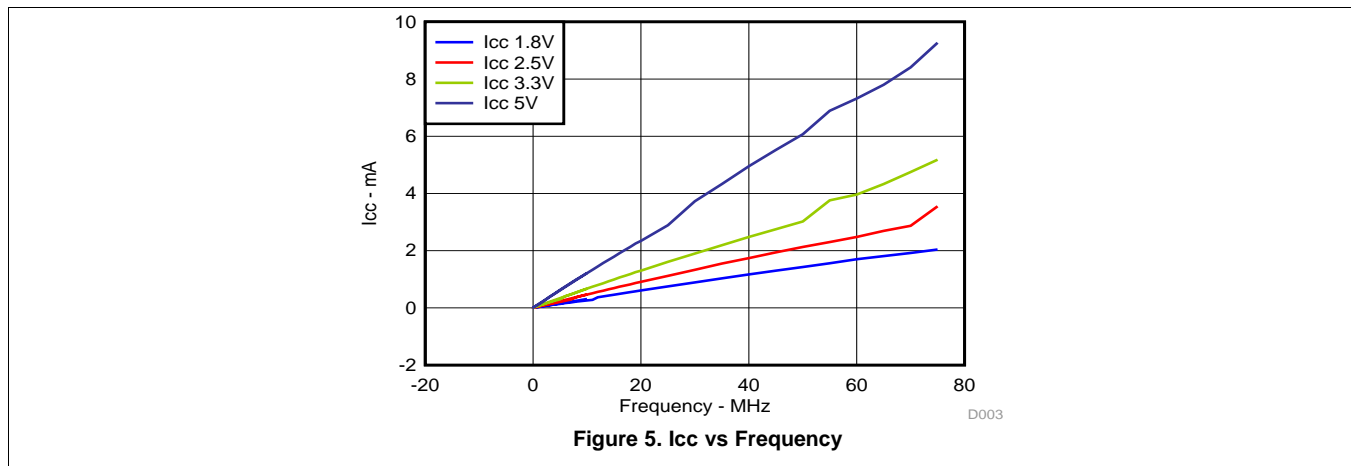
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the [Recommended Operating Conditions](#) table at any valid V_{CC} .
2. Recommended Output Conditions
 - Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

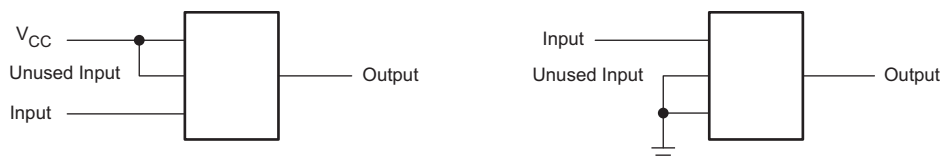
Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended and if there are multiple Vcc pins then 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or Vcc whichever make more sense or is more convenient.

11.2 Layout Example



12 デバイスおよびドキュメントのサポート

12.1 商標

All trademarks are the property of their respective owners.

12.2 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|---|-------------------------|
| SN74LVC1G08DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (C085, C08F, C08J, C08K, C08R, C 08T) (C08P, C08S) | Samples |
| SN74LVC1G08DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C08 C08P | Samples |
| SN74LVC1G08DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | C08 C08P | Samples |
| SN74LVC1G08DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (C085, C08F, C08J, C08K, C08R) (C08H, C08P, C08S) | Samples |
| SN74LVC1G08DBVTE4 | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C08 C08P | Samples |
| SN74LVC1G08DCK3 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Non-Green | SNBI | Level-1-260C-UNLIM | -40 to 125 | (CEF, CEZ) | Samples |
| SN74LVC1G08DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (CE5, CEF, CEJ, CE K, CER, CET) (CEH, CEP, CES) | Samples |
| SN74LVC1G08DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CE5 CES | Samples |
| SN74LVC1G08DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CE5 CES | Samples |
| SN74LVC1G08DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (CE5, CEF, CEJ, CE K, CER, CET) (CEH, CEP, CES) | Samples |
| SN74LVC1G08DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CE5 CES | Samples |
| SN74LVC1G08DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CE5 CES | Samples |
| SN74LVC1G08DPWR | ACTIVE | X2SON | DPW | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | M4 | Samples |
| SN74LVC1G08DRLR | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (CE7, CER) | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC1G08DRLRG4 | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (CE7, CER) | Samples |
| SN74LVC1G08DRY2 | ACTIVE | SON | DRY | 6 | 5000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CE | Samples |
| SN74LVC1G08DRYR | ACTIVE | SON | DRY | 6 | 5000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CE | Samples |
| SN74LVC1G08DSF2 | ACTIVE | SON | DSF | 6 | 5000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CE | Samples |
| SN74LVC1G08DSFR | ACTIVE | SON | DSF | 6 | 5000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CE | Samples |
| SN74LVC1G08YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (CE, CE7) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G08 :

- Automotive : [SN74LVC1G08-Q1](#)
- Enhanced Product : [SN74LVC1G08-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G08DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DCKTG4 | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |
| SN74LVC1G08DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DRY2 | SON | DRY | 6 | 5000 | 180.0 | 8.4 | 1.65 | 1.2 | 0.7 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DRY2 | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.6 | 1.15 | 0.75 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G08DSF2 | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DSF2 | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.63 | 4.0 | 8.0 | Q3 |
| SN74LVC1G08DSFR | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G08YZPR | DSBGA | YZP | 5 | 3000 | 180.0 | 8.4 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G08DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G08DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G08DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G08DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G08DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G08DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G08DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G08DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G08DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G08DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G08DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G08DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G08DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G08DRY2 | SON | DRY | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G08DRY2 | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G08DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G08DSF2 | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G08DSF2 | SON | DSF | 6 | 5000 | 202.0 | 201.0 | 28.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G08DSFR | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G08YZPR | DSBGA | YZP | 5 | 3000 | 182.0 | 182.0 | 20.0 |

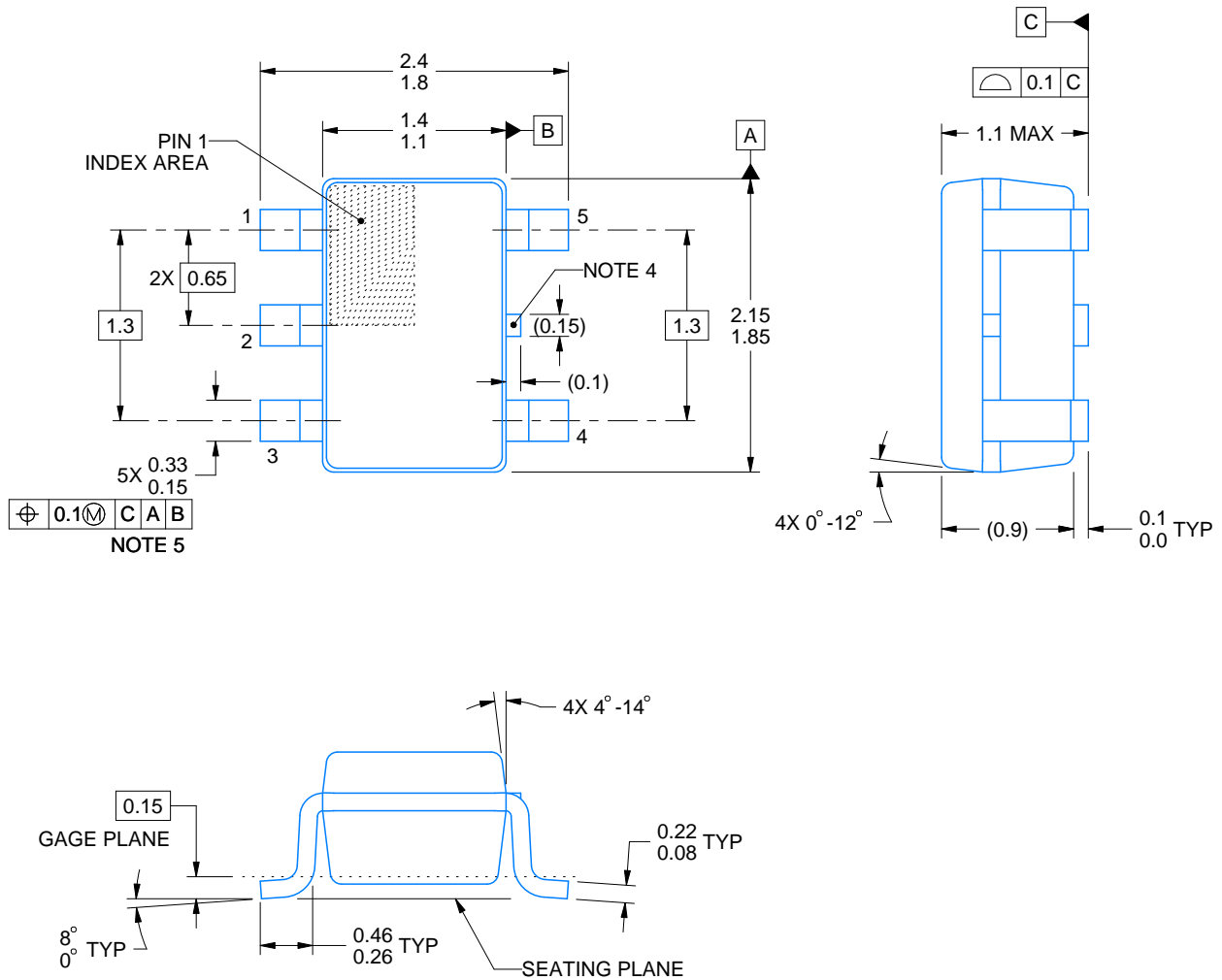
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

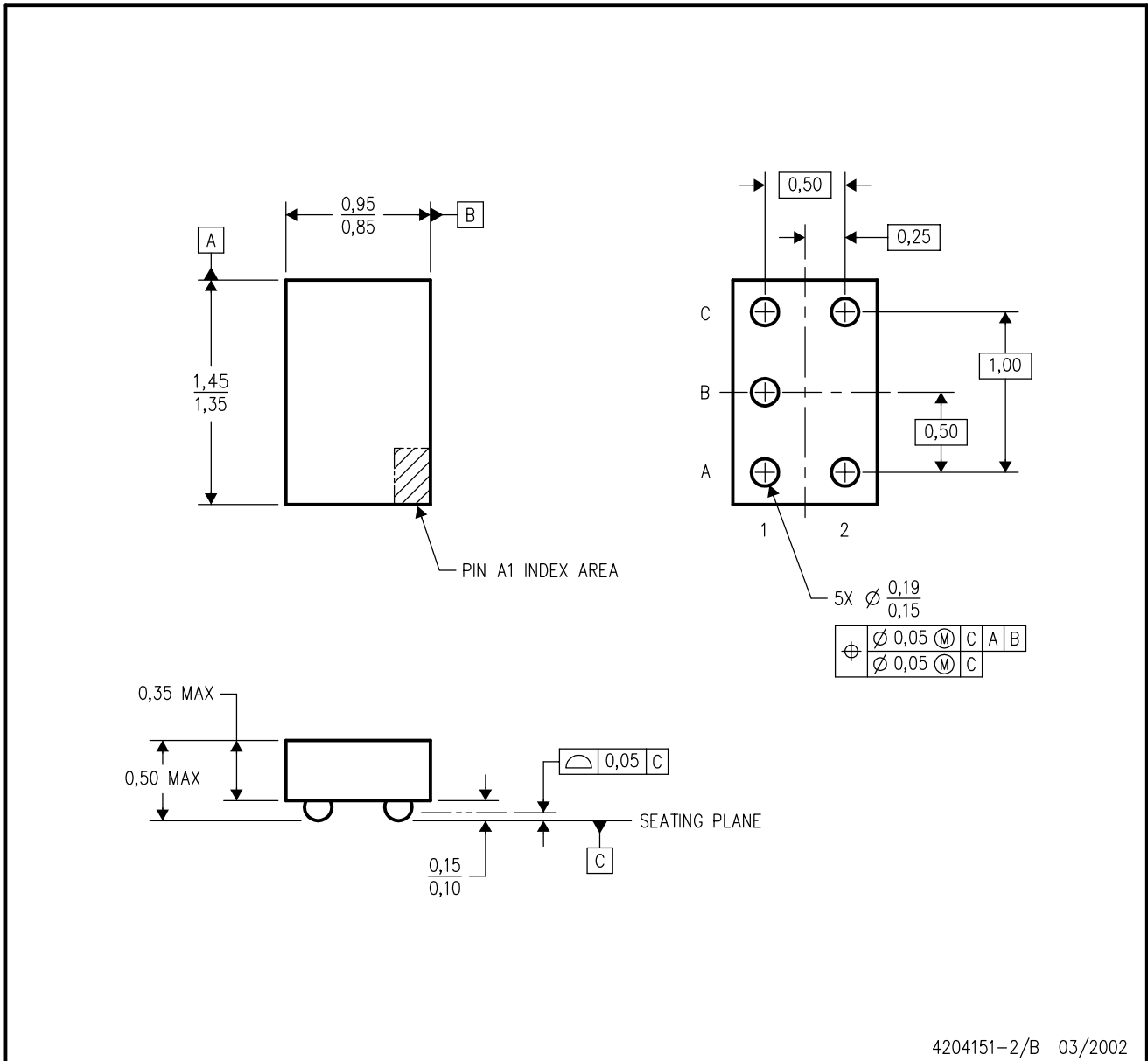
4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

GENERIC PACKAGE VIEW

DPW 5

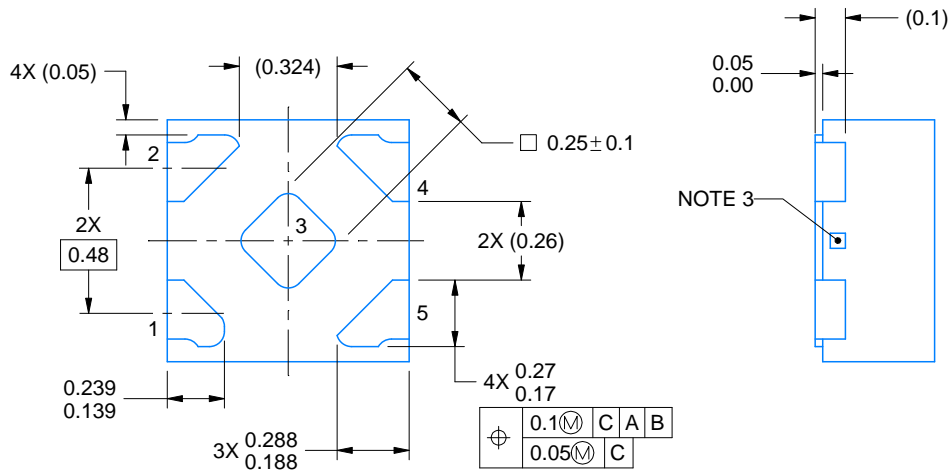
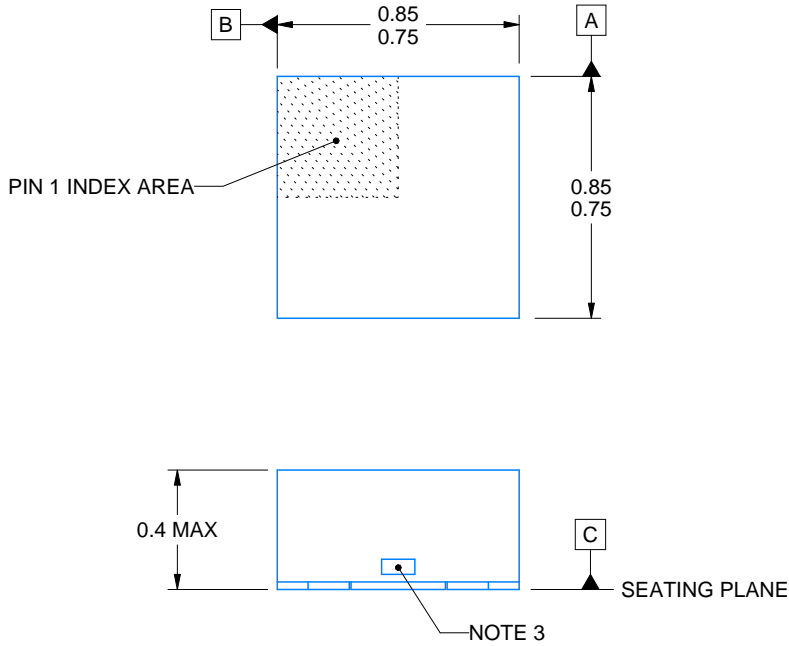
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

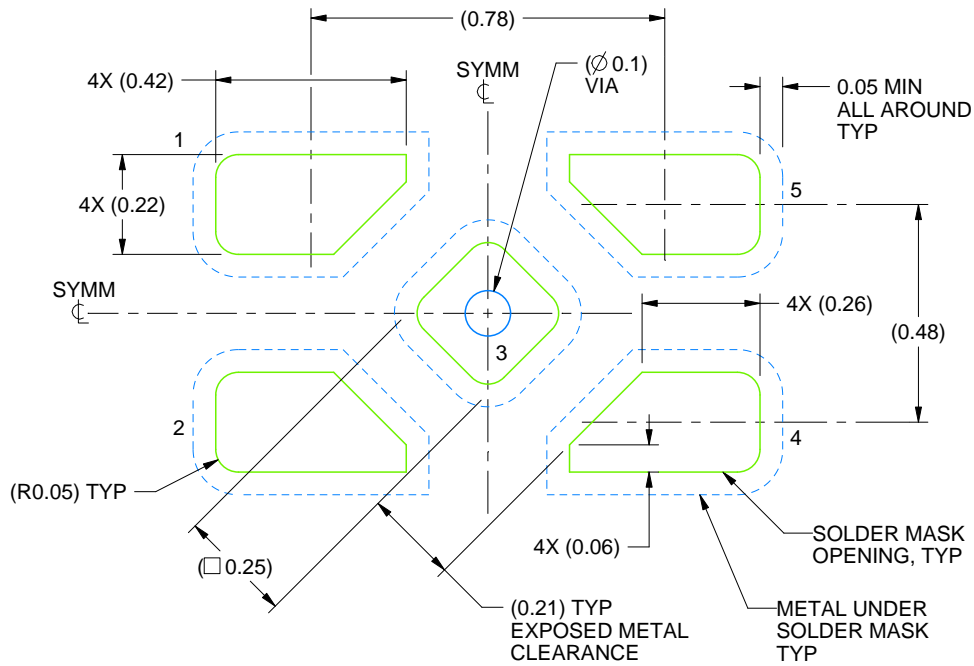
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sl原因271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

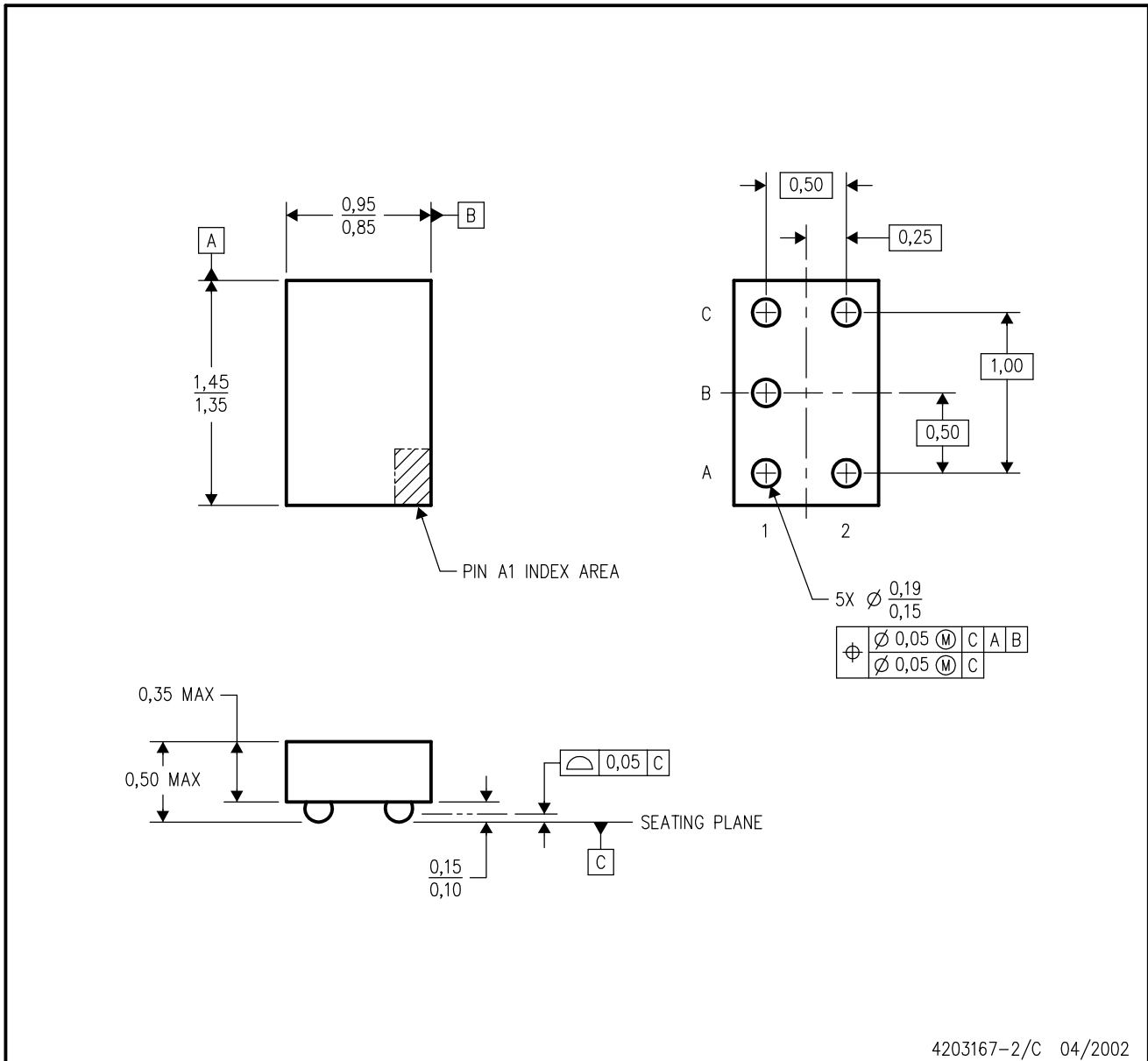
4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

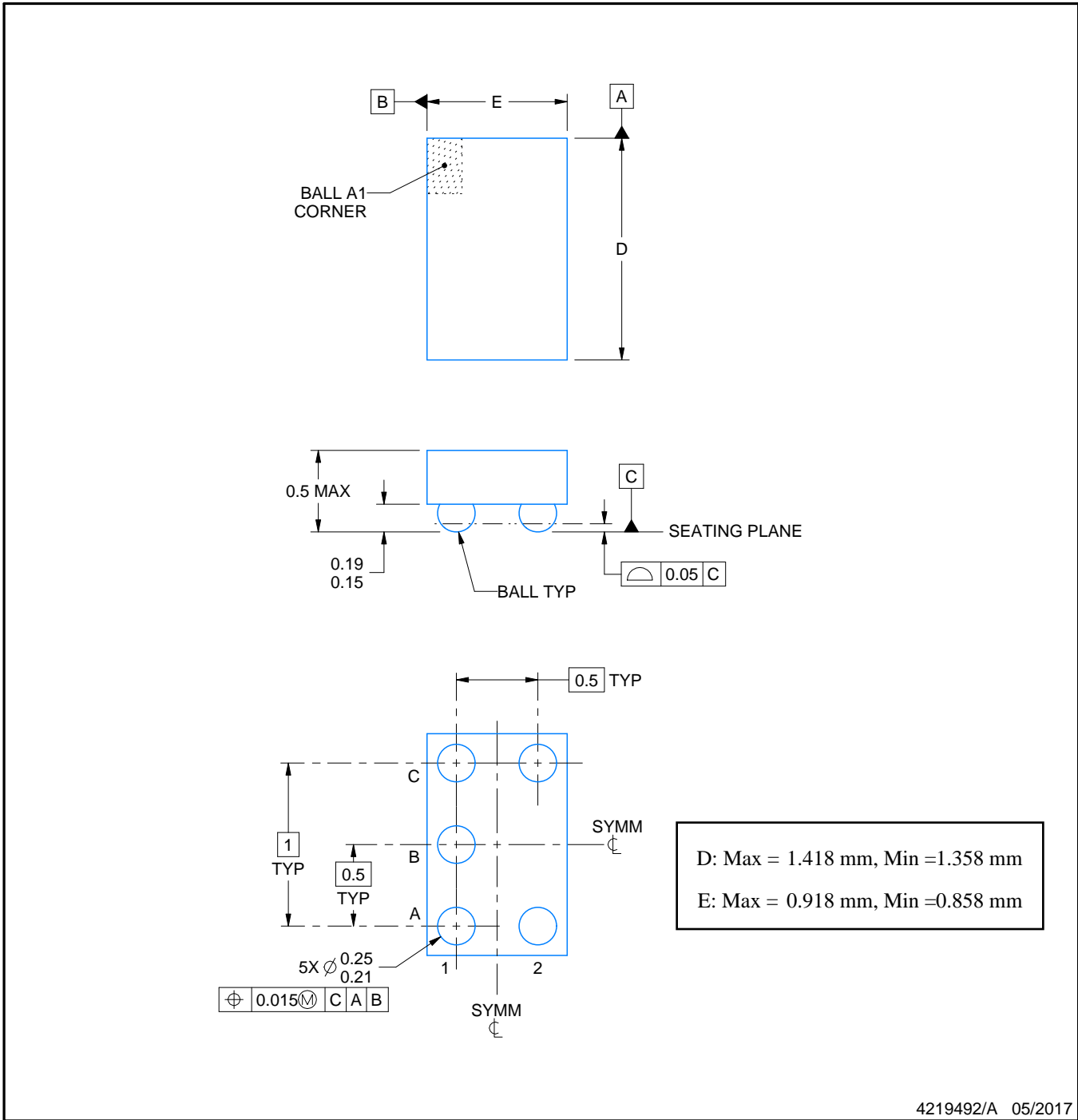
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



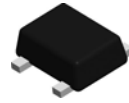
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

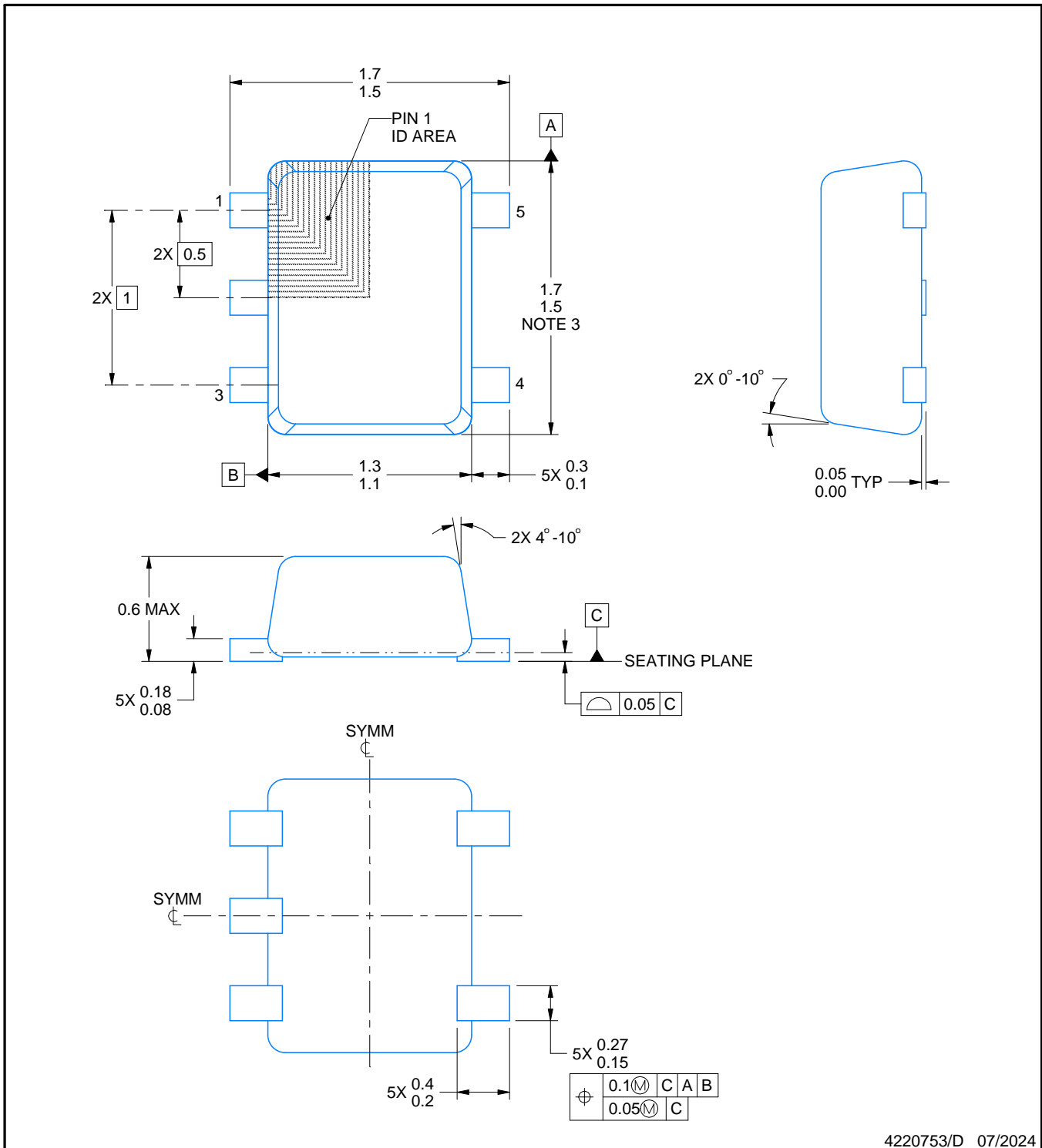
DRL0005A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/D 07/2024

NOTES:

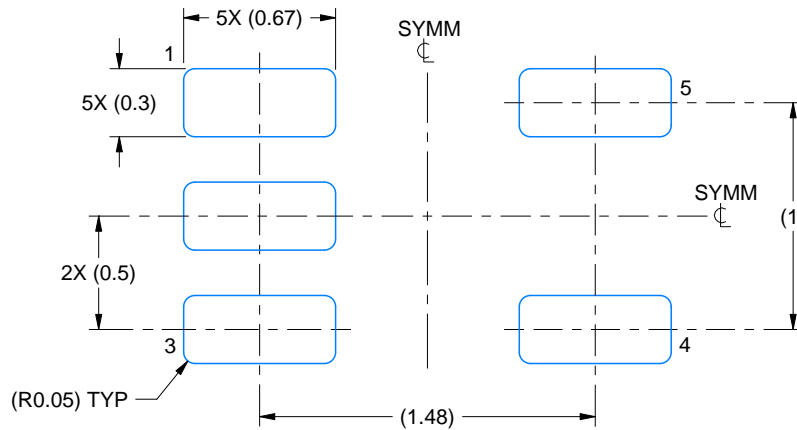
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

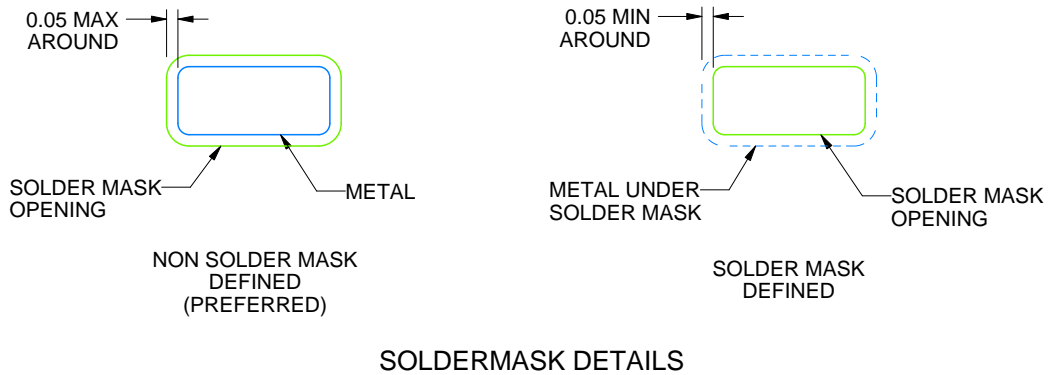
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/D 07/2024

NOTES: (continued)

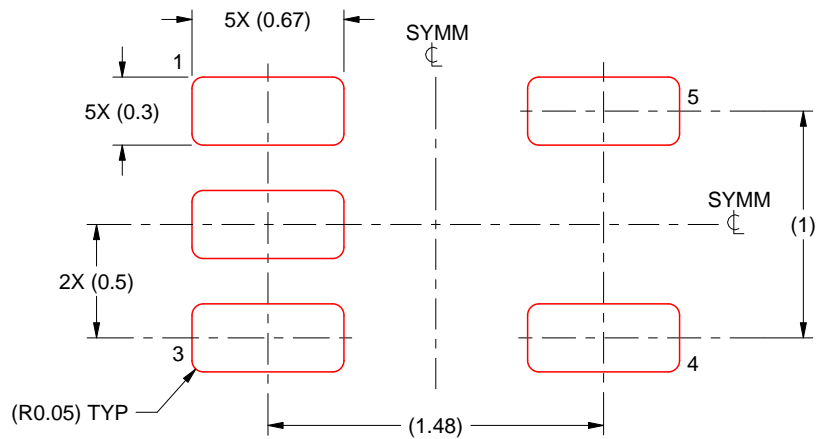
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

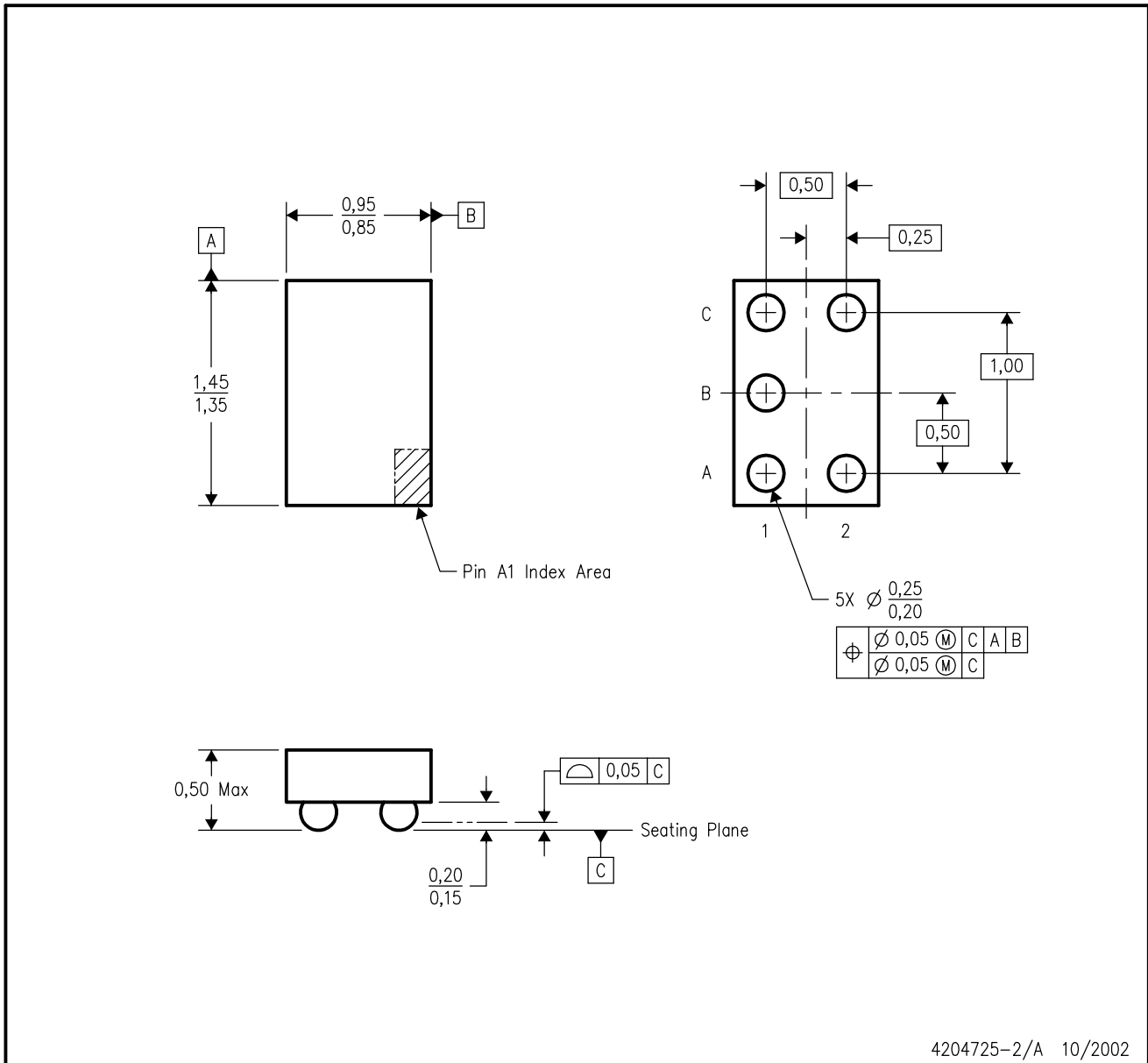
4220753/D 07/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

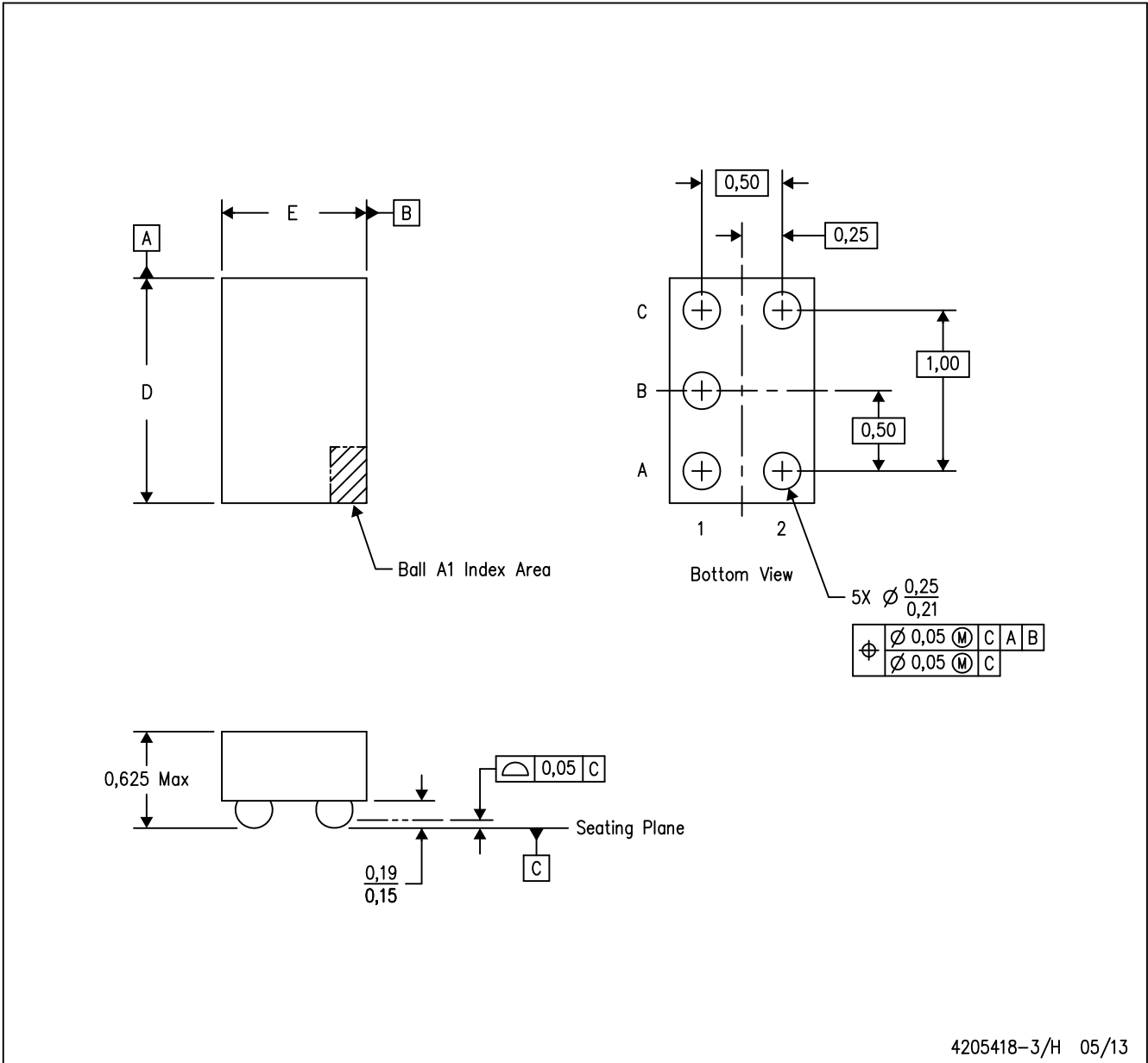


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

NanoStar is a trademark of Texas Instruments.

YZT (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

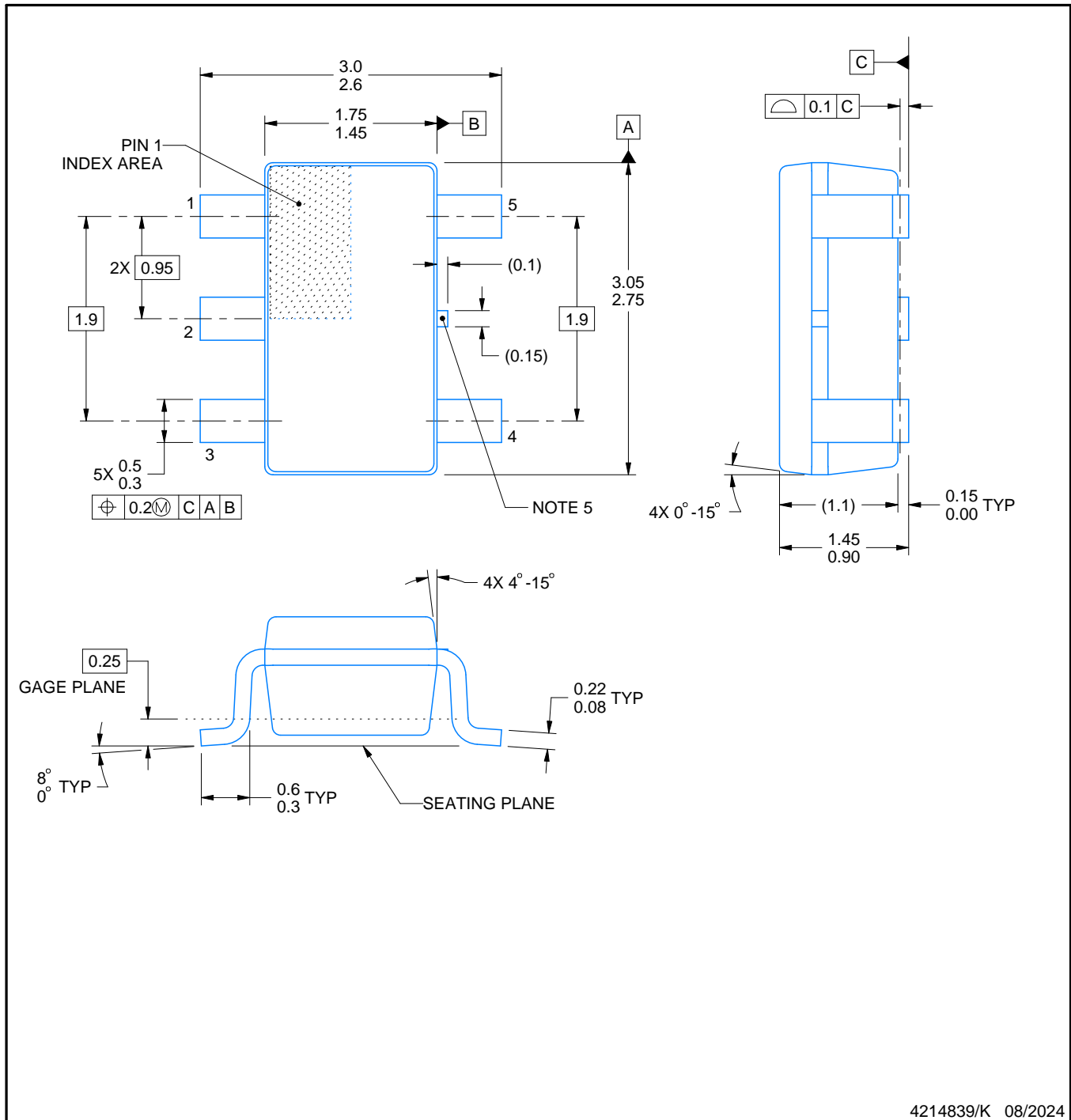
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

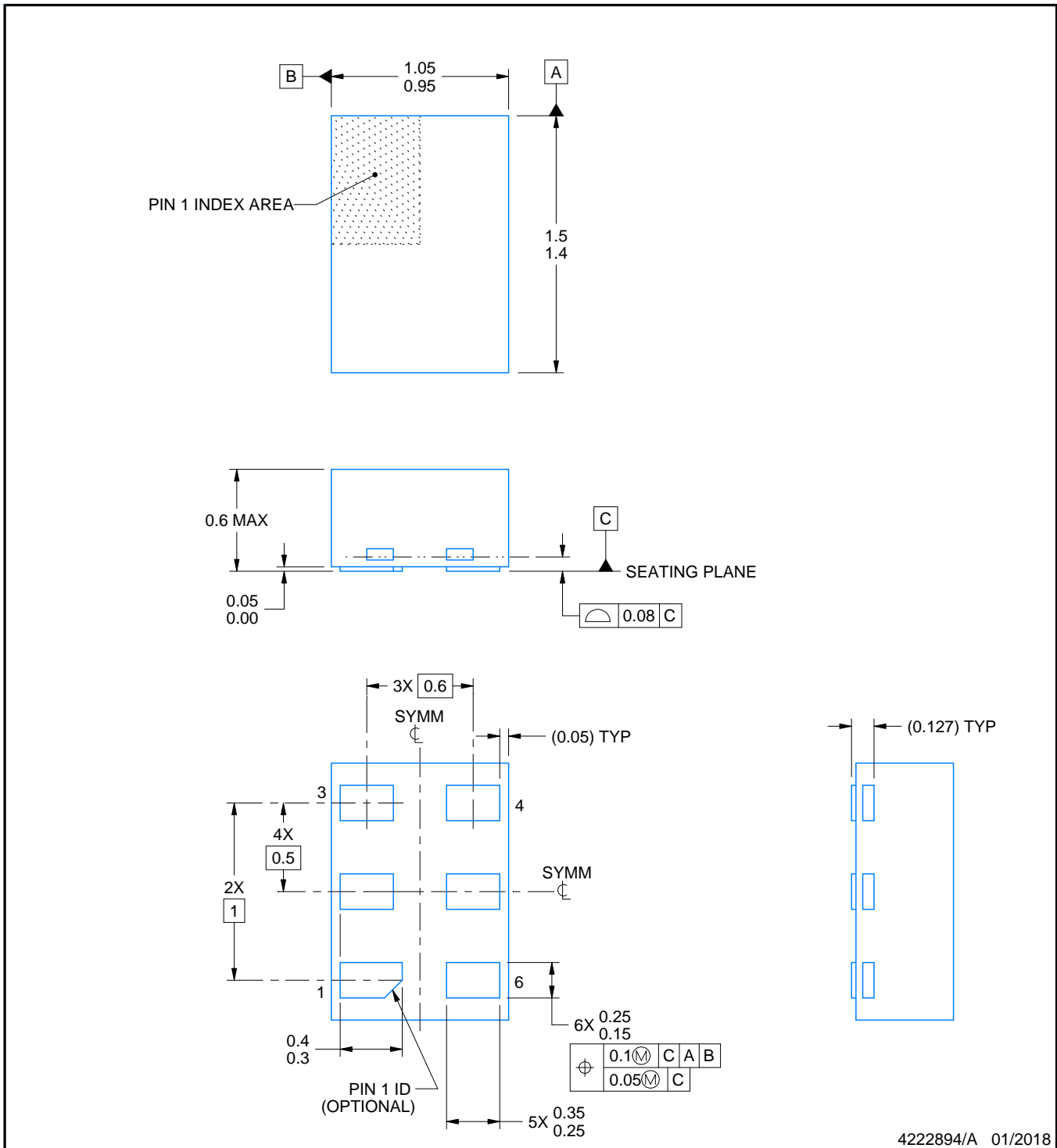
DRY0006A



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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