THS6212 差動広帯域 PLC ライン・ドライバ・アンプ

1 特長

- 低消費電力:
  - 完全バイアス モード:23mA
  - 中間バイアス モード:17.5mA
  - 低バイアス モード:11.9mA
  - 低消費電力のシャットダウン モード
  - IADJ ピンによる可変バイアス
- 低ノイズ:
  - 電圧ノイズ:2.5nV/√Hz
  - 反転電流ノイズ:18pA/√Hz
  - 非反転電流ノイズ:1.4pA/√Hz
- 低歪:
  - -86dBc HD2 (1MHz、100Ω 差動負荷)
  - -101dBc HD3 (1MHz、100Ω 差動負荷)
- 大出力電流:665mA 超 (25Ω 負荷)
- 大きな出力振幅:
  - $49V_{PP}$ (28V、100Ω 差動負荷)
- 広い帯域幅:205MHz (G_{DIFF} = 10V/V)
- PSRR:良好な絶縁時に 1MHz において 55dB 超
- 広い電源電圧範囲:10V～28V
- 過熱保護:175°C (標準値)
- 同相バッファを内蔵した代替デバイス:THS6222

2 アプリケーション

- 高電圧、大電流の駆動
- 広帯域幅の電力線通信

3 概要

THS6212 は、電流フィードバック アーキテクチャを採用した差動ライン ドライバ アンプです。このデバイスは広帯域の電力線通信 (PLC) ライン ドライバ アプリケーションでの使用を意図したもので、十分に高速なため、14.5dBm ライン電力で 30MHz までの伝送に対応できます。

THS6212 は独自のアーキテクチャにより、静止電流を最小限に抑えながら、非常に高い線形性を実現しています。フルバイアス条件での差動歪みは、1MHz で -86dBc、10MHz ではわずか -71dBc に低減されます。複数の固定バイアス設定があり、ライン長に応じてアンプの最大性能が必要ない場合は、電力をさらに削減できます。より柔軟性を増し、電力を削減するため、調整可能な電流ピン (IADJ) が用意されており、さらにバイアス電流を下げることができます。

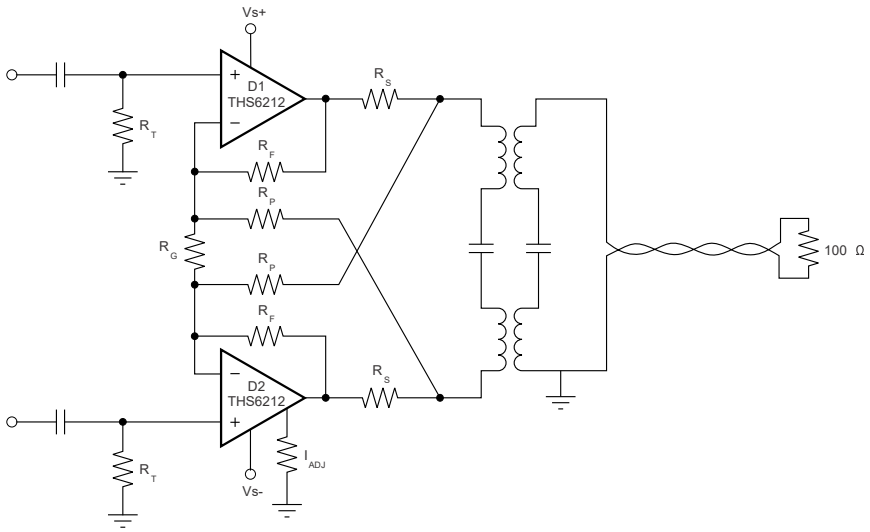
28V 電源での出力スイングが $49V_{PP}$ (100Ω 差動負荷) と広く、650mA 超の駆動電流 (25Ω 負荷) と合わせて、歪みを最小限に抑える広い動的ヘッドルームを実現します。

THS6212 は 24 ピンの VQFN パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
THS6212	RHF (VQFN、24)	5mm × 4mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



THS6212 を使用した代表的なライン ドライバ回路

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4 Pin Configuration and Functions

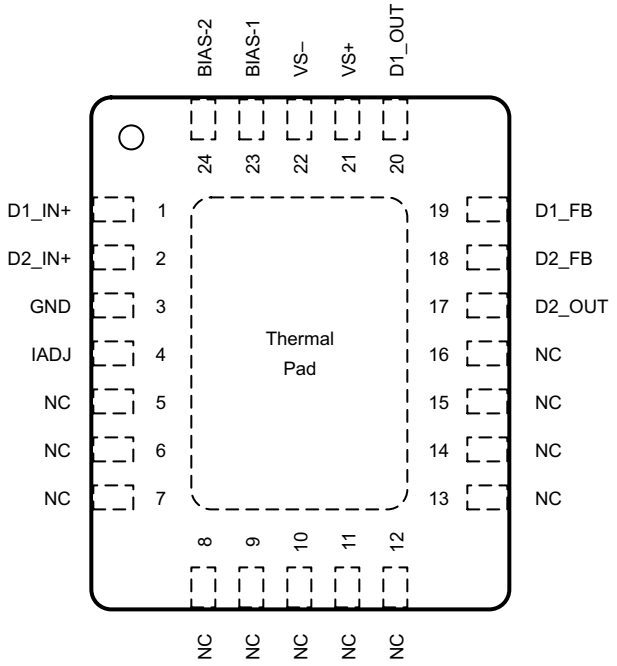


図 4-1. RHF Package, 24-Pin VQFN With Exposed Thermal Pad (Top View)

表 4-1. Pin Functions (1)

PIN		TYPE	DESCRIPTION
NAME	NO.		
BIAS-1	23	Input	Bias mode parallel control, LSB
BIAS-2	24	Input	Bias mode parallel control, MSB
D1_FB	19	Input	Amplifier D1 inverting input
D2_FB	18	Input	Amplifier D2 inverting input
D1_IN+	1	Input	Amplifier D1 noninverting input
D2_IN+	2	Input	Amplifier D2 noninverting input
D1_OUT	20	Output	Amplifier D1 output
D2_OUT	17	Output	Amplifier D2 output
GND(2)	3	Input/Output	Control pin ground reference
IADJ	4	Input/Output	Bias current adjustment pin
NC	5-16	—	No internal connection
VS–	22	Input/Output	Negative power-supply connection
VS+	21	Input/Output	Positive power-supply connection

(1) The THS6212 defaults to the shutdown (disable) state if a signal is not present on the bias pins.
(2) The GND pin ranges from VS– to (VS+ – 5 V).

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, $V_S = (V_{S+}) – (V_{S–})$		28	V
	Bias control pin voltage, referenced to GND pin	0	14.5	V
	All pins except VS+, VS–, and BIAS control	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
	Differential input voltage (each amplifier), V_{ID}		±2	V
Current	All input pins, current limit		±10	mA
	Continuous power dissipation(2)	See *Thermal Information* table		
Temperature	Maximum junction, T_J (under any condition)(3)		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The THS6212 incorporates a thermal pad on the underside of the device. This pad functions as a heat sink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which can permanently damage the device.
(3) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, $V_S = (V_{S+}) – (V_{S–})$	10		28	V
V_{GND}	GND pin voltage	$V_{S–}$		$V_{S+} – 5$	V
T_J	Operating junction temperature			125	°C
T_A	Ambient operating air temperature	–40	25	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		THS6212 RHF (VQFN) 24 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	42.3	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	32.8	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	20.9	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	3.8	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	20.9	°C/W

5.4 Thermal Information (続き)

THERMAL METRIC(1)		THS6212 RHF (VQFN) 24 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.5	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics V_S = 12 V

at T_A ≅ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 50 Ω, series isolation resistor (R_S) = 2.5 Ω each, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	A_V = 5 V/V, R_F = 1.5 kΩ, V_O = 2 V_{PP}			250		MHz
		A_V = 10 V/V, R_F = 1.24 kΩ, V_O = 2 V_{PP}			180		
		A_V = 15 V/V, R_F = 1 kΩ, V_O = 2 V_{PP}			165		
	0.1-dB bandwidth flatness				17		MHz
LSBW	Large-signal bandwidth	V_O = 16 V_{PP}			195		MHz
SR	Slew rate (20% to 80%)	V_O = 16-V step			5500		V/µs
	Rise and fall time (10% to 90%)	V_O = 2 V_{PP}			2.1		ns
HD2	2nd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 50 Ω	Full bias, f = 1 MHz		–80		dBc
			Mid bias, f = 1 MHz		–78		
			Low bias, f = 1 MHz		–78		
			Full bias, f = 10 MHz		–61		
			Mid bias, f = 10 MHz		–61		
			Low bias, f = 10 MHz		–61		
HD3	3rd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 50 Ω	Full bias, f = 1 MHz		–90		dBc
			Mid bias, f = 1 MHz		–86		
			Low bias, f = 1 MHz		–83		
			Full bias, f = 10 MHz		–69		
			Mid bias, f = 10 MHz		–65		
			Low bias, f = 10 MHz		–62		
e_n	Differential input voltage noise	f ≥ 1 MHz, input-referred			2.5		nV/√Hz
i_{n+}	Noninverting input current noise	f ≥ 1 MHz, each amplifier			1.4		pA/√Hz
i_{n-}	Inverting input current noise	f ≥ 1 MHz, each amplifier			18		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain				1300		kΩ
	Input offset voltage (each amplifier)				±12		mV
		T_A = –40°C			±16		
		T_A = 85°C			±11		
	Noninverting input bias current				±1		µA
		T_A = –40°C			±1		
		T_A = 85°C			±1		
	Inverting input bias current				±8		µA
		T_A = –40°C			±7		
		T_A = 85°C			±4		
INPUT CHARACTERISTICS							

5.5 Electrical Characteristics V_S = 12 V (続き)

at T_A ≅ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 50 Ω, series isolation resistor (R_S) = 2.5 Ω each, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Common-mode input voltage	Each input with respect to midsupply		±3.0		V
CMRR	Common-mode rejection ratio	Each input		64		dB
		T_A = –40°C		67		
		T_A = 85°C		62		
	Noninverting differential input resistance			10 || 2		kΩ || pF
	Inverting input resistance			43		Ω

5.5 Electrical Characteristics V_S = 12 V (続き)

at T_A ≅ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 50 Ω, series isolation resistor (R_S) = 2.5 Ω each, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
V_O	Output voltage swing	R_L = 100 Ω, R_S = 0 Ω		±9.7		V
		R_L = 50 Ω, R_S = 0 Ω		±9.3		
		R_L = 25 Ω, R_S = 0 Ω		±8.4		
I_O	Output current (sourcing and sinking)	R_L = 25 Ω, R_S = 0 Ω, based on V_O specification		±338		mA
	Short-circuit output current			±0.81		A
Z_O	Closed-loop output impedance	f = 1 MHz, differential		0.03		Ω
POWER SUPPLY						
V_S	Operating voltage		10	12	28	V
		T_A = –40°C to +85°C	10		28	
V_{GND}	GND pin voltage		$V_{S–}$	0	V_{S+} – 5	V
I_{S+}	Quiescent current, positive rail, V_{S+}	Full bias (BIAS-1 = 0, BIAS-2 = 0)		19.5		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		15		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		10.4		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		0.8		
$I_{S–}$	Quiescent current, negative rail, $V_{S–}$	Full bias (BIAS-1 = 0, BIAS-2 = 0)		18.8		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		14.4		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		9.6		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		0.01		
	Current through GND pin	Full bias (BIAS-1 = 0, BIAS-2 = 0)		0.8		mA
+PSRR	Positive power-supply rejection ratio	Differential		83		dB
–PSRR	Negative power-supply rejection ratio	Differential		83		dB
BIAS CONTROL						
	Bias control pin voltage	With respect to GND pin, T_A = –40°C to +85°C	0	3.3	12	V
	Bias control pin logic threshold	Logic 1, with respect to GND pin, T_A = –40°C to +85°C	2.1			V
		Logic 0, with respect to GND pin, T_A = –40°C to +85°C			0.8	
	Bias control pin current(1)	BIAS-1, BIAS-2 = 0.5 V (logic 0)		–9.6		µA
		BIAS-1, BIAS-2 = 3.3 V (logic 1)		0.3	1	
	Open-loop output impedance	Off bias (BIAS-1 = 1, BIAS-2 = 1)		70 || 5		MΩ || pF

(1) Current is considered positive out of the pin.

5.6 Electrical Characteristics V_S = 28 V

at T_A ≅ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 100 Ω, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth, –3 dB	A_V = 5 V/V, R_F = 1.5 kΩ, V_O = 2 V_{PP}			285		MHz
		A_V = 10 V/V, R_F = 1.24 kΩ, V_O = 2 V_{PP}			205		
	0.1-dB bandwidth flatness				13		MHz
LSBW	Large-signal bandwidth	V_O = 40 V_{PP}			170		MHz
SR	Slew rate (20% to 80% level)	V_O = 40-V step			11,000		V/µs
	Rise and fall time	V_O = 2 V_{PP}			2		ns
HD2	2nd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 100 Ω	Full bias, f = 1 MHz		–86		dBc
			Low bias, f = 1 MHz		–79		
			Full bias, f = 10 MHz		–71		
			Low bias, f = 10 MHz		–63		
HD3	3rd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 100 Ω	Full bias, f = 1 MHz		–101		dBc
			Low bias, f = 1 MHz		–88		
			Full bias, f = 10 MHz		–80		
			Low bias, f = 10 MHz		–65		
e_n	Differential input voltage noise	f ≥ 1 MHz, input-referred			2.5		nV/√Hz
i_{n+}	Noninverting input current noise (each amplifier)	f ≥ 1 MHz			1.7		pA/√Hz
$i_{n–}$	Inverting input current noise (each amplifier)	f ≥ 1 MHz			18		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain				1500		kΩ
	Input offset voltage				±12		mV
	Input offset voltage drift	T_A = –40°C to +85°C			–40		µV/°C
	Input offset voltage matching	Amplifier A to B			±0.5		mV
	Noninverting input bias current				±1		µA
	Inverting input bias current				±6		µA
	Inverting input bias current matching				±8		µA
INPUT CHARACTERISTICS							
	Common-mode input voltage	Each input		±9	±10		V
CMRR	Common-mode rejection ratio	Each input		53	65		dB
	Noninverting input resistance				10 || 2		kΩ || pF
	Inverting input resistance				38		Ω
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing(1)	R_L = 100 Ω			±24.5		V
		R_L = 25 Ω			±12.3		
I_O	Output current (sourcing and sinking) (1)	R_L = 25 Ω, based on V_O specification		±580	±665		mA
	Short-circuit output current				1		A
Z_O	Output impedance	f = 1 MHz, differential			0.01		Ω

5.6 Electrical Characteristics V_S = 28 V (続き)

at T_A ≅ 25°C, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 100 Ω, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Operating voltage		10	12	28	V
		T_A = –40°C to +85°C	10		28	
I_{S+}	Quiescent current, positive rail, V_{S+}	Full bias (BIAS-1 = 0, BIAS-2 = 0)		23		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		17.5		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		11.9		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		1.1	1.3	
$I_{S–}$	Quiescent current, negative rail, $V_{S–}$	Full bias (BIAS-1 = 0, BIAS-2 = 0)		22		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		16.4		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		10.8		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		0.1	0.8	
	Current through GND pin	Full bias (BIAS-1 = 0, BIAS-2 = 0)		1		mA
+PSRR	Positive power-supply rejection ratio	Differential		83		dB
–PSRR	Negative power-supply rejection ratio	Differential		77		dB
BIAS CONTROL						
	Bias control pin voltage	With respect to GND pin, T_A = –40°C to +85°C	0	3.3	14.5	V
	Bias control pin logic threshold	Logic 1, with respect to GND pin, T_A = –40°C to +85°C	1.9			V
		Logic 0, with respect to GND pin, T_A = –40°C to +85°C			0.8	
	Bias control pin current(2)	BIAS-1, BIAS-2 = 0.5 V (logic 0)	–15	–10		µA
		BIAS-1, BIAS-2 = 3.3 V (logic 1)		0.1	1	

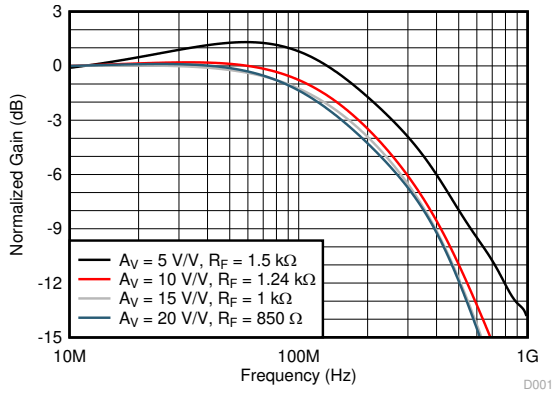
(1) See *Section 6.3.1* for output voltage vs output current characteristics.
(2) Current is considered positive out of the pin.

5.7 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{ON}	Turn-on time delay: time for output to start tracking the input		25		ns
t_{OFF}	Turn-off time delay: time for output to stop tracking the input		275		ns

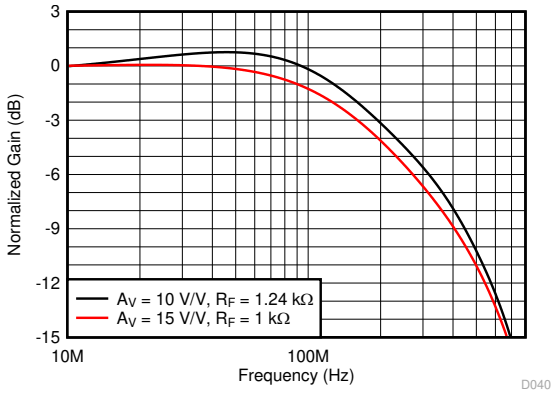
5.8 Typical Characteristics: V_S = 12 V

at T_A ≅ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode (unless otherwise noted)



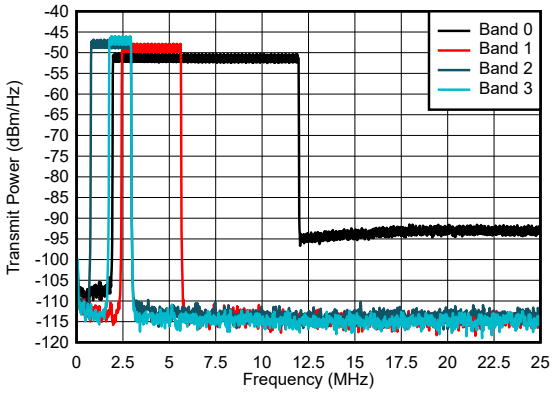
V_O = 2 V_{PP}

図 5-1. Small-Signal Frequency Response



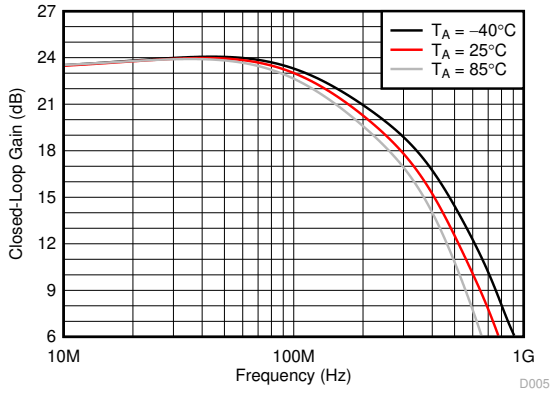
V_O = 16 V_{PP}

図 5-2. Large-Signal Frequency Response



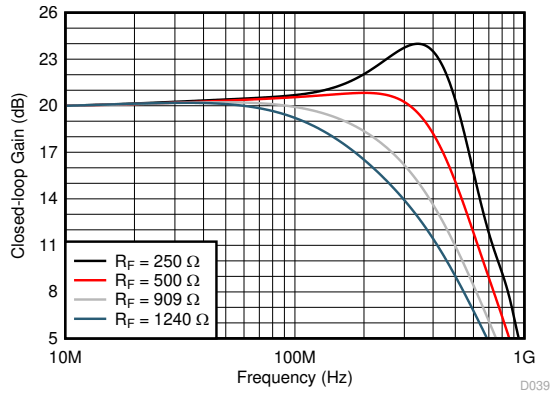
SGCC HPLC profiles, crest factor = 5 V/V

図 5-3. Out-of-Band Suppression



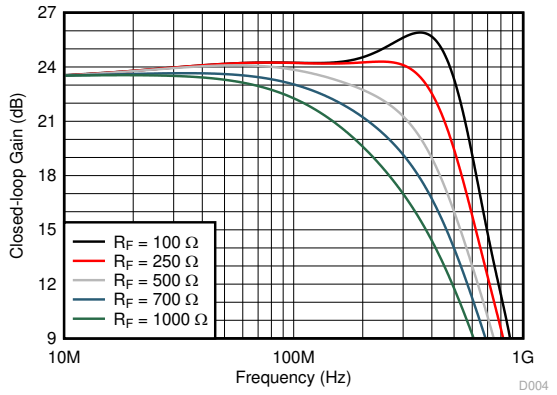
A_V = 15 V/V, V_O = 2 V_{PP}

図 5-4. Small-Signal Frequency Response vs Temperature



A_V = 10 V/V, V_O = 2 V_{PP}

図 5-5. Small-Signal Frequency Response vs R_F

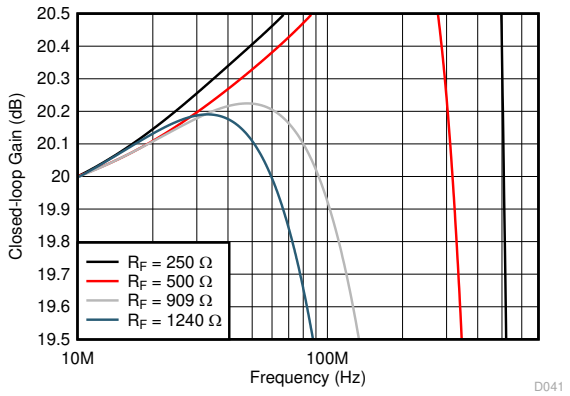


A_V = 15 V/V, V_O = 2 V_{PP}

図 5-6. Small-Signal Frequency Response vs R_F

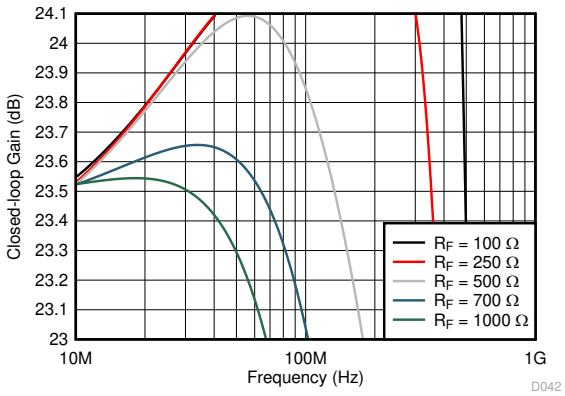
5.8 Typical Characteristics: V_S = 12 V (continued)

at T_A ≅ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode (unless otherwise noted)



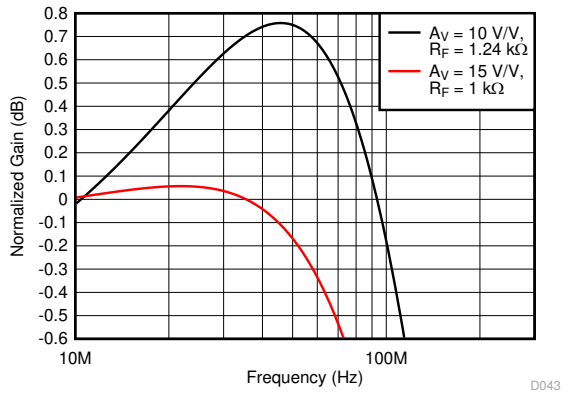
A_V = 10 V/V, V_O = 2 V_{PP}

図 5-7. Small-Signal Gain Flatness vs R_F



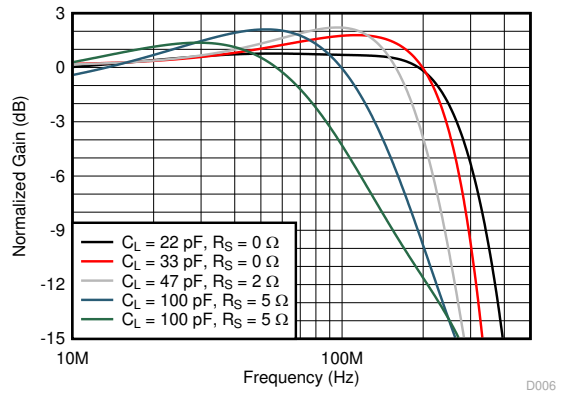
A_V = 15 V/V, V_O = 2 V_{PP}

図 5-8. Small-Signal Gain Flatness vs R_F



V_O = 16 V_{PP}

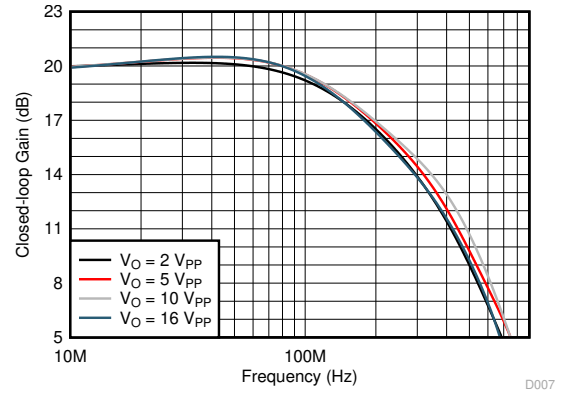
図 5-9. Large-Signal Gain Flatness



V_O = 100 mV_{PP}

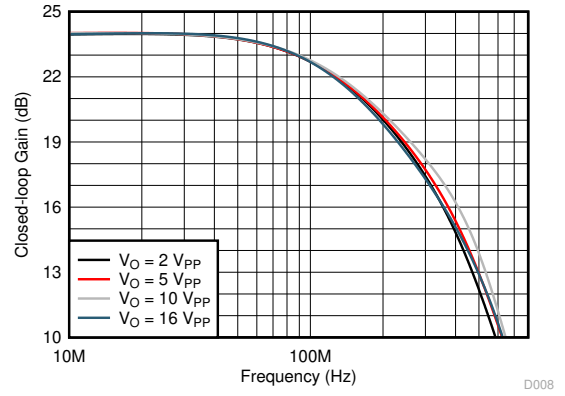
Frequency response is measured at the device output pin before the isolation resistor.

図 5-10. Small-Signal Frequency Response vs C_{LOAD}



A_V = 10 V/V

図 5-11. Large-Signal Frequency Response vs V_O

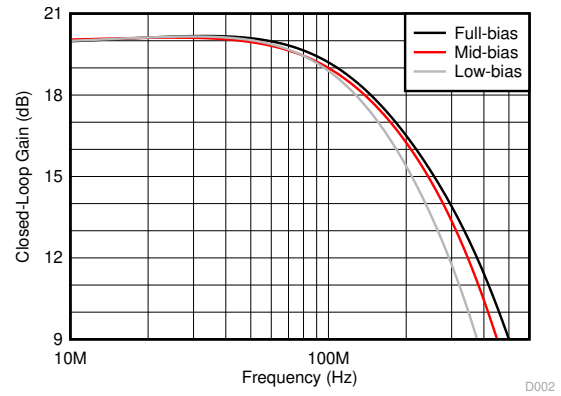


A_V = 15 V/V

図 5-12. Large-Signal Frequency Response vs V_O

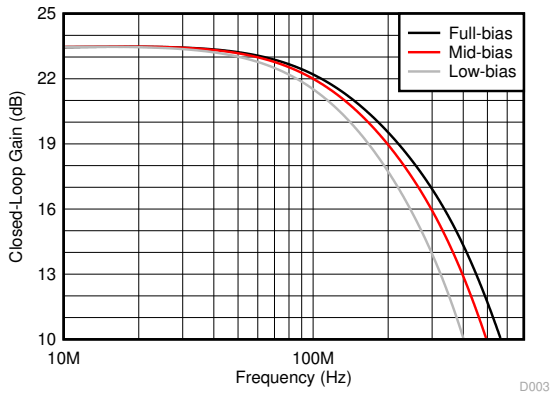
5.8 Typical Characteristics: V_S = 12 V (continued)

at T_A ≅ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode (unless otherwise noted)



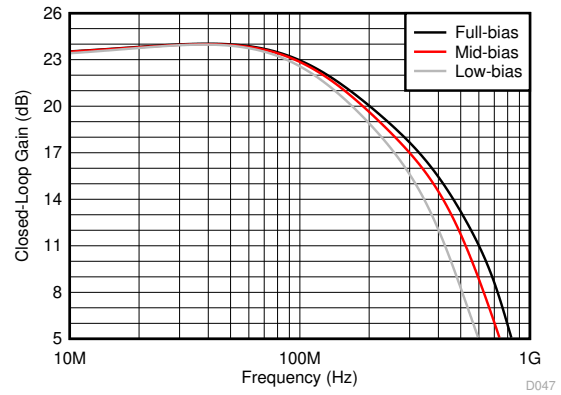
A_V = 10 V/V, V_O = 2 V_{PP}

図 5-13. Small-Signal Frequency Response vs Bias Modes



A_V = 15 V/V, V_O = 2 V_{PP}

図 5-14. Small-Signal Frequency Response vs Bias Modes



A_V = 15 V/V, V_O = 16 V_{PP}

図 5-15. Large-Signal Frequency Response vs Bias Modes

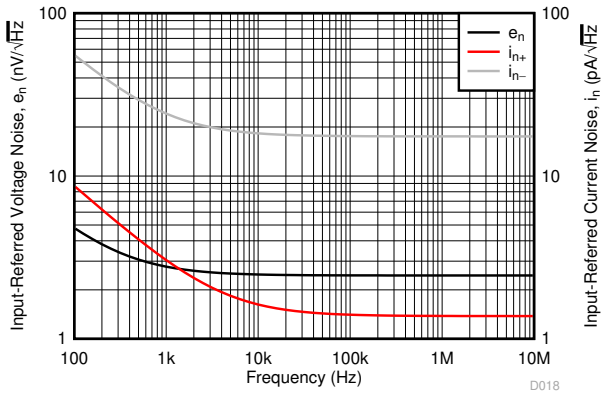
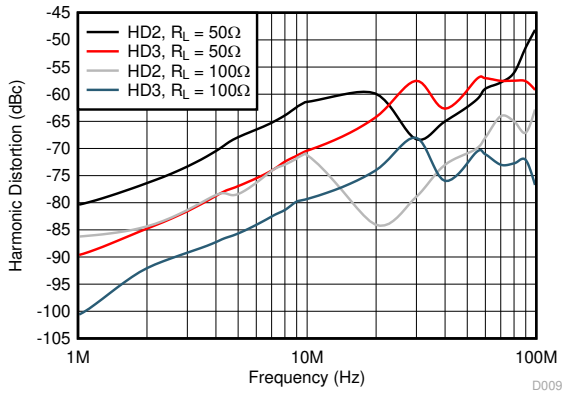
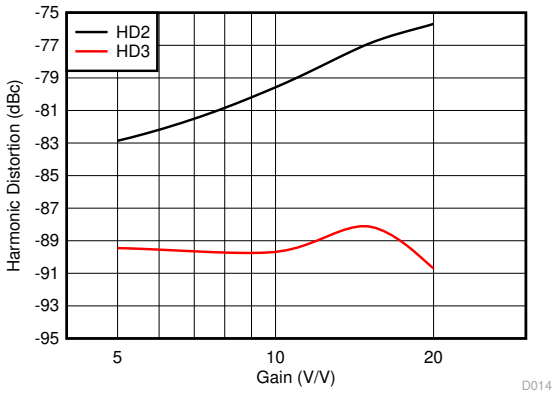


図 5-16. Input Voltage and Current Noise Density vs Frequency



V_O = 2 V_{PP}

図 5-17. Harmonic Distortion vs Frequency

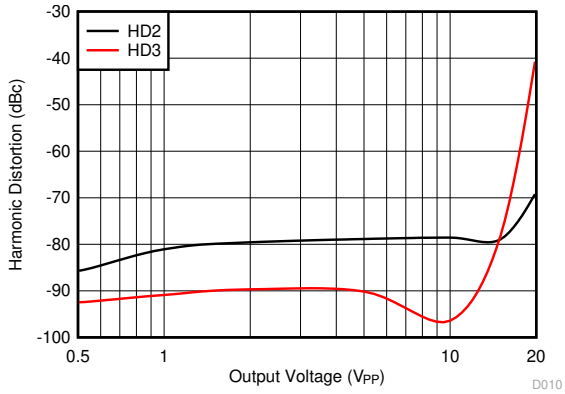


f = 1 MHz, V_O = 2 V_{PP}

図 5-18. Harmonic Distortion vs Gain

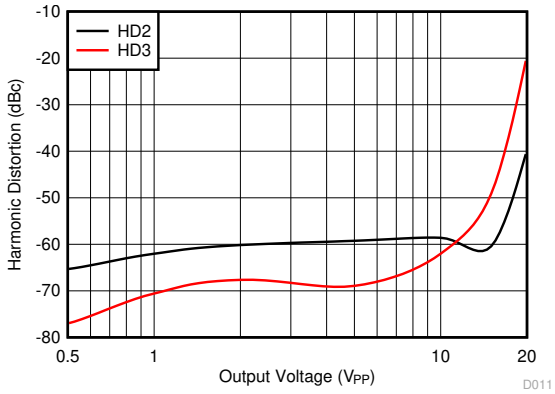
5.8 Typical Characteristics: V_S = 12 V (continued)

at T_A ≅ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode (unless otherwise noted)



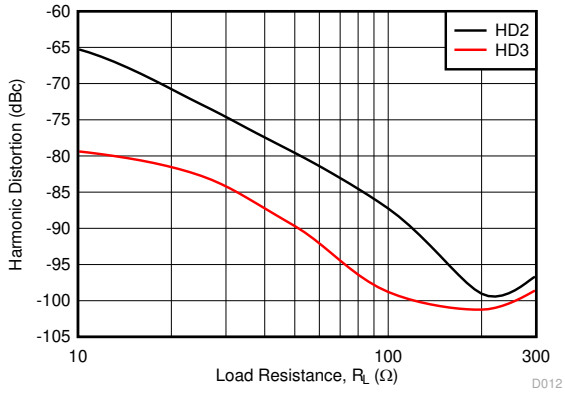
f = 1 MHz, A_V = 10 V/V

図 5-19. Harmonic Distortion vs V_O



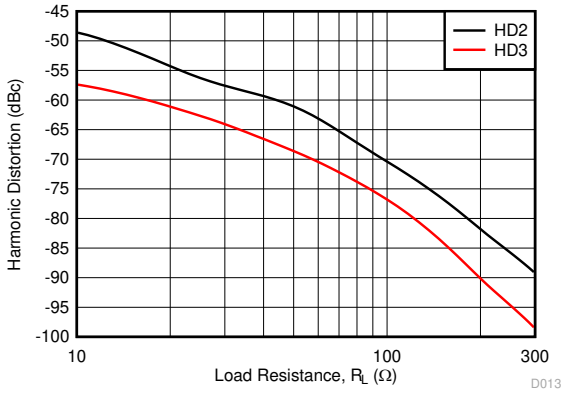
f = 10 MHz, A_V = 10 V/V

図 5-20. Harmonic Distortion vs V_O



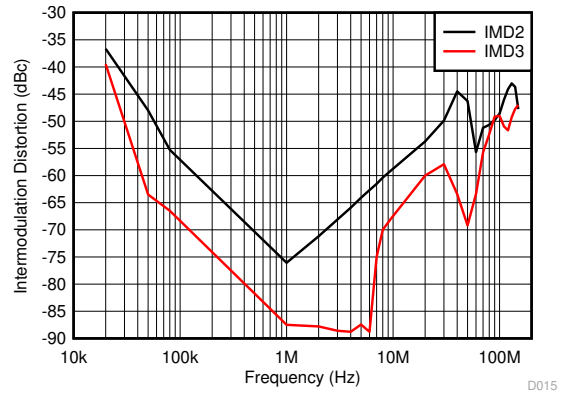
f = 1 MHz, V_O = 2 V_{PP}, A_V = 10 V/V

図 5-21. Harmonic Distortion vs R_L



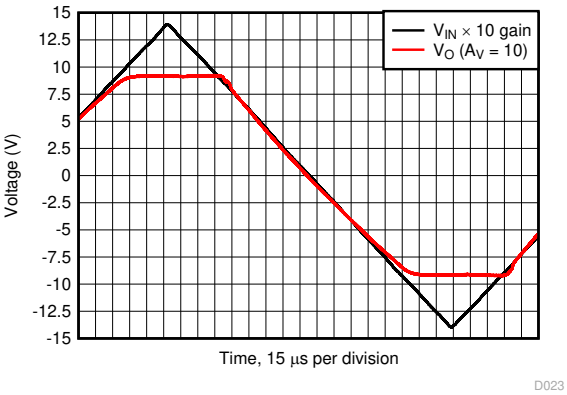
f = 10 MHz, V_O = 2 V_{PP}, A_V = 10 V/V

図 5-22. Harmonic Distortion vs R_L



±12.2 kHz tone spacing, V_O = 2 V_{PP} per tone

図 5-23. Intermodulation Distortion vs Frequency

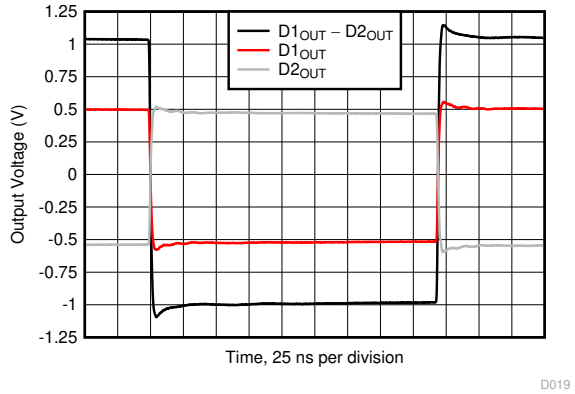


V_{IN} = 2.8-V_{PP} triangular waveform

図 5-24. Overdrive Recovery

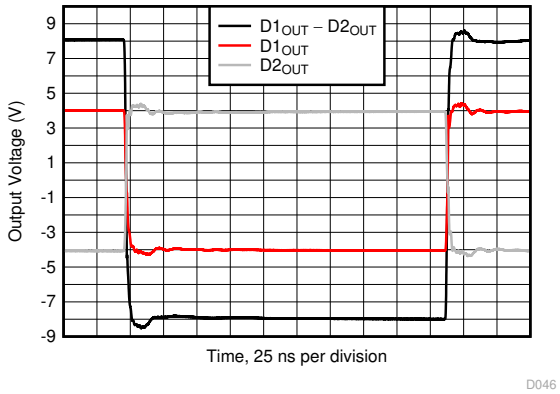
5.8 Typical Characteristics: V_S = 12 V (continued)

at T_A ≅ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode (unless otherwise noted)



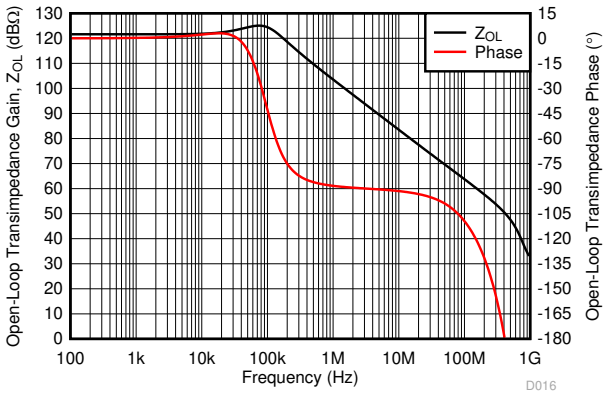
V_O step = 2 V_{PP}

図 5-25. Small-Signal Pulse Response



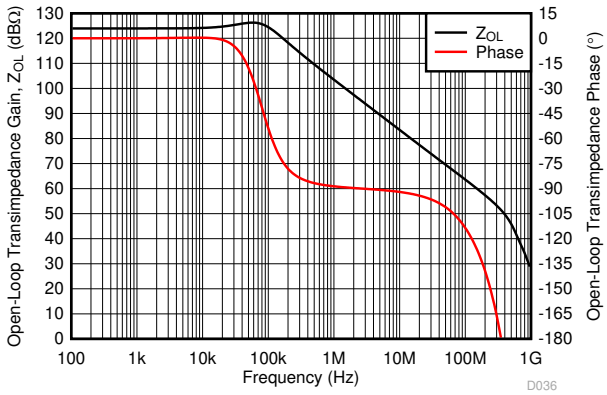
V_O step = 16 V_{PP}

図 5-26. Large-Signal Pulse Response



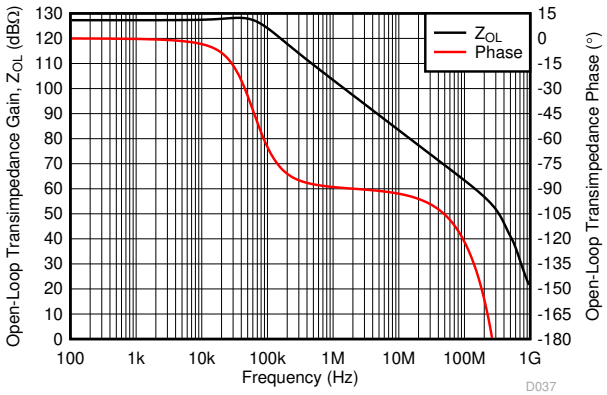
Full-bias simulation

図 5-27. Open-Loop Transimpedance Gain and Phase vs Frequency



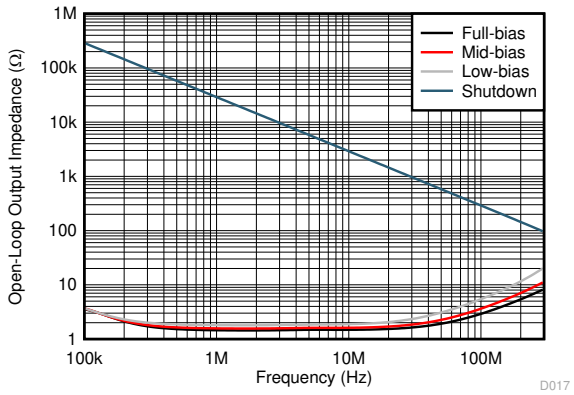
Mid-bias simulation

図 5-28. Open-Loop Transimpedance Gain and Phase vs Frequency



Low-bias simulation

図 5-29. Open-Loop Transimpedance Gain and Phase vs Frequency

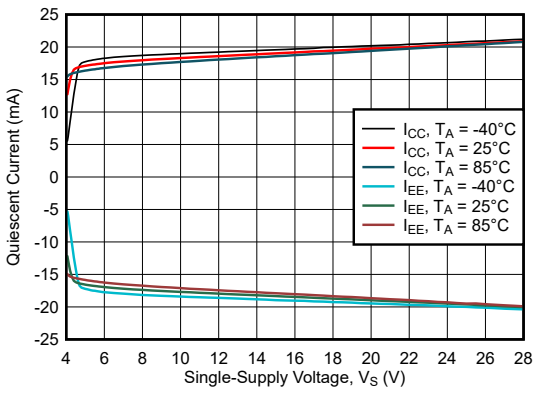


Simulation

図 5-30. Open-Loop Output Impedance vs Frequency

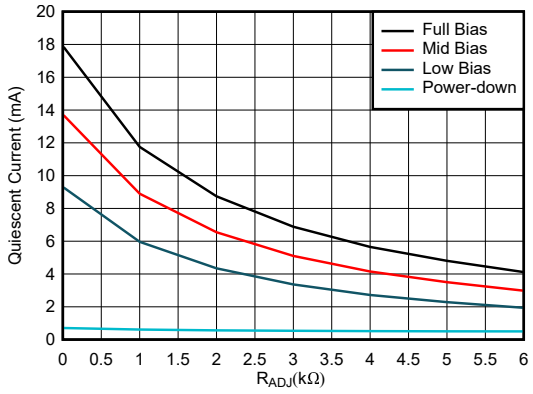
5.8 Typical Characteristics: V_S = 12 V (continued)

at T_A ≅ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode (unless otherwise noted)



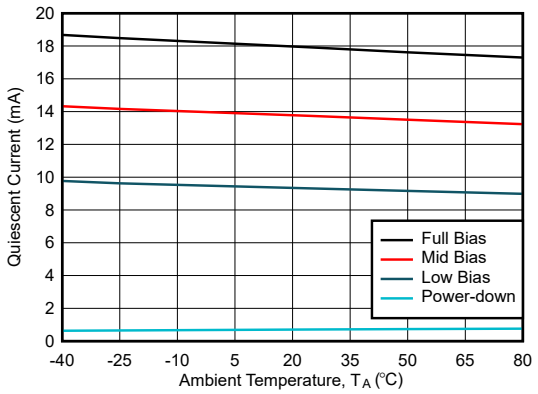
R_L = no load

図 5-31. Quiescent Current vs Single-Supply Voltage



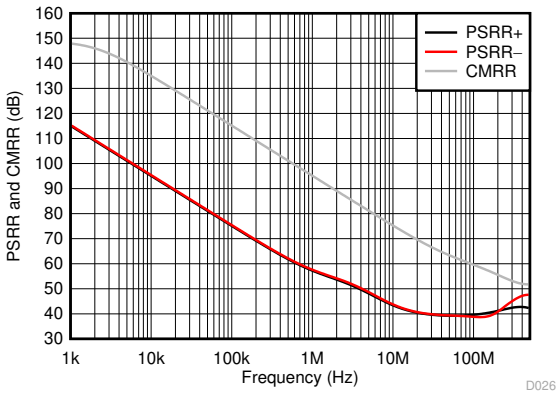
R_L = no load

図 5-32. Quiescent Current vs R_{ADJ}



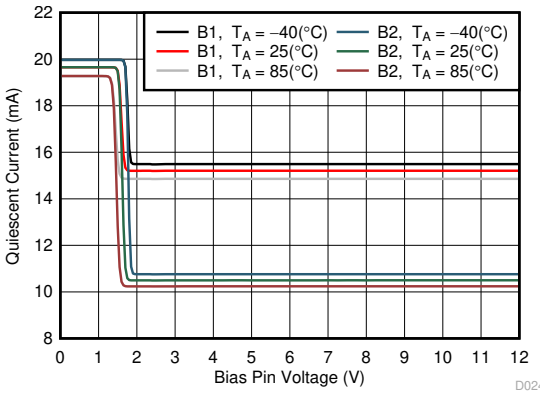
R_L = no load

図 5-33. Quiescent Current vs Temperature



T_J = 50°C, simulation

図 5-34. PSRR and CMRR vs Frequency



B1 = full-bias to mid-bias transition with B2 = GND pin,
B2 = full-bias to low-bias transition with B1 = GND pin,
GND pin = $V_{S–}$

図 5-35. Mode Transition Voltage Threshold

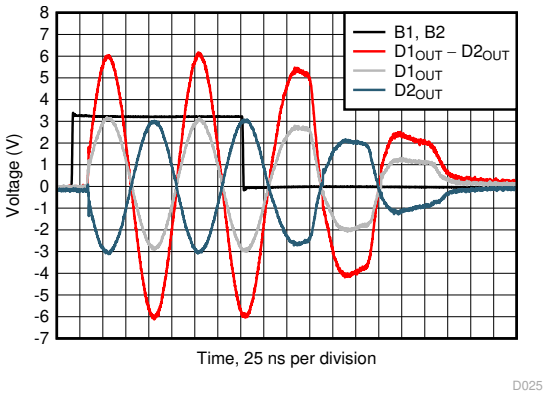
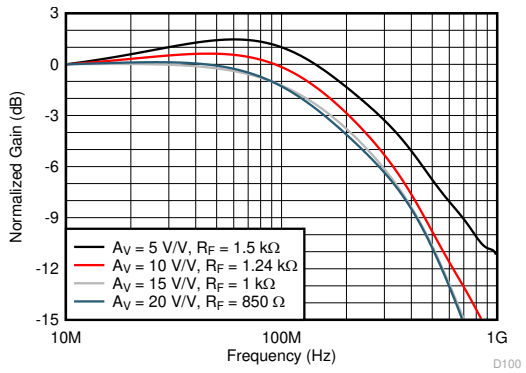


図 5-36. Full-Bias and Shutdown Mode Transition Timing

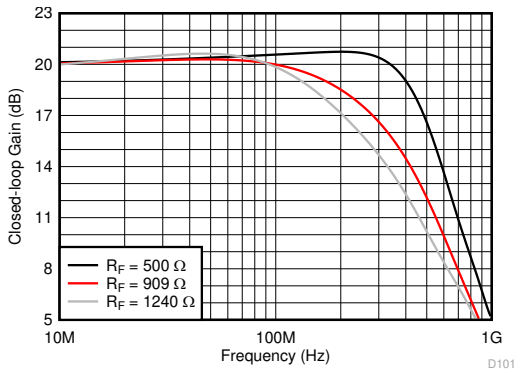
5.9 Typical Characteristics: V_S = 28 V

At T_A ≅ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 100 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode (unless otherwise noted).



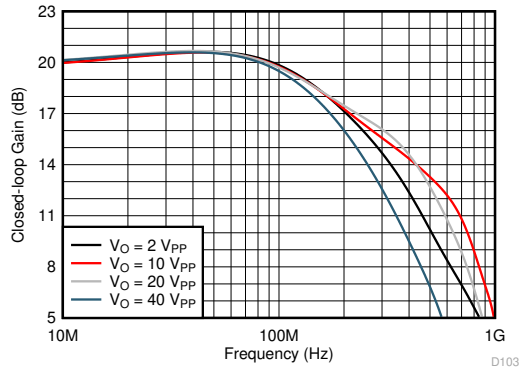
V_O = 2 V_{PP}

図 5-37. Small-Signal Frequency Response



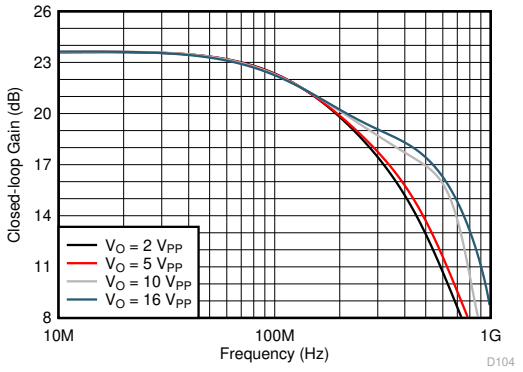
V_O = 2 V_{PP}

図 5-38. Small-Signal Frequency Response vs R_F



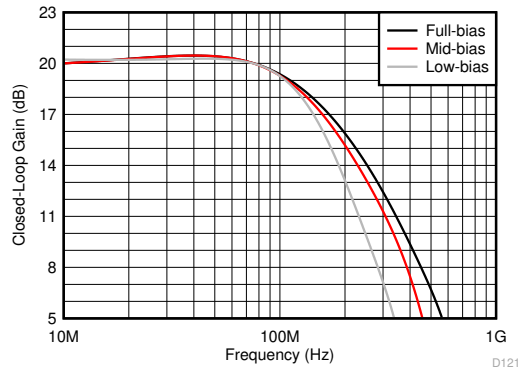
A_V = 10 V/V

図 5-39. Large-Signal Frequency Response vs V_O



A_V = 15 V/V

図 5-40. Large-Signal Frequency Response vs V_O



V_O = 40 V_{PP}

図 5-41. Large-Signal Frequency Response vs Bias Modes

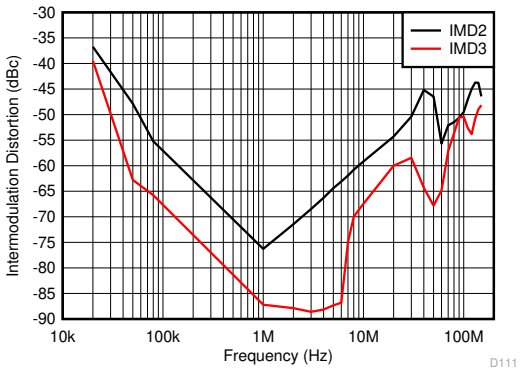
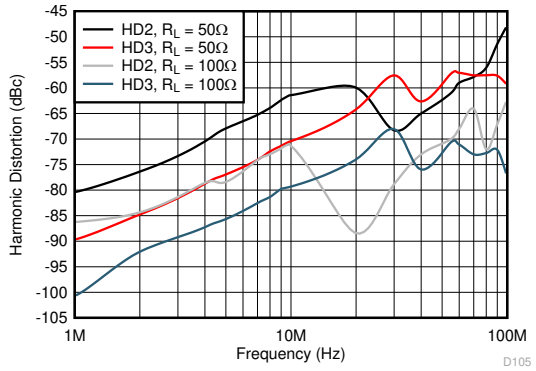


図 5-42. Intermodulation Distortion vs Frequency

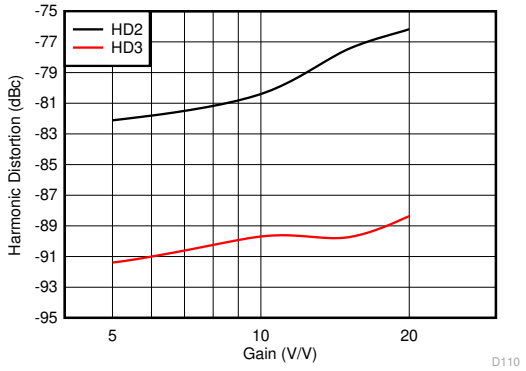
5.9 Typical Characteristics: V_S = 28 V (continued)

At T_A ≅ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 100 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode (unless otherwise noted).



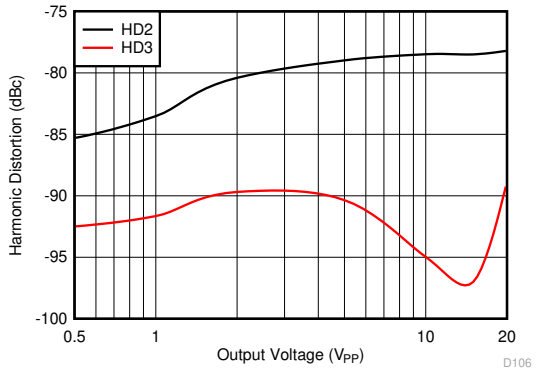
V_O = 2 V_{PP}

図 5-43. Harmonic Distortion vs Frequency



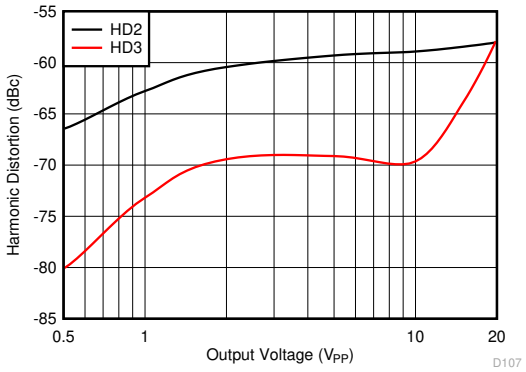
f = 1 MHz, V_O = 2 V_{PP} R_L = 50 Ω

図 5-44. Harmonic Distortion vs Gain



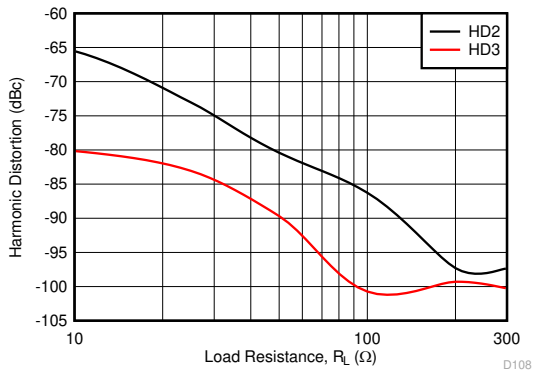
f = 1 MHz, R_L = 50 Ω

図 5-45. Harmonic Distortion vs V_O



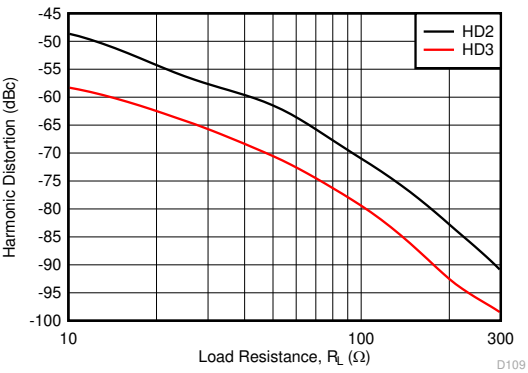
f = 10 MHz, R_L = 50 Ω

図 5-46. Harmonic Distortion vs V_O



f = 1 MHz, V_O = 2 V_{PP}

図 5-47. Harmonic Distortion vs R_L

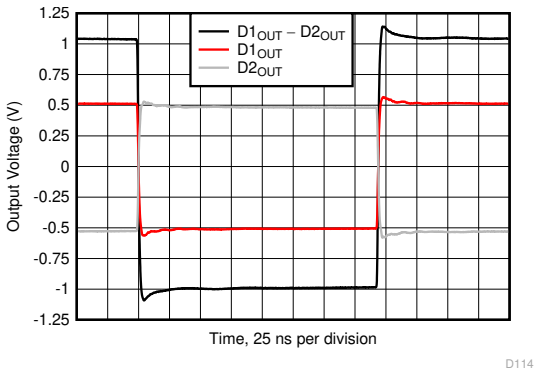


f = 10 MHz, V_O = 2 V_{PP}

図 5-48. Harmonic Distortion vs R_L

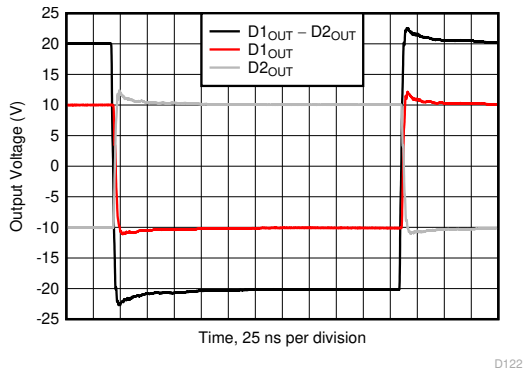
5.9 Typical Characteristics: V_S = 28 V (continued)

At T_A ≅ 25°C, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 100 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode (unless otherwise noted).



V_O step = 2 V_{PP}

図 5-49. Small-Signal Pulse Response



V_O step = 40 V_{PP}

図 5-50. Large-Signal Pulse Response

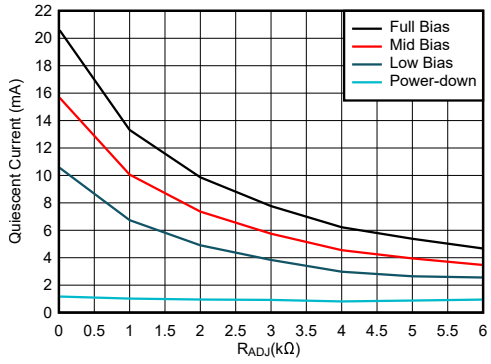


図 5-51. Quiescent Current vs R_{ADJ}

6 Detailed Description

6.1 Overview

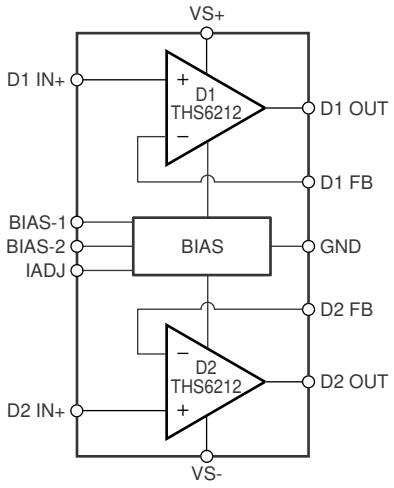
The THS6212 is a differential line-driver amplifier with a current-feedback architecture. The device is targeted for use in line-driver applications (such as wide-band power-line communications) and is fast enough to support transmissions of 14.5-dBm line power up to 30 MHz.

The THS6212 is designed as a single-channel device that can be a drop-in replacement for dual-channel footprint packages. The package pinout is compatible with the pinout of the THS6214 dual, differential line driver, and provides an alternative for systems that only require a single-channel device.

The architecture of the THS6212 is designed to provide maximum flexibility with multiple bias settings that are selectable based on application performance requirements, and also provides an external current pin (IADJ) to further adjust the bias current to the device. The wide output swing (49V_{PP}) and high current drive (650mA) of the THS6212 make the device an excellent choice for high-power, line-driving applications.

The THS6212 features thermal protection that typically triggers at a junction temperature of 175°C. The device behavior is similar to the bias off mode when thermal shutdown is activated. The device resumes normal operation when the die junction temperature reaches approximately 145°C. The device can go in and out of thermal shutdown until the overload conditions are removed because of the unpredictable behavior of the overload and thermal characteristics.

6.2 Functional Block Diagram

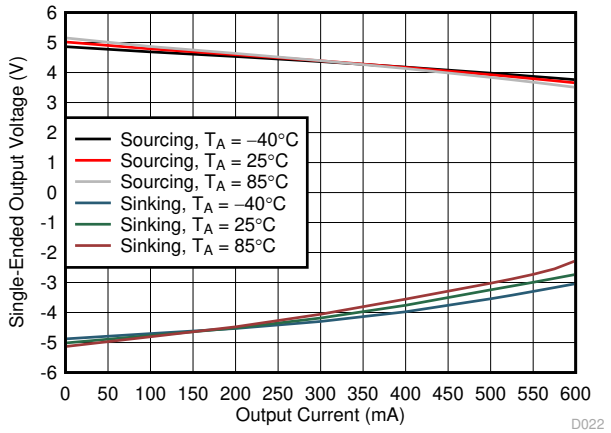


6.3 Feature Description

6.3.1 Output Voltage and Current Drive

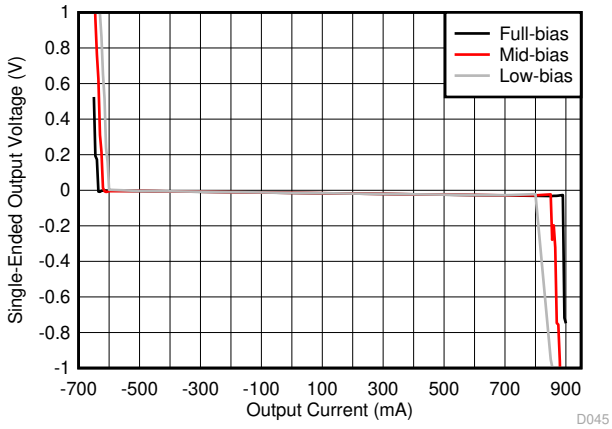
The THS6212 provides output voltage and current capabilities that are unsurpassed in a low-cost, monolithic op amp. The output voltage (under no load at room temperature) typically swings closer than 1.1 V to either supply rail and typically swings to within 1.1 V of either supply with a 100 Ω differential load. The THS6212 can deliver over 350 mA of current with a 25 Ω load.

Good thermal design of the system is important, including use of heat sinks and active cooling methods, if the THS6212 is pushed to the limits of the output drive capabilities. 図 6-1 and 図 6-2 show the output drive of the THS6212 under two different sets of conditions where T_A is approximately equal to T_J. In practical applications, T_J is often much higher than T_A and highly depends on the device configuration, signal parameters, and PCB thermal design. To represent the full output drive capability of the THS6212 in 図 6-1 and 図 6-2, $T_J \approx T_A$ is achieved by pulsing or sweeping the output current for a duration of less than 100 ms.



V_S = 12 V, $T_J \approx T_A$

図 6-1. Slammed Single-Ended Output Voltage vs I_O and Temperature



V_S = 12 V, $T_J \approx T_A \approx$ 25°C

図 6-2. Linear Single-Ended Output Voltage vs I_O and Temperature

In 図 6-1, the output voltages are differentially slammed to the rail and the output current is single-endedly sourced or sunk using a source measure unit (SMU) for less than 100 ms. The single-ended output voltage of each output is then measured prior to removing the load current. After removing the load current, the outputs are brought back to mid-supply before repeating the measurement for different load currents. This entire process is repeated for each ambient temperature. Under the slammed output voltage condition of 図 6-1, the output transistors are in saturation and the transistors start going into linear operation as the output swing is backed off for a given I_O,

In 図 6-2, the inputs are floated and the output voltages are allowed to settle to the mid-supply voltage. The load current is then single-endedly swept for sourcing (greater than 0 mA) and sinking (less than 0 mA) conditions and the single-ended output voltage is measured at each current-forcing condition. The current sweep is completed in a few seconds (approximately 3 to 4 seconds) so as not to significantly raise the junction temperature (T_J) of the device from the ambient temperature (T_A). The output is not swinging and the output transistors are in linear operation in 図 6-2 until the current drawn exceeds the device capabilities, at which point the output voltage starts to deviate quickly from the no load output voltage.

To maintain maximum output stage linearity, output short-circuit protection is not provided. This absence of short-circuit protection is normally not a problem because most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin, in most cases, permanently damages the amplifier.

6.3.2 Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that can be recommended to improve the ADC linearity. A high-speed, high open-loop gain amplifier such as the THS6212 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. One external solution to this problem is described in this section.

When the primary considerations are frequency response flatness, pulse response fidelity, and distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This series resistor does not eliminate the pole from the loop response, but shifts the pole and adds a zero at a higher frequency. The additional zero functions to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics sections describe the recommended R_S versus capacitive load (see 図 5-10) and the resulting frequency response at the load. Parasitic capacitive loads greater than 2 pF can begin to degrade device performance. Long printed-circuit board (PCB) traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the THS6212 output pin (see the Layout Guidelines section).

6.3.3 Distortion Performance

The THS6212 provides good distortion performance into a 100-Ω load on a 28V supply. Relative to alternative solutions, the amplifier provides exceptional performance into lighter loads and operation on a 12V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the second harmonic dominates the distortion with a negligible third-harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see 図 7-1), this value is the sum of R_F + R_G, whereas in the inverting configuration this value is just R_F. Providing an additional supply decoupling capacitor (0.01 µF) between the supply pins (for bipolar operation) also improves the second-order distortion slightly (from 3 dB to 6 dB).

In most op amps, increasing the output voltage swing directly increases harmonic distortion. The *Typical Characteristics* sections illustrate the second harmonic increasing at a little less than the expected 2x rate, whereas the third harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between the fundamental power and the second harmonic decreases less than the expected 6 dB, whereas the difference between the fundamental power and the third harmonic decreases by less than the expected 12 dB. This difference also appears in the two-tone, third-order intermodulation (IM3) spurious response curves. The third-order spurious levels are extremely low at low-output power levels. The output stage continues to hold the third-order spurious levels low even when the fundamental power reaches very high levels.

6.3.4 Differential Noise Performance

The THS6212 is designed to be used as a differential driver in high-performance applications. Therefore, analyzing the noise in such a configuration is important. 図 6-3 shows the op amp noise model for the differential configuration.

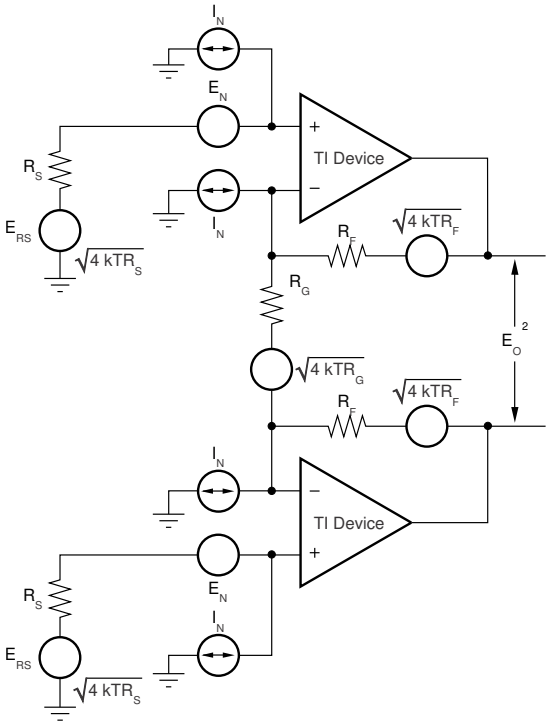


図 6-3. Differential Op Amp Noise Analysis Model

As a reminder, the differential gain is expressed in 式 1:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \tag{1}$$

The output noise can be expressed as shown in 式 2:

$$E_O = \sqrt{2 \times G_D^2 \times \left[e_N^2 + (i_N \times R_S)^2 + 4\ kTR_S\right] + 2(i_I R_F)^2 + 2(4\ kTR_F G_D)} \tag{2}$$

Dividing this expression by the differential noise gain [$G_D = (1 + 2R_F / R_G)$] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in 式 3.

$$E_O = \sqrt{2 \times \left[e_N^2 + (i_N \times R_S)^2 + 4\ kTR_S\right] + 2\left[\frac{i_I R_F}{G_D}\right]^2 + 2\left[\frac{4\ kTR_F}{G_D}\right]} \tag{3}$$

Evaluating these equations for the THS6212 circuit and component values of 図 7-1 with R_S = 50 Ω, gives a total output spot noise voltage of 53.3 nV/√Hz and a total equivalent input spot noise voltage of 6.5 nV/√Hz.

To minimize the output noise as a result of the noninverting input bias current noise, keep the noninverting source impedance as low as possible.

6.3.5 DC Accuracy and Offset Control

A current-feedback op amp such as the THS6212 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate dc accuracy. The *Electrical Characteristics* tables describe an input offset voltage that is comparable to high-speed, voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. Although bias current cancellation techniques are very effective with most voltage-feedback op amps, these techniques do not generally reduce the output dc offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the input source impedance to reduce error contribution to the output is ineffective. Evaluating the configuration of 図 7-1, using a typical condition at 25°C input offset voltage and the two input bias currents, gives a typical output offset range equal to 式 4:

$$
\begin{aligned}
V_{OFF} &= \left(\pm NG \times V_{OS(TYP)}\right) + \left(I_{BN} \times \frac{R_S}{2} \times NG\right) \pm \left(I_{BI} \times R_F\right) \\
&= \pm\left(10 \times 0.5\,mV\right) + \left(1\,\mu A \times 25\,\Omega \times 10\right) \pm \left(6\,\mu A \times 1.24\,k\Omega\right) \\
&= \pm 5\,mV + 0.250\,mV \pm 7.44\,mV \\
V_{OFF} &= -12.19\,mV \text{ to } 12.69\,mV
\end{aligned}
\tag{4}
$$

where

- NG = noninverting signal gain

6.4 Device Functional Modes

The THS6212 has four different functional modes set by the BIAS-1 and BIAS-2 pins. 表 6-1 shows the truth table for the device mode pin configuration and the associated description of each mode.

表 6-1. BIAS-1 and BIAS-2 Logic Table

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full-bias mode (100%)	Amplifiers on with lowest distortion possible (default state)
1	0	Mid-bias mode (75%)	Amplifiers on with power savings and a reduction in distortion performance
0	1	Low-bias mode (50%)	Amplifiers on with enhanced power savings and a reduction of overall performance
1	1	Shutdown mode	Amplifiers off and output has high impedance

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The THS6212 is typically used to drive high output power applications with various load conditions. In the *Typical Applications* section, the amplifier is presented in a general-purpose, wideband, current-feedback configuration, and a more specific 100-Ω twisted pair cable line driver; however, the amplifier is also applicable for many different general-purpose and specific cable line-driving scenarios beyond what is shown in the *Typical Applications* section.

7.2 Typical Applications

7.2.1 Wideband Current-Feedback Operation

The THS6212 provides the exceptional ac performance of a wideband current-feedback op amp with a highly linear, high-power output stage. Requiring only 19.5 mA of quiescent current, the THS6212 has an output swing of 49 Vpp (100-Ω load) coupled with over 650 mA current drive (25 Ω load). This low-output headroom requirement, along with biasing that is independent of the supply voltage, provides a remarkable 28-V supply operation. The THS6212 delivers greater than 285-MHz bandwidth driving a 2-V_{PP} output into 100 Ω on a 28-V supply. Previous boosted output stage amplifiers typically suffer from very poor crossover distortion when the output current goes through zero. The THS6212 achieves a comparable power gain with improved linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that ac performance (bandwidth and distortion) is relatively independent of signal gain. 図 7-1 shows the dc-coupled, gain of 10 V/V, dual power-supply circuit configuration used as the basis of the 28-V *Electrical Characteristics* tables and *Typical Characteristics* sections.

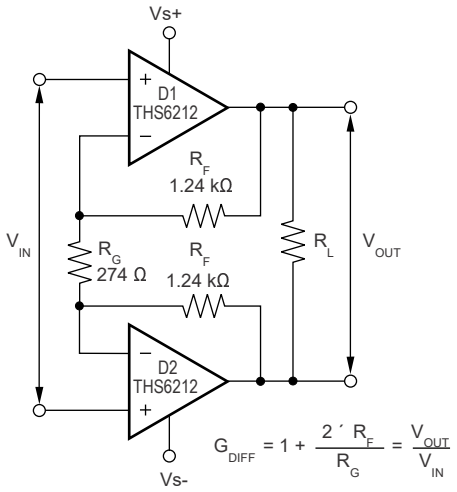


図 7-1. Noninverting Differential I/O Amplifier

7.2.1.1 Design Requirements

The main design requirements for wideband current-feedback operation are to choose power supplies that satisfy common-mode requirements at the input and output of the device, and also to use a feedback resistor value that allows for the proper bandwidth when maintaining stability. These requirements and the proper solutions are described in the *Detailed Design Procedure* section. Using transformers and split power supplies can be required for certain applications.

7.2.1.2 Detailed Design Procedure

For ease of test purposes in this design, the THS6212 input impedance is set to 50 Ω with a resistor to ground and the output impedance is set to 50 Ω with a series output resistor. Voltage swings reported in the *Electrical Characteristics* tables are taken directly at the input and output pins, whereas load powers (dBm) are defined at a matched 50-Ω load. For the circuit of 図 7-1, the total effective load is 100 Ω || 1.24 kΩ || 1.24 kΩ = 86.1 Ω. This approach allows a source termination impedance to be set at the input that is independent of the signal gain. For instance, simple differential filters can be included in the signal path right up to the noninverting inputs with no interaction with the gain setting. The differential signal gain for the circuit of 図 7-1 is given by 式 5:

$$A_D = 1 + 2 \times \frac{R_F}{R_G} \tag{5}$$

where

- A_D = differential gain

A value of 274 Ω for the A_D = 10-V/V design is given by 図 7-1. The device bandwidth is primarily controlled with the feedback resistor value because the THS6212 is a current-feedback (CFB) amplifier; the differential gain, however, can be adjusted with considerable freedom using just the R_G resistor. In fact, R_G can be reduced by a reactive network that provides a very isolated shaping to the differential frequency response.

Various combinations of single-supply or ac-coupled gain can also be delivered using the basic circuit of 図 7-1. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1 V/V because an equal dc voltage at each inverting node does not create current through R_G. This circuit does show a common-mode gain of 1 V/V from the input to output. The source connection must either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface can also be used to reject that common-mode signal. For instance, most modern differential input analog-to-digital converters (ADCs) reject common-mode signals very well, and a line-driver application through a transformer also attenuates the common-mode signal through to the line.

7.2.1.3 Application Curves

図 7-2 and 図 7-3 show the frequency response and distortion performance of the circuit in 図 7-1. The measurements are made with a load resistor (R_L) of 100 Ω, and at room temperature. 図 7-2 is measured using the three different device power modes, and the distortion measurements in 図 7-3 are made at an output voltage level of 2 V_{PP}.

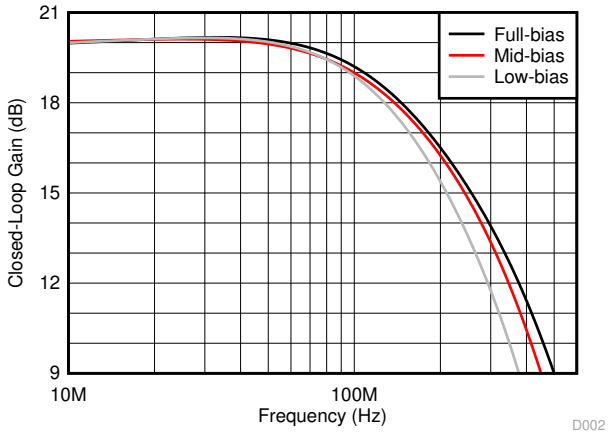


図 7-2. Frequency Response

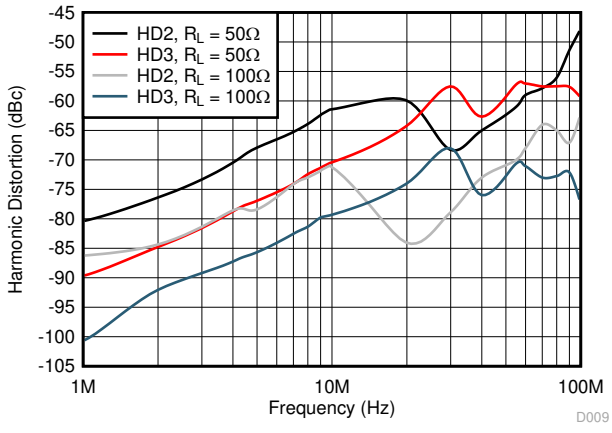


図 7-3. Harmonic Distortion

7.2.2 Dual-Supply Downstream Driver

図 7-4 shows an example of a dual-supply downstream driver with a synthesized output impedance circuit. The THS6212 is configured as a differential gain stage to provide a signal drive to the primary winding of the transformer (a step-up transformer with a turns ratio of 1:n is shown in 図 7-4). The main advantage of this configuration is the cancellation of all even harmonic-distortion products. Another important advantage is that each amplifier must only swing half of the total output required driving the load.

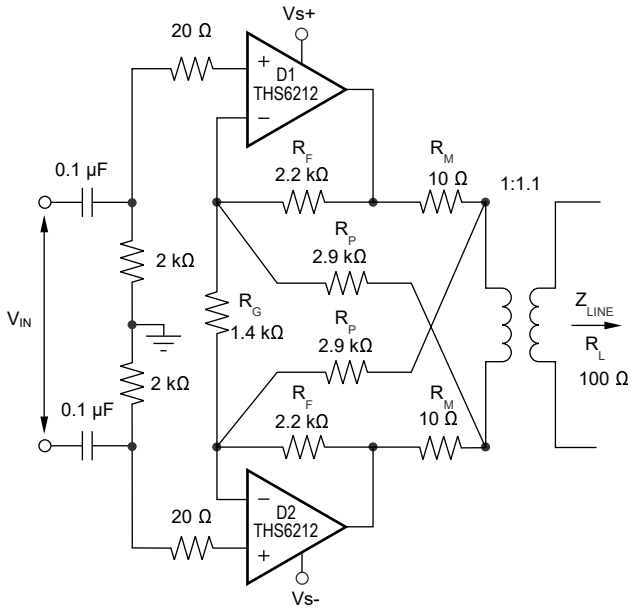


図 7-4. Dual-Supply Downstream Driver

The analog front-end (AFE) signal is ac-coupled to the driver, and the noninverting input of each amplifier is biased to the mid-supply voltage (ground in this case). In addition to providing the proper biasing to the amplifier, this approach also provides a high-pass filtering with a corner frequency that is set at 5 kHz in this example. Because the signal bandwidth starts at 26 kHz, this high-pass filter does not generate any problems and has the advantage of filtering out unwanted lower frequencies.

7.2.2.1 Design Requirements

The main design requirements for 図 7-4 are to match the output impedance correctly, satisfy headroom requirements, and confirm that the circuit meets power driving requirements. These requirements are described in the *Detailed Design Procedure* section and include the required equations to properly implement the design. The design must be fully worked through before physical implementation because small changes in a single parameter can often have large effects on performance.

7.2.2.2 Detailed Design Procedure

For 図 7-4, the input signal is amplified with a gain set by 式 6:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (6)$$

The two back-termination resistors (R_M = 10 Ω, each) added at each terminal of the transformer make the impedance of the amplifier match the impedance of the line, and also provide a means of detecting the received signal for the receiver. The value of these resistors (R_M) is a function of the line impedance and the transformer turns ratio (n), given by 式 7:

$$R_M = \frac{Z_{LINE}}{2n^2} \tag{7}$$

7.2.2.2.1 Line Driver Headroom Requirements

The first step in a transformer-coupled, twisted-pair driver design is to compute the peak-to-peak output voltage from the target specifications. This calculation is done using 式 8 to 式 11:

$$P_L = 10 \times \log \frac{V_{RMS}^2}{(1\ mW) \times R_L} \tag{8}$$

where

- P_L = power at the load
- V_{RMS} = voltage at the load
- R_L = load impedance

These values produce the following:

$$V_{RMS} = \sqrt{(1\ mW) \times R_L \times 10^{\frac{P_L}{10}}} \tag{9}$$

$$V_P = \text{Crest Factor} \times V_{RMS} = CF \times V_{RMS} \tag{10}$$

where

- V_P = peak voltage at the load
- CF = crest factor

$$V_{LPP} = 2 \times CF \times V_{RMS} \tag{11}$$

where

- V_{LPP} = peak-to-peak voltage at the load

Consolidating 式 8 to 式 11 allows the required peak-to-peak voltage at the load to be expressed as a function of the crest factor, the load impedance, and the power at the load, as given by 式 12:

$$V_{LPP} = 2 \times CF \times \sqrt{(1\ mW) \times R_L \times 10^{\frac{P_L}{10}}} \tag{12}$$

V_{LPP} is usually computed for a nominal line impedance and can be taken as a fixed design target.

The next step in the design is to compute the individual amplifier output voltage and currents as a function of peak-to-peak voltage on the line and transformer-turns ratio.

When this turns ratio changes, the minimum allowed supply voltage also changes. The peak current in the amplifier output is given by 式 13:

$$\pm I_P = \frac{1}{2} \times \frac{2 \times V_{LPP}}{n} \times \frac{1}{4\ R_M} \quad (13)$$

where

- V_{PP} is as defined in 式 12, and
- R_M is as defined in 式 7 and 図 7-5

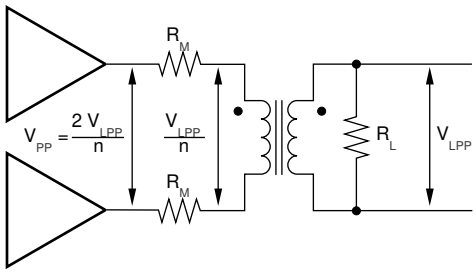


図 7-5. Driver Peak Output Voltage

With the previous information available, a supply voltage and the turns ratio desired for the transformer can now be selected, and the headroom for the THS6212 can be calculated.

The model shown in 図 7-6 can be described with 式 14 and 式 15 as:

1. The available output swing:

$$V_{PP} = V_{CC} - (V_1 + V_2) - I_P \times (R_1 + R_2) \quad (14)$$

2. Or as the required supply voltage:

$$V_{CC} = V_{PP} + (V_1 + V_2) + I_P \times (R_1 + R_2) \quad (15)$$

The minimum supply voltage for power and load requirements is given by 式 15.

V_1, V_2, R_1, and R_2 are given in 表 7-1 for the ±14-V operation.

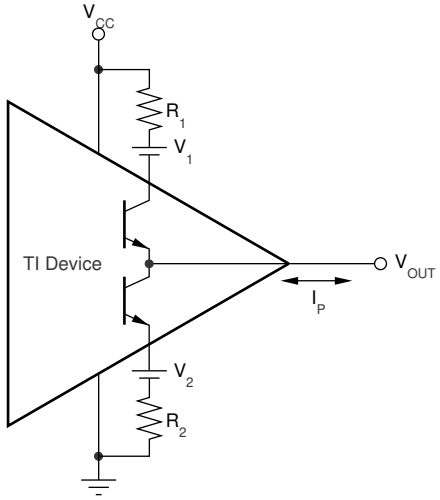


図 7-6. Line Driver Headroom Model

表 7-1. Line Driver Headroom Model Values

V_S	V_1	R_1	V_2	R_2
±14 V	1 V	0.6 Ω	1 V	1.2 Ω

When using a synthetic output impedance circuit (see 図 7-4), a significant drop in bandwidth occurs from the specification provided in the *Electrical Characteristics* tables. This apparent drop in bandwidth for the differential signal is a result of the apparent increase in the feedback transimpedance for each amplifier. This feedback transimpedance equation is given by 式 16:

$$Z_{FB} = R_F \times \frac{1 + 2 \times \frac{R_S}{R_L} + \frac{R_S}{R_P}}{1 + 2 \times \frac{R_S}{R_L} + \frac{R_S}{R_P} - \frac{R_F}{R_P}} \tag{16}$$

To increase the 0.1-dB flatness to the frequency of interest, adding a serial RC in parallel with the gain resistor can be needed, as shown in 図 7-7.

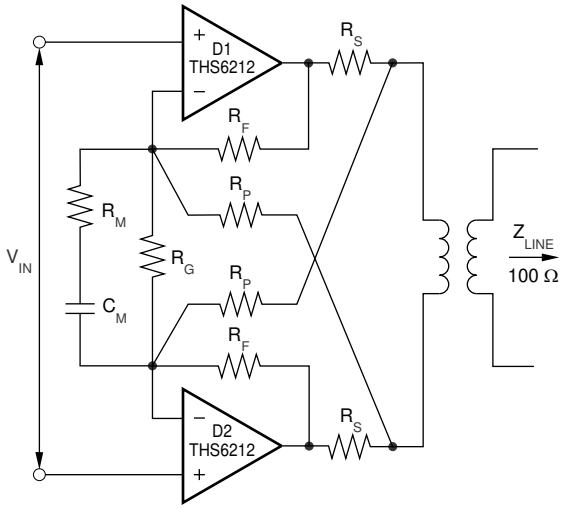


図 7-7. 0.1-dB Flatness Compensation Circuit

7.2.2.2.2 Computing Total Driver Power for Line-Driving Applications

The total internal power dissipation for the THS6212 in a line-driver application is the sum of the quiescent power and the output stage power. The THS6212 holds a relatively constant quiescent current versus supply voltage—giving a power contribution that is simply the quiescent current times the supply voltage used (the supply voltage is greater than the solution given in 式 15). The total output stage power can be computed with reference to 図 7-8.

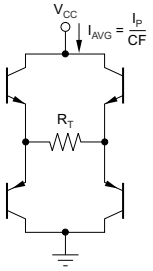


図 7-8. Output Stage Power Model

The two output stages used to drive the load of 図 7-5 are shown as an H-Bridge in 図 7-8. The average current drawn from the supply into this H-Bridge and load is the peak current in the load given by 式 13 divided by the crest factor (CF) for the signal modulation. This total power from the supply is then reduced by the power in R_T, leaving the power dissipated internal to the drivers in the four output-stage transistors. That power is simply the target line power used in 式 8 plus the power lost in the matching elements (R_M). In the following examples, a perfect match is targeted giving the same power in the matching elements as in the load. The output stage power is then set by 式 17.

$$P_{OUT} = \frac{I_P}{CF} \times V_{CC} - 2P_L \tag{17}$$

The total amplifier power is then given by 式 18:

$$P_{TOT} = I_Q \times V_{CC} + \frac{I_P}{CF} \times V_{CC} - 2P_L \tag{18}$$

For the example given by 図 7-4, the peak current is 159 mA for a signal that requires a crest factor of 5.6 with a target line power of 20.5 dBm into a 100-Ω load (115 mW).

With a typical quiescent current of 19.5mA and a nominal supply voltage of ±14V, the total internal power dissipation for the solution of 図 7-4 is given by 式 19:

$$P_{TOT} = 19.5\,mA(28\,V) + \frac{159\,mA}{5.6}(28\,V) - 2(115\,mW) = 1111\,mW \tag{19}$$

7.3 Best Design Practices

- Include a thermal design at the beginning of the project.
- Use well-terminated transmission lines for all signals.
- Use solid metal layers for the power supplies.
- Keep signal lines as straight as possible.
- Use split supplies where required.
- Do not use a lower supply voltage than necessary.
- Do not use thin metal traces to supply power.
- Do not forget about the common-mode response of filters and transmission lines.

7.4 Power Supply Recommendations

The THS6212 is designed to operate optimally using split power supplies. The device has a very wide supply range of 10V～28V to accommodate many different application scenarios. Choose power-supply voltages that allow for adequate swing on both the inputs and outputs of the amplifier to prevent affecting device performance. The ground pin provides the ground reference for the control pins and must be within V_{S-} to (V_{S+} – 5 V) for proper operation.

7.5 Layout

7.5.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS6212 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

1. Minimize parasitic capacitance to any ac ground for all signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, this capacitance can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins must be opened in all ground and power planes around these pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. Minimize the distance (less than 0.25 in, or 6.35 mm) from the power-supply pins to high-frequency 0.1-µF decoupling capacitors. At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at lower frequencies, must also be used on the main supply pins. These capacitors can be placed somewhat farther from the device and can be shared among several devices in the same area of the PCB.
3. Careful selection and placement of external components preserve the high-frequency performance of the THS6212. Resistors must be of a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition, axially-leaded resistors can also provide good high-frequency performance.

   Again, keep leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described in the Wideband Current-Feedback Operation *Detailed Design Procedure* section. Increasing the value reduces the bandwidth, whereas decreasing the value leads to a more peaked frequency response. The 1.24-kΩ feedback resistor used in the *Typical Characteristics* sections at a gain of 10 V/V on 28V supplies is a good starting point for design. Note that a 1.5-kΩ feedback resistor, rather than a direct short, is recommended for a unity-gain follower application. A current-feedback op amp requires a feedback resistor to control stability even in the unity-gain follower configuration.
4. Make connections to other wideband devices on the board with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils [0.050 in to 0.100 in, or 1.27 mm to 2.54 mm]) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the recommended R_S versus capacitive load plots (see 図 5-10). Low parasitic capacitive loads (less than 5 pF) do not always need an isolation resistor because the THS6212 is nominally compensated to operate with a 2-pF parasitic load. If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is not necessary on board; in fact, a higher impedance environment improves distortion (see the distortion versus load plots). With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS6212 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device.

This total effective impedance must be set to match the trace impedance. The high output voltage and current capability of the THS6212 allows multiple destination devices to be handled as separate transmission lines, each with respective series and shunt terminations. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only.

Treat the trace as a capacitive load in this case and set the series resistor value as shown in the recommended R_S versus capacitive load plots. However, this configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation as a result of the voltage divider formed by the series output into the terminating impedance.

5. Socketing a high-speed part such as the THS6212 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, and can make achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the THS6212 directly onto the board.
6. Solder the exposed thermal pad to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.

7.5.2 Layout Example

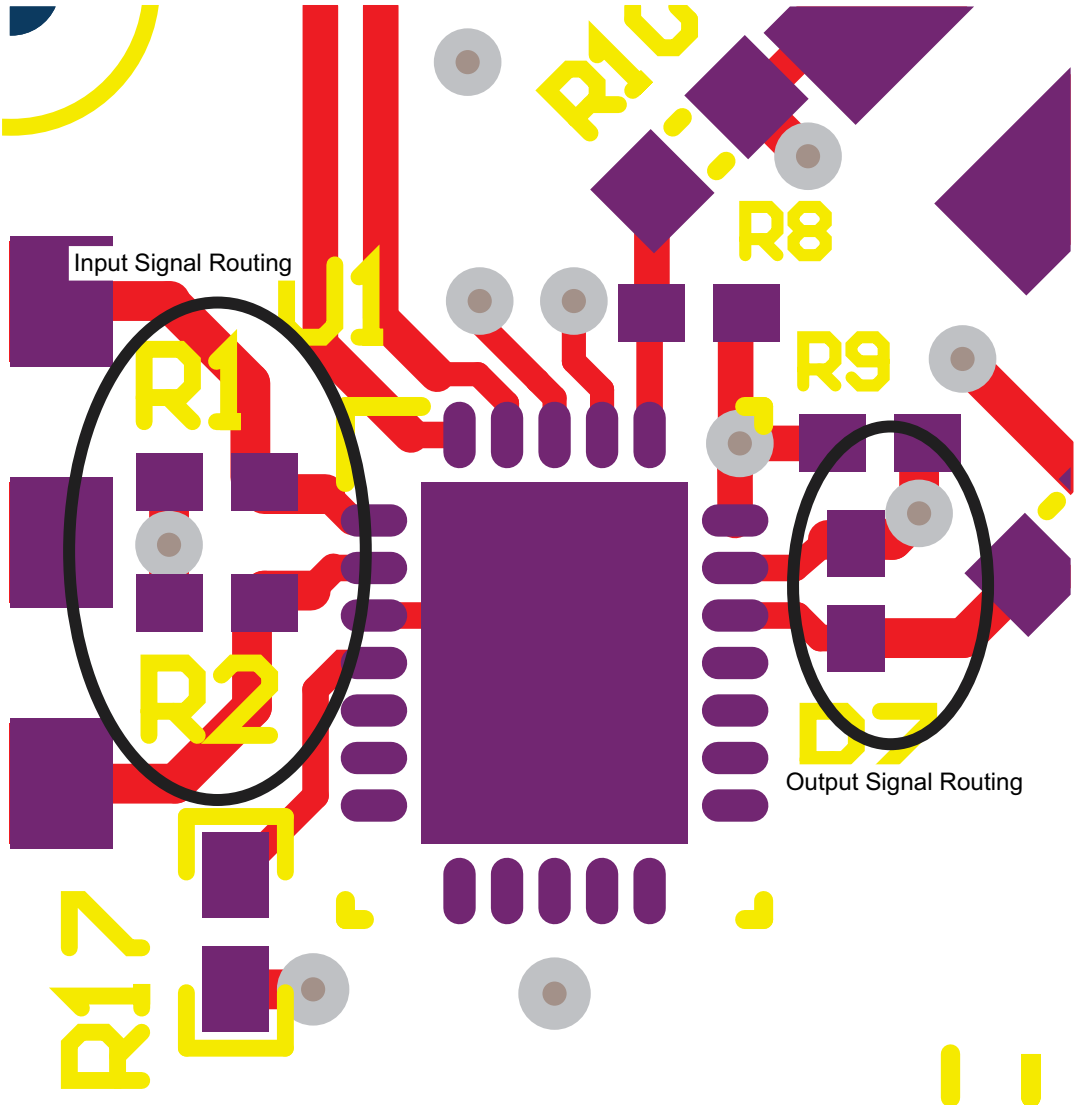


図 7-9. THS6212EVM Top-Layer Example

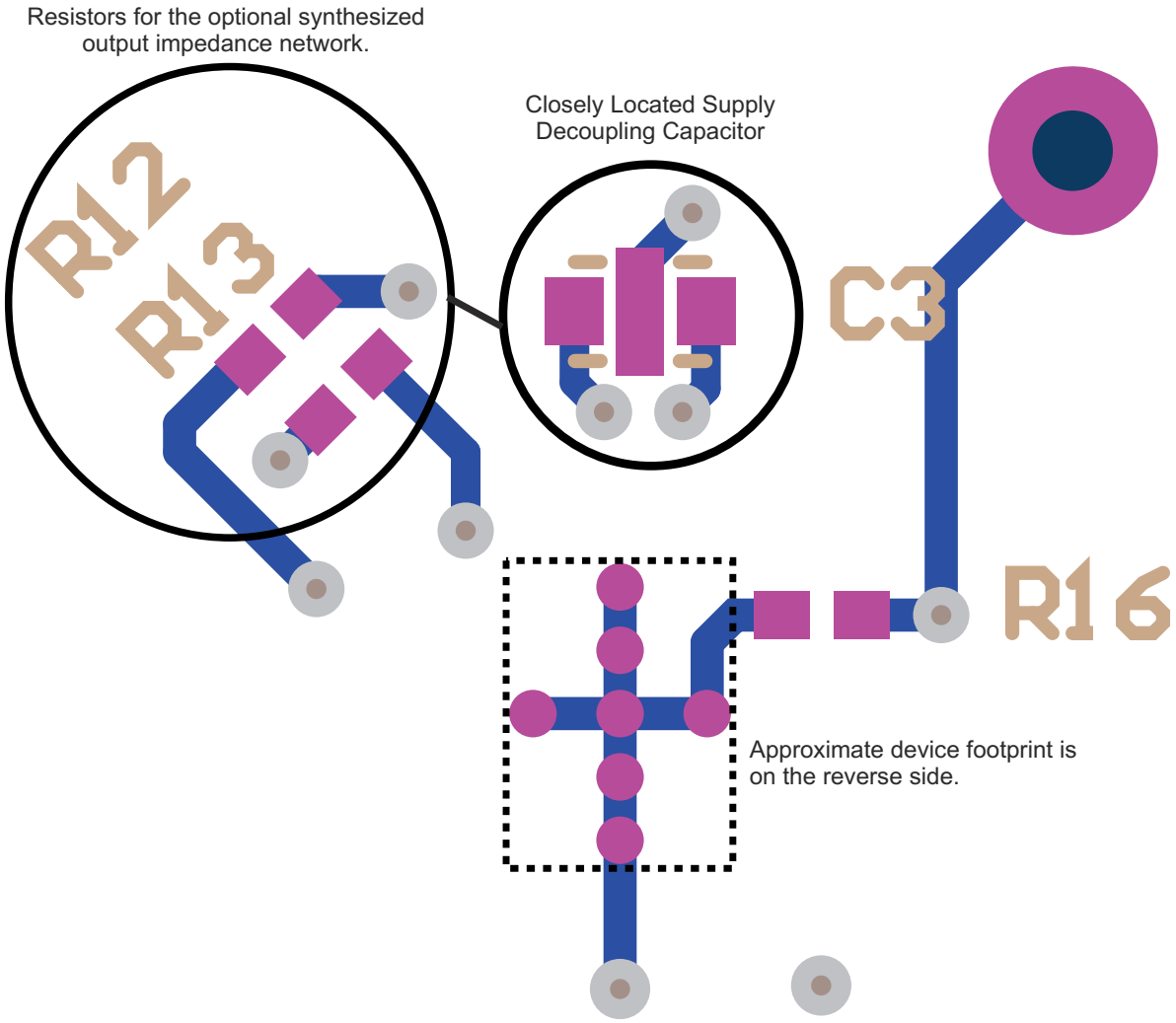


図 7-10. THS6212EVM Bottom Layer Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *THS6214 Dual-Port, Differential, VDSL2 Line Driver Amplifiers* data sheet
- Texas Instruments, *THS6222 8-V to 32-V, Differential Broadband HPLC Line Driver With Common-Mode Buffer* data sheet
- Texas Instruments, *THS6212EVM User's Guide*

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (May 2021) to Revision F (June 2024)	Page
• 「概要」の「パッケージ情報」表を更新	1
• Deleted maximum junction temperature continuous operation, long-term reliability from *Absolute Maximum Ratings*	4

Changes from Revision D (November 2019) to Revision E (May 2021)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「特長」で中バイアス モードの値を 17.7mA から 17.5mA に変更	1
• 「特長」で低バイアス モードの値を 12.2mA から 11.9mA に変更	1

- Updated noise evaluation in *Differential Noise Performance* 22
- Added R_S = 50 Ω in *Differential Noise Performance* 22
- Changed 38.9 nV/√Hz calculation to 53.3 nV/√Hz in *Differential Noise Performance* 22
- Changed 7 nV/√Hz calculation to 6.5 nV/√Hz in *Differential Noise Performance* 22
- Changed output offset calculation to typical rather than worst case in *DC Accuracy and Offset Control* section..... 23
- Changed quiescent current value from 23 mA to 19.5 mA in *Wideband Current-Feedback Operation* section..... 24
- Changed swing from 1.9 V from either rail to 49 Vpp in *Wideband Current-Feedback Operation* section..... 24
- Changed current drive from 416 mA to 650 mA in*Wideband Current-Feedback Operation* section..... 24
- Changed ± 6 V supply to 28 V supply in*Wideband Current-Feedback Operation* section..... 24
- Changed 140 MHz bandwidth to 285 MHz in*Wideband Current-Feedback Operation* section..... 24
- Changed *Noninverting Differential I/O Amplifier*figure in*Wideband Current-Feedback Operation* section..... 24
- Changed *Frequency Response* and *Harmonic Distortion* figures in *Application Curves* section..... 25
- Changed *Dual-Supply Downstream Driver* figure..... 26
- Changed supply voltages to ±14 V in *Line Driver Headroom Requirements* section..... 27
- Changed quiescent current value from 23 mA to 19.5 mA and ±12 V to ±14 V in *Computing Total Driver Power for Line-Driving Applications* 29
- Changed 23 mA to 19.5 mA, 24 V to 28 V and 1003 mW to 11 mW in *Computing Total Driver Power for Line-Driving Applications* 29
- Changed supply range from "±5 V to ±14 V" to "10 V to 28 V" in *Power Supply Recommendations* section.. 30
- Changed referenced figures for R_S versus capacitive load in *Driving Capacitive Loads* section..... 31
- Deleted *Wafer and Die Information* section..... 31
- Changed ±12-V to 28-V in *Layout Guidelines* section..... 31

Changes from Revision C (May 2016) to Revision D (November 2019) **Page**

- 2 つの「特長」項目を最後に追加..... 1
- Added GND pin voltage spec in *Recommended Operating Conditions* 4
- Added last paragraph to *Overview* section 19
- Changed *Dual-Supply Downstream Driver* figure..... 26

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6212IRHFR	ACTIVE	VQFN	RHF	24	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	THS6212	Samples
THS6212IRHFT	ACTIVE	VQFN	RHF	24	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	THS6212	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

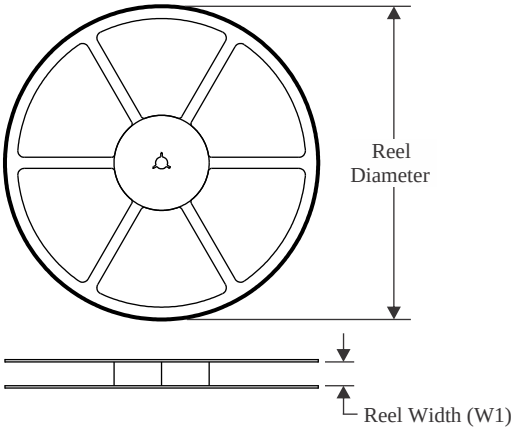
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

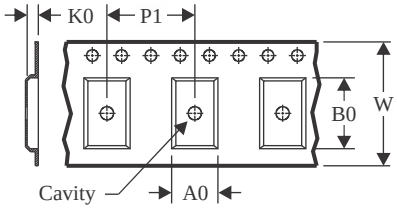
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

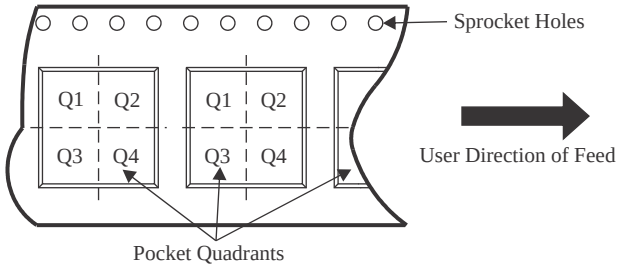


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

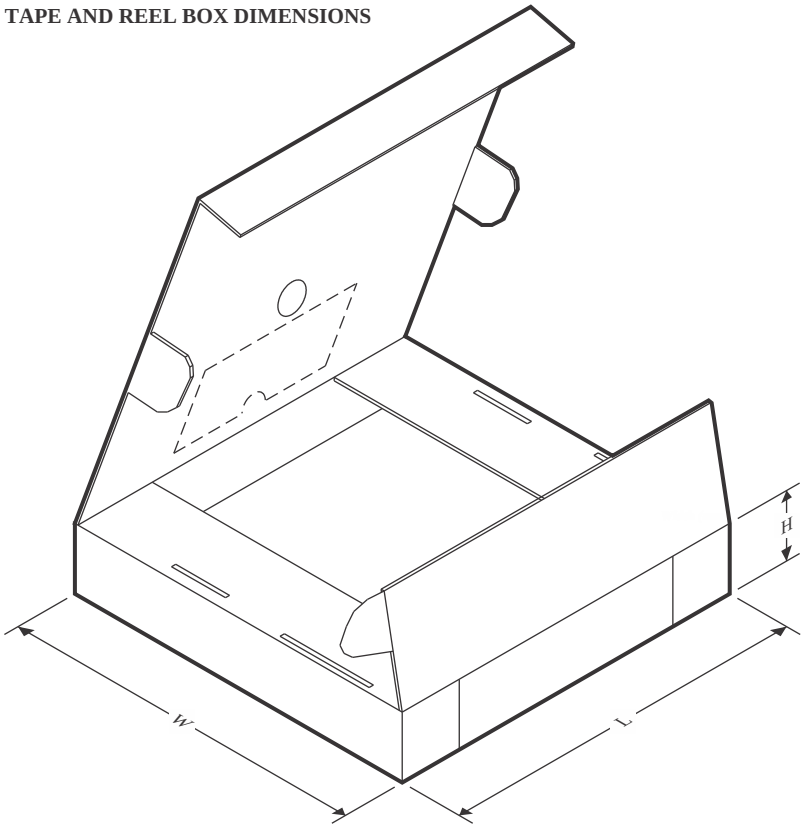
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6212IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
THS6212IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
THS6212IRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

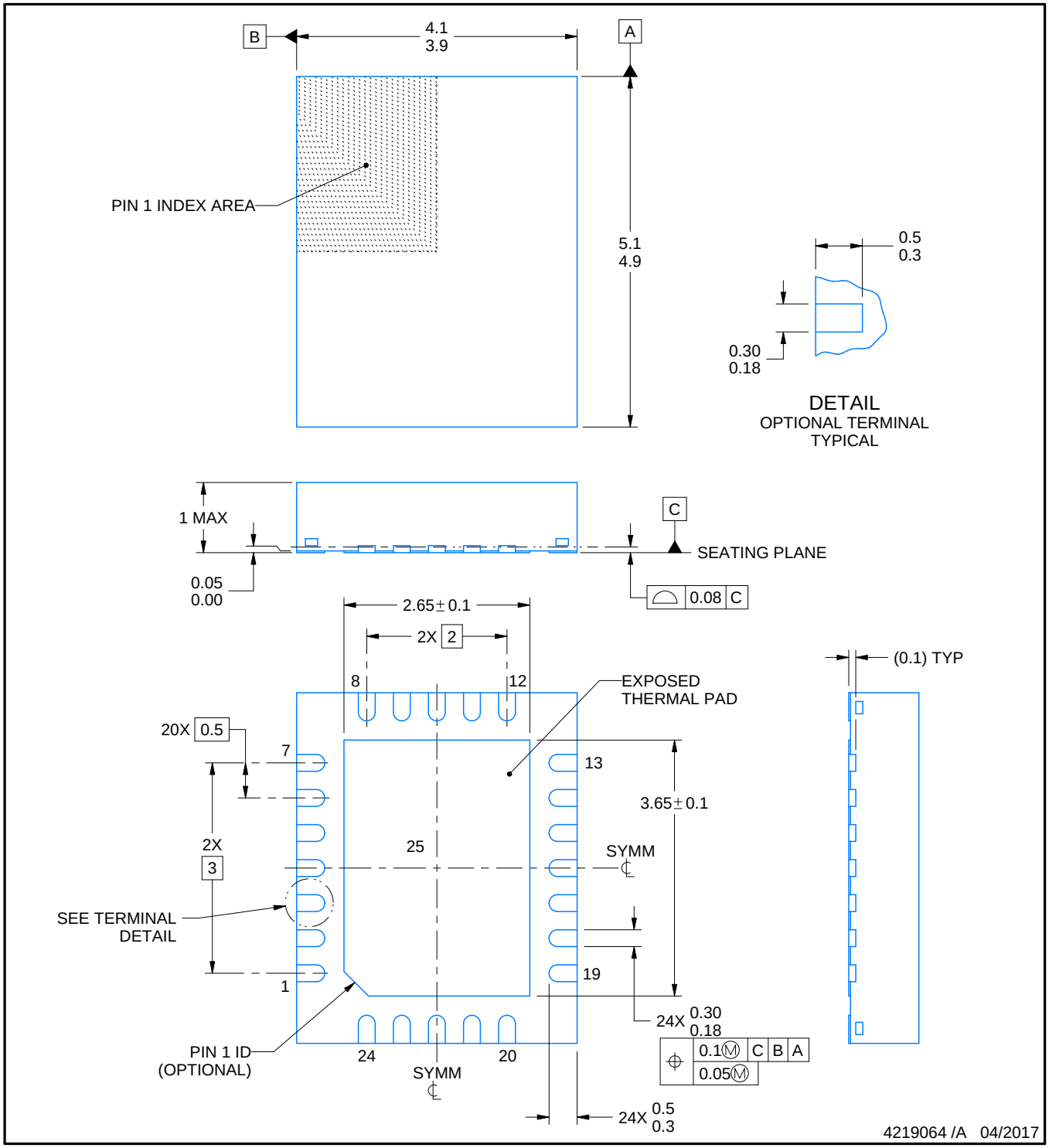
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6212IRHFR	VQFN	RHF	24	3000	356.0	356.0	35.0
THS6212IRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
THS6212IRHFT	VQFN	RHF	24	250	210.0	185.0	35.0

PACKAGE OUTLINE

RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

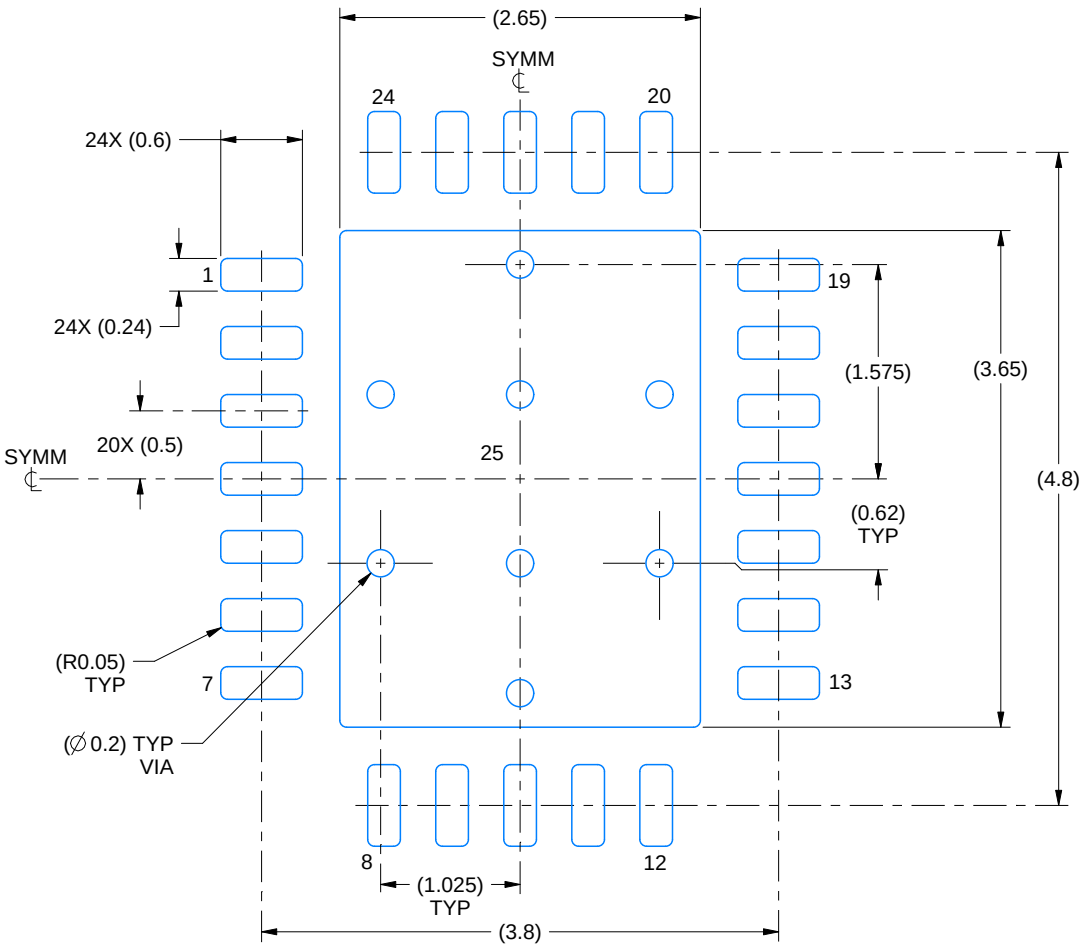
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

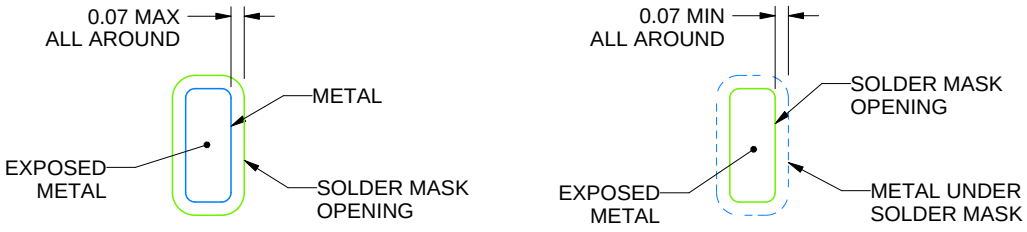
RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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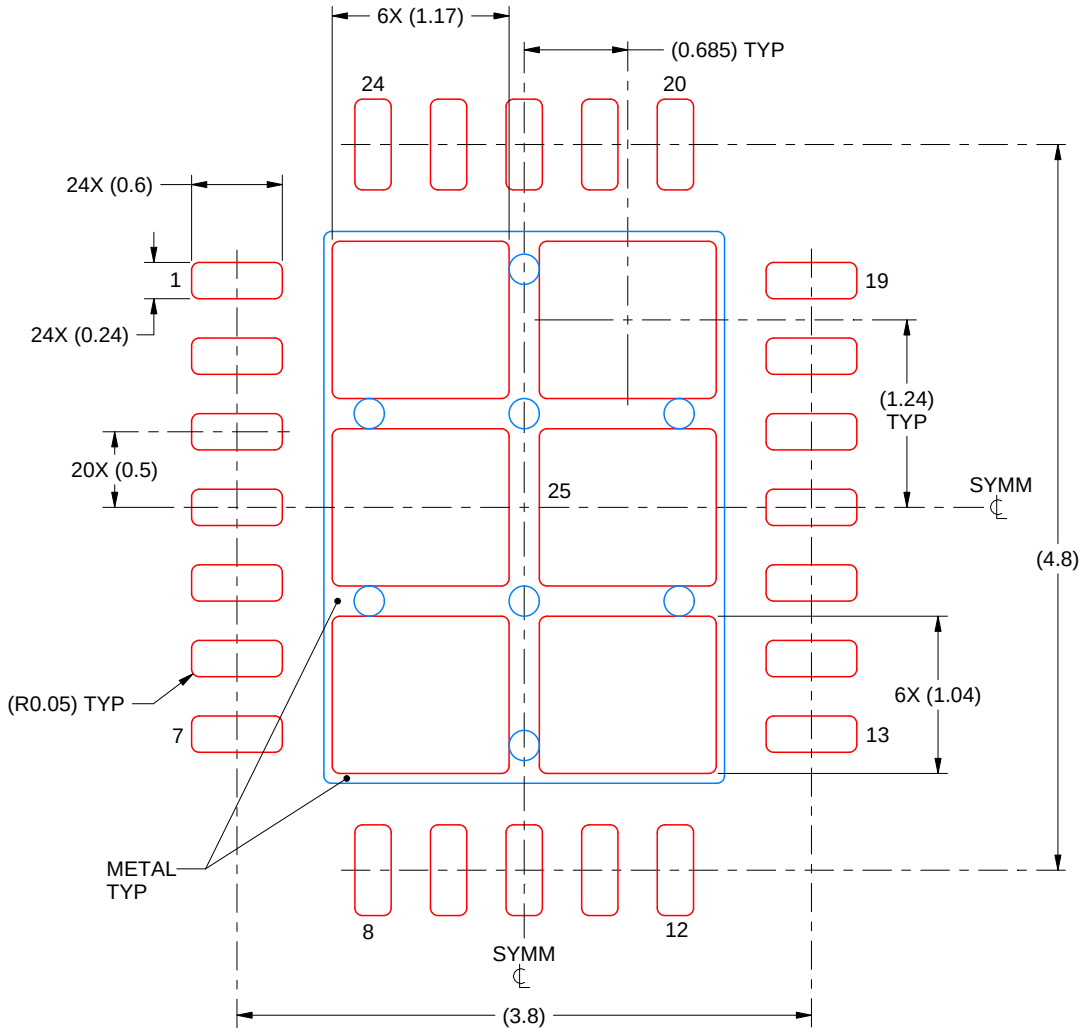
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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