Application Note

AM26x Hardware Design Guidelines

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ABSTRACT

The AM26x Hardware Design Guidelines is an essential document for hardware designers creating PCB systems based on the AM26x family of MCU devices. This document serves to integrate device-specific schematic and PCB layout recommendations by utilizing hardware design examples from the various AM263x, AM263Px, and AM261x evaluation modules (EVMs). The AM26x EVMs include the following hardware platforms:

Table 1-1. AM26x Evaluation Module (EVM) Platforms

Device Family	Hardware Platform		
	LaunchPad	ControlCARD	System on Module (SOM)
AM263x	LP-AM263	TMDSCNCD263	
AM263Px	LP-AM263P	TMDSCNCD263P	
AM261x	LP-AM261		AM261-SOM-EVM

In general, AM26x LaunchPads are lower-cost, entry-level evaluation platforms, while ControlCARDs and SOMs are meant for engineers designing complex systems with higher I/O requirements.

Additional collateral documents and tools can be found in References.

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1 Introduction

The AM263x, AM263Px, and AM261x devices are single, dual, or quad-core Arm® Cortex®-R5F based MCUs in the Sitara™ MCU family intended for industrial and automotive motion control applications.

Note

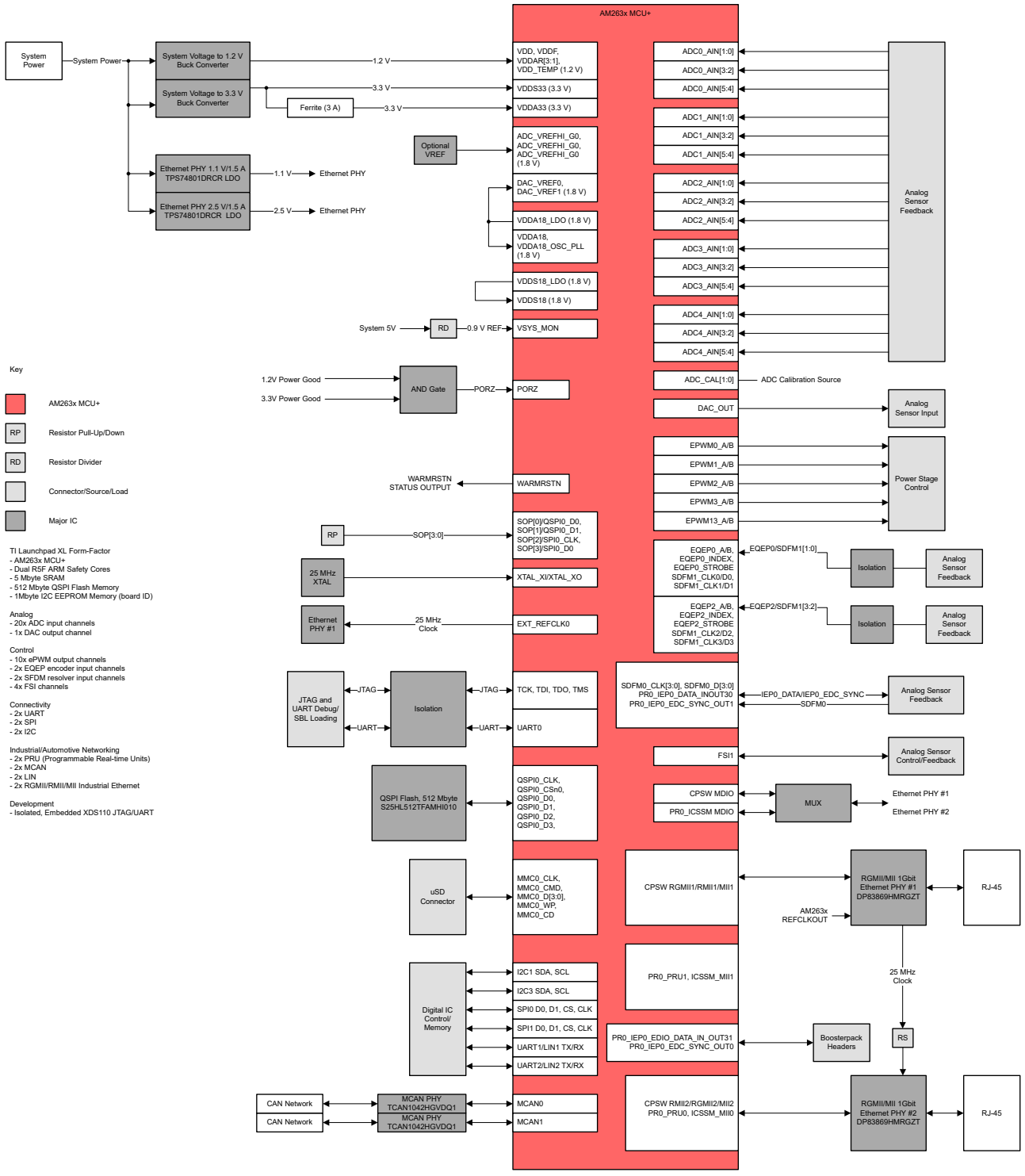
In this document, AM26x refers to the TI Sitara™ MCU family of high-performance microcontrollers. This includes the AM263x, AM263Px, and AM261x devices. Device-specific references are denoted by the full general product number (AM263x, AM263Px, AM261x), while general device information are denoted by AM26x.

A typical AM26x design with a discrete power design is shown in Figure 1-1. This diagram is excerpted from the AM263x LaunchPad (LP-AM263) system block diagram.

A typical AM26x design with a Power Management Integrated Circuit (PMIC)-based power design is shown in Figure 1-2. This diagram is excerpted from the AM263Px controlCard (TMDSCNCD263P) system block diagram.

A typical AM261x design with a smaller footprint PMIC is shown in Figure 1-3. This diagram is taken from the AM261x LaunchPad (LP-AM261) system block diagram.

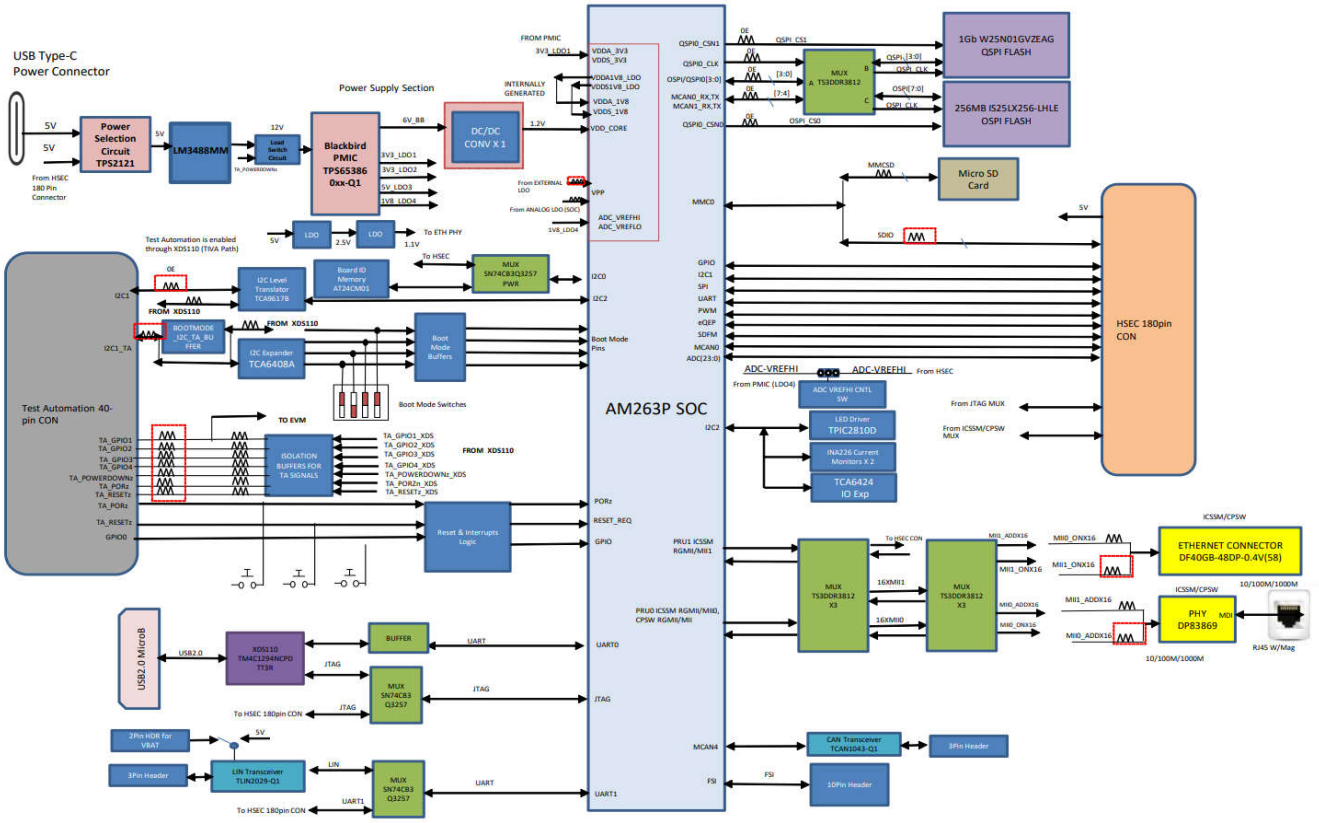
As seen in the following block diagrams, the AM26x devices offer designers a wide range of digital connectivity, control and analog sensor feedback options with multiple power design options supported.



Note

The current requirement for the *System Voltage to 1.2V Buck Converter* for AM263x, AM263Px is 3A. For AM261x, the current limit is 2A.

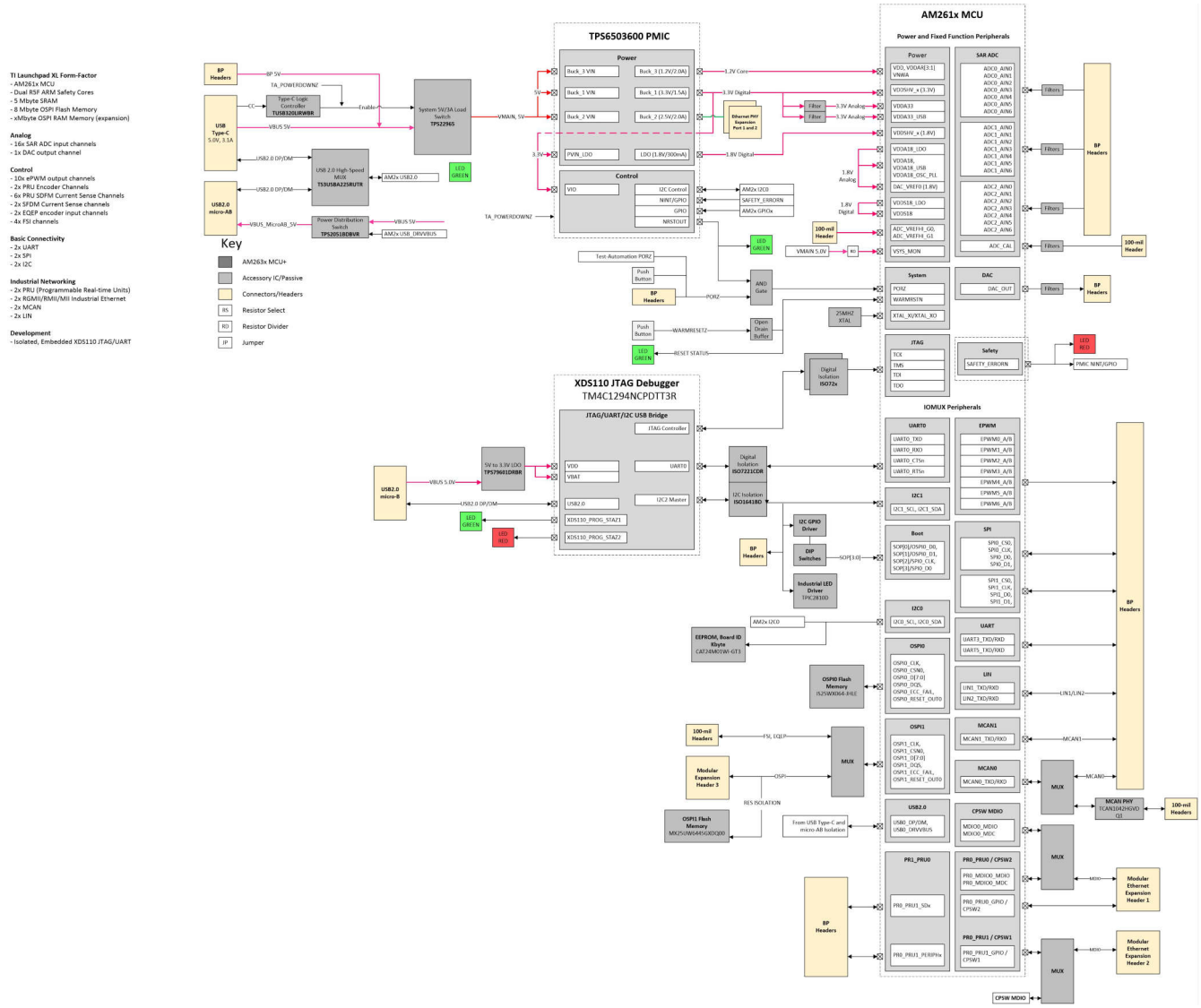
Figure 1-1. Typical AM26x System Block Diagram with Discrete Power (Based on LP-AM263 Launchpad Design)



Note

For AM263x, AM263Px, the 1.2V DC/DC converter must output 3A. For AM261x, the DC/DC converter must be current limited to 2A.

Figure 1-2. Typical AM26x System Block Diagram with PMIC Power (Based on TMDSCNCD263P controlCard Design)



Note

Due to the current output of the Buck_3 of the TPS6503600 (2A), this system block diagram is only applicable to AM261x systems.

Figure 1-3. Typical AM261x System Block Diagram with PMIC Power (Based on LP-AM261 Design)

This document must be referenced along with the other key AM26x collateral references. See Section 16 for a complete list of supplementary documents for the AM26x MCU devices.

Table 1-1. Acronyms Used in This Document

Acronym	Description
EVM	Evaluation Module. Referencing TI PCB assemblies such as the AM263x controlCard (TMDSCNCD263) or AM263x LaunchPad (LP-AM263).
PDN	Power Distribution Network. The active and passive components providing regulated power to a load such as the AM263x MCU power pins.
EMI	Electromagnetic Interference
PI	Power Integrity
SI	Signal Integrity
BOM	Bill of Materials
PMIC	Power Management Integrated Circuit
SOM	System on Module
LP	LaunchPad
SoC	System on a Chip

2 Power

2.1 Discrete DC-DC Power Solution

The AM263x LaunchPad and AM263x controlCard EVM designs both integrate a set of buck-converter, DC-DC regulators that are useful as a reference power design for some systems. This design consists of a pair of TPS62913 buck-converter regulators for AM263x MCU core, system digital and analog I/O power, and a set of TPS74801 LDO for powering paired industrial Ethernet PHY.

Current and transient requirements of the DC-DC closed-loop and passive power plane and decoupling network are taken from the power consumption and transient loading tables: Table 2-5 and Table 2-6. Many DC-DC regulators can be matched to fit within these requirements and the maximum power consumption.

TI also recommends to use the power-good generation circuits available on these and similar DC-DC regulators to drive the power on reset (PORz) into the AM26x.

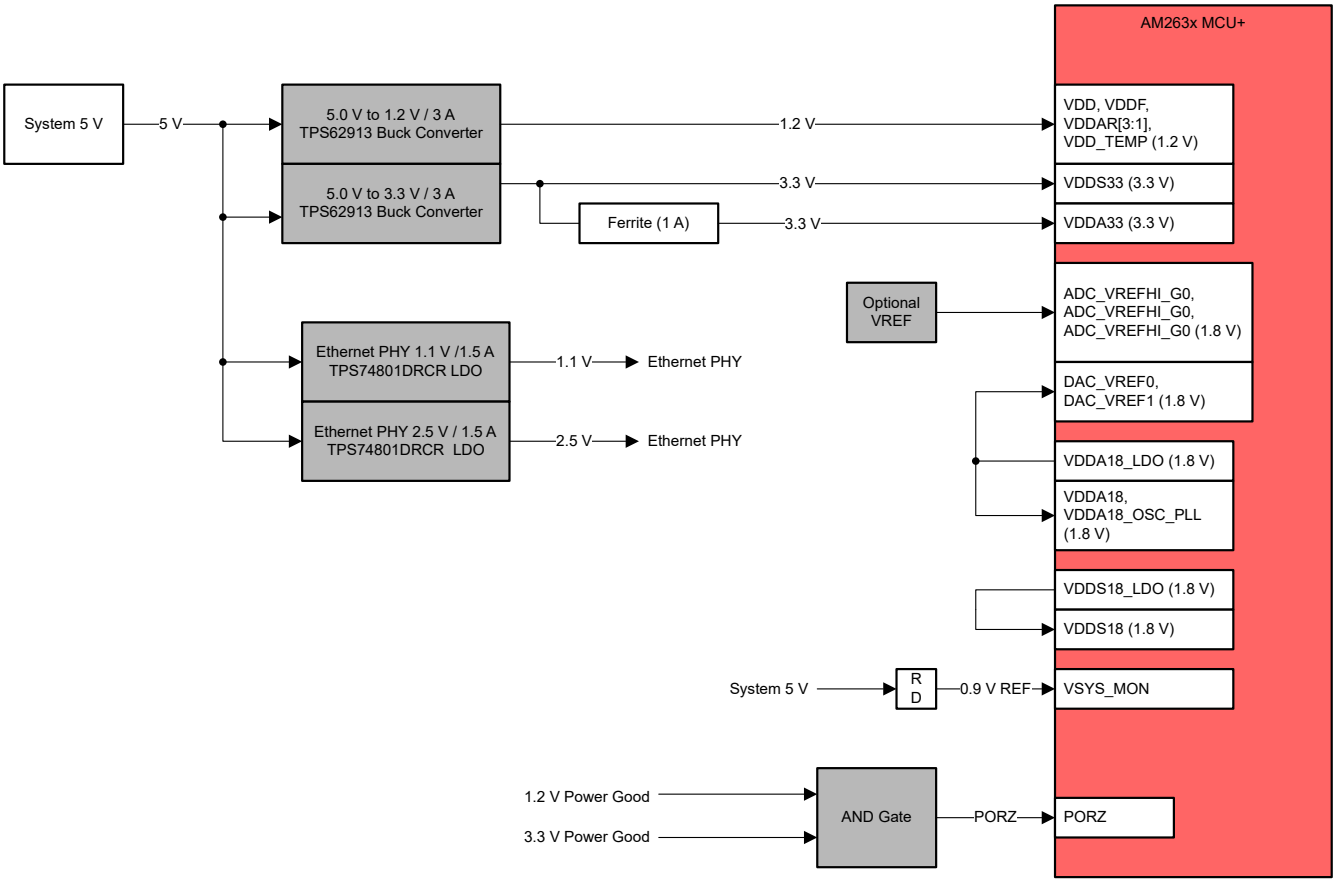


Figure 2-1. AM263x DC-DC Regulator Example Design

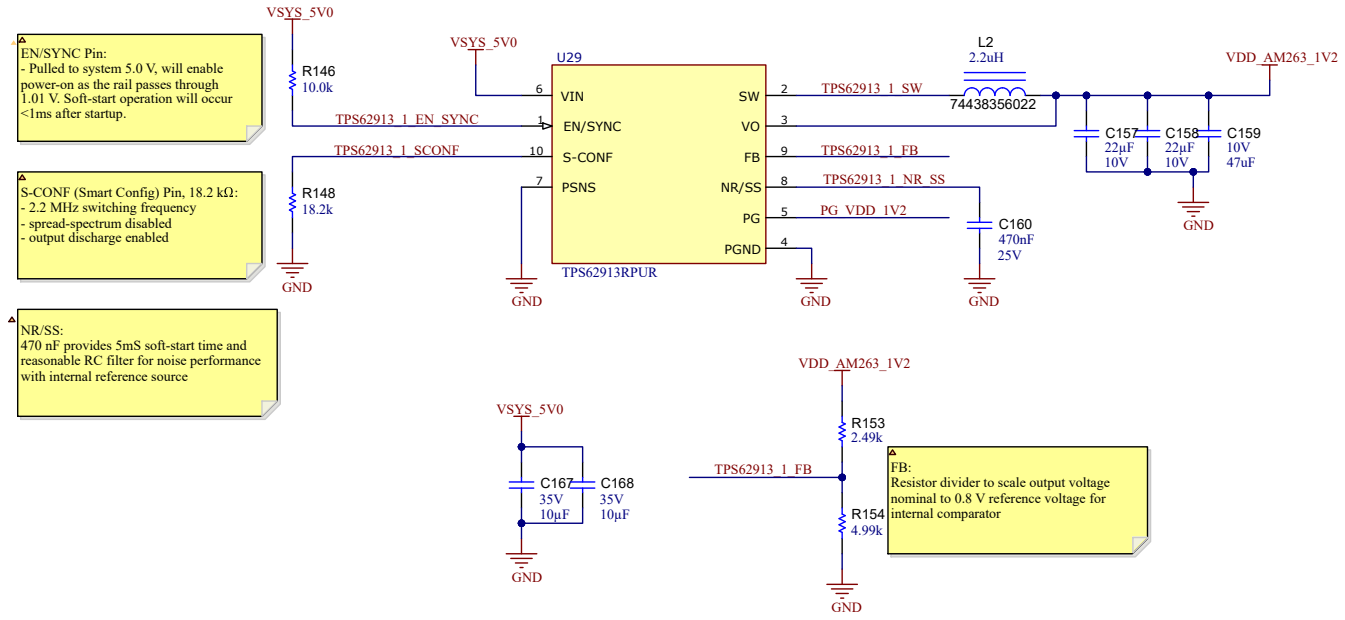


Figure 2-2. AM263x LP-AM263 Schematic Excerpt 1.2V Core Power Implementation

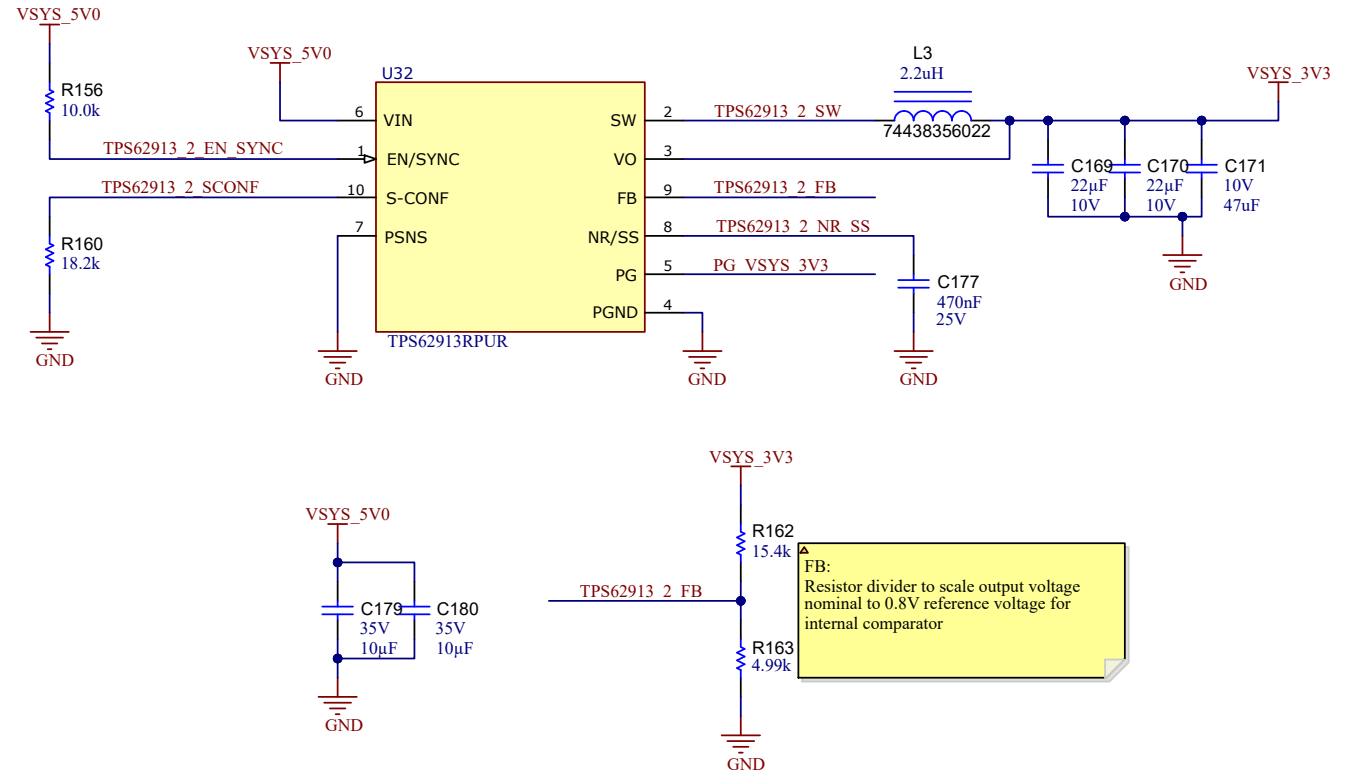


Figure 2-3. AM263x LP-AM263 Schematic Excerpt 3.3V System Digital, Analog I/O Power Implementation

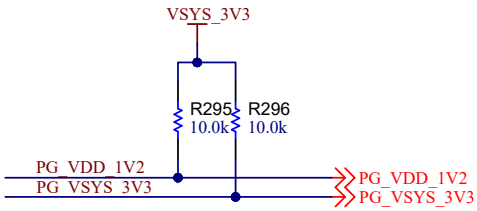


Figure 2-4. AM263x LP-AM263 Schematic Excerpt – Power Good Implementation (see PORz Reset Implementation)

2.2 Integrated PMIC Power Solution

Using TPS653860 with AM26x

The AM263Px controlCard EVM and AM261x controlSOM EVM designs make use of a multirail power supply for microcontrollers in safety-relevant applications (TPS6538600QDCARQ1). The PMIC integrates **four**= supply rails to power the MCU, CAN, and other on-board peripherals.

The NRES output of the PMIC needs to be used to help drive the PORz reset input to the AM263x, AM263Px, or AM261x device to make sure the power on sequencing of the power rails is complete before releasing the MCU from reset.

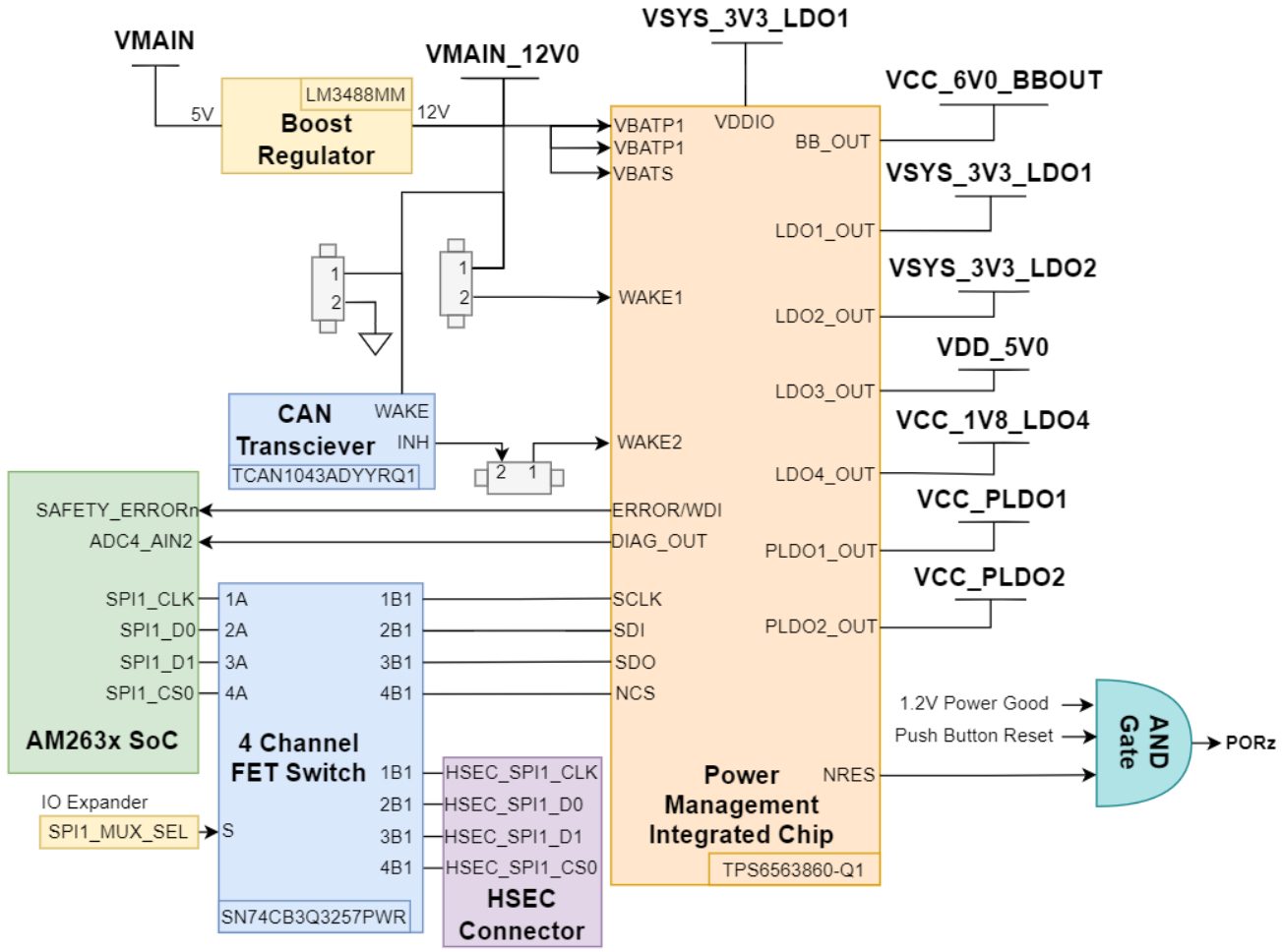


Figure 2-5. AM263Px TMDSCNCD263P PMIC Implementation

Using TPS650360 with AM261x

The AM261x LaunchPad EVM design makes use of the smaller-package, lower-cost TPS6503600 PMIC. This PMIC integrates four supply rails to power the MCU and other on-board peripherals.

Note

This PMIC can output 1.2V at 2A, which meets the VDD CORE supply requirements of the AM261x MCU. AM263x and AM263Px require 1.2V at 3A, so this PMIC must not be used to power these devices.

The nRSTOUT output of the PMIC must be used to help drive the PORz reset input to the AM261x device to make sure the power on sequencing of the power rails is complete before releasing the MCU from reset.

2.3 Power Decoupling and Filtering

Table 2-1 describes the initial BGA decoupling and power filtering required for the ZCZ package of the AM263x, AM263Px. and AM261x microcontrollers. These decoupling capacitor quantities and sizes were based on the initial simulation feedback of the Control Card EVM PCB and AM263x package with the transient use-cases shown in Table 2-5. Table 2-2 describes the BGA decoupling and power filtering required for the ZFG, ZNC, and ZEJ packages of the AM261x MCU. These packages support 3.3V and 1.8V flash IO on the OSPI/QSPI peripherals, and thus have slightly different device power rails compared to the ZCZ package devices, which only support 3.3V flash IO on the OSPI peripherals. Variation in overall power pin counts also account for differences in decoupling on the AM261x ZFG/ZNC/ZEJ packages.

The decoupling network presented in the sections below and in the AM263x EVM schematics and layouts are reasonable starting points for any AM263x, AM263Px, or AM261x PCB design. However, due to specific PCB routing differences and the resulting plane capacitance and decoupling mounting inductances and other parasitics, TI highly recommends that designers simulate and measure the specific power distribution network performance. Simulations and measurements are usually done with target application software active, and intended operating environment conditions applied to the system.

Table 2-1. AM263x, AM263Px, AM261x-ZCZ Recommended Decoupling per Power Net

Device Supply	Quantity	Comment	Part #	Manufacturer
VDD_CORE	17	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	3	3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
VDDAR[3:1]	2	3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	3	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDS18_LDO	1	3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDS18	4	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDA18_LDO	1	4.7uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDA18	2	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDA18_OSC_PLL LC filter	1	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	1	Ferrite bead	BLM18EG121SN1D	Murata
VDDS33	7	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	1	3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
VDDA33	3	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	1	3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1	Ferrite bead	BLM18EG121SN1D	Murata
System 3.3V Power LC filter	1	3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata

Table 2-2. AM261x (all other packages) Recommended Decoupling per Power Net

Device Supply	Package or Quantity			Comment	Part #	Manufacturer
	ZFG	ZEJ	ZNC			
VDD_CORE	13	12	18	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	3			3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
VDDAR[3:2]	2			3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	2			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDS18_LDO	1			3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDS18	1			3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	7	8	8	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDA18_LDO	1			4.7uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	2	1	1	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDA18_USB	1			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDA18	2			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDA18_OSC_PLL LC filter	1			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	1			Ferrite bead	BLM18EG121SN1D	Murata
VDDSHV_D	1	2	2	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	1			3.3uF, 0603, X5R	C1608X5R1A335K080AC	Murata
VDDSHV_E	1			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	1			3.3uF, 0603, X5R	C1608X5R1A335K080AC	Murata
VDDSHV_A	6	5	6	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	3			3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
VDDSHV_B	1			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDSHV_C	1			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDSHV_F	1			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDSHV_G	N/A	2	N/A	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
VDDA33	2			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
	1			3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1			Ferrite bead	BLM18EG121SN1D	Murata
System 3.3V Power LC filter	1			3.3uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1			0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata

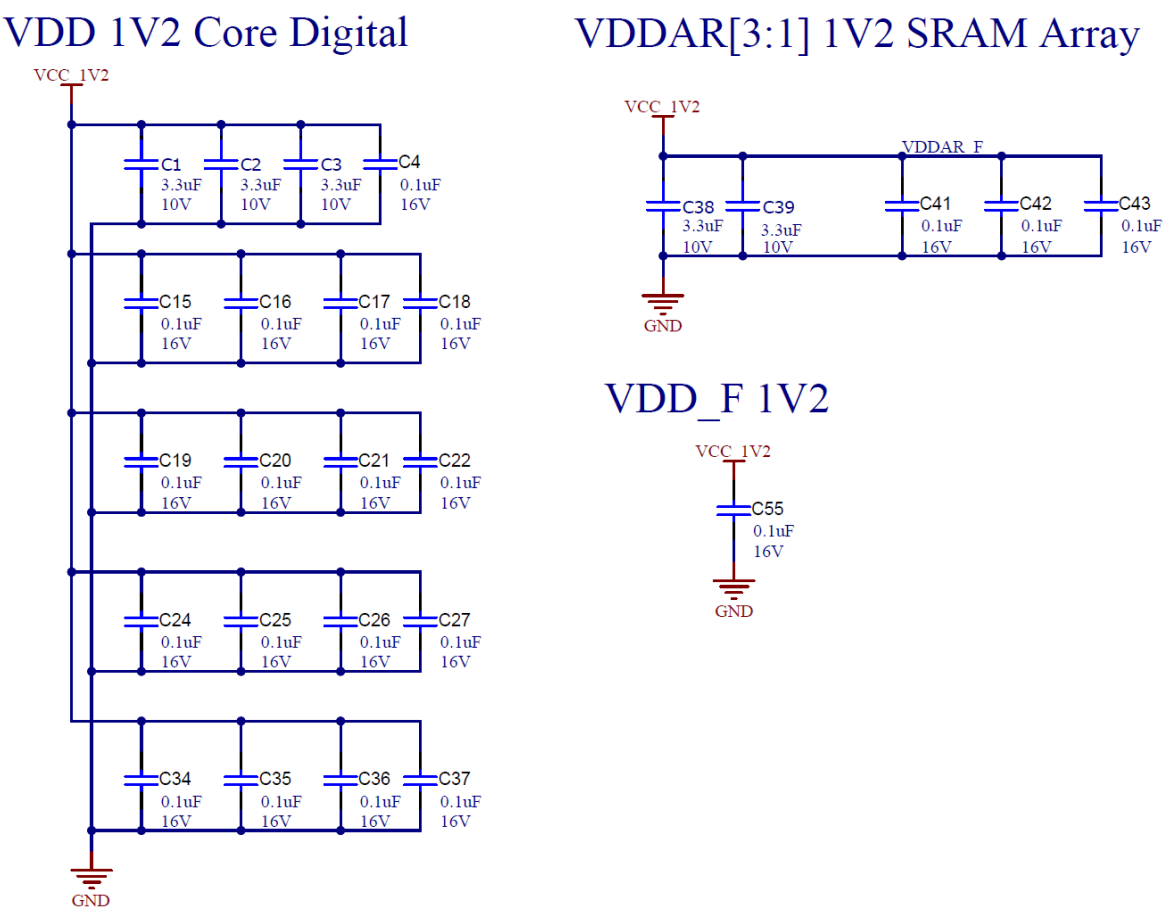


Figure 2-6. AM263x LaunchPad Excerpt – 1.2V Power Decoupling Schematic

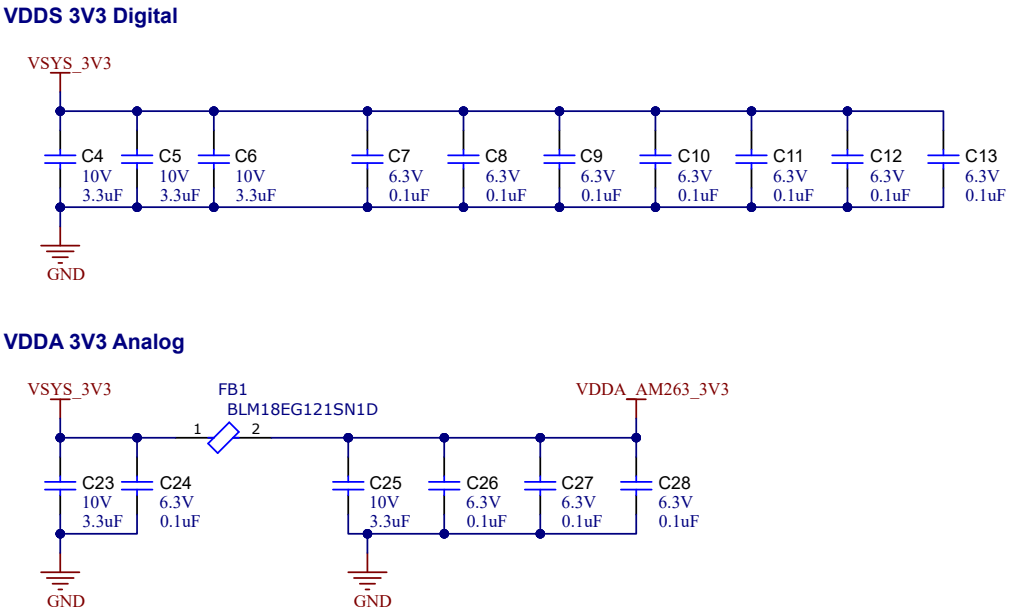


Figure 2-7. AM263x LaunchPad Excerpt – 3.3V Digital I/O and Analog I/O Decoupling and Filtering Schematic

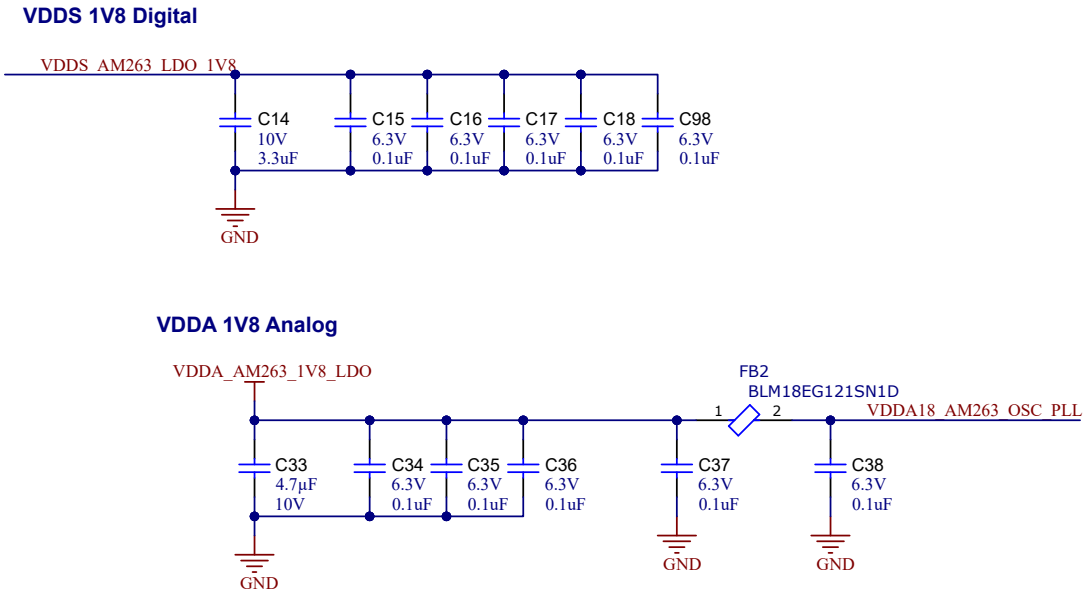


Figure 2-8. AM263x LaunchPad Excerpt – 1.8V Digital I/O and Analog I/O Decoupling and Filtering Schematic

2.3.1 ADC/DAC Voltage Reference Decoupling

The ADC and DAC voltage reference pins on AM26x devices also require specific decoupling. The requirements are outlined in the table below.

Table 2-3. AM26x ADC/DAC VREF Decoupling

ADC VREF	Quantity	Comment	Part #	Manufacturer
ADC_VREFHI_G[1:0]	1	4.7uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	2	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
ADC_VREFHI_G[2]	1	4.7uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
ADC_VREFHI_G[3] (1)	1	4.7uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
DAC_VREF[0]	1	4.7uF, 0603, X5R	C1608X5R1A335K080AC	TDK
	1	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata
DAC_VREF[1] (2)	1	0.1uF, 0201, X5R	GRM033R61A104KE15D	Murata

(1) The AM263Px Sensor Package (ZCZ_S) has additional set of ADC reference voltages, ADC_VREFHI_G3 and ADC_VREFLO_G3.
(2) AM263x and AM263Px have an additional DAC reference voltage, DAC_VREF1. An additional 0.1uF decoupling capacitor must be used at this pin.

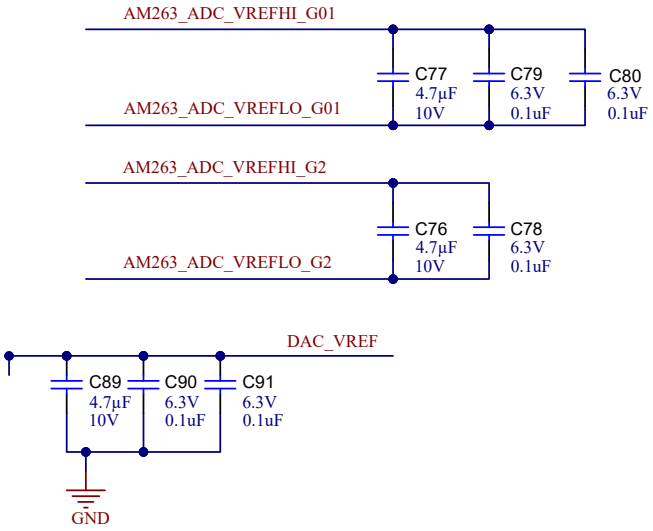


Figure 2-9. AM263x LaunchPad Excerpt – ADC and DAC VREF Decoupling Schematic

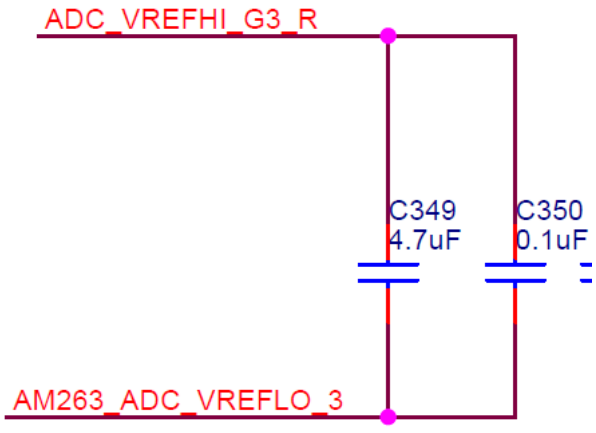


Figure 2-10. AM263Px controlCard Excerpt – additional VREFHI_G3 and VREFLO_G3 connections

2.4 Estimated Power Consumption

This section outlines the latest estimates of the AM263x, AM263Px, and AM261x peak power consumption on a per device power net basis. These values can change as more power modeling and characterization is performed. This data can be used to scale peak DC-DC conversion power margin, perform IR drop analysis of the PCB layout, and help with thermal loading analysis.

These estimates are based on initial power simulations of the device when operating at 150°C junction temperature. For the latest characterized, peak power numbers, see the specific AM26x device data sheet.

A use-case based power estimation tool (PET) is also provided for the AM26x MCUs. These tools can help further bound the peak power based on specific core and peripheral utilization duty-cycle.

Table 2-4. Estimated Peak Power Consumption at 150°C Junction Temperature

Device Supply Name	Nominal Voltage (V)	AM263x Peak Current (mA)	AM263Px Peak Current (mA)	AM261x Peak Current (mA)	Supply Description
VDD, VDDAR[3:1]	1.2	**2500**	**2800**	TBD	Digital core power
VDDS33	3.3	**200**	**200**	TBD	3.3V digital I/O power
VDDA33	3.3	**100**	**200**	TBD	3.3V analog I/O power

2.5 Power Distribution Network

This section outlines the latest estimates of the AM26x transient current requirements on a per net basis. These values can change as more power modeling and characterization is performed.

These transient use-case values were used to constrain the PDN design of the AM26x EVMs (controlCards, LaunchPads, and controlSOM) by creating a set of minimum/maximum operating frequency and PDN impedance (Z_{max}) target limits. These limits were based on the magnitude and slew-rate of simulated transient current use-cases. The use-cases were used to estimate the PDN bandwidth needed to adequately decouple the resulting transient event. Additional z-parameter simulation of the EVM PDN was used to verify that the power plane design and decoupling placement and component values meet the defined limits. This is summarized in Figure 2-11.

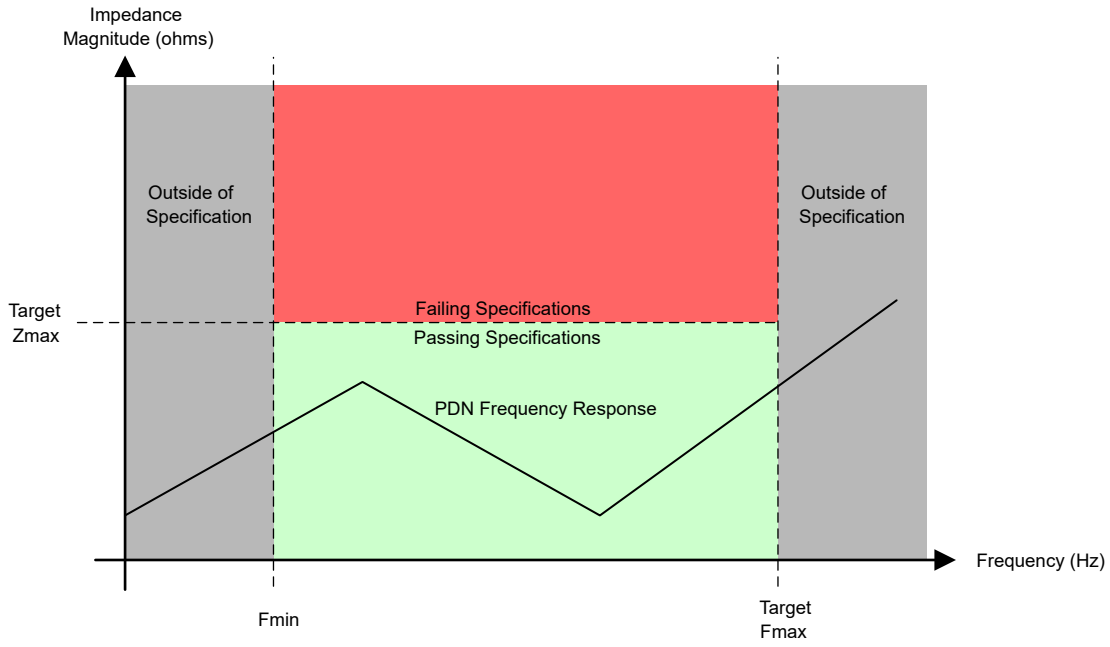


Figure 2-11. AM26x PDN Requirements – Example Diagram

Table 2-5. AM26x Transient Current Model – Use-case Conditions

Transient Case	Net Name	Nominal Voltage (V)	DC IR Budget (%)	AC Ripple Budget (%)	Idle Current (mA)	Peak Current (mA)	Idle to Peak Slew Rate (ns)	Comment
VDD BASELINE1	VDD	1.2	2.5	2.5	0	2402	2.5	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle.
VDD XTAL_PLL1	VDD	1.2	2.5	2.5	42	875	10	XTAL to PLL turn-on transient
VDD WFI1	VDD	1.2	2.5	2.5	750	1117	12.5	4x RF5 WFI event transient
VDDS33 BASELINE1	VDDS33	3.3	2.5	2.5	0	84	2.5	Baseline, simple transient model assuming 0 to peak transition in a single R5F clock cycle
VDDA33 BASELINE1	VDDA33	3.3	2.5	2.5	0	34	2.5	Baseline, simple transient model assuming 0 to peak transition in a single R5F clock cycle
VDDS18LDO BASELINE1	VDDS18LDO	1.8	2.5	2.5	0	01	2.5	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle
VDDA18LDO BASELINE1	VDDA18LDO	1.8	2.5	2.5	0	66	2.5	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle

Table 2-6. AM26x Transient Current Model – Resulting PDN Requirements

Transient Case	Net Name	Fmax (MHz)	Current Step (mA)	PCB DC Tolerance (mV)	PCB AC Tolerance (mV)	PCB Target DC IR (mΩ)	PCB Target AC Zmax (mΩ)	Comment
VDD BASELINE1	VDD	200	2402	30	30	12	12	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle.
VDD XTAL_PLL1	VDD	50	833	30	30	36	36	XTAL to PLL turn-on transient.
VDD WFI1	VDD	40	367	30	30	82	82	4x RF5 WFI event transient.
VDDS33 BASELINE1	VDDS33	200	84	83	83	982	982	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle.
VDDA33 BASELINE1	VDDA33	200	34	83	83	2419	2419	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle.
VDDS18LDO BASELINE1	VDDS18LDO	200	1	45	45	45	45	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle.
VDDA18LDO BASELINE1	VDDA18LDO	200	66	45	45	682	682	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle.

2.5.1 Simulations

The following simulated PDN z-parameter performance was extracted from the AM263x LaunchPad and controlCard layouts using Ansys SI wave. Wide-band s-parameter models of each of the selected capacitors were taken from the manufacturer. Simulations capture only 25°C (room temperature) PCB and capacitor model performance.

2.5.1.1 Core Digital Power 1.2V

Z11 simulations were performed on the 1.2V core digital power net of the AM263x LaunchPad EVM to verify transient power margin. The simulation domain included the:

- AM263x BGA (UI) 1.2V digital and GND return fan-out
- Internal PCB 1.2V and GND return planes
- Decoupling placed on the 1.2V power net,
- U29 buck regulator output LC filter up to switch node

These simulations were done iteratively with multiple capacitor BOM changes made between each iteration. Each iteration was characterized primarily by the maximum and minimum frequency bandwidth below Ztarget (see above sections) and the BOM selection changed to maximize bandwidth and maximum Ztarget margin. Only the initial and final chosen BOM iterations are shown in Figure 2-12 and Figure 2-13.

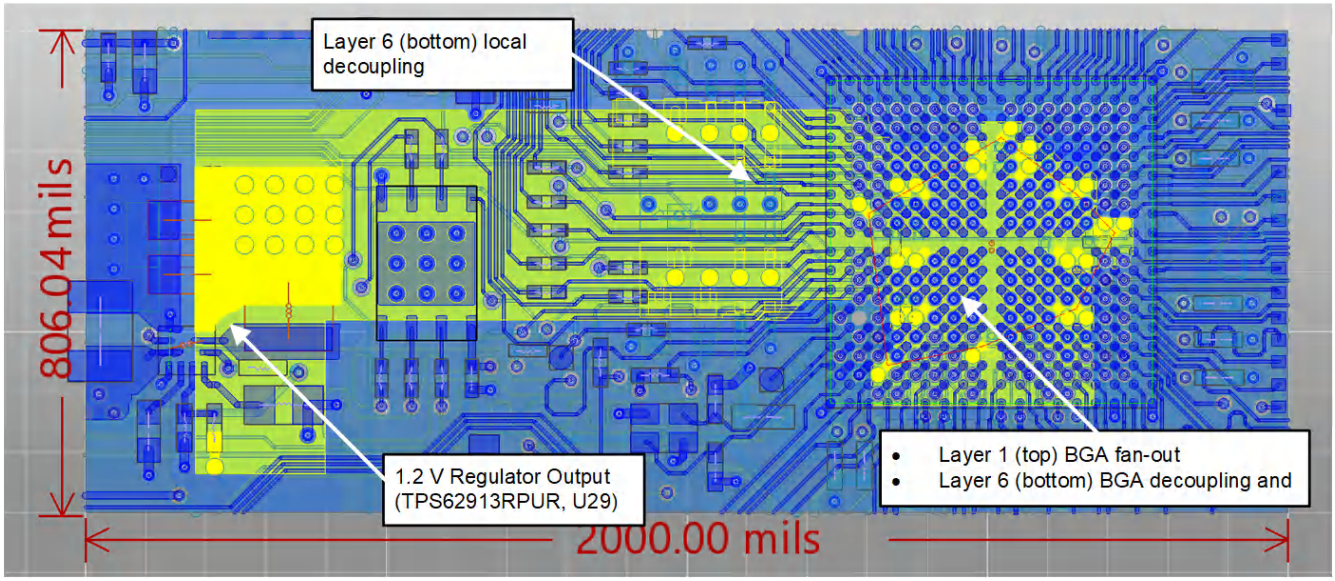


Figure 2-12. AM263x LaunchPad PDN Simulations – 1.2V Core Power Simulation Domain

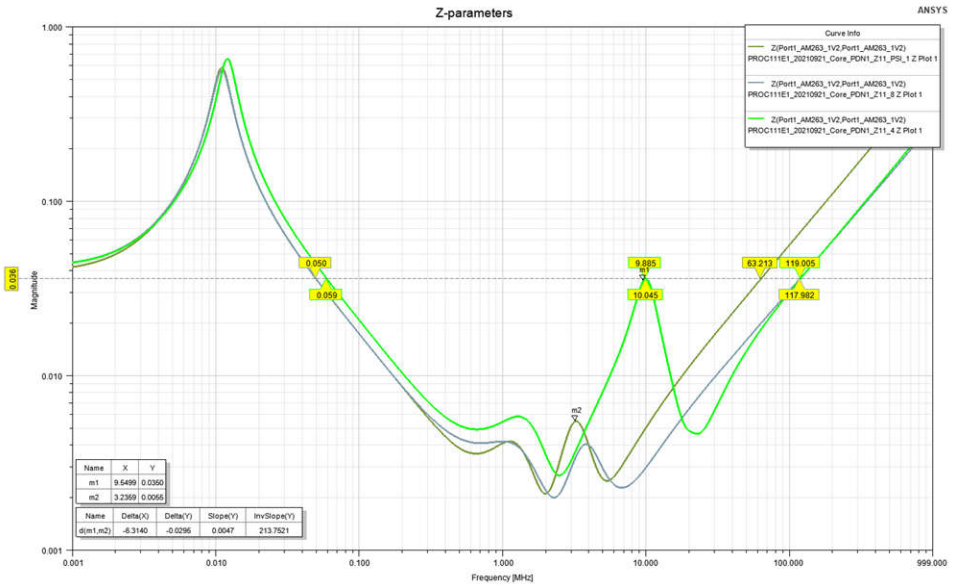


Figure 2-13. AM263x LaunchPad PDN Simulations – 1.2V Core Power Simulated Z11

- AM263x LaunchPad PDN Simulations – 1.2V Core Power Simulated Z11
  - This resulted in the marker (m2) point of 5.5mΩ
  - Z_{target} requirement of 36mΩ maintained from 50KHz to 63MHz
  - Major difference in BOM was replacing all 0.1µF BGA and local decoupling capacitors with 1.0µF capacitors - this entirely removed the 10MHz resonant point in the PDN impedance spectrum

2.5.1.2 Digital and Analog I/O Power 3.3V

Z11 simulations were performed on the 3.3V digital and analog power net of the controlCard EVM to verify transient power margin. The simulation domain included the:

- AM263x BGA (U1) 3.3V power and ground return BGA and fan-out
- Internal power and ground return routing layers
- Regulator output

Initial runs of these simulations showed that no BOM changes were needed to meet the maximum and minimum frequency bandwidth below Ztarget (see above sections). Only the initial simulation with the final chosen BOM iterations are shown below.

The simulations were divided between the VDDS33 digital 3.3V plane and decoupling network and the VDDA33 analog 3.3V traces and decoupling local to the design. The difference between these simulations is the FL18 ferrite bead element that was used to separate these two decoupling performance simulations.

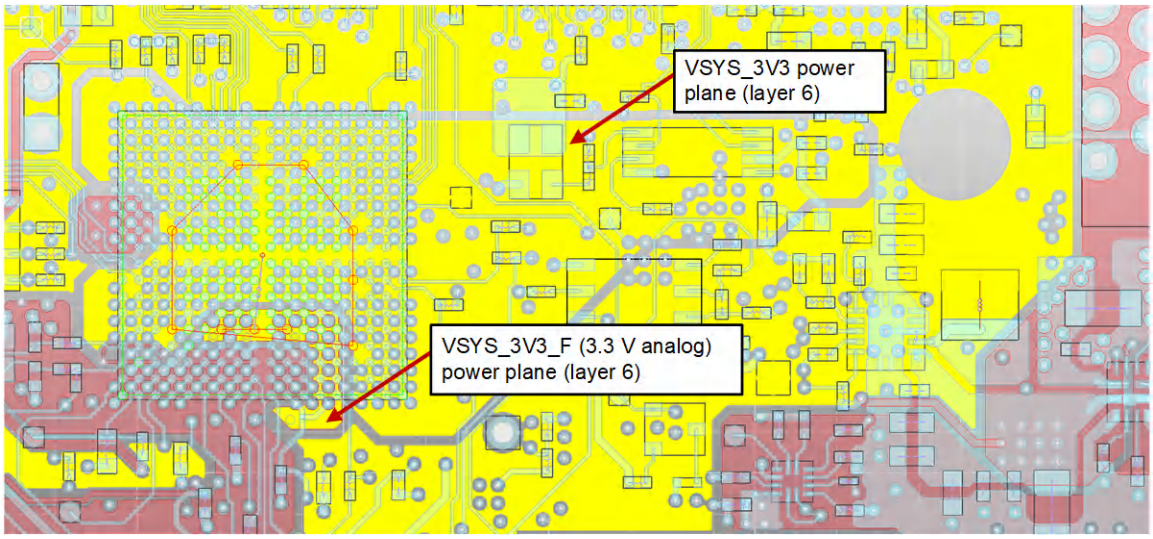


Figure 2-14. AM263x LaunchPad PDN Simulations – 3.3V Digital and Analog I/O Power Simulation Domain (A)

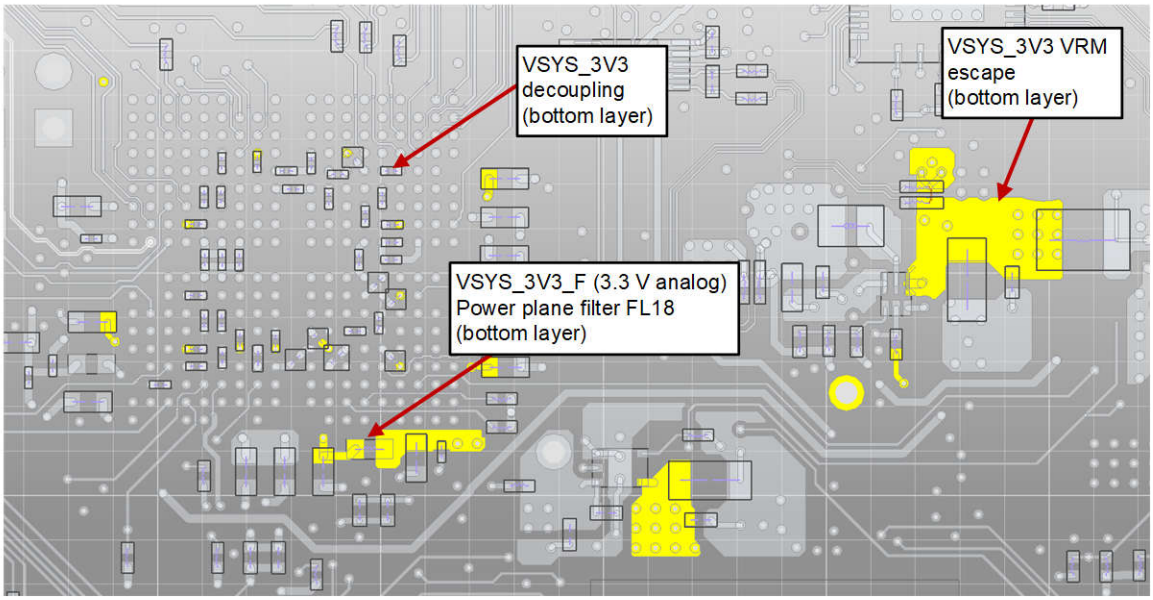


Figure 2-15. AM263x LaunchPad PDN Simulations – 3.3V Digital and Analog I/O Power Simulation Domain (layer 8, bottom)

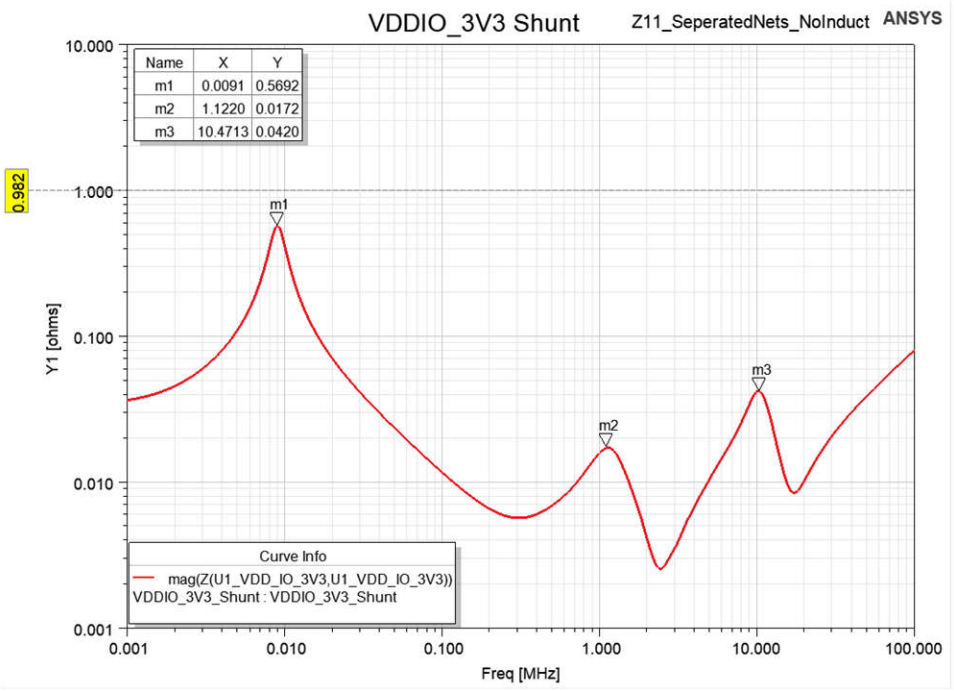


Figure 2-16. AM263x LaunchPad PDN Simulations – 3.3V Digital I/O Power Simulated Z11

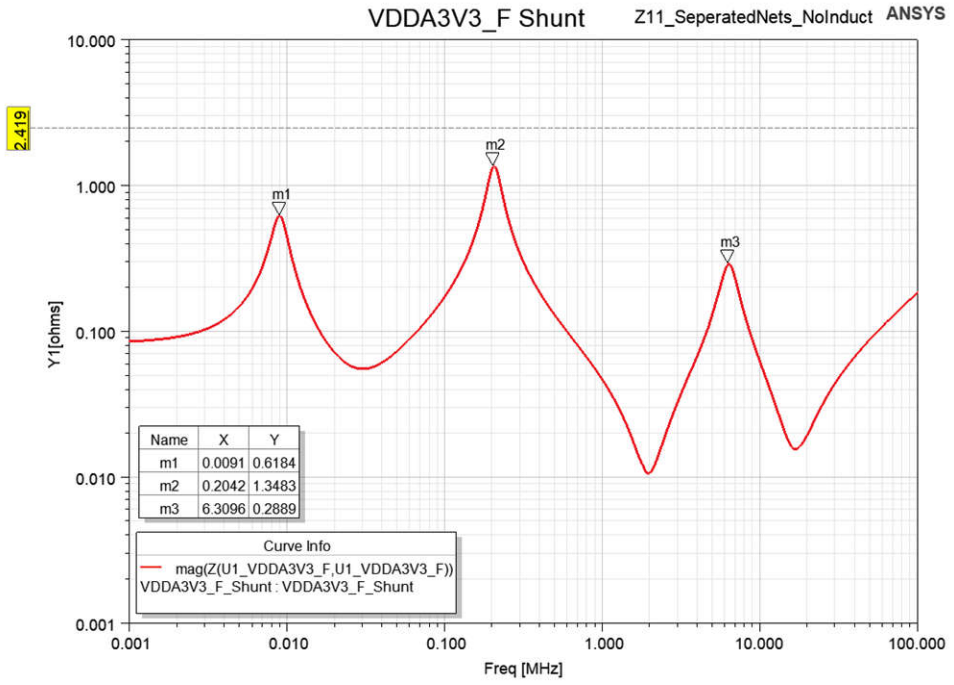


Figure 2-17. AM263x LaunchPad PDN Simulations – 3.3V Analog I/O Power Simulated Z11

2.6 eFuse Power

The AM26x MCUs have a one-time programmable eFuse memory that can be utilized for storing customer cryptographic keys and other information specific to individual devices. These e-Fuse memory locations can only be programmed when the target device eFuse power pin (VPP), is powered by a 1.7V nominal output voltage, 100mA peak current supply. This 1.7V VPP power supply can be on-board, off-board or sourced from the AM26x devices' internal 1.8V LDO, re-programmed to the required 1.7V/100mA supply.

The eFuse programming typically follows one or both of the following scenarios:

- **Factory programming** – eFuse memory programmed during post assembly test of the AM26x system.
- **Field programming** – eFuse memory is programmed after the device has left the factory and is installed in the end-equipment.

If the factory programming scenario is required for a product, then implementing the VPP power supply off-board reduces the number of components required to be placed on the PCB assembly. The VPP supply is only be used during this programming sequence, so keeping this hardware on the board is not an efficient use of PCB floor plan area, BOM cost, or test time.

However, if the eFuse memory must be programmed outside the factory environment, the VPP power must either be supplied from an onboard component or from an attached accessory board that can supply this power as needed.

External VPP Supply

The specific placement of the VPP supply and implementation depend on how the eFuse memory is utilized by the designer. The implementation must follow the diagram shown in Figure 2-18

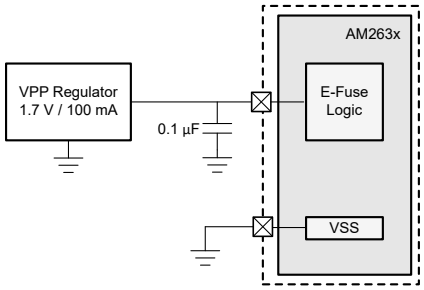


Figure 2-18. AM26x eFuse VPP - External Power Supply Implementation

On the AM263x controlCARD design, the VPP supply is populated on the board to enable convenient eFuse programming for customers experimenting with this process. On the controlCARD, the TLV75801PDRVR LDO (U66) is used to drop down the 3.3V system I/O voltage to the VPP 1.7V.

On-Chip VPP Supply

The AM263Px and AM261x MCUs have the option to source VPP internally using the 1.8V Analog LDO (ANALDO). The ANALDO must be overwritten to provide 1.7V during eFuse programming, then reverted back to normal operation.

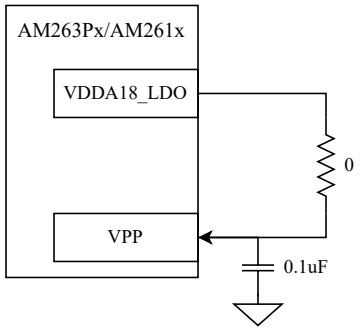


Figure 2-19. AM263Px/AM261x eFuse VPP - Internal Analog LDO Implementation

For the full VPP electrical requirements and eFuse programming sequence, see the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the device-specific AM26x Technical Reference Manual.

3 Clocking

3.1 Crystal and Oscillator Input Options

The AM26x XTAL_XI and XTAL_XO clock input can be sourced from either an attached crystal or a single-ended oscillator output.

Crystal Clocking Mode

The attached crystal needs to be a fundamental mode crystal operating at 25MHz. The crystal requires shunt capacitors, with capacitance ranging from 12pF-24pF. Figure 3-1 shows an example of the AM26x being clocked in crystal mode.

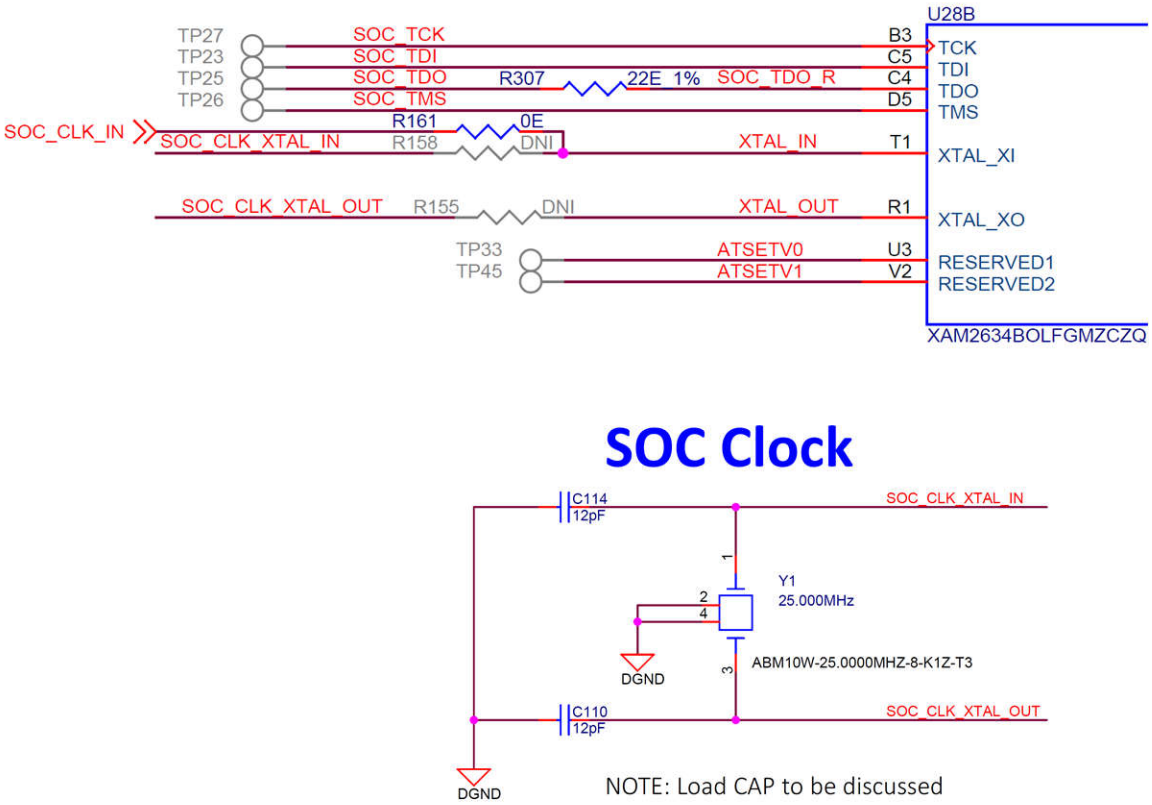


Figure 3-1. Excerpt From AM263x Control Card Schematics (for full crystal and oscillator input requirements)

Oscillator Clocking Mode

If operating from a single-ended oscillator output, then the XTAL_XI pin needs to be connected to the oscillator and the XTAL_XO pin must be left floating, unconnected on the PCB. In oscillator input mode, the XTAL_XI pin can be tied to either a 1.8V square wave or sine wave oscillator. For full oscillator input requirements, see the device specific AM26x data sheet. Figure 3-2 shows an example of an AM26x clock tree using a clock distributor and buffer circuit.

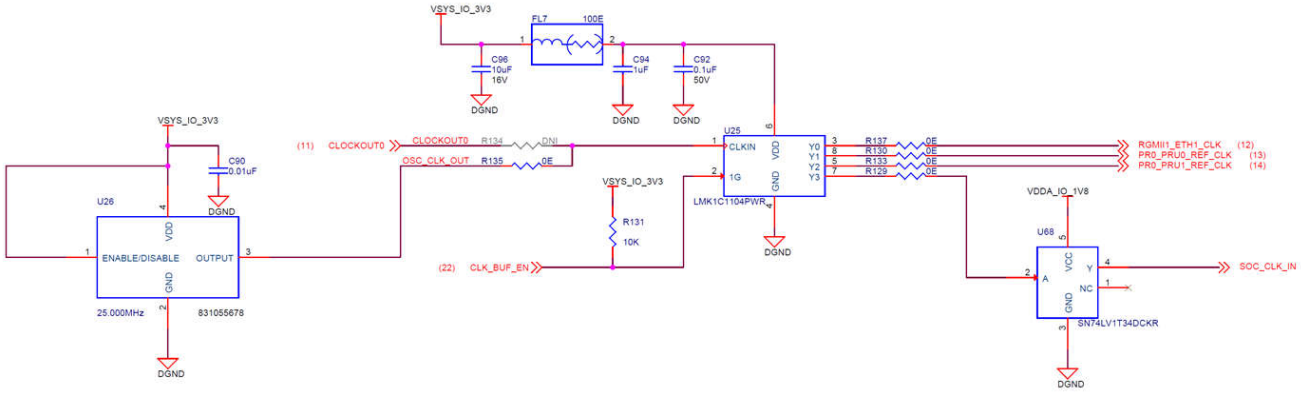


Figure 3-2. Excerpt From AM263x controlCard Schematics - Oscillator Clock Source and Clock Distributor

In the case of the AM263x Control Card, an onboard ABM10W-25.0000MHZ-8-K1Z-T3 25MHz crystal provides crystal mode clocking. Alternatively, an LMK1C1104PWR clock distributor circuit and SN74LV1T34 buffer provide the 1.8V square-wave clock to the XTAL_XI pin. The LMK1C1104PWR is also used to provide a clock source to the onboard Ethernet PHY.

3.2 Output Clock Generation

The AM26x devices include two output clock sources, CLKOUT0 and CLKOUT1. These are intended to be used to clock attached peripheral IC such as Industrial/Automotive Ethernet PHYs. This can save on BOM cost and additional IC placement and routing space. The AM263x and AM263Px Launchpads include an optional path for the CLKOUT0 (pin M2) signal to clock the onboard DP83869HMRGZT Ethernet PHY. The AM261x LaunchPad includes an optional path for the CLKOUT1 pin signal to clock an Ethernet PHY via the Ethernet Add-on Board Connector. Unused CLKOUT pins can be left unconnected on the PCB.

The AM26x devices include one external reference clock source, EXT_REFCLK0. This pin is intended to be used as an external reference clock input to the device clock generator PLL circuits. Unused EXT_REFCLK pins can be left unconnected on the PCB. For more information on EXT_REFCLK0, see the device-specific Technical Reference Manual.

Figure 3-3. Excerpt From AM263x LaunchPad Layout – CLKOUT0 and EXT_REFCLK0 Output

3.3 Crystal Selection and Shunt Capacitance

In crystal operating mode, the AM26x can be interfaced to a wide variety of compatible crystals. Based on PCB parasitic capacitance and crystal selected, the additional load capacitance needs to be modified to achieve the best start-up stability and frequency accuracy.

For full crystal loading tolerances, see the device-specific AM26x data sheet.

3.4 Crystal Placement and Routing

Crystal oscillator input needs to be placed as close as possible to the AM26x XTAL_XI/XO with minimal length traces between crystal and MCU pads. A ground ring shorted to the local VSS plane needs to be placed adjacent and between the XTAL_XI and XTAL_XO traces to help prevent coupling from adjacent signals onto the clock higher impedance crystal input paths.

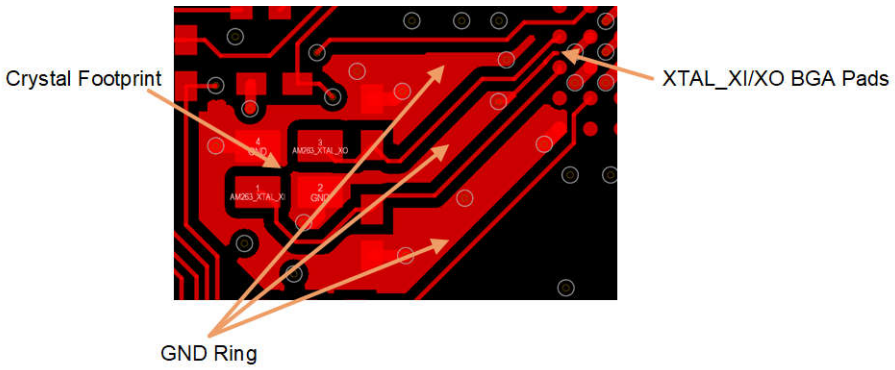


Figure 3-4. Excerpt From AM263x Launchpad Layout - Crystal Layout and Ground Ring Structure

4 Resets

The AM26x MCUs have two hardware reset sources:

- PORz: Power on reset (logic low enable) pin
  - Must be driven from the power-good circuits of the associated VDD 1.2V core and VDDS33 3.3V I/O regulators or PMIC reset signal
  - For a valid reset the PORz signal must transition from logic low to logic high only after the VDD 1.2V core and VDDS33 3.3V I/O regulators are stable at the nominal values. For power-on-reset timing requirements, see the device-specific data sheet.
- WARMRSTn: Warm reset (logic low enable) input and reset status output pin
  - At power-on, the default configuration sets this pin as open-drain output, which outputs the reset status of the device.
  - When the device enters reset, this signal is driven logic low.
  - When the device is fully out of reset, this signal is driven logic high.

PORz

The PORz is intended to be kept at logic low at initial startup of the system. Once each regulator sourcing the AM26x power pins has been verified to be operating at nominal output voltage, then the PORz signal can be brought up to logic high. This action starts the MCU boot ROM execution, beginning with sampling of the SOP pins.

PORz - Discrete Power Tree Implementation

The AM263x LaunchPad implementation utilizes a single SN74LVC1G11 AND gate which takes the open-drain output power-good signals from the onboard DC-DC regulators and an optional push-button reset switch as inputs to the AND gate. A weak pull-down resistor is recommended on the PORz signal to keep the signal at logic low before system startup. PORz must be forced low if either VDD 1.2V or VDDS33 3.3V rail power goes below the nominal operating range.

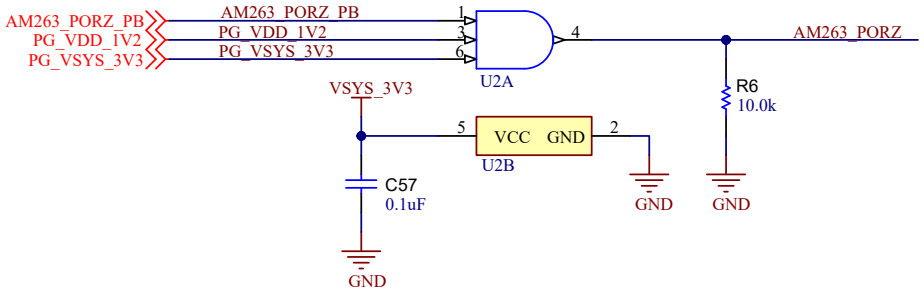


Figure 4-1. Excerpt From AM263x Launchpad Schematic – PORz Generation

PORz - PMIC Based Power Solution Implementation

For AM26x systems that utilize a PMIC-based power design, the PORz logic is slightly more complex. On the AM263Px controlCARD, the open-drain output power-good signal from the 1.2V regulator, the optional push-button reset switch, and the nRST signal from the PMIC are inputs to a SN74LVC1G11 AND gate. The output of the 3-input AND gate is connected to the input of a 2-input SN74LVC1G08 AND gate, with the other input being the output of a voltage divider of the system input voltage (5V) divided down to 0.88V. The output of the SN74LVC1G08 is connected to the AM26x PORz. The SN74LVC1G08 low-level input voltage is 0.8V, so the AND gate outputs a logic 0 if the input voltage drops below 0.8V, thus triggering a reset.

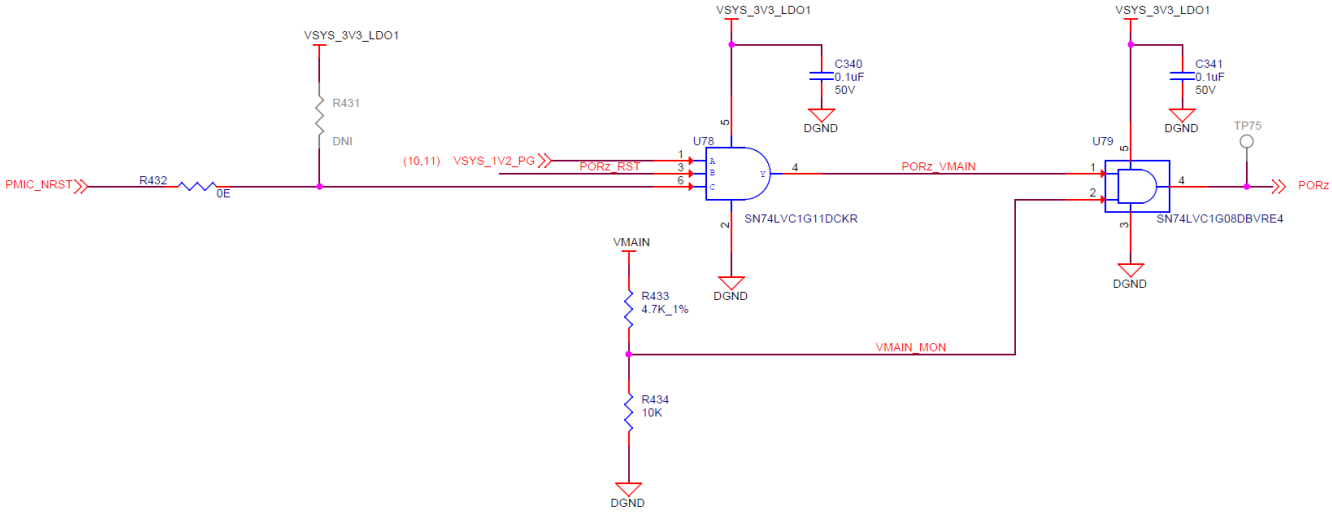


Figure 4-2. Excerpt from AM263Px controlCARD Schematic- PORz Generation

For a full description of the power-on and power-off reset sequencing requirements, see the device specific AM26x data sheet.

WARMRSTn

The WARMRSTn pin is a multi-purpose software reset input and hardware reset status pin. In the power-on-default configuration, this pin is configured as an open-drain output and requires an external pull-up resistor to VDDS33 3.3V I/O voltage rail. In this mode, WARMRSTn can be used as an MCU reset indicator and can be used to drive reset input for attached peripheral IC such as Ethernet PHY and memories.

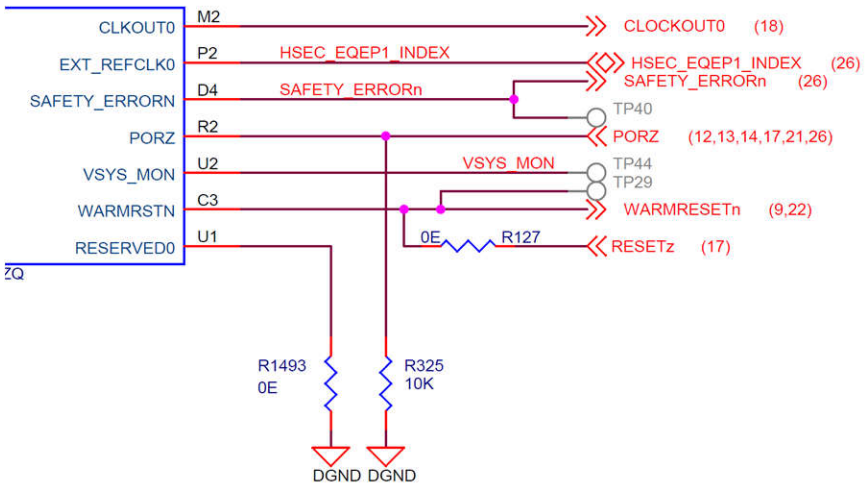


Figure 4-3. Excerpt From AM263x Control Card Schematic – PORz and WARMRSTn Pinout

WARMRSTn can also be configured as a software reset. Additional software reset sources are available on the AM26x devices. For more information on reset functionality, see the *Reset* chapter in the device specific AM26x Technical Reference Manual.

Because of the default open-drain configuration of this pin, if both the reset status output mode and the software reset input mode is needed in a design, open-drain buffers are recommended to drive the optional reset input status. In the case of the AM263x Control Card, a SN74LVC1G07 open-drain buffer is used to optionally drive the push-button WARMRSTn without conflicting with the reset status output which is used to reset the Ethernet PHY onboard during initial board power-on.

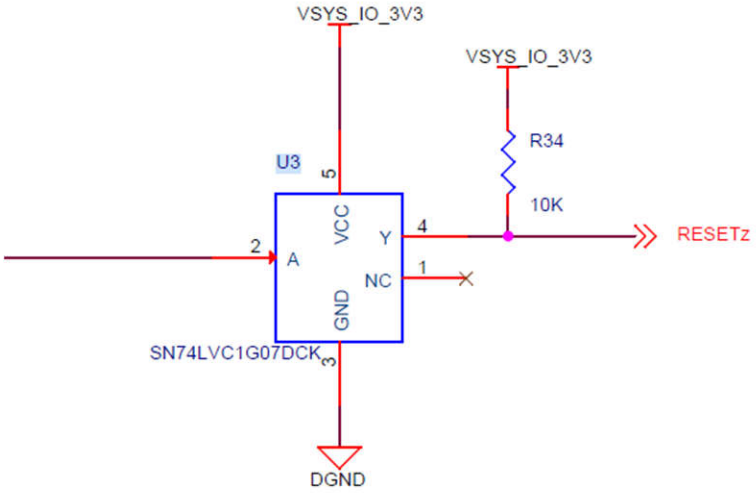


Figure 4-4. Excerpt From AM263x Control Card Schematic – WARMRSTn Push-Button Open-Drain Driver

5 Bootstrapping

The sense-on-power (SOP) signals are used to latch in the selected boot mode into the AM26x device. During the PORz rising edge (low to high logic transition) the SOP[3:0] signals are sampled. The resulting 4 bits are used to branch the boot ROM into the selected boot mode. Not all combinations are supported. For a full description of the SOP pin states and supported boot modes, see the device-specific AM26x Technical Reference Manual.

5.1 SOP Signal Implementation

Each SOP bootmode selection signal is multiplexed with a subset of OSPI/QSPI and SPI peripheral functional mode signals. For all signal descriptions, see the *Signal Description* tables in the device-specific AM26x Data Sheet.Data Sheet. The SOP signal descriptions are excerpted in Figure 5-1. The SoC pin number differs depending on device package type.

Table 5-1. SOP and Functional Mode Signal Mapping

SOP Mode Signal	Primary Pinmux Signal	AM26x ZCZ Pin	AM261x ZFG Pin	AM261x ZNC Pin	AM261x ZEJ Pin
SOP[0]	OSPI0/QSPI0_D0	N1	R2	N2	M2
SOP[1]	OSPI0/QSPI_D1	N4	R1	N1	N1
SOP[2]	SPI0_CLK	A11	A13	A12	A12
SOP[3]	SPI0_D0	C10	B12	B12	A10

Because of this SOP/functional-mode multiplexing additional care must be taken in schematic and layout to make sure that the SOP mode selection resistors, jumpers or switch paths are routed in such a way that the SOP mode branches do not present inductive PCB trace stubs to the functional mode signal paths. Failing to take care of this can result in non-functional OSPI/QSPI or SPI.

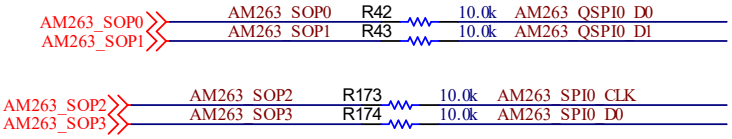


Figure 5-1. Excerpt From AM263x Launchpad Schematic – SOP[3:0] Functional and SOP Paths

In the AM26x EVM designs, this SOP mode isolation is accomplished by including a 10KΩ resistor in the SOP signal path. The resistor is placed such that one pad is as close to the AM263x BGA pad and in-line with the functional mode path. This creates a layout where the additional stub length necessary to breakout the SOP path results in minimal impact to the functional mode operation of the signals, as shown in Figure 5-2 and Figure 5-3.

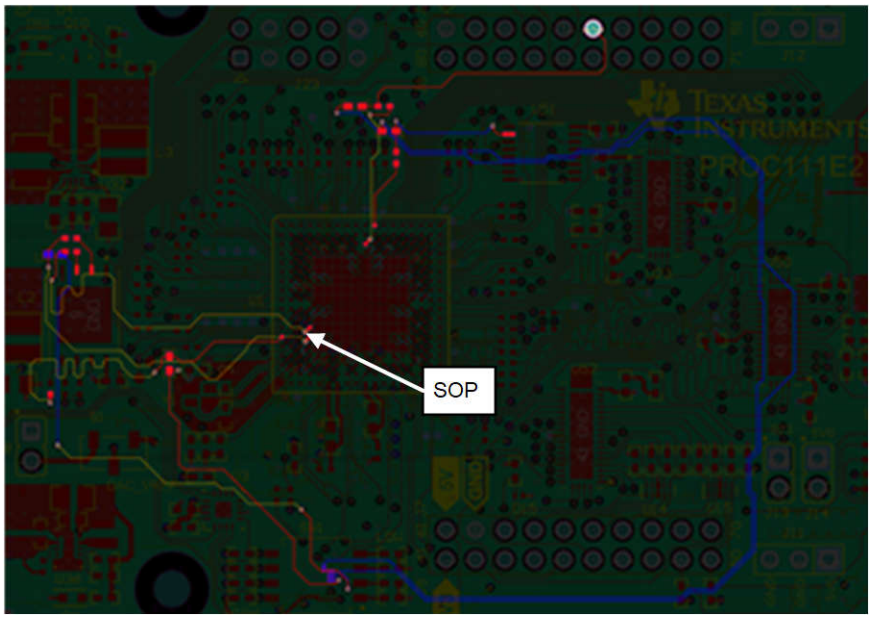


Figure 5-2. Excerpt From AM263x Launchpad Layout – All SOP[3:0] Functional and SOP Paths

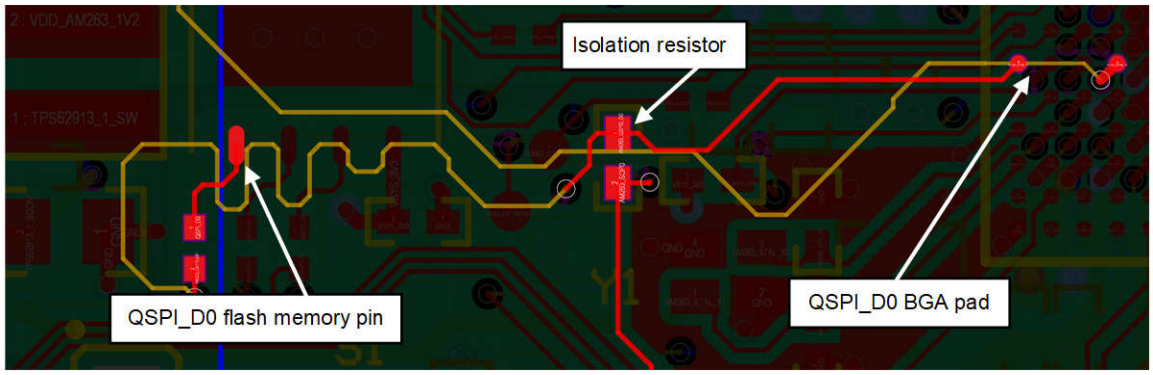


Figure 5-3. Excerpt From AM263x Launchpad Layout – Highlighting SOP0/QSPI_D0 Path and SOP Isolation Resistor

6 OSPI/QSPI Memory Implementation

The OSPI Flash memory interface is the primary bootloader memory location for the AM263Px and AM261x MCUs, and the QSPI Flash memory interface is the primary bootloader memory location for the AM263x MCU. For a full description of boot ROM execution, including OSPI and QSPI boot information, see the device specific AM26x Technical Reference Manual. The excerpt from Figure 6-1 shows the implementation of the QSPI NOR flash interface from the LP-AM263 design. The excerpt from Figure 6-2 shows the implementation of the OSPI NOR flash interface on the TMDSCNCD263P AM263Px controlCard design.

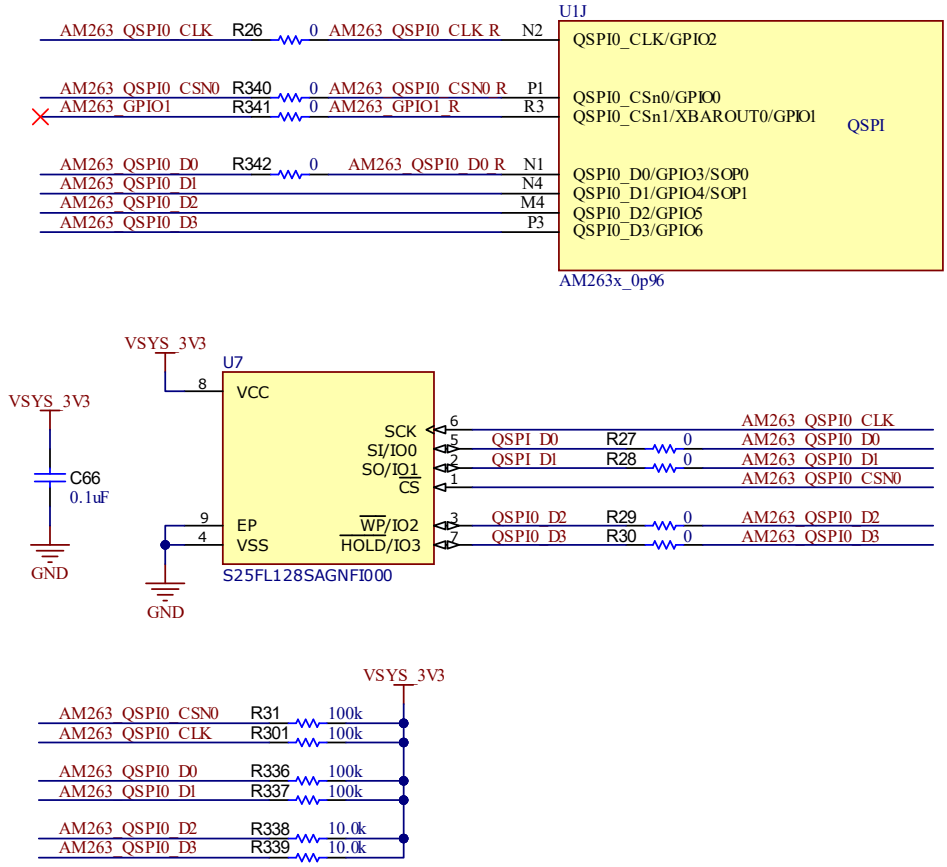


Figure 6-1. Example AM263x QSPI Controller and NOR Flash Memory Schematic

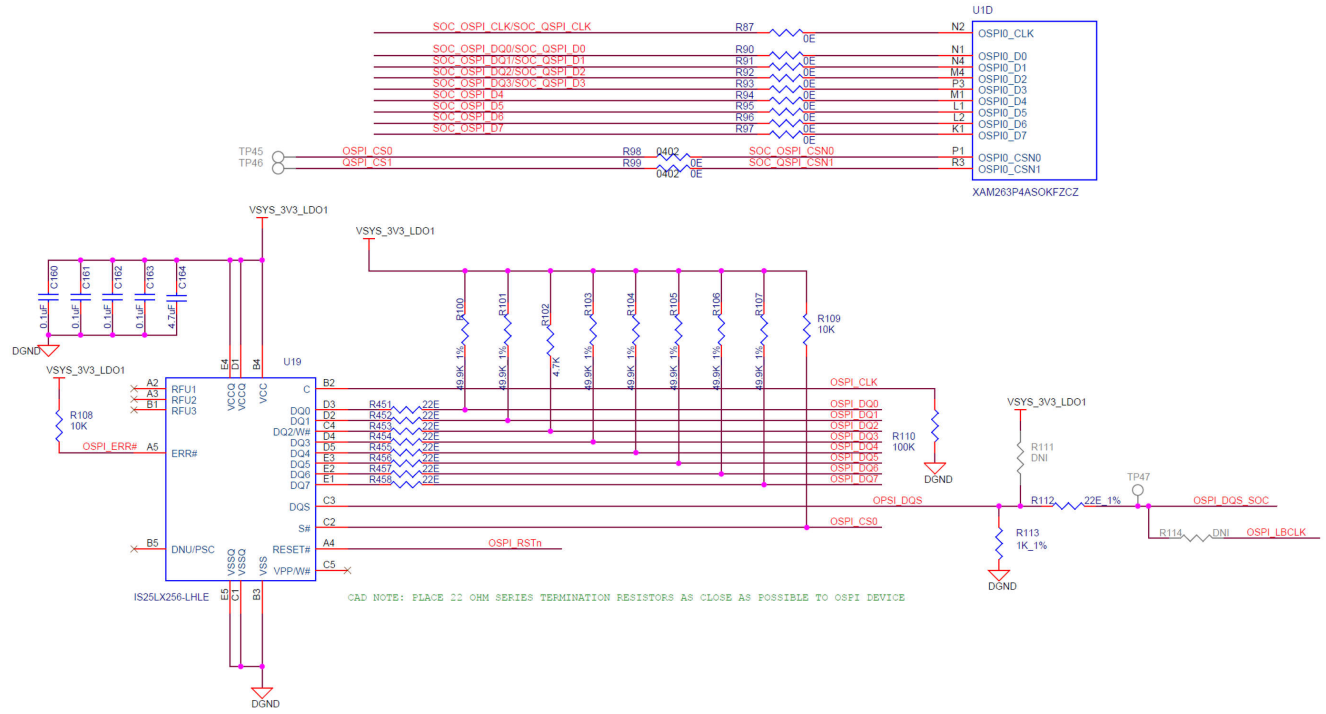


Figure 6-2. Example AM263Px OSPI Controller and NOR Flash Memory Schematic

To control OSPI/QSPI bus transition overshoot and undershoot, include the following series termination resistors close to the OSPI/QSPI memory pins and the AM26x BGA.

- Series termination at the AM26x MCU, transmit side of QSPI0_CLK, and QSPI0_CS[1:0]
- Series termination at OSPI/QSPI memory side of OSPI0_D[7:0] or QSPI0_D[3:0]

For recommended series termination resistor placement, see Figure 6-4.

The OSPI_D[7:1] and QSPI_D[3:1] bits of the interface are used as a read interface and series termination resistor are used at the memory side of the bus. OSPI/QSPI_D0 can benefit from termination resistors at both the MCU side and the OSPI/QSPI memory side of the bus when used as both a single-mode write and part of single-mode and octal/quad-mode reads. However, placement of additional termination on both sides of this bus can be difficult to achieve from a PCB floor-planning perspective. The termination scheme presented here must be used as a minimum recommendation. For more details on termination requirements, see Section 10.

Pull resistors are also necessary on the OSPI/QSPI clock, chip-select and data lines. Different QSPI memories can have different pull-up/down requirements depending on the specific memory and application requirements. These pull resistor recommendations are based on the implementation of the S25FL128x memory used on the LP-AM263 design. To confirm all pin memory configuration details, see the device-specific QSPI Flash memory data sheet. Include the following pull resistors on the QSPI signals:

- QSPI_CLK, QSPI_CS[1:0], and QSPI_D[1:0] - include 100kΩ pull-up to VDDS33 IO supply.
- QSPI_D[2] - 10kΩ pull-up to VDDS33 IO supply. This disables write-protect mode on the S25FL128 flash memories.
- QSPI_D[3] - 10kΩ pull-up to VDDS33 IO supply. This disables hold mode on the S25FL128 flash memories.

Different OSPI memories have different pull-up/down requirements depending on the specific memory and application requirements. These pull resistor recommendations are based on the implementation of the IS25LX256x memory used on the TMDSCNCD263P design. To confirm all pin memory configuration details, see the device specific OSPI Flash memory data sheet. Include the following pull resistors on the OSPI signals:

- OSPI_CLK - include 100kΩ pull-down to GND
- OSPI_CS - 10kΩ pull-up to VDDS33 IO supply
- OSPI_DQS - 1kΩ pull-down to GND

- OSPI_D[2] - 4.7kΩ pull-up to VDDS33 IO supply. This disables write-protect mode on the IS25LX256 flash memories
- OSPI_D[1:0] and OSPI_D[7:3] - 49.9kΩ pull-up to VDDS33 IO supply

Stronger pull-up resistors are used to disable write-protect and hold modes by default. Weaker pull-up resistors are used to keep the lines at valid logic levels between transactions. Pull resistors must be placed close to the OSPI/QSPI memory pins to prevent any additional routing stubs from being formed.

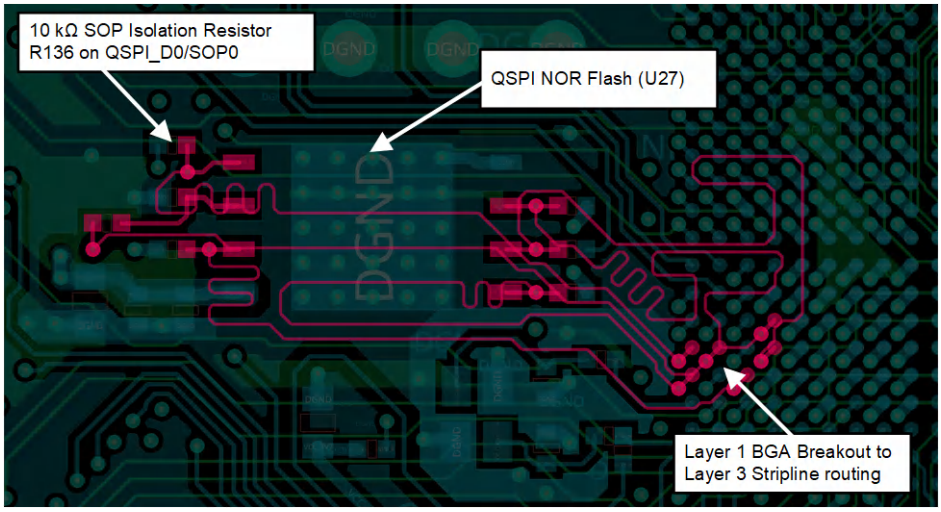


Figure 6-3. Excerpt From LP-AM263 Launchpad Layout – Highlighting SOP0/QSPI_D0 Path and SOP Isolation Resistor

Additional routing guidelines for the QSPI memory interface are provided in Figure 6-4 and Table 6-1. These must be used as maximum routing delay and skew match limits. The QSPI memory must be placed close to the AM26x BGA footprint as possible. This allows for routing that maximizes the delay margins and skew margins and minimizes transmission-line effects.

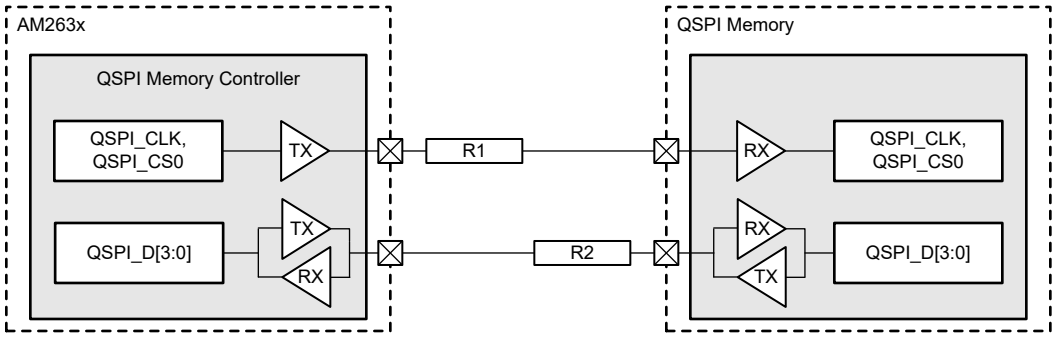


Figure 6-4. AM26x QSPI - Routing Rules Diagram

Additional routing guidelines for the OSPI memory interface are provided in Figure 6-5 and Table 6-2. These are used as maximum routing delay and skew match limits. The OSPI memory must be placed close to the AM263Px/AM261x BGA footprint as possible. This allows for routing that maximizes the delay margins and skew margins and minimizes transmission-line effects.

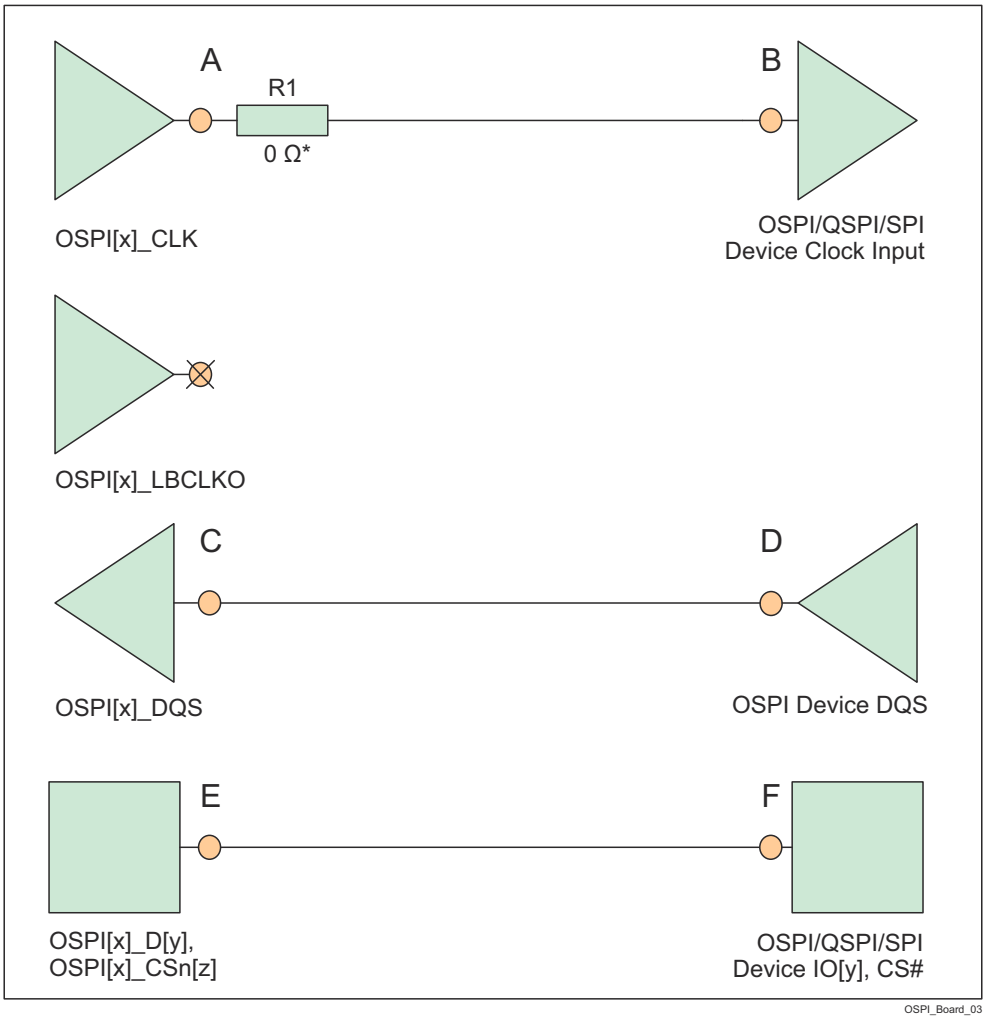


Figure 6-5. AM263Px. AM261x OSPI - Routing Rules Diagram

Table 6-1. AM26x QSPI – Recommended Routing Rules

Spec No.	Specification	Value	Unit
1	QSPI_CLK, QSPI_CS0, QSPI_D[3:0] maximum delay	450	ps
2	QSPI_CLK to QSPI_D[3:0] maximum skew	50	ps
3	Approximate maximum routing distances	3214	mils
4	Approximate maximum routing skew	357	mils
5	A series termination resistor (R1 in diagram above) must be placed close to the QSPI_CLK transmit pin of the AM263x/AM263Px/AM261x to control rise-time and reflections of the clock line.	Variable, 0 to 40	Ω
6	A series termination resistor (R2 in diagram above) must be placed close to the QSPI data pins of the attached memory to control rise-time and reflections of the data lines.	Variable, 0 to 40	Ω

Table 6-2. AM263Px, AM261x OSPI – Recommended Routing Rules

Spec No.	Specification	Value	Unit
1	OSPI_CLK, OSPI_CS0, OSPI_D[7:0] maximum delay (1)	450	ps
2	OSPI_CLK to OSPI_D[7:0] and OSPI_CSn maximum skew	60	ps
3	OSPI_CLK to OSPI_DQS maximum skew	30	ps
4	Approximate maximum routing distances (1)	3214	mils
5	OSPI_CLK to OSPI_D[7:0] and OSPI_CSn approximate maximum routing skew	429	mils
6	OSPI_CLK to OSPI_DQS approximate maximum routing skew	214	mils
7	A series termination resistor (R1 in diagram above) must be placed close to the OSPI_CLK transmit pin of the AM263Px to control rise-time and reflections of the clock line.	Variable, 0 to 40	Ω
8	Series termination resistor must be placed close to the OSPI data pins of the attached memory and the AM263Px device to control rise-time and reflections of the data lines.	Variable, 0 to 40	Ω

(1) This routing limit is applicable only in **Fixed Timing** modes in **Internal PHY Loopback, Internal Pad Loopback, or External Board Loopback** clock topologies. This does not apply when using DQS Clocking topology.

Note

Approximate routing distances are computed assuming a typical 140ps/inch propagation delay in 50Ω FR4 Microstrip or Stripline transmission lines. A 2D field solver or appropriate closed-form approximate impedance model must be used to find more exact propagation delay for your specific stackup and routing.

6.1 ROM OSPI/QSPI Boot Requirements

For more information concerning QSPI flash memory compatibility and boot requirements on the AM263x microcontroller, see the *AM263x QSPI Flash Selection Guide*.

For more information concerning OSPI flash memory compatibility and boot requirements on the AM263Px microcontroller, see the *AM263P OSPI, QSPI Flash Selection Guide*.

For more information concerning OSPI flash memory compatibility and boot requirements on the AM261x microcontroller, see the *AM261x OSPI, QSPI Flash Selection Guide*.

Note

The S25FL128SAGNFI000 Quad-SPI device from Infineon is utilized on the AM263x controlCard and LaunchPad EVMs.

Note

The IS25LX256-LHLE Octal-SPI device from ISSI is utilized on the AM263Px controlCard and LaunchPad EVMs and the AM261x controlSOM and LaunchPad EVMs.

Note

The MX25UW6445GXDQ00 Octal-SPI device from Macronix is utilized on the AM261x LaunchPad EVM.

7 JTAG Emulators and Trace

The AM26x MCUs support multiple different classes of JTAG emulators with or without additional ARM Trace capture capabilities.

For out of box convenience, the LP-AM263, LP-AM263P, LP-AM261, TMDSCNCD263, and TMDSCNCD263P EVM designs implement an onboard XDS110 emulator with JTAG and auxiliary UART-USB bridge implemented with a TI TM4C MCU and high-voltage isolation. However, for actual custom systems, a simpler JTAG or Trace debug header must be implemented. This allows for external JTAG and Trace pods to be attached to the system as needed during development. The header can then be removed entirely or depopulated for full production of the system to save cost.

One popular JTAG and Trace implementation is the MIPI industry standard MIPI-60 shown in Figure 7-1. This is based on the Samtec QSH-030-01-L-D-A. The AM263x controlCARD Docking Station (TMDSHSECDOCK-AM263) and the AM261x controlSOM EVM (AM261-SOM-EVM) feature a MIPI-60 with the full JTAG and 16-bit trace interface of the microcontroller broken out to the header. This implementation is compatible with TI XDS560v2 JTAG or trace pods and other third-party JTAG/Trace pods. Additional TI JTAG debugger connections can be found in the JTAG Connectors and Pinout document.

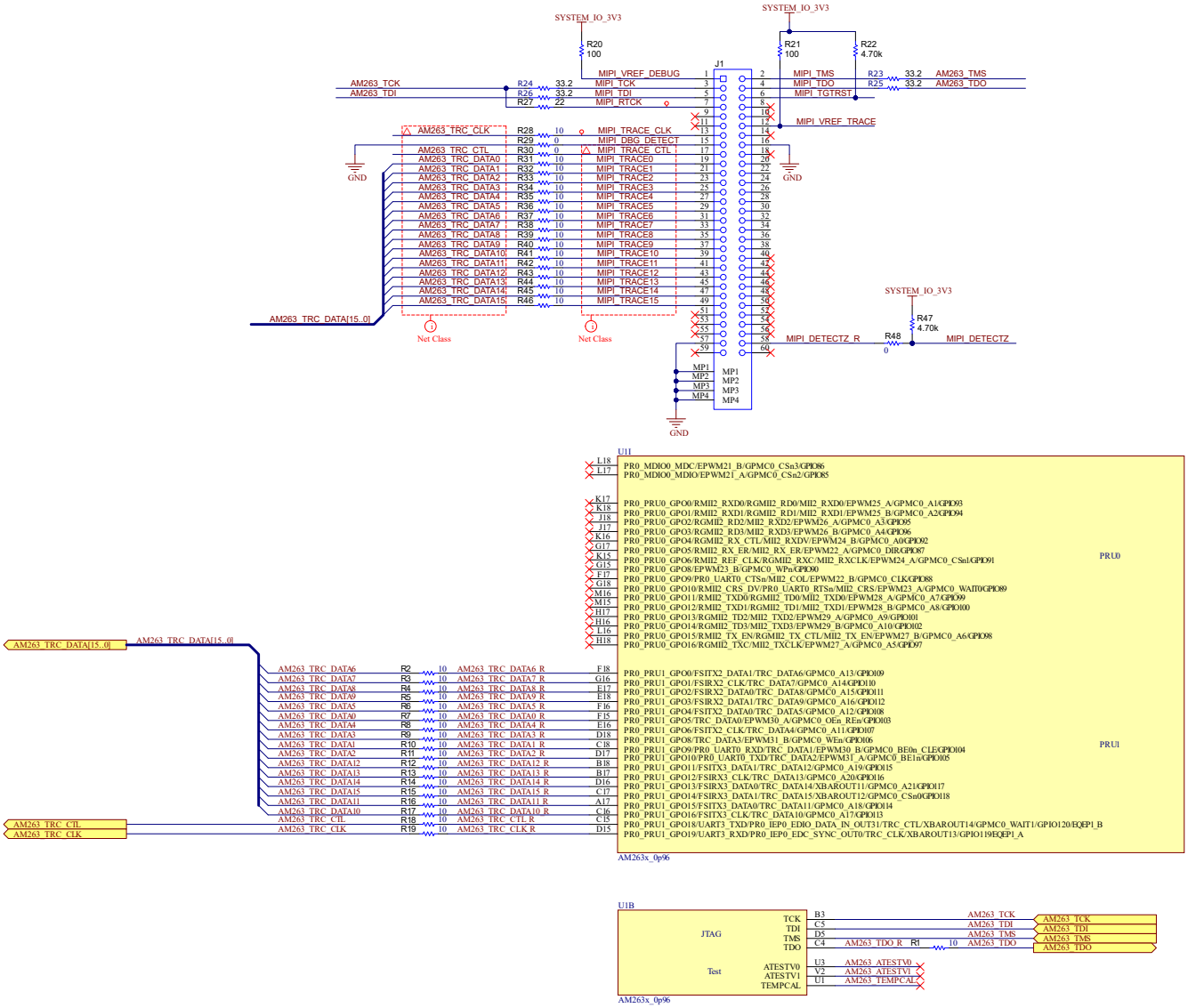


Figure 7-1. Example MIPI-60 JTAG and 16-bit Trace Implementation

8 USB

The AM261x family of microcontroller devices include an internal USB 2.0 PHY that supports USB Device Mode, USB Host Mode, and USB Dual-Role Mode operation. The internal USB 2.0 PHY is capable of high speed (HS, 480Mbps) and full speed (FS, 12Mbps) operation in both USB 2.0 Host and Device mode, and low speed (LS, 1.5Mbps) operation in host mode only.

The critical component of the internal USB PHY is the bidirectional differential data pins USB0DM (D-) and USB0DP (D+). The USB0_ID signal is an external net that interfaces with the USB receptacle, indicating which mode the USB2.0 PHY is operating in. On the AM261x EVMs, USB0_ID is set with a switch, allowing evaluation of the USB 2.0 PHY for both modes.

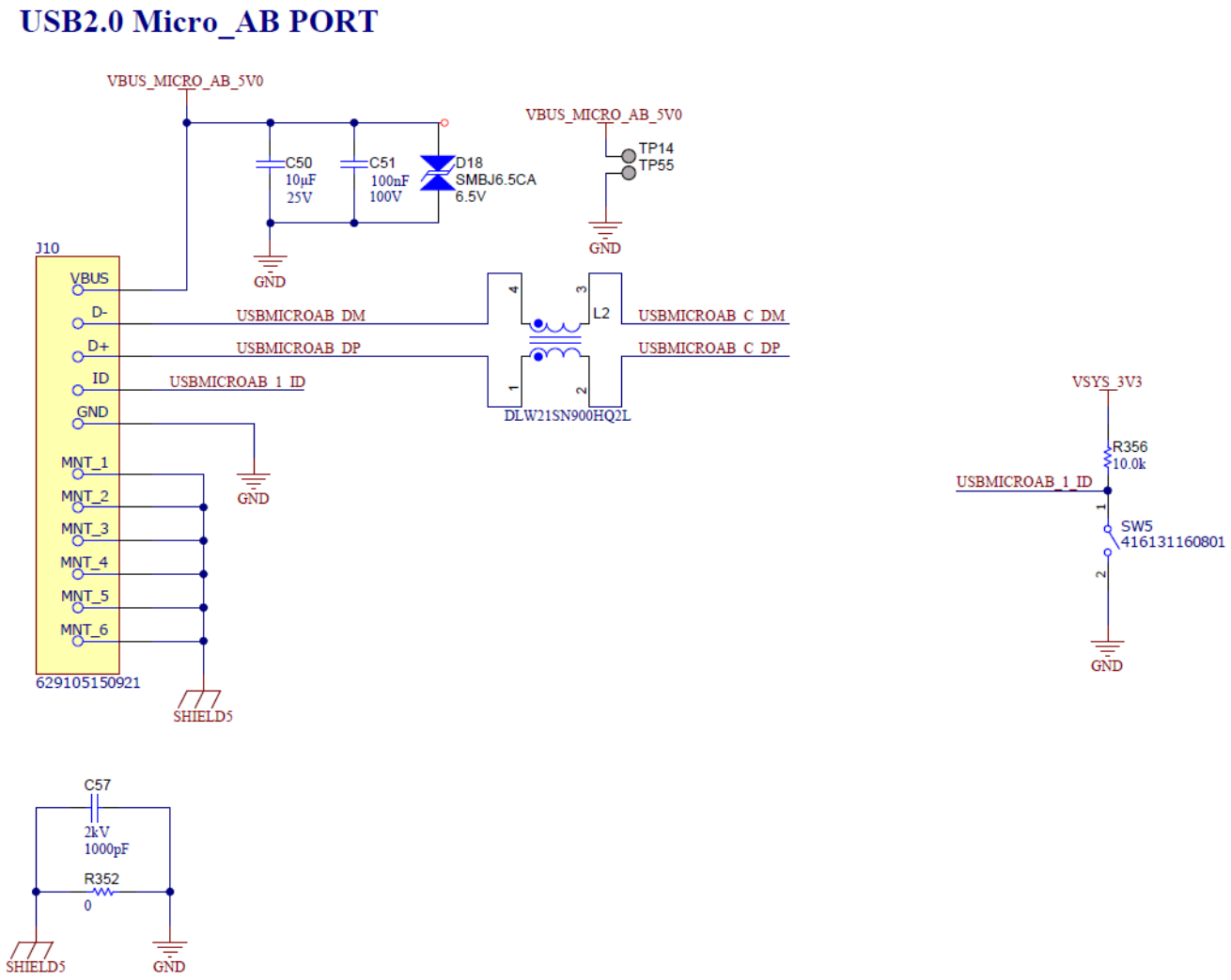


Figure 8-1. USB 2.0 Micro-AB Port Showing Critical Signals - LP-AM261

The following design rules and recommendations need to be followed when routing the USB differential pair for best results:

- Route the USB differential pair on the top layer with trace width and differential spacing tuned to the PCB stack-up for 90Ω differential impedance.
  - This can be difficult to implement a trace geometry that achieves both 90Ω differential impedance and 45Ω single-ended impedance. The most critical parameter to optimize in this design is the 90Ω differential impedance.
  - The trace width and spacing to maintain the required 90Ω differential trace impedance directly at the pins of the microcontroller and directly at the ESD suppressor and USB connector is not possible to achieve. Minimize these deviations as much as possible being sure to maintain symmetry.
- The individual traces within the differential pair needs to be length-matched to within 0.150in (3.81mm).
- Avoid stubs when adding components to D+ and D– signals. Devices such as ESD suppressors must be located directly on the signal traces.
- Maintain symmetry when routing differential pairs. Some PCB layout tools can assist with this kind of routing. Avoid vias if possible. If this is necessary to switch layers, then both signals in the pair pass through a via at the same distance on the trace.
- Total trace length for the USB differential pair is limited to 12 in (30.48 cm).
- Place ESD suppressors as close as possible to the USB connector to minimize any areas of impedance discontinuities. AM261x EVMs utilize the TPD4E02B04 ESD protection diode.

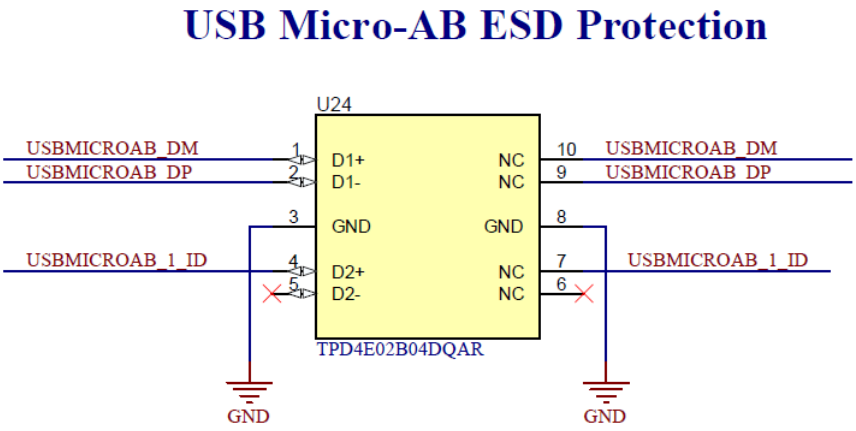


Figure 8-2. USB ESD Suppression - LP-AM261

- For best ESD and EMI performance, create a chassis ground to which the metal shield of the USB connector is connected.
- Depending on the system design, a common mode choke can be helpful to pass EMI testing. A DLW21SN common mode choke by Murata is one recommended device, and is utilized on the AM261x EVMs. If EMI is a concern for the design, then TI recommends that a footprint for the choke be included in the design placed close to the USB connector. Figure 8-3 shows the placement of a DLW21SN choke.
- Additional High Speed USB Platform Design Guidelines including more details on using a common mode choke can be found at USB.org.

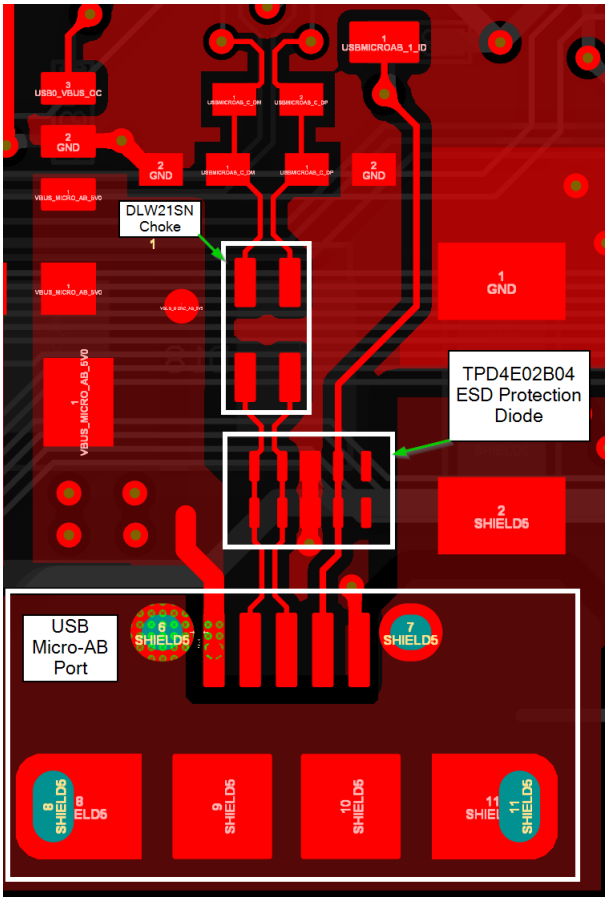


Figure 8-3. USB Routing Example

8.1 USB Device Mode

For using an AM261x device in USB2.0 Device Mode, the only signal used in addition to USB0_DM and USB0_DP is USB0_VBUS, which is located on pin 1 of USB 2.0 Micro-AB, USB2.0 Type-A, and USB 2.0 Type-B receptacles. In USB device mode, USB0_VBUS is used to detect when voltage has been applied to or removed from the USB connector, which triggers software to manage the internal USB PHY accordingly.

To indicate Device Mode operation, the USB0_ID pin on the USB receptacle needs to be left floating or pulled up to a valid logic level using a 10kΩ resistor.

8.2 USB Host Mode

For AM261x devices that are used in a host-only configuration, the USB0_DRVVBUS signal is required. This USB 2.0 PHY signal connects to a power switch, such as the TPS2051B that is implemented in the AM261x LaunchPad and AM261x controlSOM EVM designs. The power switch controls power to the host's USB connector. Refer to the AM261x data sheet to determine which IO pins the USB0_DRVVBUS functions are available on.

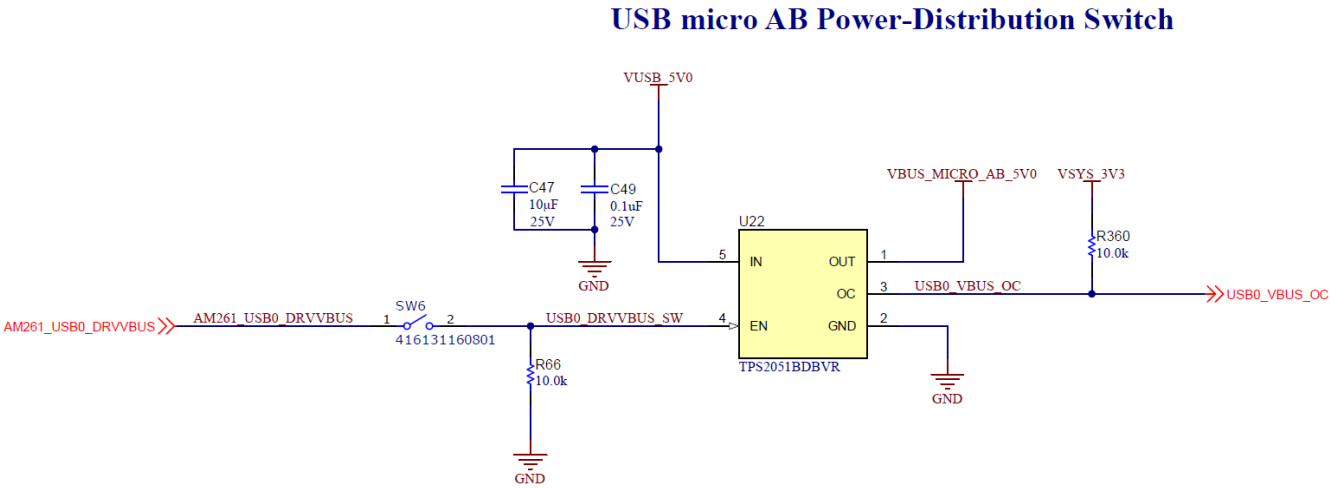


Figure 8-4. USB Host Mode Power Switch - LP-AM261

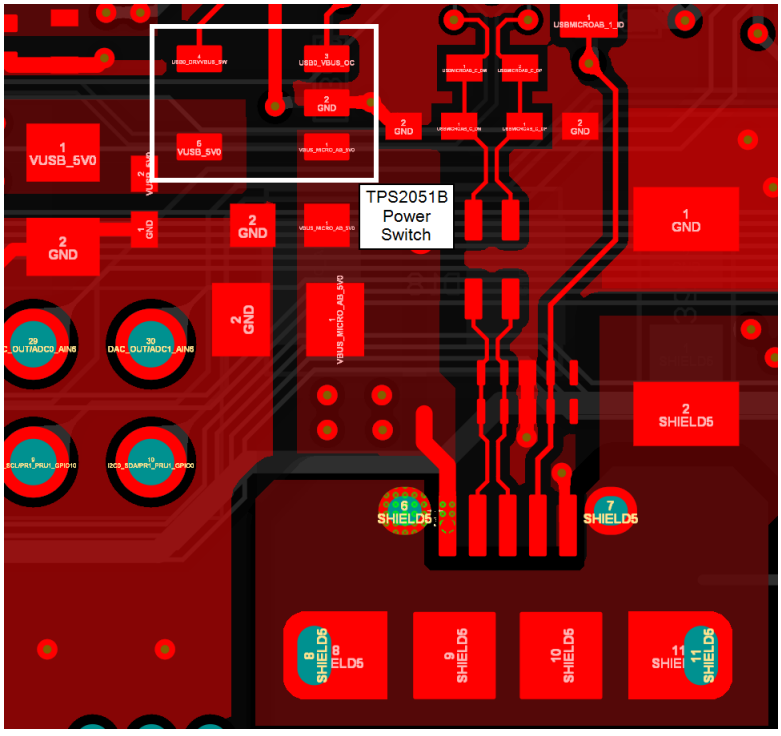


Figure 8-5. TPS2051B Layout Example - LP-AM261

To indicate Host Mode operation, the USB0_ID pin on the USB receptacle is connected to GND.

9 Multiplexed Peripherals

With the large number of multiplexed digital I/O present on the AM26x MCU IOMUX, designers are recommended to make full use of the TI System Configuration tool (SysConfig) to experiment and plan different pin multiplexing scenarios before committing the design to hardware. The resulting SysConfig pin multiplexing configurations can then be used for schematic capture, layout, and software driver creation.

For more details, see https://www.ti.com/tool/SYSCONFIG.

10 Digital Peripherals

10.1 General Digital Peripheral Routing Guidelines

The following general routing recommendations need to be followed throughout an AM26x PCB design. The 45nm LVCMOS process I/O can produce relatively fast edge-rates. Without transmission-line effects planned for, this can result in severe overshoot or undershoot even with relatively short traces on the PCB. These uncontrolled level transitions can damage associated components by presenting attached I/O with over/under-voltage conditions. Additionally, these uncontrolled transitions can radiate excessively which creates cross-talk and EMI compliance problems.

To mitigate these problems:

- Route all digital I/O as controlled impedance transmission-lines (microstrip or stripline).
- Place series termination near each AM26x transmit pin and attached transmit pins of associated IC.
  - The values and performance of these termination resistors need to be validated during wake-up of new PCB hardware.
  - In some cases, these termination resistors are not required, but need to only be removed or eliminated from the design after testing. 0Ω resistors can aid in creating footprints where termination resistors are needed.
- Route with solid ground return planes on adjacent layers.
- Route with ground return rings surrounding constantly switching signals (clocks, EPWM).
- Route with ground return rings surrounding sensitive analog signals (ADC/DAC channels, VREF).

For additional guidance on peripheral routing, refer to *High-speed Interface Layout Guidelines*.

10.2 Trace Length Matching

AM26x microcontrollers are equipped with several peripherals that require strict adherence to trace length matching guidelines. TI highly recommends that any engineer designing a PCB system using AM26x and utilizing the following device peripherals reviews the contents of *High-speed Interface Layout Guidelines* and applies these guidelines to the AM26x PCB design.

AM26x digital peripherals that require trace length matching are listed below:

Table 10-1. AM26x Digital Peripherals - Trace Length Matching

AM26x Peripheral	Applicable Devices	Notes
USB	AM261x	• See Section 8 for more information
QSPI	AM263x, AM263Px, AM261x	• Critical signals are QSPI_D[3:0] and QSPI_CLK
OSPI	AM263Px, AM261x	• Critical signals are OSPI_D[7:0] and OSPI_CLK
MMC	AM263x, AM263Px, AM261x	• Critical signals are MMC0_D[3:0], CLK, and CMD
FSI	AM263x, AM263Px, AM261x	• Lower priority, but helps reduce skew between signals
RGMII Ethernet	AM263x, AM263Px, AM261x	• RX and TX signals are critical • RX signals only need to be matched to other RX signals • TX signals only need to be matched to other TX signals • RX or TX signal groups can be different lengths

11 Analog Peripherals

11.1 General Analog Peripheral Routing Guidelines

The following general routing recommendations need to be followed throughout the analog portions of an AM26x PCB design. Analog signals as especially sensitive to cross talk and requiring clean signal return paths for maximizing signal integrity.

To mitigate these problems:

- Isolate all analog signals as much as possible with ground isolation between the analog trace and any adjacent trace.
- Route analog signals with solid ground return layers on adjacent layers.
- Avoid routing analog signals near high speed or current signals.
  - When impossible to totally avoid high speed or current signals, cross the traces perpendicularly to avoid as much cross-talk as possible.
- Adding signal amplifier and filter networks can promote signal integrity.

For the SAR ADCs on AM26x, refer to the *Choosing an Acquisition Window Duration* section of the device-specific AM26x Technical Reference Manual and Register Addendum documents for additional guidance.

11.1.1 Resolver ADC Routing Guidelines

The AM263Px Sensor package includes two Resolver to Digital Converter (RDC) peripherals. A resolver is a type of rotary electrical transformer used for measuring degrees of rotation which is typically attached to an electrical motor. A typical resolver consists of a rotary transformer (exciter winding) and two windings separated by 90 degrees on the stator. An excitation sinusoidal signal is applied to the excitation coil of the resolver and the rotation of the motor causes modulated sine and cosine outputs on the sine and cosine sense coils of the resolver. The angle of the modulated sine and cosine signals is directly related to the mechanical angle of the rotor compared to the stator and the speed of the motor rotation.

The AM263Px RDCs generate an excitation signal as a PWM which is routed through an excitation amplifier before being applied to the exciter winding on the motor resolver. The resolver sine and cosine outputs are then routed back into the RDC analog inputs, where the RDC IP converts and interprets the signals to determine motor angle and rotational speed. Figure 11-1 shows an example block diagram of a resolver based design with an AM263P device.

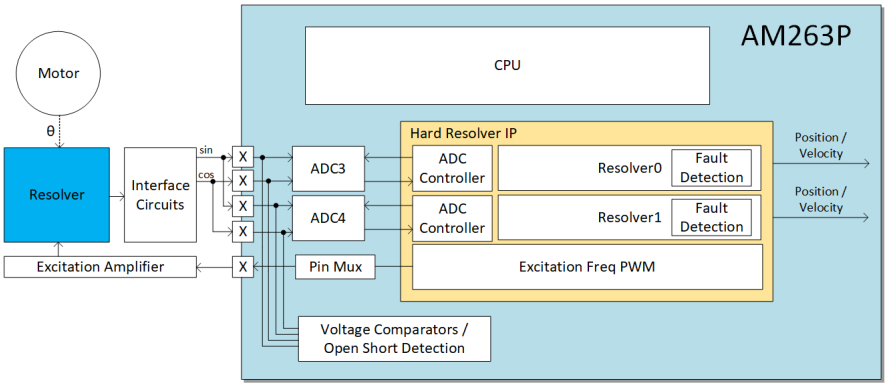


Figure 11-1. AM263P Resolver ADC System

The excitation PWM signals from the AM263Px support up to 20KHz and follows the same guidelines for PCB routing as other similar frequency digital signals. For guidance on routing digital signals, see General Digital Peripheral Routing Guidelines.

The Excitation Amplifier is used to convert the excitation PWM signals to sine waves as inputs to the motor resolver. These signals and the sine and cosine signals output from the resolver to the RDC inputs of the AM263Px need to follow the same guidelines for PCB routing as other analog signals. For guidance on routing analog signals, see General Analog Peripheral Routing Guidelines.

12 Layer Stackup

The AM263x, AM263Px, and one of the four packages of the AM261x MCUs are packaged in a ZCZ0324A 324 ball, 0.8mm pitch, 18 x 18 full NFBGA array 15mm x 15mm package (referred to as 'ZCZ package' in this document). The larger pitch on this package allows for a low layer count for power and full signal fan-out. In the case of the LP-AM263 EVM, a 6-layer stackup design was able to fully route all power and signal pins across the device for the LaunchPad form-factor of boards. The LP-AM263 LaunchPad stackup below represents the most optimized stackup example for the ZCZ package devices at this time.

Lower layer count stackups for the ZCZ package are likely possible, especially when considering partial signal fan-out designs. However, these have not yet been explored by TI.

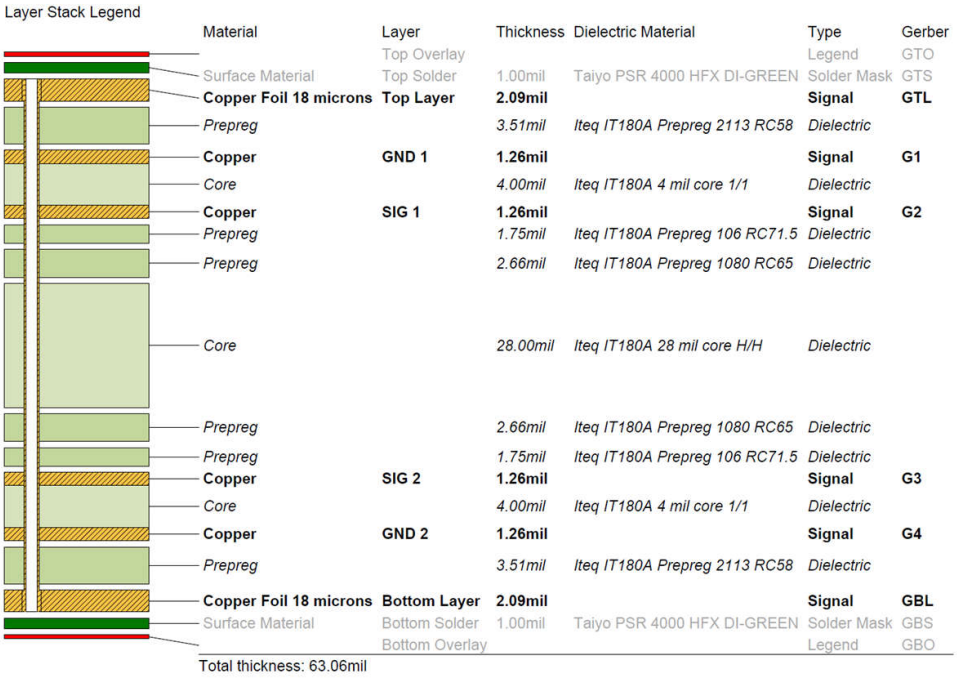


Figure 12-1. LP-AM263 Stackup

The other three packages of the AM261x MCU are described in the table below:

Table 12-1. AM261x Package Sizes

Package Name (Type, Ball Count)	Package Dimensions	BGA Pitch	BGA Array
ZNC (NFBGA, 293)	10mm x 10mm	0.5mm	19 x 19
ZEJ (NFBGA, 256)	13mm x 13mm	0.8mm	16 x 16
ZFG (NFBGA, 304)	13.25mm x 13.25mm	0.65mm	20 x 20

In the case of the LP-AM261 EVM, a 6-layer stackup design was able to fully route all power and signal pins across the ZFG package device for the LaunchPad form-factor of boards. The LP-AM261 LaunchPad stackup below represents an optimized, full-system stackup example for the ZFG package at this time:

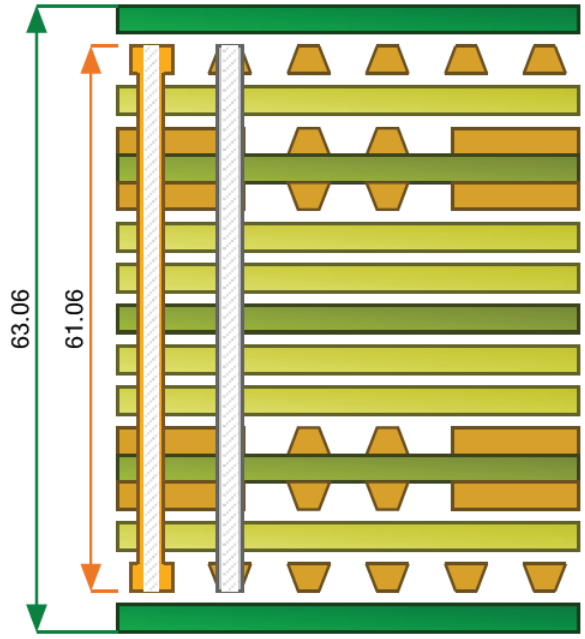
Layer	Stack up	Description	Type	Processed Thickness
		Taiyo PSR 4000 HFX DI-GREEN	SolderMask	1.000
1		Copper Foil 18 microns	Copper	2.087
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.511
2				1.260
		Iteq IT180A 4 mil core 1/1	FR4	4.000
3				1.260
		Iteq IT180A Prepreg 106 RC71.5	Dielectric	1.750
		Iteq IT180A Prepreg 1080 RC65	Dielectric	2.663
		Iteq IT180A 28 mil core H/H	FR4	28.000
		Iteq IT180A Prepreg 1080 RC65	Dielectric	2.663
		Iteq IT180A Prepreg 106 RC71.5	Dielectric	1.750
4				1.260
		Iteq IT180A 4 mil core 1/1	FR4	4.000
5				1.260
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.511
6		Copper Foil 18 microns	Copper	2.087
		Taiyo PSR 4000 HFX DI-GREEN	SolderMask	1.000

Figure 12-2. LP-AM261 Stackup

Lower layer count stackups for the AM261x ZFG and ZNC packages have been explored by TI. Pictured below is an example of a 4-layer stackup for PCB systems utilizing the AM261x ZFG or ZNC package sizes:

#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.4mil	3.5
1	L1	CF-004	Signal	1oz	1.378mil	
	Dielectric 1	PP-006	Prepreg		7mil	4.1
2	L2		Signal	1oz	1.38mil	
	Dielectric1	FR-4 High Tg	Dielectric		42mil	4.8
3	L3		Signal	1oz	1.38mil	
	Dielectric 2	PP-006	Prepreg		7mil	4.1
4	L4	CF-004	Signal	1oz	1.378mil	
	Bottom Solder	Solder Resist	Solder Mask		0.4mil	3.5
	Bottom Overlay		Overlay			

Figure 12-3. AM261x ZFG/ZNC PCB System Stackup

12.1 Key Stackup Features

Table 12-2. Stackup Features by Package Size

	ZCZ (15mm x15mm, 0.8mm Pitch), ZFG (13.25mm x 13.25mm, 0.65mm Pitch)	ZFG (13.25mm x 13.25mm, 0.65mm Pitch), ZNC (10mm x 10mm, 0.5mm Pitch)
Total Layers	6	4
PCB Thickness	62 mil +/- 10%	62 mil +/- 10%
Optionally Controlled Impedance Routing Layers	4 (L1, L3, L4, L6)	2 (L1, L4)
Signal/Power Layers have Adjacent GND Reference	Yes	Yes
Core Center Layer Thickness	28 mil	42 mil
BGA Fan-out Via Type	Through-hole	Through-hole

Note

In a 6-layer design, minimal dielectric thickness between L4 power and L5 GND return layers allows for best plane capacitance performance, aiding power integrity and EMI.

Table 12-3. 6-Layer PCB: Layer Utilization

Layer Number	Comment
Copper 1 (Top)	Top layer mounting and signal routing
Copper 2	Ground return plane
Copper 3	Embedded microstrip or stripline signal routing and power routing
Copper 4	Embedded microstrip or stripline and power routing
Copper 5	Ground return plane
Copper 6 (Bottom)	Bottom layer mounting and signal routing

Table 12-4. AM263x, AM263Px, AM261x ZCZ Package, 6-Layer PCB: Controlled Impedance Planning Options

Layer Number	Reference Layer Number	Structure Name (1)	Trace Width (mils)	Trace Separation (mils)	Target Impedance (Ω)	Calculated Impedance (Ω)	Notes
L1	L2	Coated Microstrip	5.300	0.000	50.000	50.140	
L1	L2	Edge Coupled Coated Microstrip	4.200	5.000	90.000	89.830	L1, USB differential
L1	L2	Edge Coupled Coated Microstrip	4.000	7.700	100.000	99.840	
L1	L2	Edge Coupled Coated Microstrip	4.100	6.800	120.000	120.030	
L3	L3	Offset Stripline	4.750	0.000	50.000	49.960	
L3	L2	Edge Coupled Offset Stripline	4.000	6.000	90.000	90.040	L3, USB differential
L3	L2	Edge Coupled Offset Stripline	3.500	8.100	100.000	99.880	
L3	L2	Edge Coupled Offset Stripline	4.000	12.000	100.000	100.160	
L6	L5	Coated Microstrip	5.300	0.000	50.000	50.140	
L6	L5	Edge Coupled Coated Microstrip	4.200	5.000	90.000	89.830	

Table 12-4. AM263x, AM263Px, AM261x ZCZ Package, 6-Layer PCB: Controlled Impedance Planning Options (continued)

Layer Number	Reference Layer Number	Structure Name (1)	Trace Width (mils)	Trace Separation (mils)	Target Impedance (Ω)	Calculated Impedance (Ω)	Notes
L6	L5	Edge Coupled Coated Microstrip	4.000	7.700	100.000	99.840	
L6	L4	Edge Coupled Coated Microstrip	4.100	6.800	120.000	120.030	

Table 12-5. 4-Layer PCB: Layer Utilization

Layer Number	Comment
Copper 1 (Top)	Top layer mounting and signal routing
Copper 2	Ground return plane
Copper 3	Power routing
Copper 4 (Bottom)	Bottom layer mounting and signal routing

Table 12-6. AM261x ZFG Package, 4-Layer PCB: Controlled Impedance Planning Options

Layer Number	Reference Layer Number	Structure Name (1)	Trace Width (mils)	Trace Separation (mils)	Target Impedance (Ω)	Calculated Impedance (Ω)	Notes
L1	L2	Coated Microstrip	4.000	3.900	50.000	49.640	
L1	L2	Edge Coupled Coated Microstrip	4.200	5.800	90.000	93.700	L1, USB differential
L1	L2	Edge Coupled Coated Microstrip	4.000	7.700	100.000	99.840	
L1	L2	Edge Coupled Coated Microstrip	4.100	6.800	120.000	120.030	
L4	L3	Coated Microstrip	5	8.5	50.000	47.400	
L4	L3	Edge Coupled Coated Microstrip	4.200	5.000	90.000	89.830	
L4	L3	Edge Coupled Coated Microstrip	4.000	7.700	100.000	99.840	
L4	L3	Edge Coupled Coated Microstrip	4.100	6.800	120.000	120.030	

Table 12-7. AM261x ZNC Package, 4-Layer PCB: Controlled Impedance Planning Options

Layer Number	Reference Layer Number	Structure Name (1)	Trace Width (mils)	Trace Separation (mils)	Target Impedance (Ω)	Calculated Impedance (Ω)	Notes
L1	L2	Coated Microstrip	3.200	3.300	50.000	52.960	
L1	L2	Edge Coupled Coated Microstrip	4.200	5.800	90.000	93.700	L1, USB differential
L1	L2	Edge Coupled Coated Microstrip	4.000	7.700	100.000	99.840	
L1	L2	Edge Coupled Coated Microstrip	4.100	6.800	120.000	120.030	
L4	L3	Coated Microstrip	3.500	6.650	50.000	49.980	
L4	L3	Edge Coupled Coated Microstrip	4.200	5.000	90.000	89.830	
L4	L3	Edge Coupled Coated Microstrip	4.000	7.700	100.000	99.840	
L4	L3	Edge Coupled Coated Microstrip	4.100	6.800	120.000	120.030	

(1) All impedance calculated using Polar 2D field solver on given copper and dielectric thicknesses, widths and dissipation constants.

13 Vias

The AM26x EVMs show different examples of via construction for BGA fan-out and overall board routing. All AM26x EVMs make use of PTH via construction.

Table 13-1. AM26x EVM Via Types

EVM	Via Type	Via Diameter (mils)	Via Drill (mils)
AM263x LaunchPad	PTH	18.000	8.000
AM263Px LaunchPad	PTH	18.000	8.000
AM261x LaunchPad	PTH	18.000	8.000
AM263x controlCard	PTH	18.000	8.000
AM263Px controlCard	PTH	18.000	8.000
AM261x controlSOM	PTH	18.000	8.000

14 BGA Power Fan-Out and Decoupling Placement

45nm CMOS technology allows for faster core and SRAM clock rates, and faster edge rates for LVCMOS I/O buffers. Therefore, in comparison with previous MCU process nodes, careful power and ground return placement is critical to achieving best power integrity, signal integrity and EMI performance with AM263x, AM263Px, and AM261x designs.

TI recommends that designers follow a similar power distribution layout as implemented in the AM263x, AM263Px, and AM261x EVM PCB designs to achieve good power integrity results across all operating conditions and EMI testing conditions.

The AM263x controlCard EVM represents the most optimized and scrutinized power distribution layout for ZCZ package AM26x devices. The controlCard example is referenced in the ZCZ-specific sections. For non-ZCZ AM261x devices, refer to the ZFG/ZNC-specific sections.

Table 14-1. BGA Attribute Sections by Device Package

BGA Attribute	AM263x/AM263Px/AM261x (ZCZ)	AM261x (ZFG)	AM261x (ZNC)
Ground Return	Section 14.1.1	Section 14.1.2	
1.2V Core Digital Power	Section 14.2.1	Section 14.2.2	N/A
3.3V Digital and Analog Power	Section 14.3.1	Section 14.3.2	N/A
1.8V Digital and Analog Power	Section 14.4.1	Section 14.4.2	N/A

14.1 Ground Return

This section summarizes the main elements of the ground return routing on AM26x devices.

14.1.1 Ground Return - ZCZ Package AM26x Devices

All available ground return BGA must be utilized to create the best possible electrical and thermal connection between the AM263x, AM263Px, or AM261x package and the attached PCB. Maximizing VSS BGA usage is critical from signal integrity, EMI/EMC and thermal perspectives.

Unless a separate top package heat sink is used in the design, the VSS BGA (and VDDCORE to a lesser extent) are the only heat sinking thermal connection for the BGA package. For required, thermal performance, AM26x-ZCZ PCB designs must adhere to following thermal via design requirements.

- A minimum of 49 VSS vias in the center of the BGA must be shorted to PCB ground return planes. However, if possible, and for best thermal performance, then all VSS BGA needs to be connected to PCB ground return planes.
- Solid ground return planes shall be used directly under the BGA on as many layers as possible.
- Solid ground return, or the widest possible traces shall be used on the top or bottom mounting layer for VSS BGA pad connection.
- VSS via drills shall use largest possible drill diameter. This maximizes surface area of the via, providing lowest thermal resistance.
- VSS vias need to be conductively filled, if possible.

All of these thermal via requirements must be balanced against the necessary power and signal fan-out of the design.

The AM26x devices contain both analog and digital ground return pins. Both analog and digital ground return pins need to be shorted to a common set of ground return planes on the PCB for best noise and EMI performance as this creates the lowest possible impedance path for all return currents to follow. TI does not recommend to separate these two return paths as this typically ends up with lower performance return paths for both digital and analog signal paths.

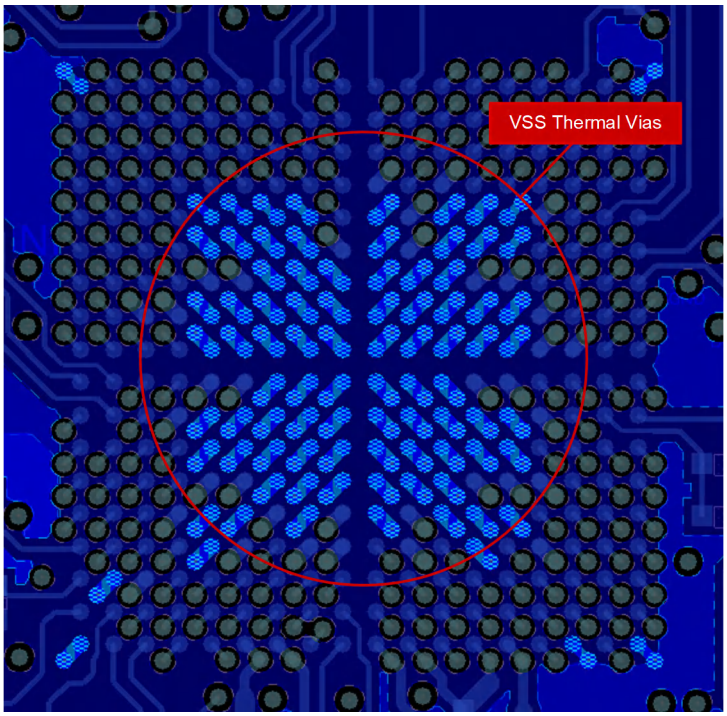


Figure 14-1. AM263x controlCARD Excerpt – Ground Return Vias Under AM263x BGA Layer 1 and Layer 2

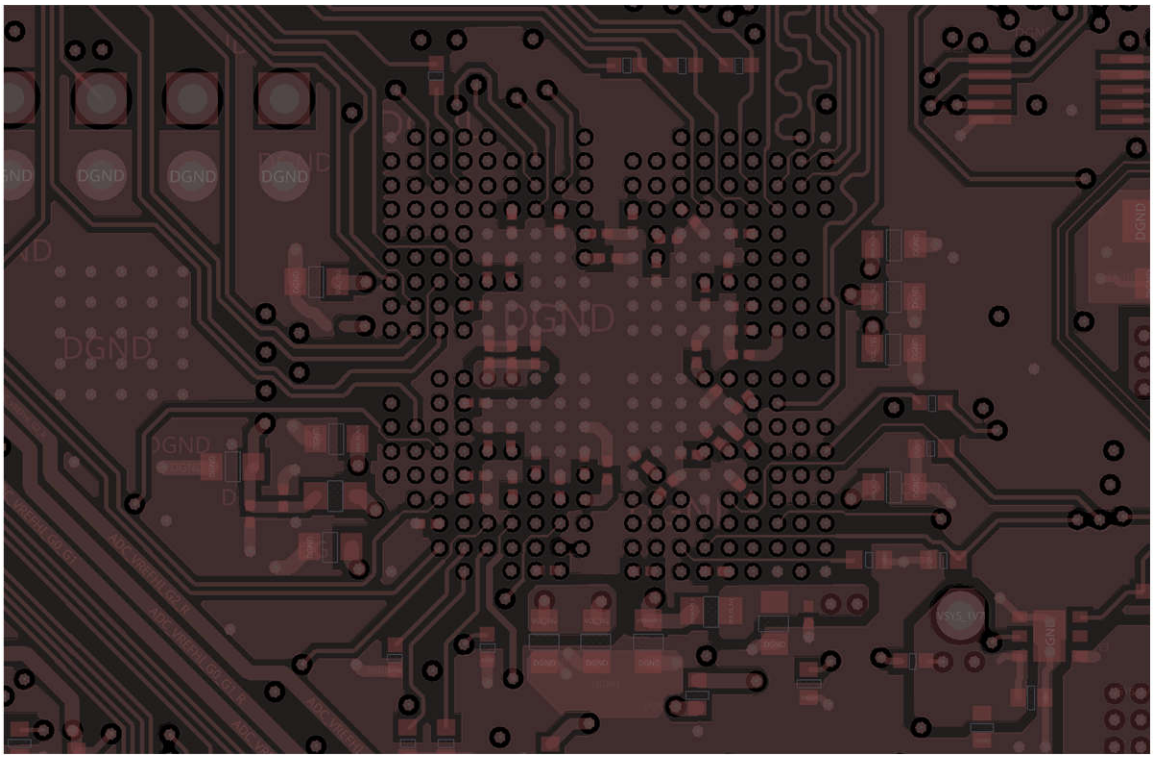


Figure 14-2. AM263x controlCARD Excerpt – Ground Return Vias Under AM263x BGA Layer 10

14.1.2 Ground Return - ZNC and ZFG Package AM261x Devices

All available ground return BGA must be utilized to create the best possible electrical and thermal connection between the AM261x package and the attached PCB. Maximizing VSS BGA usage is critical from signal integrity, EMI/EMC and thermal perspectives.

Unless a separate top package heat sink is used in the design, the VSS BGA (and VDDCORE to a lesser extent) are the only heat sinking thermal connection for the BGA package. For required thermal performance, AM261x PCB designs must adhere to following thermal via design requirements.

- A minimum of 60 VSS vias (ZNC) or 49 VSS vias (ZFG) in the center of the BGA must be shorted to PCB ground return planes. However, if possible, and for best thermal performance, then all VSS BGA are connected to PCB ground return planes
- Solid ground return planes shall be used directly under the BGA on as many layers as possible.
- Solid ground return, or the widest possible traces shall be used on the top or bottom mounting layer for VSS BGA pad connection.
- VSS by drills use largest possible drill diameter. This maximize surface area of the via, providing lowest thermal resistance.
- VSS vias need to be conductively filled, if possible.

All of these thermal via requirements must be balanced against the necessary power and signal fan-out of the design.

The AM261x devices contain both analog and digital ground return pins. Both analog and digital ground return pins need to be shorted to a common set of ground return planes on the PCB for best noise and EMI performance as this creates the lowest possible impedance path for all return currents to follow. TI does not recommend to separate these two return paths as this typically ends up with lower performance return paths for both digital and analog signal paths.

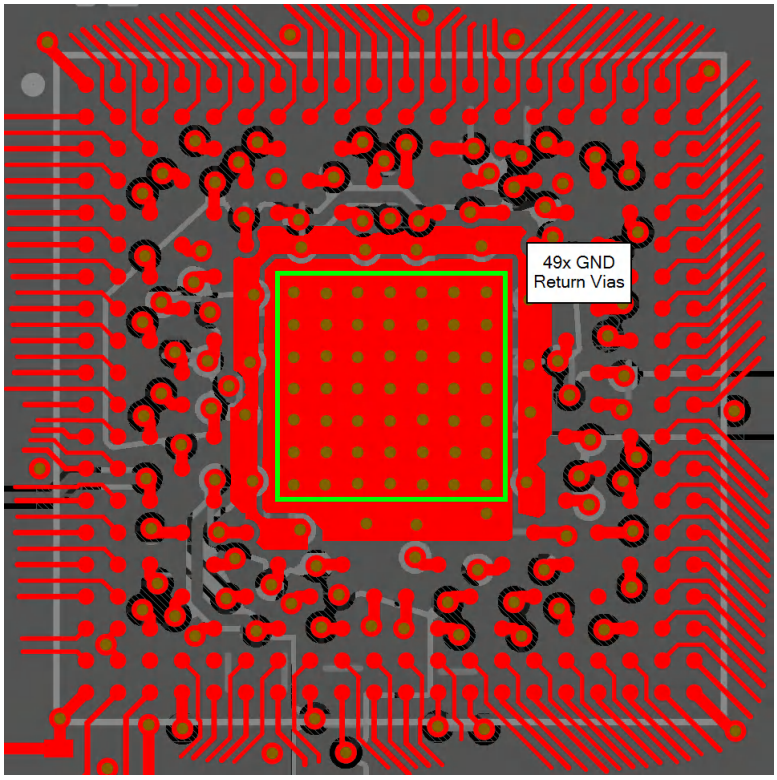


Figure 14-3. AM261x ZFG Routing Study - Ground Return Vias on Layer 1

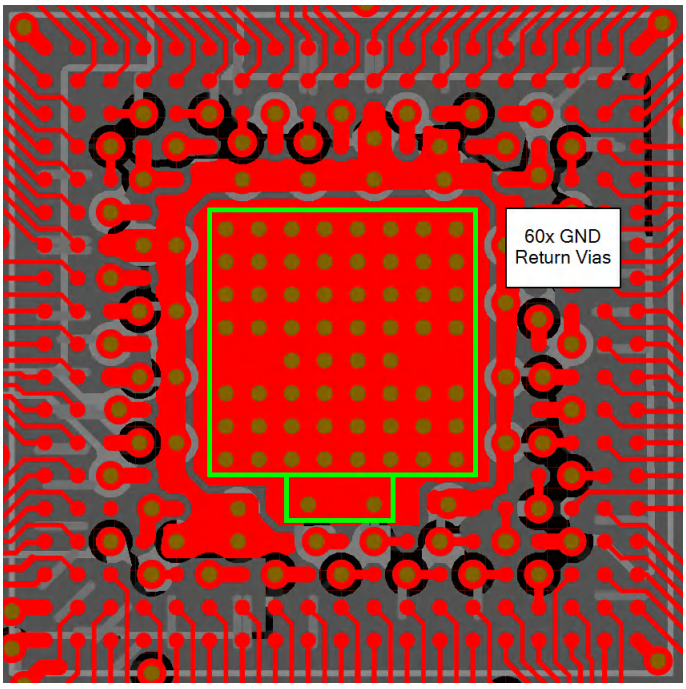


Figure 14-4. AM261x ZNC Routing Study - Ground Return Vias on Layer 1

14.2 1.2V Core Digital Power

This section summarizes the main elements of the 1.2V core digital power routing on AM26x devices.

14.2.1 1.2V Core Digital Power Key Layout Considerations - ZCZ

For AM26x ZCZ package devices, the 1.2V core digital power routing of the AM263x controlCARD EVM (TMDSCNCD263) is explored - from the 1.2V buck-converter (TPS62913RPUR, U65) through the board power planes and ending at the BGA bulk and per pin decoupling capacitor array.

- AM263x, AM263Px, or AM261x must be co-located with the 1.2V core digital regulator to allow for minimal IR drop from the regulator to the BGA power pins.
- Wide 15 mil traces must be used for all power and ground return via fan-out.
- A dedicated power layer, with tightly coupled ground return reference plane must be used for best transient performance and EMI coupling.
- A wide power plane entry into the center of the BGA 1.2V power pin areas must be used for minimal IR drop and best transient performance.
- Larger packaged, lower-frequency, bulk capacitance must be placed adjacent to the BGA with vias directly to power plane paths.
- Smaller packaged, higher-frequency decoupling capacitance must be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible.

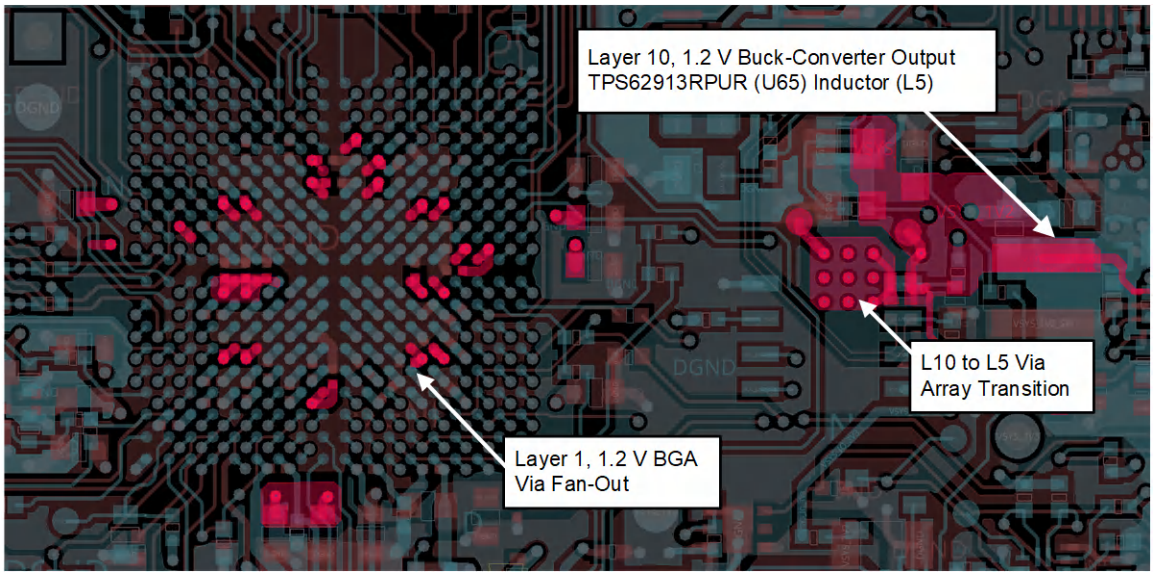


Figure 14-5. AM263x controlCARD Excerpt – 1.2V Core Power Output, Power Plane Vias and BGA Vias

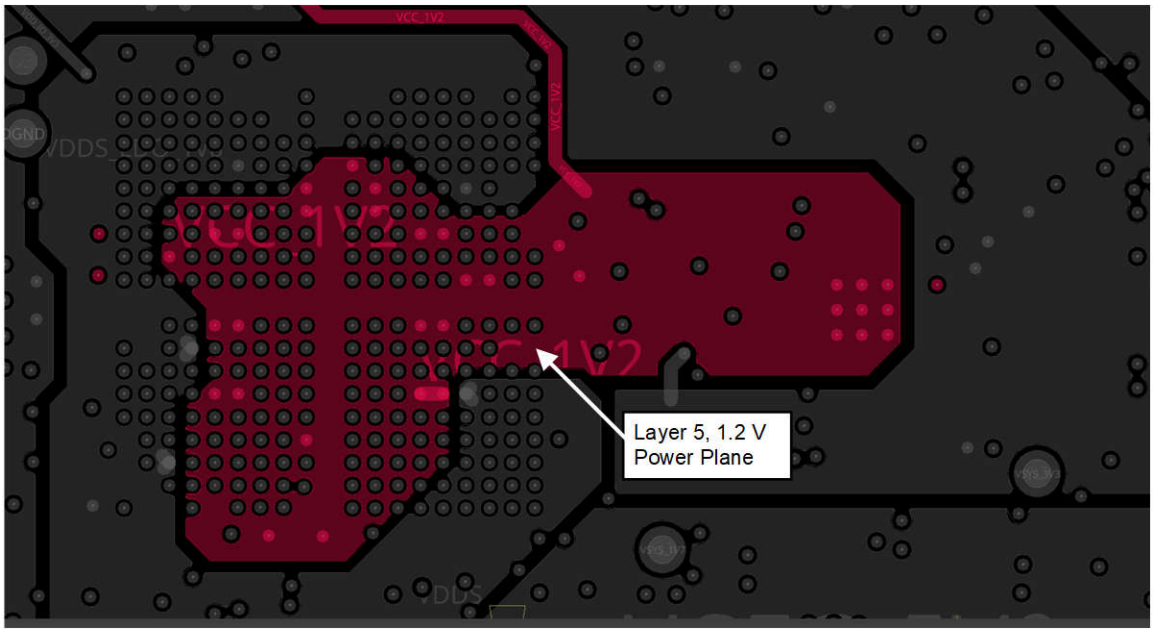


Figure 14-6. AM263x controlCARD Excerpt – 1.2V Core Power Plane, Layer 5

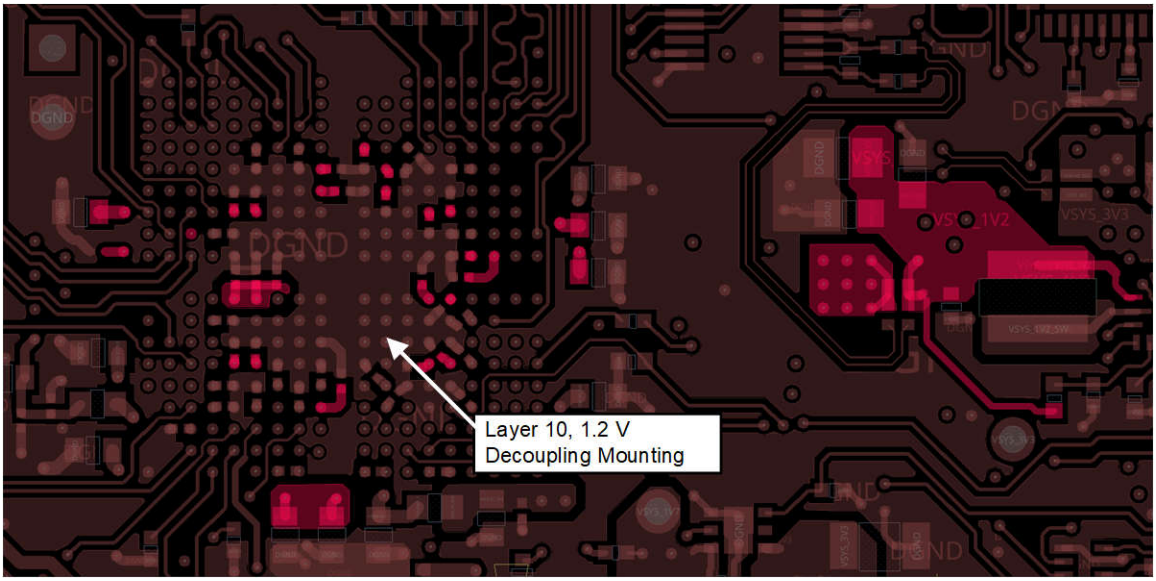


Figure 14-7. AM263x controlCARD Excerpt – 1.2V Core Power Decoupling Mounting, Layer 10

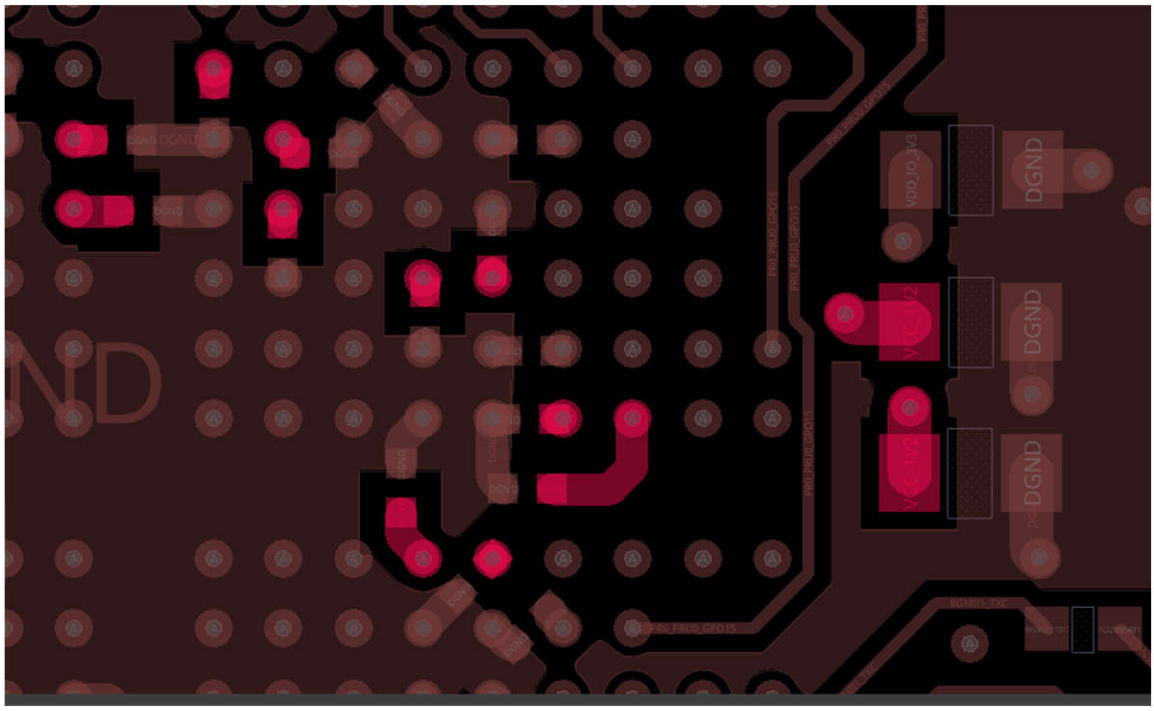


Figure 14-8. AM263x controlCARD Excerpt – 1.2V Core Power Decoupling Mounting, Layer 10

14.2.2 1.2V Core Digital Power Key Layout Considerations - ZFG

For AM261x ZFG package devices, the 1.2V core digital power routing of the AM261x LaunchPad EVM (LP-AM261) is explored - from the 1.2V buck output of the PMIC (TPS650366), through the board power planes and ending at the BGA bulk and per pin decoupling capacitor array. A 4-layer PCB layout is also explored at the end of this section.

- AM261x (ZFG) must be co-located with the 1.2V core digital regulator to allow for minimal IR drop from the regulator/PMIC to the BGA power pins.
- Wide 10 mil traces must be used for all power and ground return via fan-out.
- A dedicated power layer, with tightly coupled ground return reference plane must be used for best transient performance and EMI coupling
- A wide power plane entry into the center of the BGA 1.2V power pin areas must be used for minimal IR drop and best transient performance
- Larger packaged, lower-frequency, bulk capacitance must be placed adjacent to the BGA with vias directly to power plane paths
- Smaller packaged, higher-frequency decoupling capacitance must be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible

The below figures detail the 1.2V core digital power flow from the source to AM261x device on the AM261x LaunchPad EVM (LP-AM261).

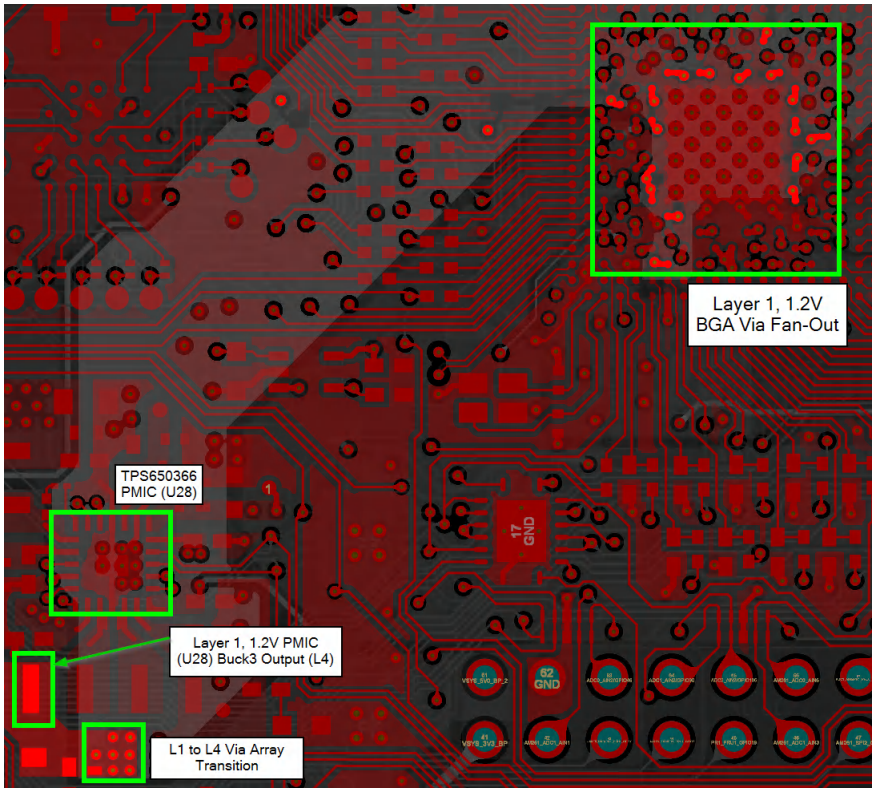


Figure 14-9. AM261x LaunchPad Excerpt – 1.2V Core Power Output, Power Plane Vias and BGA Vias

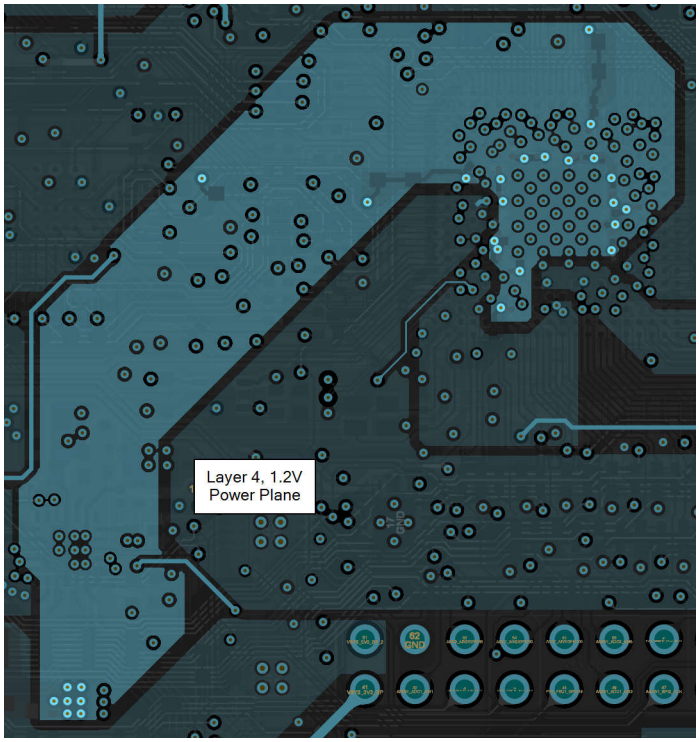


Figure 14-10. AM261x LaunchPad Excerpt – 1.2V Core Power Plane, Layer 4

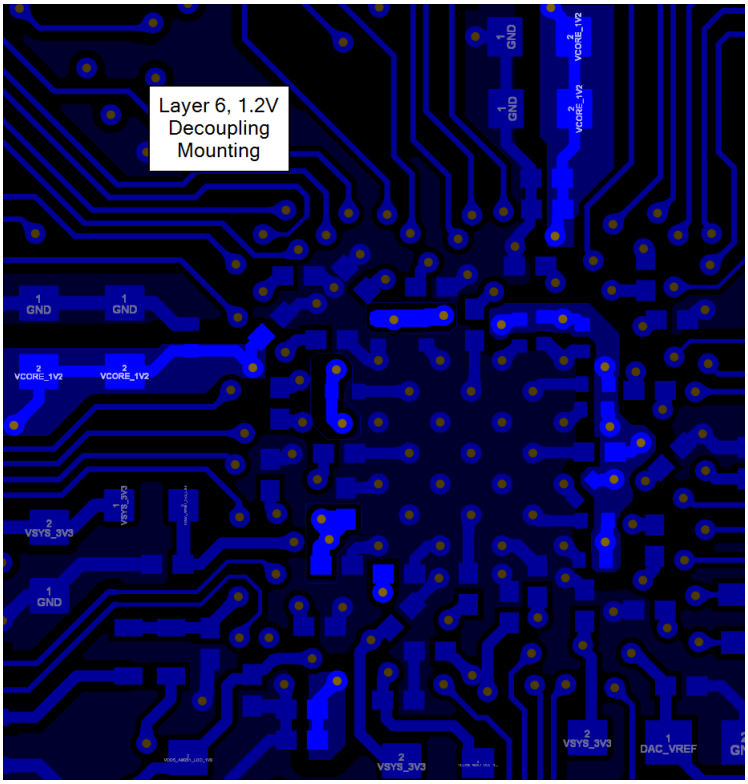


Figure 14-11. AM261x LaunchPad Excerpt – 1.2V Core Power Decoupling Mounting, Layer 6

A 1.2V core digital power flow for a 4-layer PCB is under study for a future revision of this document.

14.3 3.3V Digital and Analog Power

This section summarizes the main elements of the 3.3V digital I/O and analog I/O power routing of the AM26x devices.

14.3.1 3.3V I/O Power Key Layout Considerations - ZCZ

The 3.3V power system on AM26x ZCZ devices are explored using the AM263x controlCARD EVM (TMDSCNCD263), from the 3.3V buck-converter (TPS62913RPUR, U30) through the board power planes and ending in at the BGA bulk and per pin decoupling capacitor array. A common buck-converter supplies power for all of the AM263x digital I/O, analog I/O and the rest of the controlCard 3.3V loads. This is common in most designs where all 3.3V digital level I/O share a common power supply. Additional filtering for the local AM263x 3.3V analog power net is done through the LC filter of ferrite-bead FL13 and associated capacitors. This is used to create a low-IR drop low-pass filter that attenuates the higher frequency switching harmonics of the TPS62913RPUR regulator.

- Wide 15 mil traces need to be used for all power and ground return via fan-out.
- 3.3V I/O power tends to be shared across multiple devices in the system, recommend routing with very wide power planes across the PCB to minimize IR drops to all components including AM263x, AM263Px, or AM261x.
- A tightly coupled, adjacent ground return reference plane needs to be used for best transient performance and EMI coupling.
- A wide power plane entry that covers the BGA 3.3V power pin areas needs to be used for minimal IR drop and best transient performance.
- Larger packaged, lower-frequency, bulk capacitance needs to be placed adjacent to MCU BGA with vias directly to power plane paths.
- Smaller packaged, higher-frequency decoupling capacitance needs to be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible.

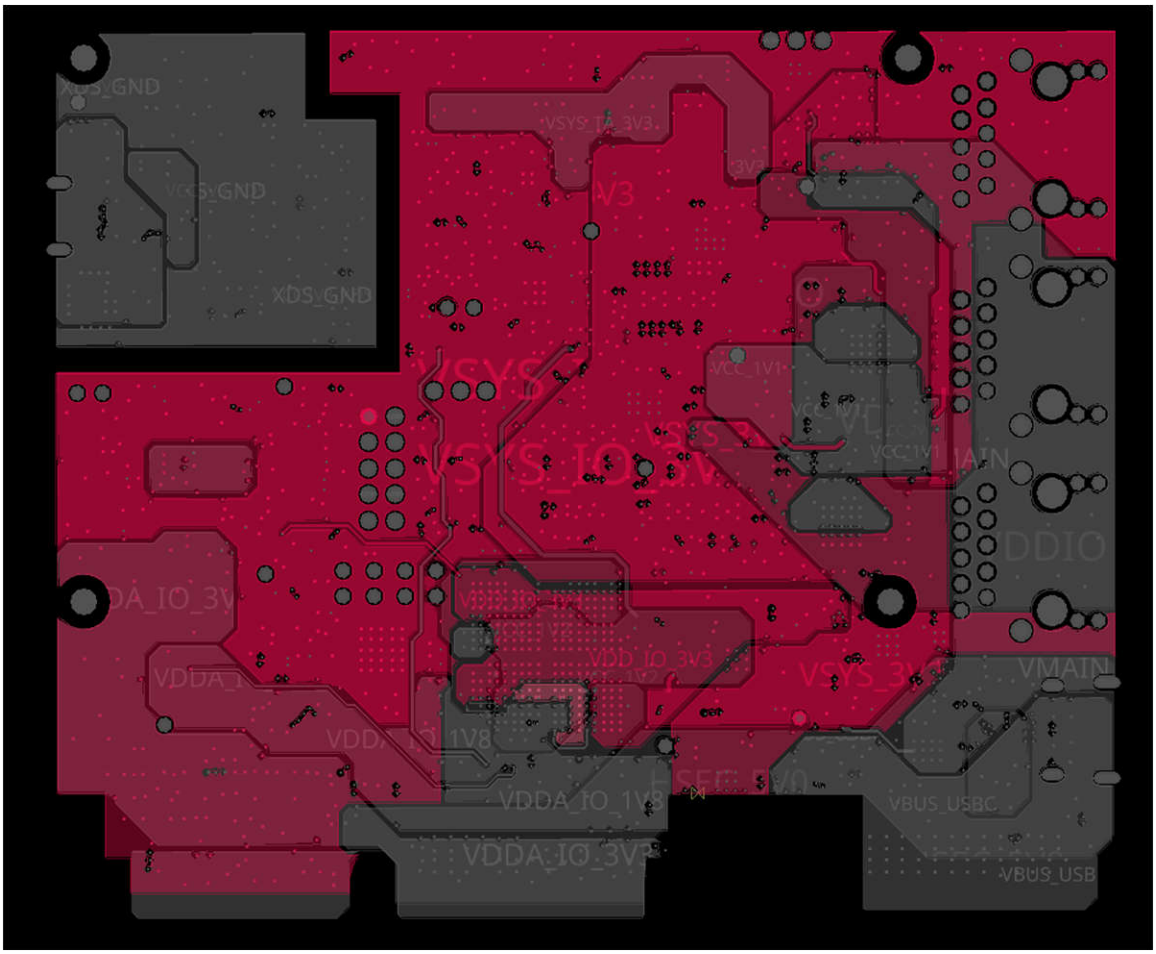


Figure 14-12. AM263x controlCARD Excerpt – 3.3V Digital and Analog Power Planes on Layer 5 and Layer 6

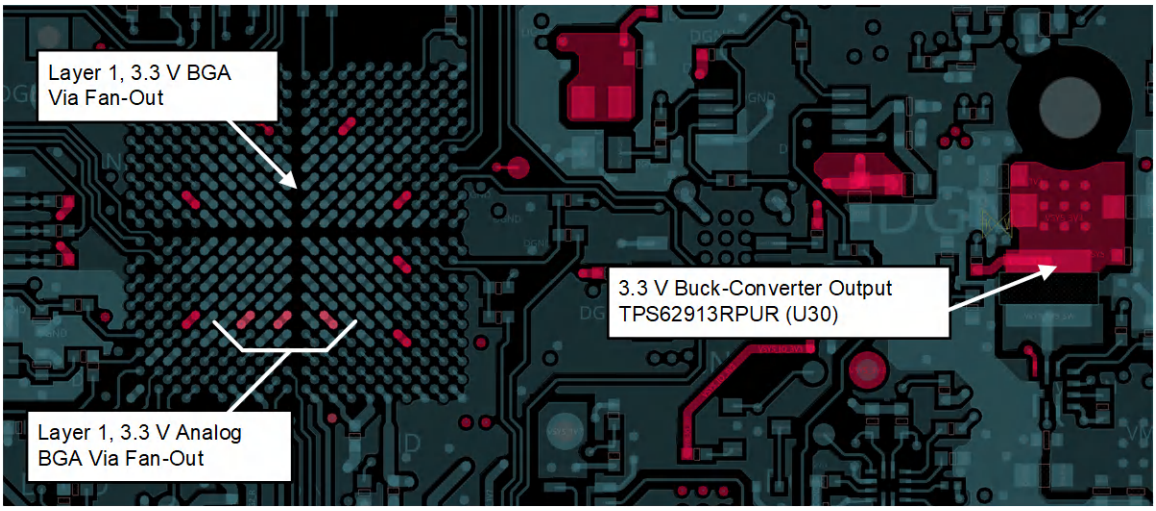


Figure 14-13. AM263x controlCARD Excerpt – 3.3V Digital I/O and Analog I/O BGA Pinout and Regulator Output

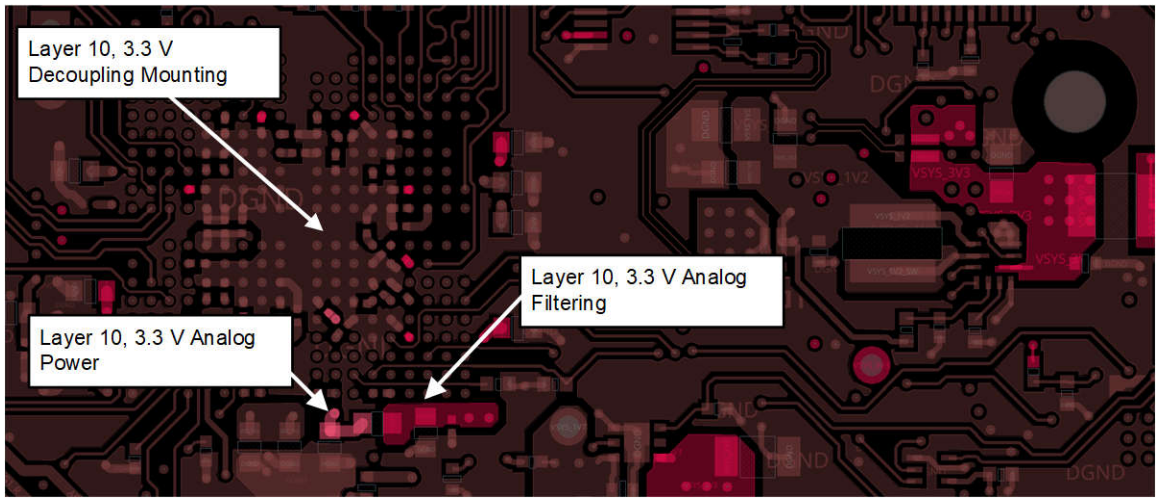


Figure 14-14. AM263x controlCARD Excerpt – Common 3.3V Plane Transition Vias

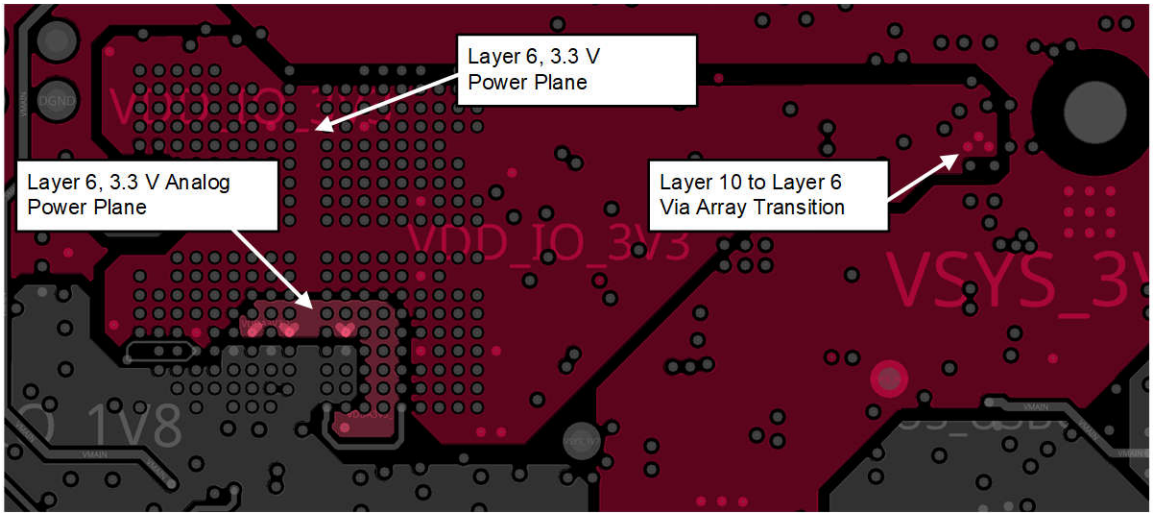


Figure 14-15. AM263x controlCARD Excerpt – 3.3V Digital and Analog Planes Layer 6

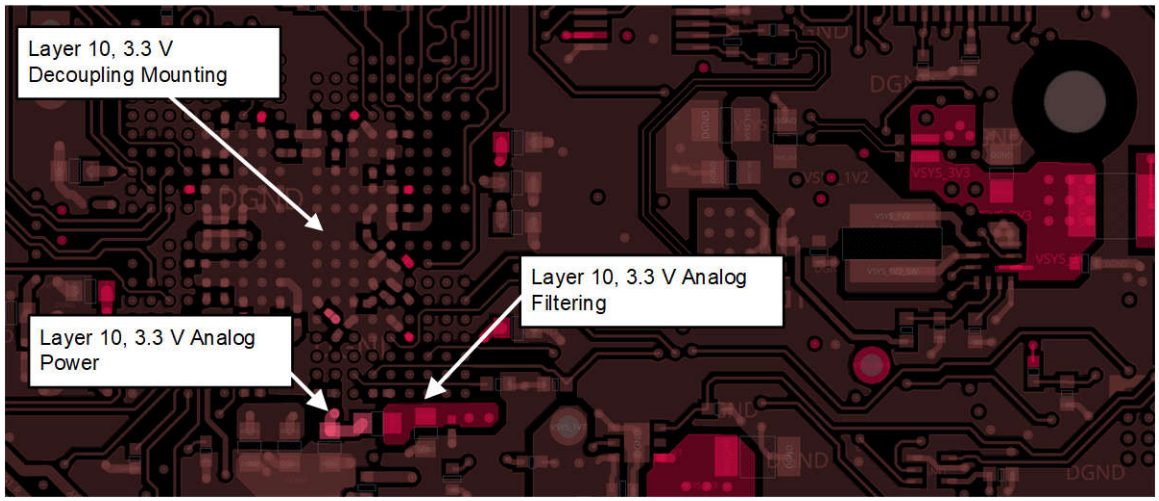


Figure 14-16. AM263x controlCARD Excerpt – 3.3V Digital and Analog Power Decoupling Mounting, Layer 10

14.3.2 3.3V I/O Power Key Layout Considerations - ZFG

The 3.3V power system on AM261x ZFG devices are explored using the AM261x LaunchPad EVM (LP-AM261), from the 3.3V buck output of the PMIC (TPS650366) through the board power planes and ending in at the BGA bulk and per pin decoupling capacitor array. The PMIC 3.3V buck output supplies power for all of the AM261x digital I/O, analog I/O, and the rest of the LaunchPad loads. This is common in most designs where all 3.3V digital level I/O share a common power supply. Additional filtering for the local AM261x 3.3V analog power net is done through the LC filter of ferrite-bead FB2 and associated capacitors. This is used to create a low-IR drop low-pass filter that attenuates the higher frequency switching harmonics of the PMIC buck output.

- Wide 10 mil traces need to be used for all power and ground return via fan-out.
- 3.3V I/O power tends to be shared across multiple devices in the system, recommend routing with very wide power planes across the PCB to minimize IR drops to all components (including AM261x SoC).
- A tightly coupled, adjacent ground return reference plane needs to be used for best transient performance and EMI coupling.
- A wide power plane entry that covers the BGA 3.3V power pin areas need to be used for minimal IR drop and best transient performance.
- Larger packaged, lower-frequency, bulk capacitance needs to be placed adjacent to MCU BGA with vias directly to power plane paths.
- Smaller packaged, higher-frequency decoupling capacitance needs to be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible.

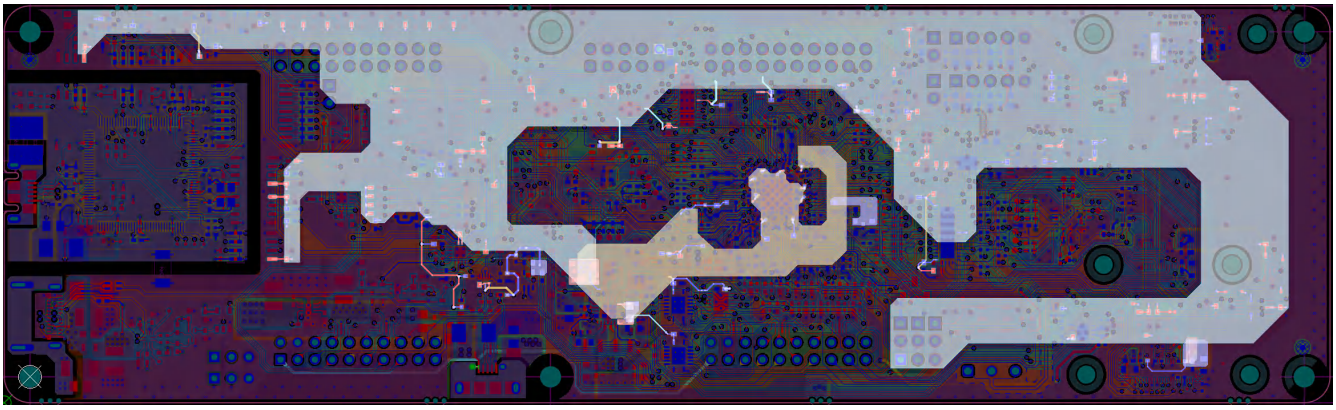


Figure 14-17. AM261x LaunchPad Excerpt – 3.3V Digital and Analog Power Planes on Layer 3 and Layer 4

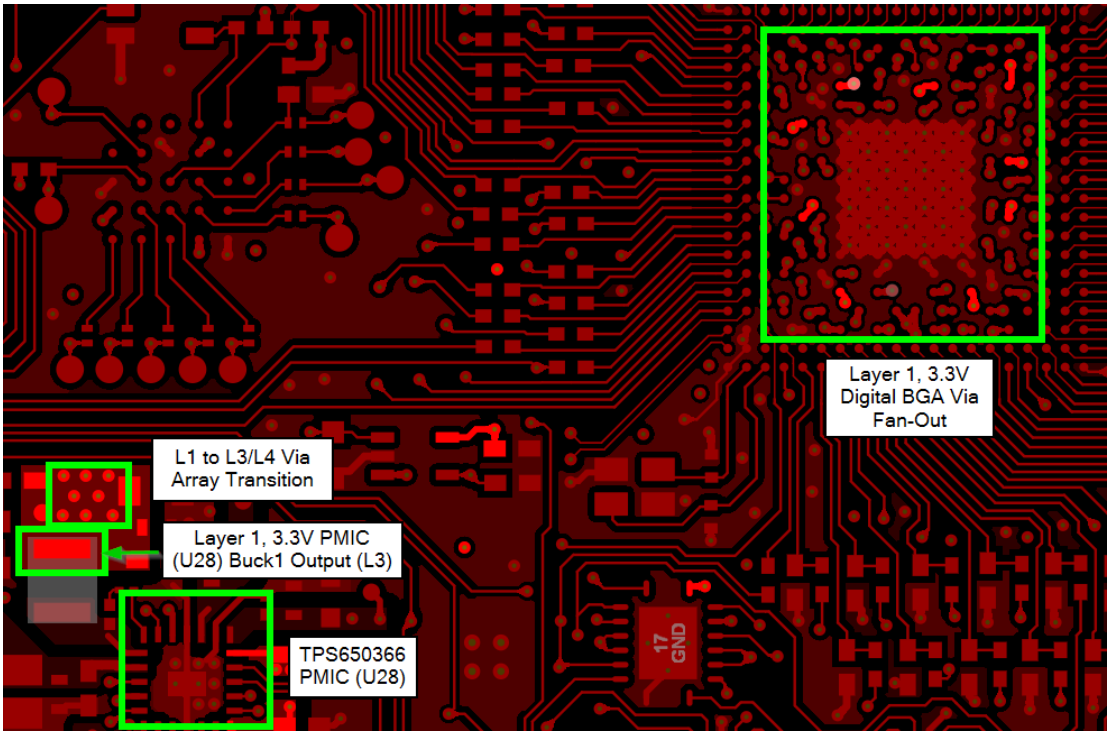


Figure 14-18. AM261x LaunchPad Excerpt – 3.3V Digital I/O BGA Pinout and PMIC Output

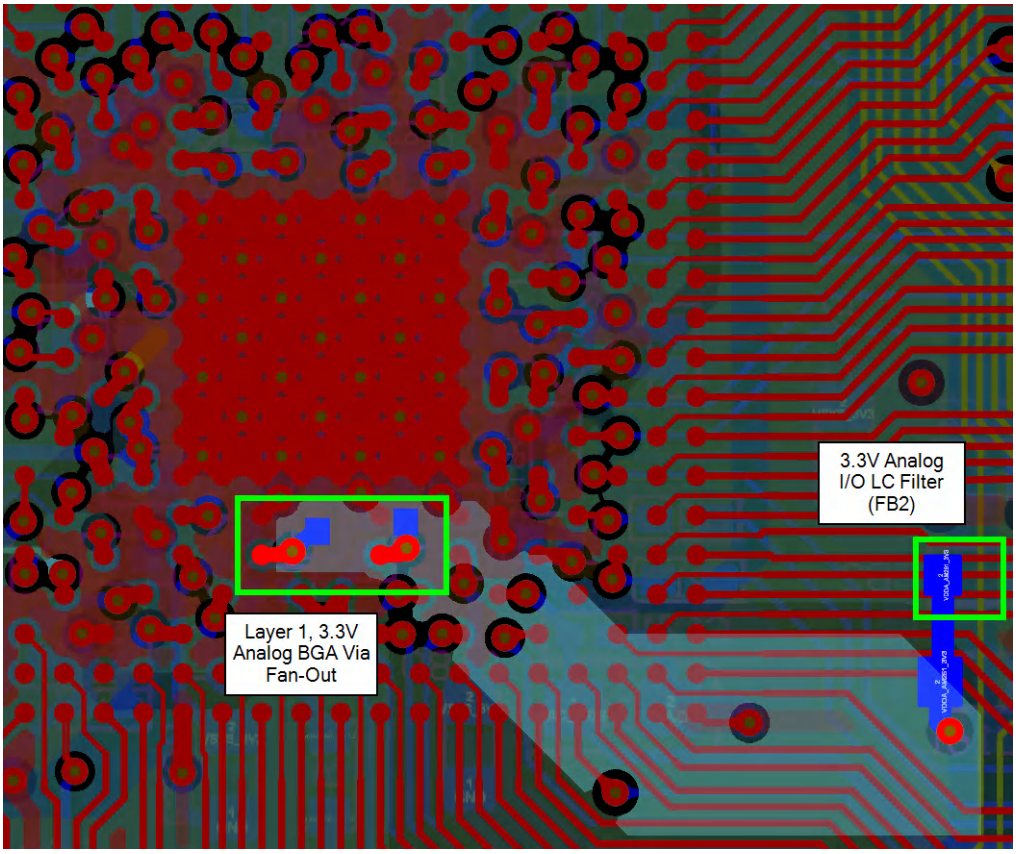


Figure 14-19. AM261x LaunchPad Excerpt - 3.3V Analog IO BGA Pinout

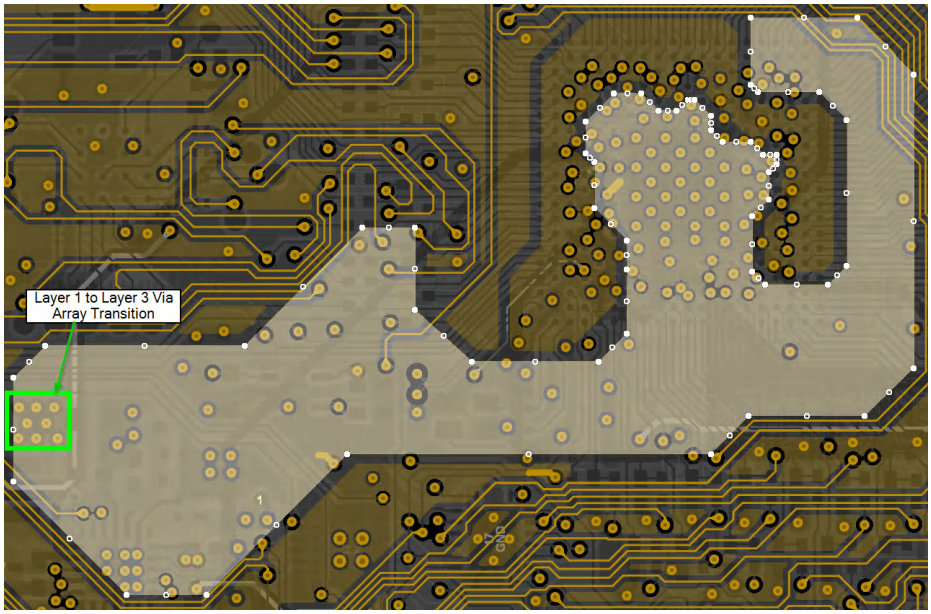


Figure 14-20. AM261x LaunchPad Excerpt – 3.3V Digital Plane on Layer 3

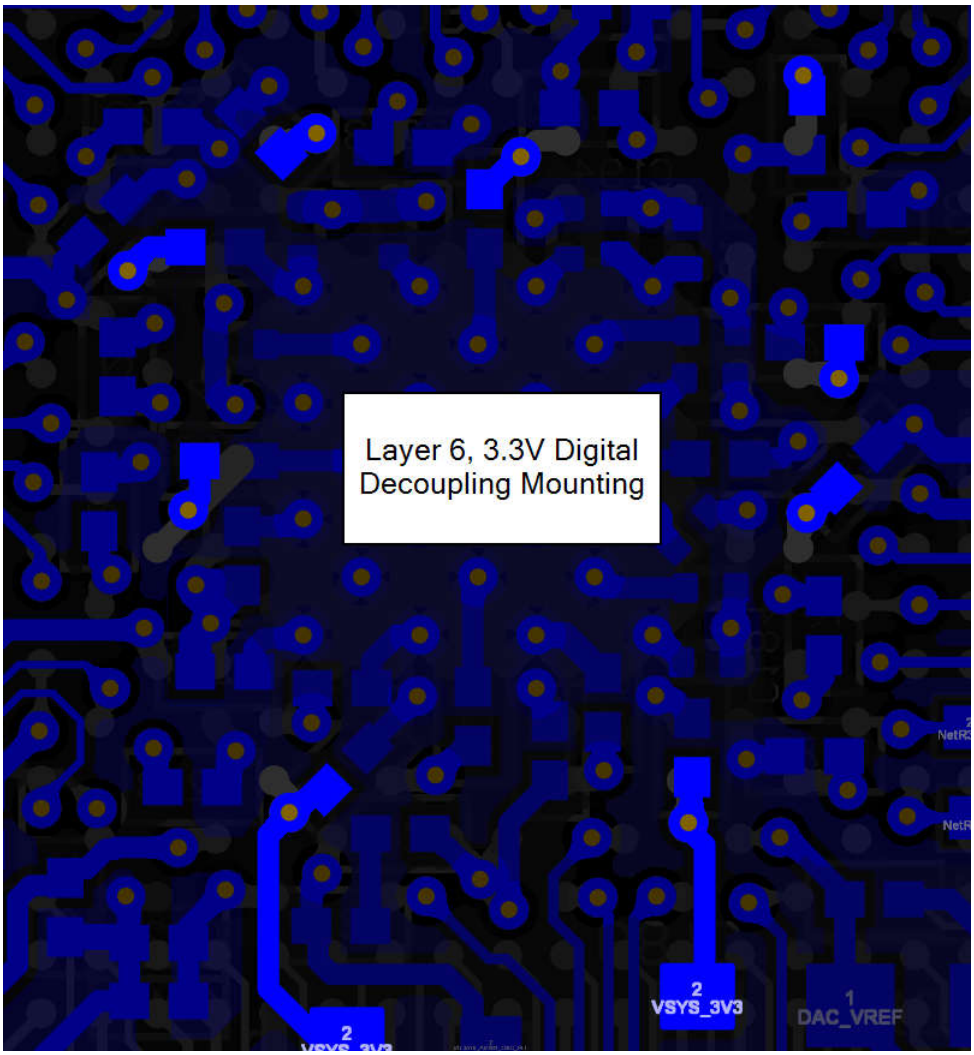


Figure 14-21. AM261x LaunchPad Excerpt – 3.3V Digital Power Decoupling Mounting, Layer 6

A 1.2V core digital power flow for a 4-layer PCB is under study and may be included in a future revision of this document.

14.4 1.8V Digital and Analog Power

This section summarizes the main elements of the 1.8V digital I/O and analog I/O power routing of the AM26x MCU devices. Both 1.8V power nets are generated from an on-chip LDO which are in turn supplied by either the 3.3V digital or 3.3V analog power nets from the PCB.

14.4.1 1.8V Key Layout Considerations - ZCZ

For ZCZ package devices, the AM263x controlCard EVM is explored as an example. Additional filtering for the local AM263x 1.8V PLL power net is done through the LC filter of ferrite-bead FL12 and associated capacitors. This is used to create an additional low-IR drop low-pass filter that attenuates any high frequency noise present on the 1.8V LDO analog output.

- Wide, minimum 15 mil traces, needs to be used for all power and ground return via fan-out.
- 1.8V digital and analog is generated from on-chip LDO and so is highly localized to the BGA pinout.
- A tightly coupled, adjacent ground return reference plane needs to be used for best transient performance and EMI coupling.
- Smaller power planes or wider traces needs to be used for minimal IR drop and best transient routing across the associated BGA pins.
- Smaller packaged, higher-frequency decoupling capacitance needs to be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible.

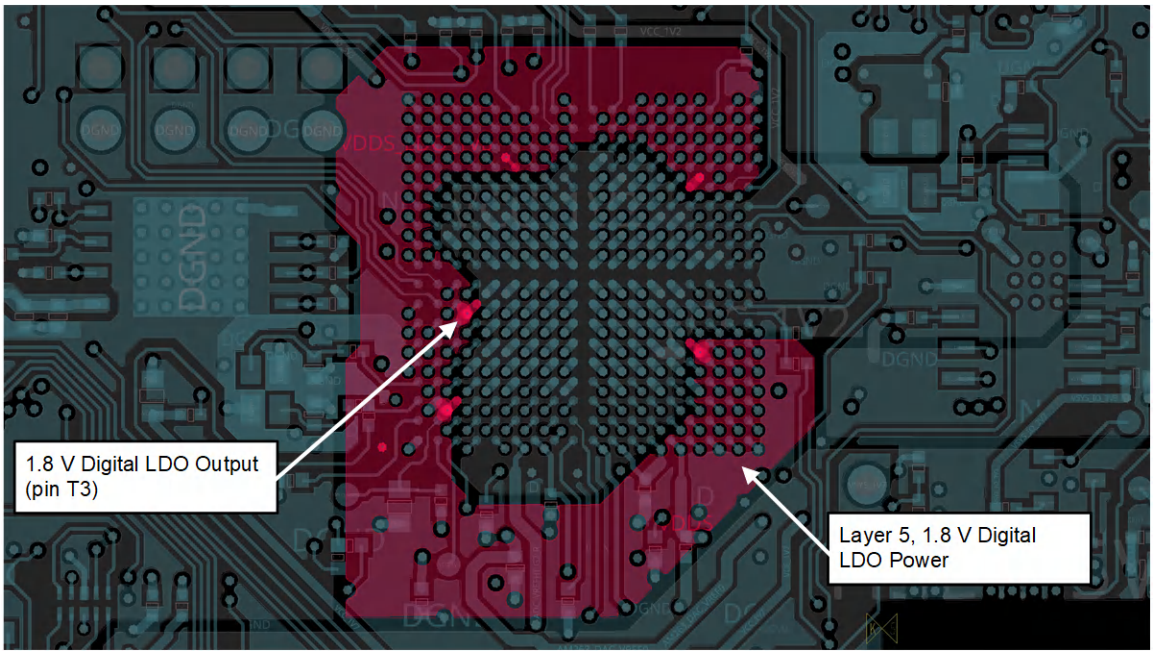


Figure 14-22. AM263x controlCARD Excerpt – 1.8V Digital Power Via Fan-Out and Plane Routing Layer 6

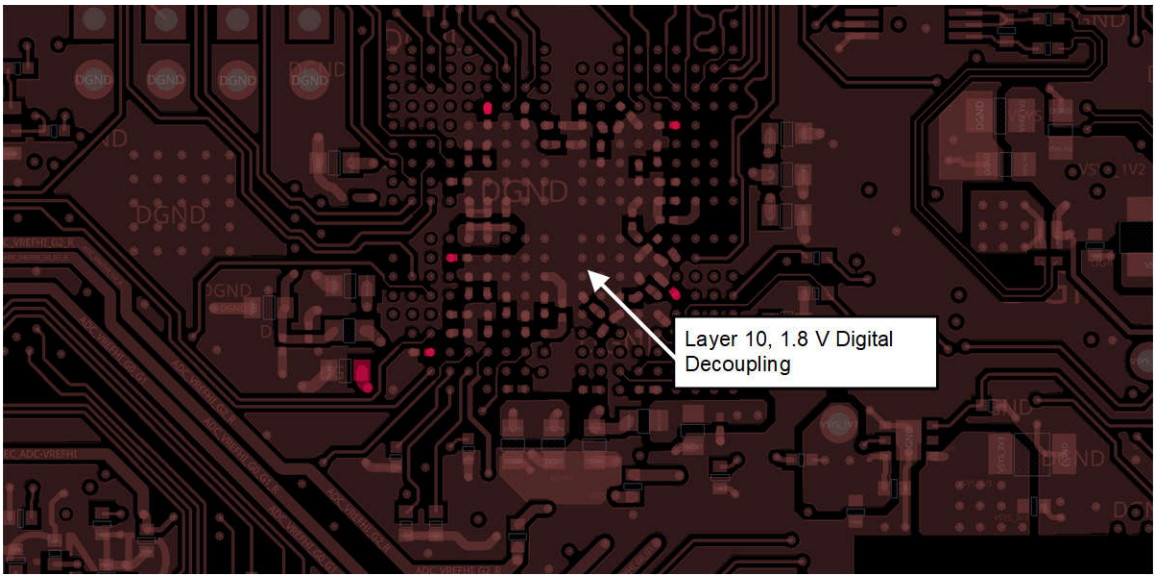


Figure 14-23. AM263x controlCARD Excerpt – 1.8V Digital Power Decoupling on Layer 10

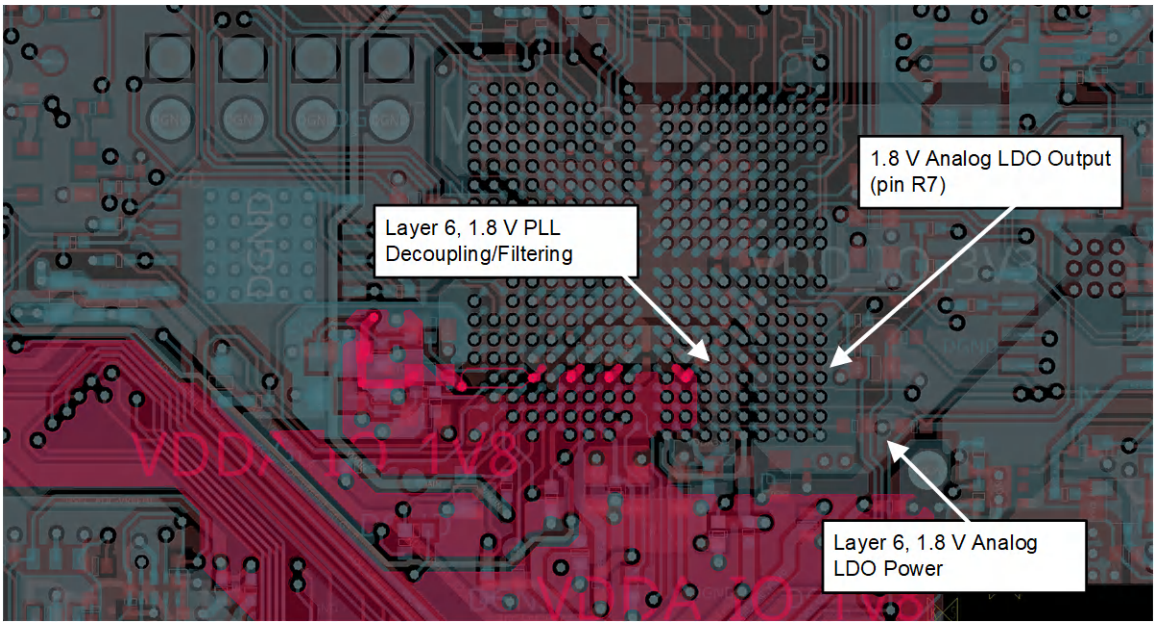


Figure 14-24. AM263x controlCARD Excerpt – 1.8V Analog Power Via Fan-Out and Plane Routing Layer 6

Note

Figure 2-13 shows an example of an unacceptable routing between the FL12 filter output and the BGA pads. The output of the FL12 filter needs to be routed as a wide trace or small plane, and not smaller traces as was done on this initial revision of the controlCard EVM.

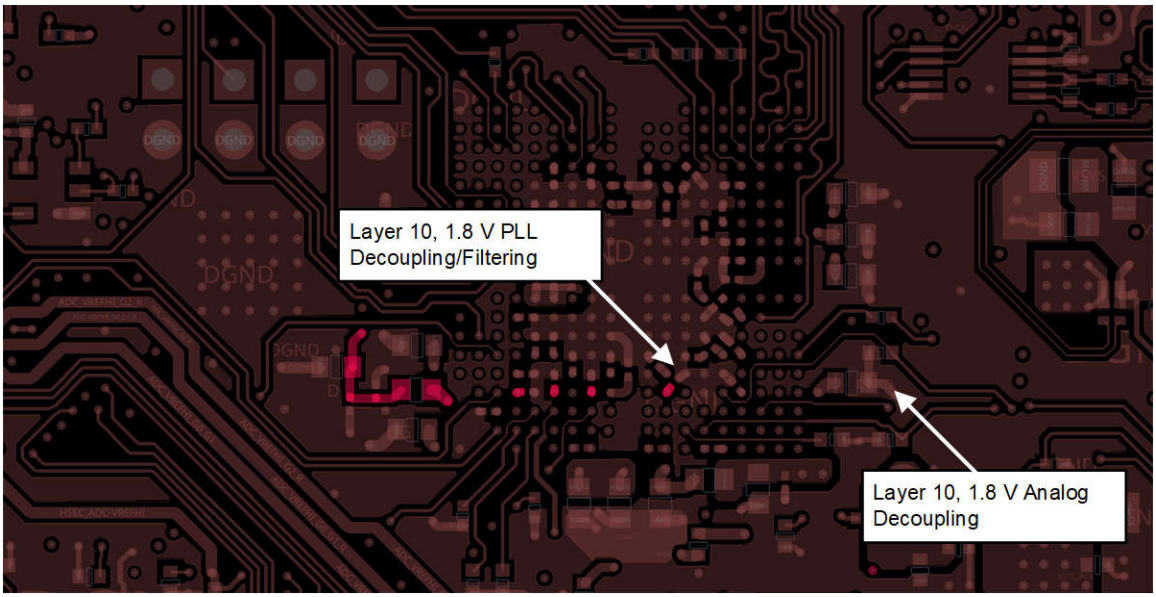


Figure 14-25. AM263x controlCARD Excerpt – 1.8V Analog Power Decoupling on Layer 10

14.4.2 1.8V Key Layout Considerations - ZFG

The 1.8V power nets on AM261x ZFG devices are explored using the AM261x LaunchPad EVM (LP-AM261). Additional filtering for the local AM261x 1.8V PLL power net is done through the LC filter of ferrite-bead FB3 and associated capacitors. This is used to create an additional low-IR drop low-pass filter that attenuates any high frequency noise present on the 1.8V LDO analog output.

- Wide 10 mil traces need to be used for all power and ground return via fan-out.
- 1.8V digital and analog is generated from on-chip LDO, and is highly localized to the BGA pinout.
- A tightly coupled, adjacent ground return reference plane needs to be used for best transient performance and EMI coupling.
- Smaller power planes or wider traces need to be used for minimal IR drop and best transient routing across the associated BGA pins.
- Smaller packaged, higher-frequency decoupling capacitance needs to be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible.

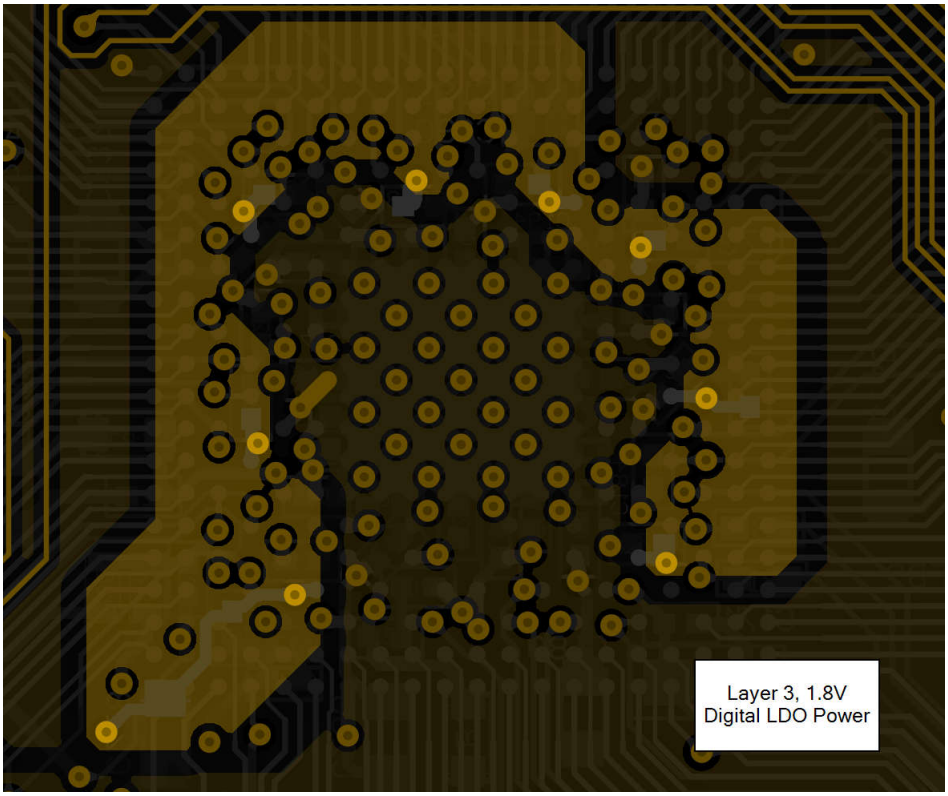


Figure 14-26. AM261x LaunchPad Excerpt – 1.8V Digital Power Via Fan-Out and Plane Routing - Layer 3

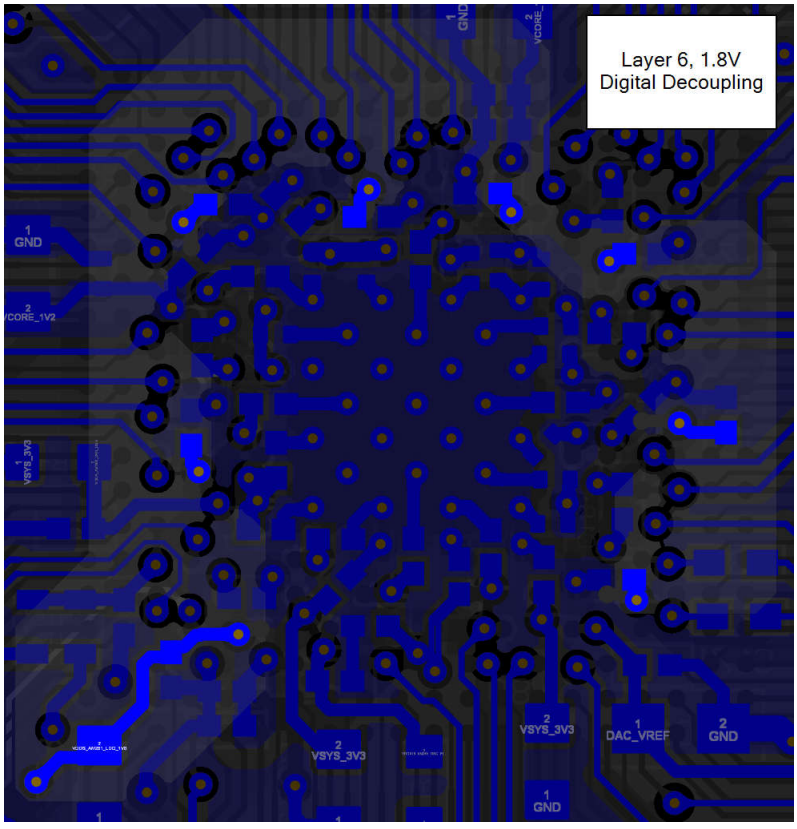


Figure 14-27. AM261x LaunchPad Excerpt – 1.8V Digital Power Decoupling on Layer 6

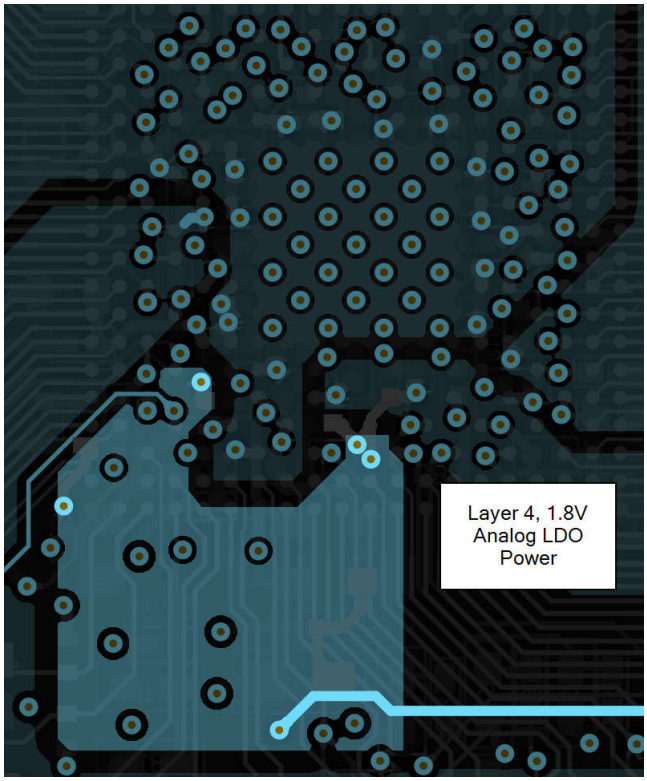


Figure 14-28. AM261x LaunchPad Excerpt – 1.8V Analog Power Via Fan-Out and Plane Routing - Layer 4

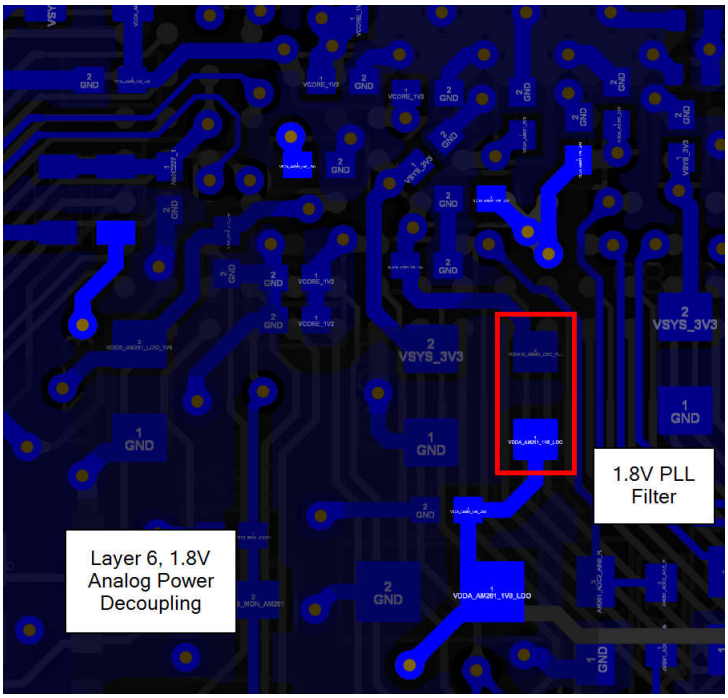


Figure 14-29. AM261x LaunchPad Excerpt – 1.8V Analog Power Decoupling on Layer 6

A 1.2V core digital power flow for a 4-layer PCB is under study and may be included in a future revision of this document.

15 Summary

The guidelines outlined in this document are essential to follow during the design phase of any AM26x-based PCB system. By strcitly adhering to the requirements, an engineer can expect their PCB system to behave properly out of the box, and avoid having to do multiple rounds of prototyping.

Once an AM26x-based custom PCB has completed the fabrication and assembly process, the engineer should refer to the AM26x Custom PCB System Getting Started Guide for initial bring-up and validation of the PCB.

16 References

AM263x

Device Documentation

1. Texas Instruments, *AM263x Sitara™ Microcontroller*, data sheet
2. Texas Instruments, *AM263x Sitara™ Microcontroller Technical Reference Manual*, technical reference manual
3. Texas Instruments, *AM263x Sitara™ Microcontroller Technical Reference Manual Addendum*, register addendum

EVM Documentation

1. Texas Instruments, LP-AM263, AM263x LaunchPad EVM
2. Texas Instruments, TMDSCNCD263, AM263x controlCARD EVM

Software Development

1. Texas Instruments, MCU-PLUS-SDK-AM263X, AM263x MCU software development kit

AM263Px

Device Documentation

1. Texas Instruments, *AM263Px Sitara™ Microcontroller*, data sheet
2. Texas Instruments, *AM263Px Sitara™ Microcontroller Technical Reference Manual*, technical reference manual
3. Texas Instruments, *AM263Px Sitara™ Microcontroller Technical Reference Manual Addendum*, register addendum

EVM Documentation

1. Texas Instruments, LP-AM263P, AM263Px LaunchPad EVM
2. Texas Instruments, TMDSCNCD263P, AM263Px controlCard EVM

Software Development

1. Texas Instruments, MCU-PLUS-SDK-AM263PX, AM263Px MCU software development kit

AM261x

Device Documentation

1. Texas Instruments, *AM261x Sitara™ Microcontrollers*, data sheet
2. Texas Instruments, *AM261x Sitara Microcontrollers Technical Reference Manual*, technical reference manual
3. Texas Instruments, *AM261x Sitara Microcontrollers Register Addendum*, register addendum

EVM Documentation

1. Texas Instruments, LP-AM261, AM261x LaunchPad EVM
2. Texas Instruments, AM261-SOM-EVM, AM261x controlSOM EVM

Software Development

1. Texas Instruments, MCU-PLUS-SDK-AM261X, AM261x MCU software development kit

Software Development Tools

1. Texas Instruments, System Configuration Tool (SYSCONFIG)
2. Texas Instruments, Code Composer Studio IDE

General HW Design Resources

1. MIPI Alliance, Recommendation for Debug and Trace Connectors, MIPI Debug & Trace Connector Recommendations, white papter
2. Texas Instruments, JTAG Connectors and Pinout, webpage
3. Texas Instruments, Sitara MCU Thermal Design, application note
4. Texas Instruments, High-speed Interface Layout Guidelines, application note

17 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2023) to Revision C (January 2025)	Page
• [Integrated PMIC Power Solution] Added details for using TPS650360 with AM261x	10
• [eFuse Power] Updated for AM261x and added figure to show on-chip supply for VPP	22
• [Resets] Add AM261x information and PMIC-specifc reset logic information	27
• [SOP Signal Implementation] Added AM261x package data	30
• [ROM OSPI/QSPI Boot Requirements] Added AM261x information and links	36
• [JTAG Emulators and Trace] Add AM261x info, additional EVM information for the MIPI-60	37
• [USB] Added new section for AM261x	38
• [Trace Length Matching] Added new section	42
• [Layer Stackup] Added layer stackup for AM261x LaunchPad and 4-layer stackup for AM261x-ZFG/ZNC package sizes	44
• [Vias] Deleted incorrect information on via-in-pad construction	49
• [Vias] Added AM261x EVM information	49
• [BGA Power Fan-Out and Decoupling Placement] added AM261x package information	49

Changes from Revision A (June 2023) to Revision B (November 2023)	Page
• [Abstract] Added AM263Px throughout the document	1
• [Introduction] Added example system block diagram showing PMIC based power design option	3
• [Integrated PMIC Power Solution] Updated to reference TMDSCNCD263P PMIC solution	10
• [Power Decoupling and Filtering] Added schematic example for ADC_VREFHI_G3 and ADC_VREFLO_G3 on AM263Px Sensor package	11
• [eFuse Power] updated to include AM263Px internally sourcing VPP	22
• [SOP Signal Implementation] Added AM263P Bootmodes	30
• [OSPI/QSPI Memory Implementation] Added AM263Px and OSPI information	32
• [Analog Peripherals] Added Analog Peripherals section	43

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