Application Note

AM62x, AM62Lx DDR Board Design and Layout Guidelines

ABSTRACT

This application note is to describe how to make the DDR system implementation of AM62x, AM62Lx processor board designs straightforward for all designers. The requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies TI supports. The topics in this document include the board layout guidelines, board stackup, supported implementations, schematics, component placement, and trace length matching targets.

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1 Overview

The AM62x, AM62Lx processors support two different types of DDR memories: DDR4 and LPDDR4. This allows customer board designs to be implemented with the memory type that best meets the target market at the lowest possible DDR SDRAM cost. This document has generic information that is applicable to both DDR4 and LPDDR4, as well as separate sections that are specific to each supported DDR memory type.

Note

To facilitate software configuration of the DDRSS, use the DDR Configuration Tool in SysConfig (*https://dev.ti.com/sysconfig*).

1.1 Board Designs Supported

The goal of this document is to make the DDR system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. At this time, TI does not provide timing parameters for the processor’s DDR PHY interface.

The PCB design work (design, layout, and fabrication) is expected to be performed and reviewed by a highly knowledgeable high-speed PCB designer. Problems such as impedance discontinuities when signals cross a split in a reference plane can be detected visually by those with the proper experience.

TI only supports board designs using DDR4 and LPDDR4 memory that follow the guidelines in this document. These guidelines are based on well-known transmission line properties for copper traces routed over a solid reference plane. Declaring insufficient PCB space does not allow routing guidelines to be discounted.

1.2 General Board Layout Guidelines

To verify good signaling performance, the following general board design guidelines must be followed:

- Always follow TI's example layouts and EVM designs as close as possible. If concepts or routing strategies are not understood, then ask questions on E2E.
- All signals need ground reference (strongly suggest on both sides).
- Avoid crossing plane splits in the signal reference planes.
- Use the widest trace that is practical between decoupling capacitors and memory modules.
- Minimize inter-symbol interference (ISI) by keeping impedances matched. This is especially true for any *T-branch* signals where trace widths are adjusted to match trace impedance.
- Minimize crosstalk by isolating sensitive signals, such as strobes and clocks, and by using a proper PCB stack-up.
- Avoid return path discontinuities by adding vias or capacitors whenever signals change layers and reference planes.
- Minimize reference voltage noise through proper isolation and proper use of decoupling capacitors on the reference input pins on the SDRAMs.
- Keep the signal routing stub lengths as short as possible.
- Add additional spacing for clock and strobe nets to minimize crosstalk.
- Maintain a common ground (also called VSS) reference for all signals and for all bypass and decoupling capacitors.
- Consider the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.
- Via-to-via coupling can be significant part of PCB-level crosstalk. Dimension and pitch of vias is important. For high speed interfaces, consider GND shielding vias. This via coupling is one factor for recommending data signals be routed on layers closest to processor.
- Via stubs affect signal integrity. Via back-drilling can improve signal integrity, and is required in some instances.

For more information, see the *High-Speed Interface Layout Guidelines* application note. This provides additional general guidance for successful routing of high-speed signals.

1.3 PCB Stack-Up

The minimum stack-up for routing the DDR interface is a six-layer stack up. However, this can only be accomplished on a board with routing room with large keep-out areas. Additional layers are required if:

- The PCB layout area for the DDR Interface is restricted, which limits the area available to spread out the signals to minimize crosstalk.
- Other circuitry must exist in the same area, but on layers isolated from the DDR routing.
- Additional planes layers are needed to enhance the power supply routing or to improve EMI shielding.

Board designs that are relatively dense require 10 or more layers to properly allow the DDR routing to be implemented such that all rules are met.

DDR signals with the highest frequency content (such as data or clock) must be routed adjacent to a solid VSS reference plane. Signals with lower frequency content (such as address) can be routed adjacent to either a solid VSS or a solid VDDS_DDR reference plane. If a VDDS_DDR reference plane is used, bypass capacitors must be implemented near both ends of every route to provide a low-inductance, AC path to ground for these routes. Similarly, when multiple VSS reference planes exist in the DDR routing area, stitching vias must be implemented nearby wherever vias transfer signals to a different VSS reference plane. This is required to maintain a low-inductance return current path.

TI strongly recommends all DDR signals be routed as strip-line. Some PCB stack-ups implement signal routing on two adjacent layers. This is acceptable only as long as the routing on these layers is perpendicular and does not allow for broad-side coupling. Severe crosstalk occurs on any trace routed parallel to another trace on an adjacent layer, even for a short distance. Also, DDR signal routing on two adjacent layers is only allowed when implementing offset stripline routing, where the distance between the adjacent routing layers is more than 3x the distance from the traces to the adjacent reference plane.

Table 1-1. PCB Stack-up Specifications

Number	Parameter	MIN	TYP	MAX	UNIT
PS1	PCB routing plus plane layers	6			
PS2	Signal routing layers	3			
PS3	Full VSS reference layers under DDR routing region (1)	1			
PS4	Full VDDS_DDR power reference layers under the DDR routing region (1)	1			
PS5	Number of reference plane cuts allowed within DDR routing region (2)			0	
PS6	Number of layers between DDR routing layer and reference plane (3)			0	
PS7	PCB routing feature size		4		Mils
PS8	PCB trace width, w		4		Mils
PS9	Single-ended impedance		40		Ω
PS10	Differential impedance		80		Ω
PS11	Impedance control (4)	Z-10%	Z	Z+10%	Ω

(1) Ground reference layers are preferred over power reference layers. Return signal vias need to be near layer transitions. When using power reference layers, include bypass caps to accommodate reference layer return current, as the trace routes switch routing layers.
(2) No traces must cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths, which can lead to excessive crosstalk and EMI radiation. Beware of reference plane voids caused by via antipads, as these also cause discontinuities in the return current path.
(3) Reference planes are to be directly adjacent to the signal layer, to minimize the size of the return current loop.
(4) Z is the nominal singled-ended impedance selected for the PCB specified by PS9 and PS10.

1.4 Bypass Capacitors

1.4.1 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR SDRAMs and other circuitry. Table 1-2 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Table 1-2 only covers the bypass needs of the SoC's DDR PHY. Additional bulk bypass capacitance can be needed for other circuitry. For any additional decoupling requirements for the SDRAM devices, see the manufacturer's data sheet.

Table 1-2. Bulk Bypass Capacitors

Number	Parameter	MIN (2)	MAX	UNIT
1	VDDS_DDR bulk bypass capacitor count (1)	1		Devices
2	VDDS_DDR bulk bypass total capacitance	22		µF

(1) These capacitors need to be placed near the devices that are bypassing, but preference needs to be given to the placement of the high-speed (HS) bypass capacitors and DDR signal routing.
(2) The capacitor recommendations in this guide reflect only the needs of this processor. For determining the appropriate decoupling capacitor arrangement for the memory device, see the guidelines of the memory vendor.

1.4.2 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR interface operation. This is particularly important to minimize the parasitic series inductance of the HS bypass capacitors to VDDS_DDR and the associated ground connections. Table 1-3 contains the specification for the HS bypass capacitors and for the power connections on the PCB. Generally speaking, TI recommends:

- Fitting as many HS bypass capacitors as possible.
- Minimizing the distance from the bypass capacitor to the pins and balls being bypassed.
- Using the smallest physical sized ceramic capacitors possible with the highest capacitance readily available.
- Connecting the bypass capacitor pads to the vias using the widest traces possible and using the largest via hole size possible.
- Minimizing via sharing. Note the limits on via sharing shown in Table 1-3.
- Using three-terminal capacitors instead of two terminal capacitors. Three-terminal capacitors provide lower loop inductance, and one three-terminal capacitor can take the place of multiple two-terminal capacitors, further optimizing loop inductance.

For any additional SDRAM requirements, see the manufacturer's data sheet.

Table 1-3. High-Speed Bypass Capacitors

Parameter	MIN	TYP	MAX	UNIT
HS bypass capacitor package size (1)		0201	0402	Mils
Distance, HS bypass capacitor to processor being bypassed (2) (3) (4)			150	Mils
Processor HS bypass capacitor count per VDDS_DDR rail(5)	5			Devices
Processor HS bypass capacitor total capacitance per VDDS_DDR rail(5)	1.4			uF
Number of connection vias for each device power/ground ball	1			Vias
Trace length from processor power/ground ball to connection via (2)		35	70	Mils
Distance, HS bypass capacitor to DDR device being bypassed (6)			150	Mils
DDR device HS bypass capacitor count	Refer to DDR manufacturer guidelines			
Number of connection vias for each HS capacitor (7) (8)	2			Vias
Trace length from bypass capacitor to connection via (2) (8)		35	100	Mils
Number of connection vias for each DDR device power/ground ball	1			Vias
Trace length from DDR device power/ground ball to connection via (2)		35	60	Mils

(1) LxW, 10-mil units, that is, a 0402 is a 40x20-mil surface-mount capacitor.
(2) Closer or shorter is preferable.
(3) Measured from the nearest processor power or ground ball to the center of the capacitor package.
(4) Three of these capacitors need to be located underneath the processor, among the cluster of VDDS_DDR balls.
(5) Decoupling capacitor counts and capacitor values need to be derived from power aware PCB simulations. The PCB designer has a responsibility to make sure that any design meets the provided PDN targets.

(6) Measured from the DDR device power or ground ball to the center of the capacitor package. Refer to the guidance from the SDRAM manufacturer.

(7) An additional HS bypass capacitor can share the connection vias only if the bypass is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

(8) An HS bypass capacitor can share a via with a DDR device mounted on the same side of the PCB. A wide trace must be used for the connection, and the length from the capacitor pad to the DDR device pad needs to be less than 150 mils.

1.4.3 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR signals hopping from one signal layer to another, resulting in the reference plane changing from VDDS_DDR to VSS. The bypass capacitor here provides a path for the return current to hop planes along with the signal. Use as many of these return current bypass capacitors as possible – up to one per signal via. Because these are returns for signal current, the via size for these bypass capacitors can be the smaller via used for signal routing.

1.5 Velocity Compensation

Because portions of the DDR signal traces are microstrip (top and bottom layers), while the majority of the trace segment length is stripline (internal layers), and because there is a wide variation in the proportion of track length routed as microstrip or stripline, the length or delay matching process must include a mechanism for compensating for the velocity delta between these two types of PCB interconnects. A compensation factor of 1.1 has been specified for this purpose by JEDEC. All microstrip segment lengths are to be divided by 1.1 before summation into the length matching equation. The resulting compensated length is termed the *stripline equivalent length*. While some amount of residual velocity mismatch skew remains in the design, the process is a substantial improvement over simple length matching.

2 DDR4 Board Design and Layout Guidance

2.1 DDR4 Introduction

DDR4 board designs are similar to DDR3 board designs. Fly-by routing is required, similar with DDR3, and thus leveling is required. To achieve higher data rates with DDR4, there are several enhancements added to the interface specification that must be accommodated by both the SDRAM and the processor's interface (PHY). The enhancements that affect the board interconnect and layout are listed below:

- Addition of ACT_n pin – This pin provides signaling to allow the pins previously called Command pins (RAS_n, CAS_n and WE_n) to be used as additional address pins. These pins behave as row address pins when ACT_n is low and as command pins when ACT_n is high. This is valid only when CS_n is low.
- Removal of one BA (Bank Address) pin and addition of 2 BG (Bank Group) pins – This adds flexibility with accesses similar to DDR3, but with 16 banks bundled in four bank groups of four banks each. This results in additional timing parameters, because adjacent accesses within a bank group are faster than adjacent accesses to another bank group. Successive accesses to locations within a single bank are the fastest option.
- Addition of PAR (Parity) and ALERT_n pins (use is optional) – The PAR pin supplies parity monitoring for the command and address pins using even parity from the controller to the SDRAM. ALERT_n is the indicator (open-drain output) from the SDRAMs that indicate when a parity error has been detected.
- Change to POD termination – Pseudo-Open Drain (POD) output buffers are implemented rather than traditional SSTL push-pull outputs. This allows the data bit termination, ODT, to go to the I/O power rail, VDDQ, rather than to the mid-level voltage, VTT. Power consumption can be reduced, because only driving a bit low draws current.
- Addition of DBI – Data bus invert (DBI) is a feature that allows the data bus to be inverted whenever more than half of the bits are zero. This feature can reduce active power and enhance the data signal integrity when coupled with POD termination.
- Addition of a VPP power input – The VPP power supply (2.5V) provides power to the internal word line logic. This voltage increase allows the SDRAM to reduce overall power consumption.
- Separation of data VREF from address and control VREF – The data reference voltage, VREFDQ, is now internally generated both within the SDRAM and within the PHY. This can be programmed to various levels to provide the optimum sampling threshold. The optimum threshold varies based on the ODT impedance chosen, the drive strength, and the PCB track impedance. The address and control reference voltage, VREFCA, is a mid-level reference voltage, and is the same on DDR3.

Note

These features are not supported on all devices. Refer to the data sheet and the *DDR Subsystem (DDRSS)* chapter in the Technical Reference Manual for the associated device.

2.2 DDR4 Device Implementations Supported

There are several possible combinations of SDRAM devices supported by the DDR4 EMIF. Table 2-1 lists the supported device combinations. The SDRAMs used in each combination must be identical; the SDRAMs must have the same part number.

Table 2-1. Supported DDR4 SDRAM Combinations

SDRAM Bus Width	Number of SDRAM Devices	Number of Dies in Package	BG Signals	Number of Ranks (CS Signals)	Schematic	Max Addressable Range
x16	1	1	BG0	1 (CS0_n)	Figure 2-1	4GBytes
x16	1	2	BG[1:0]	1 (CS0n) or 2 (CS[1:0]_n)	Figure 2-2 (VTT optional)	4GBytes (1 rank), 8GBytes (2 ranks)
x8	2	1	BG[1:0]	1 (CS0n) or 2 (CS[1:0]_n)	Figure 2-2 (with VTT)	4GBytes (1 rank), 8GBytes (2 ranks)

Note

ECC is supported on the DDR4 interface. Unlike traditional ECC interfaces, which require dedicated memory pins and devices, ECC is supported inline. The ECC system impact is in interface bandwidth and overall memory density, as ECC data is stored alongside non-ECC data. Max addressable range are reduced if ECC is enabled. See the **device TRM** for more details.

Note

Refer to the *Terminal Configuration and Functions* section of the **data sheet** for a list of DDR pins available. For example, AM62Lx does not support 2 ranks.

2.3 DDR4 Interface Schematics

This section discusses implementations (also called topologies) using x16 and x8 SDRAM devices. This section does not discuss recommendations for implementations that support low-power operation, such as when the SDRAM is held in self-refresh and the processor is powered off. This section also does not discuss the DDR-less implementations. These options are under study and can be supported in future versions of this document.

Only implementations with 16-bit data width are supported. Implementations with only 8-bits of data are not supported.

2.3.1 DDR4 Implementation Using 16-Bit SDRAM Devices

The DDR4 interface schematics vary, depending upon the width of the DDR4 SDRAM devices used and the width of the EMIF bus implemented. General connectivity is straightforward and consistent between the implementations. 16-bit SDRAM devices look like two 8-bit devices. Figure 2-1 shows the schematic connections for a 16-bit interface using a single x16 SDRAM.

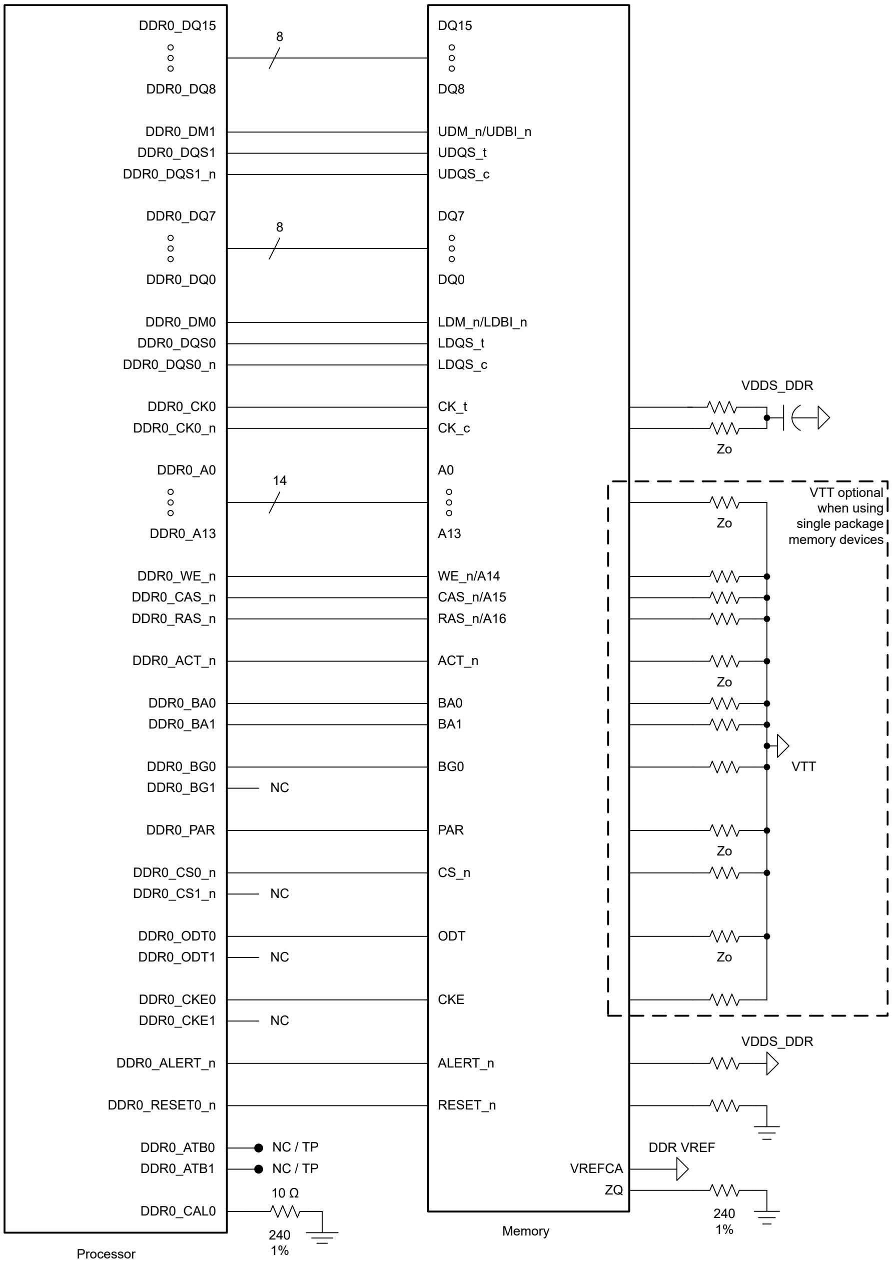


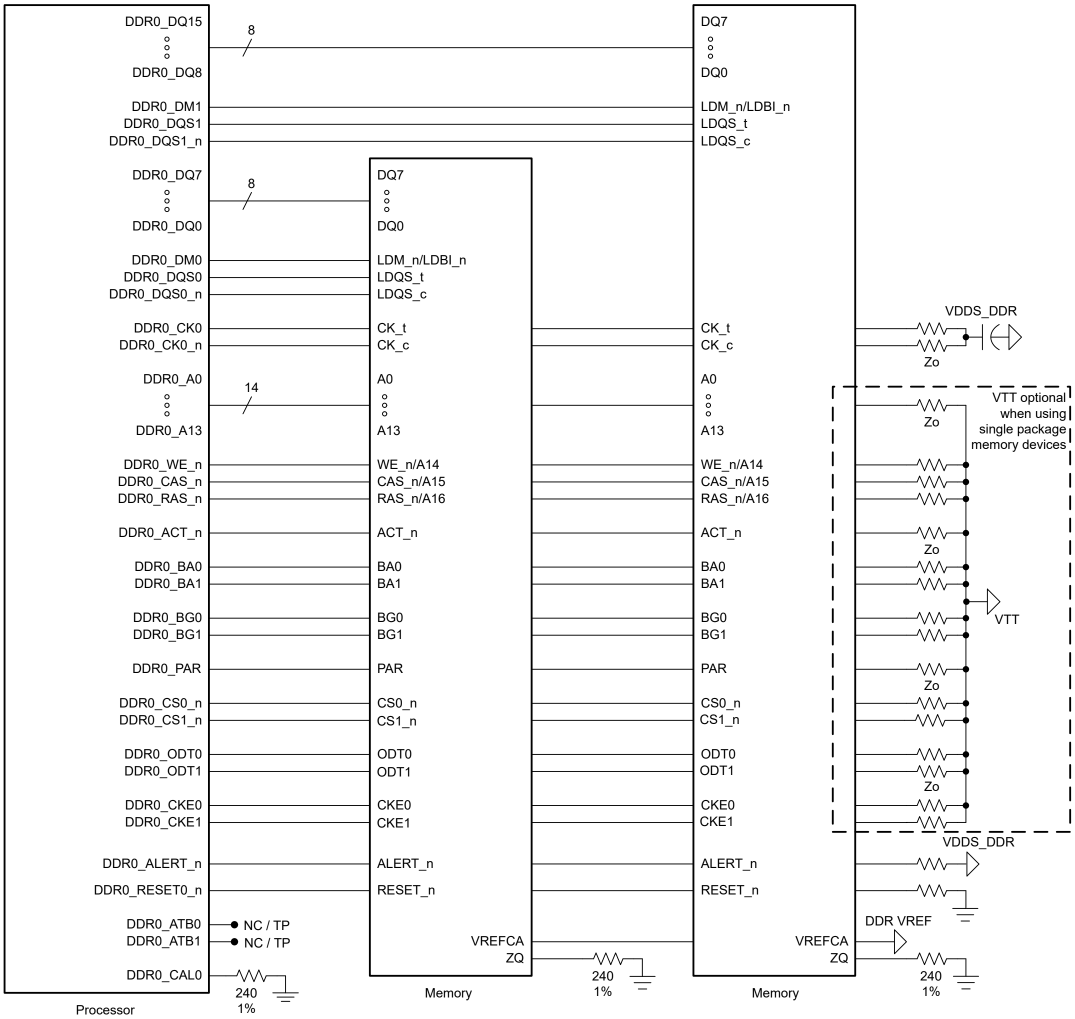
Figure 2-1. 16-Bit, Single-Rank DDR4 Implementation Using x16 SDRAM

1. When designing with VTT regulator (LDO), which can source and sink current, decoupling capacitors (minimum of one capacitor (1.0uF value) must be used for every two termination resistors) must be used to minimize the effect of VTT supply noise. Refer to the AM64x GP EVM for reference
2. Zo value for resistors is 30-47ohm. Resistor value must closely match trace impedance.
3. VTT is optional on address and control signals when using single package memory devices, but termination as shown on CK0/CK0_n is always required
4. DDR_VREF is supplied by the VTT regulator. When VTT is not used, VREFCA needs to be connected to a voltage divider. Consult the EVM schematic for an example of the voltage divider implementation.
5. An external 240Ω ±1% resistor must be connected between the DDR0_CAL0 pin and VSS. The maximum power dissipation for the resistor is 5.2mW. No external voltage must be applied to the DDR0_CAL0 pin. Tolerance of ±1% required throughout life of component or product.
6. RESET_n shall have an external 10k pull-down resistor to control RESET low until the DDR controller drives the signal. RESET_n has no length matching requirement.

2.3.2 DDR4 Implementation Using 8-Bit SDRAM Devices

Figure 2-2 shows the schematic connections for a dual rank,16-bit interface using two x8 devices.

Use memory devices with two dies in one package to achieve higher density designs. The connection looks similar to Figure 2-2, except the two x8 memories are in one package, so VTT implementation is not necessary. Make sure to connect BG[1:0] when using these devices, as the internal implementation is still using two x8 memories.



1. When designing with VTT regulator (LDO), which can source and sink current, decoupling capacitors (minimum of one capacitor (1.0uF value) must be used for every two termination resistors) must be used to minimize the effect of VTT supply noise. Refer to the AM64x GP EVM for reference.
2. Zo value for resistors is 30-47ohm. Resistor value must closely match trace impedances.
3. VTT is optional on address and control signals when using single package memory devices, but termination as shown on CK0/CK0_n is always required.
4. DDR_VREF is supplied by the VTT regulator. When VTT is not used, VREFCA needs to be connected to a voltage divider. Consult the EVM schematic for an example of the voltage divider implementation.
5. For single-rank designs, CS1_n, ODT1, and CKE1 can be left unconnected
6. Single package memories with two x8 dies do not require VTT.
7. An external 240Ω ±1% resistor must be connected between the DDR0_CAL0 pin and VSS. The maximum power dissipation for the resistor is 5.2mW. No external voltage must be applied to the DDR0_CAL0 pin. Tolerance of ±1% required throughout life of component or product.
8. RESET_n shall have an external 10k pull-down resistor to control RESET low until the DDR controller drives the signal. RESET_n has no length matching requirement.

Figure 2-2. 16-Bit, Dual-Rank DDR4 Implementation Using x8 SDRAMs

2.4 Compatible JEDEC DDR4 Devices

Table 2-2 shows the parameters of the JEDEC DDR4 devices compatible with this interface. Generally, the DDR4 interface is compatible with all JEDEC-compliant DDR4 SDRAM devices in x8 or x16 widths.

Table 2-2. Compatible JEDEC DDR4 Devices

Number	Parameter	MIN	MAX	UNIT
1	JEDEC DDR4 data rate(2) (3)		1600	MT/s
2	JEDEC DDR4 device bit width	x8	x16	Bits
3	JEDEC DDR4 device count(1)	1	2	Devices

(1) For valid DDR4 device configurations and device counts, see DDR4 Interface Schematics.
(2) For supported data rates, see the device-specific data manual.
(3) SDRAMs in faster speed grades can be used provided the SDRAMs are properly configured to operate at the supported data rates. Faster speed grade SDRAMs can have faster edge rates, which can affect signal integrity. SDRAMs with faster speed grades must be validated on the target board design.

2.5 Placement

Figure 2-3 shows the required placement for the processor and the DDR4 devices. The dimensions for this figure are defined in Table 2-3. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space.

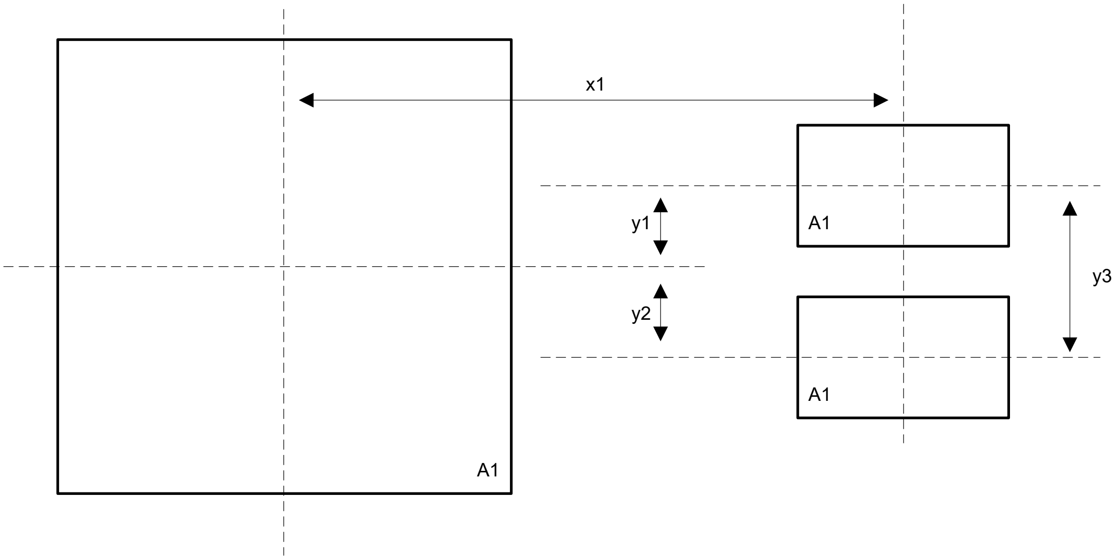


Figure 2-3. DDR4 Placement Specifications

Table 2-3. Placement Parameters

Number	Parameter	MIN	MAX	UNIT
1	x1		2000	Mils
2	y1		500	Mils
3	y2		1000	Mils
4	y3		750	Mils

2.6 DDR4 Keepout Region

The region of the PCB used for DDR4 circuitry must be isolated from other signals. The DDR4 keepout region is defined for this purpose and is shown in Figure 2-4. The size of this region varies with the placement and DDR routing. Non-DDR4 signals must not be routed on the DDR signal layers within the DDR4 keepout region. Non-DDR4 signals can be routed in this region only if the signals are routed on other layers separated from the DDR signal layers by a ground layer. No breaks are allowed in the reference ground layers in this region. In addition, a solid VDDS_DDR power plane exists across the entire keepout region.

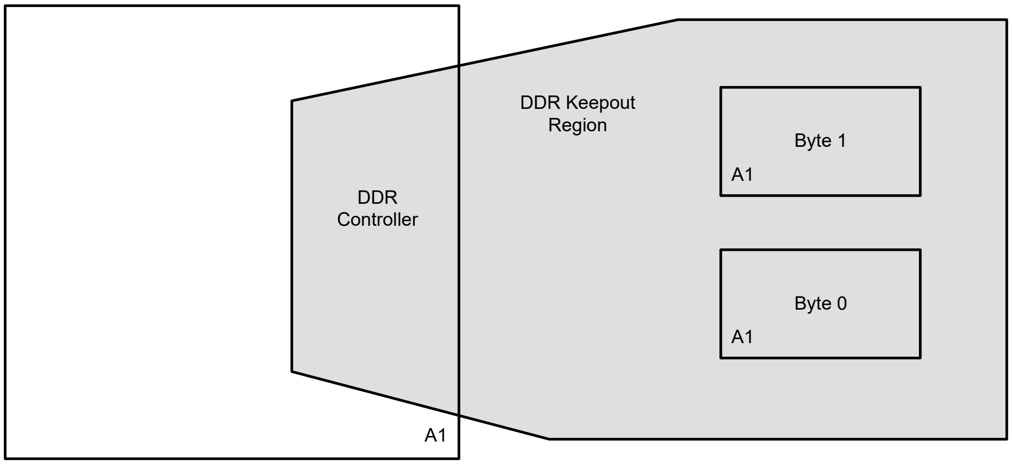


Figure 2-4. DDR4 Keepout Region

2.7 DBI

DBI is recommended to reduce supply/ground noise and to improve the data eye. Therefore the DDR Subsystem Configuration Tool enables Read DBI as a default for DDR4 configurations.

2.8 VPP

VPP is a new supply input on DDR4 SDRAMs. This supply must provide an average of less than 5mA in active and standby modes and 10mA to 20mA during refresh. There is not a constant current draw during refresh. The VPP power supply and decoupling capacitors must be able to supply short bursts of current up to 60mA during this time.

2.9 Net Classes

Routing rules are applied to signals in groups called net classes. Each net class contains signals with the same routing requirements. This simplifies the implementation and compliance of these routes. Table 2-4 lists the clock net classes for the DDR4 interface. Table 2-5 lists the signal net classes, and associated clock net classes, for signals in the DDR4 interface. These net classes are then linked to the termination and routing rules that follow.

Table 2-4. Clock Net Class Definitions

Clock Net Class	Processor Pin Names
CK	DDR0_CK0 / DDR0_CK0_n
DQS0	DDR0_DQS0 / DDR0_DQS0_n
DQS1	DDR0_DQS1 / DDR0_DQS1_n

Table 2-5. Signal Net Class Definitions

Signal Net Class	Associated Clock Net Class	Processor Pin Names
ADDR_CTRL	CK	DDR0_A[13:0], DDR0_WE_n, DDR0_CAS_n, DDR0_RAS_n, DDR0_ACT_n, DDR0_BA0, DDR0_BA1, DDR0_BG0, DDR0_BG1, DDR0_PAR, DDR0_CS0_n, DDR0_CS1_n, DDR0_ODT0, DDR0_ODT1, DDR0_CKE0, DDR0_CKE1
BYTE0	DQS0	DDR0_DQ[7:0], DDR0_DM0
BYTE1	DQS1	DDR0_DQ[15:8], DDR0_DM1

2.10 DDR4 Signal Termination

Signal terminators are required on designs with multiple memory devices for the CK and ADDR_CTRL net classes. For designs with a single memory package, VTT termination is optional on the ADDR_CTRL net class (termination is still required for the differential clock signals CK0 and CK0_n). This is shown in the schematic figures in DDR4 Interface Schematics. The data group nets are terminated by ODT in the processor and SDRAM memories, and thus the data group PCB traces must be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

2.11 VREF Routing

JEDEC defines two reference voltages that are used with DDR4 memory interfaces. These are VREFDQ and VREFCA. VREFDQ is the reference voltage used for the data group nets during reads and writes. VREFCA is the reference voltage used for command and address inputs to the SDRAMs. DDR4 SDRAMs generate VREFDQ internally. Similarly, the DDR4 PHY of the processor generates VREFDQ internally. The VREFCA reference voltage must be generated on the board and propagated to all of the SDRAMs. VREFCA is intended to be 50% of the DDR4 power supply voltage and is typically generated with the DDR4 VTT power supply. VREFCA must be routed as a nominal 20-mil wide trace with 0.1μF bypass capacitors near each device connection. Narrowing the VREF trace is allowed to accommodate routing congestion for short lengths near endpoints.

When a VTT power supply is not used, VREFCA must be generated using a voltage divider circuit. Consult the EVM schematics for examples of how the voltage divider circuit is implemented. Make sure high precision resistors (1% tolerance) are using for the voltage divider.

2.12 VTT

As with VREFCA, the nominal value of the VTT supply is 50% of the DDR4 supply voltage. Unlike VREFCA, the VTT supply is expected to source and sink current; specifically the termination current for the ADDR_CTRL net class Thevenin terminators. VTT is needed at the end of the address and control bus and needs to be routed as a power sub-plane. VTT must be bypassed with decoupling capacitors near the terminator resistors. VTT is optional if the design contains only one memory device (that is, all signals are point to point).

2.13 POD Interconnect

Prior to DDR4, the output buffers were push-pull CMOS buffers. The buffers sink current when driving low and source current when driving high. The buffers were then terminated to a mid-level Thevenin resistance to obtain optimum power transfer and signal integrity. Unfortunately, this resulted in current flowing, and power being dissipated, whenever the buffers were enabled at either high or low. Pseudo Open Drain (POD) is a connection type where the termination at the load, ODT, is only connected to VDDQ. POD connections only consume power when driving low, thus reducing power. In DDR4, both the PHY (for reads) and SDRAM (for writes) provide these terminations to VDDQ internally on all of the data group pins.

Signals look different on connections using POD terminations as compared to previous DDR connections, where the data group signals went from VSS to VDDQ and sampling was based on a mid-level reference voltage. The high level is still at VDDQ. However, the low level is now calculated based on the drive impedance and the ODT resistance. If the drive impedance and the ODT resistance are both set to 50Ω, then the low-level voltage is now at VDDQ/2. Then, that requires a sampling voltage halfway between those voltages, or 3/4*VDDQ, for best performance.

2.14 CK and ADDR_CTRL Topologies and Routing Guidance

The CK and ADDR_CTRL net classes are routed similarly, and are length matched from the DDR PHY in the processor to each SDRAM to minimize skew between them. The CK net class requires more care because the CK net class runs at a higher transition rate and is differential.

The CK and ADDR_CTRL net classes are routed in a *fly-by* implementation. This means that the CK and ADDR_CTRL net classes are routed as a multi-drop bus from the DDR controller in the processor sequentially to each SDRAM, and each signal has a termination at the end. To complete this routing, a small stub trace exists on each net at each SDRAM. These stubs must be short and approximately the same length to manage the reflections. The ADDR_CTRL net class is length matched to the CK net class, at each SDRAM, so that the ADDR_CTRL signals are properly sampled at each SDRAM.

Note

Fly-by routing is required for DDR4 layouts. Balanced-T routing, previously used for DDR2 layouts, is not supported.

Section 2.2 discussed that there are multiple possible memory topologies, or implementations, ranging from a single x16 SDRAM up to a maximum of two x8 SDRAMs. Regardless of the number of SDRAMs implemented, the routing requirements must be followed. TI recommends that all SDRAMs be implemented on the same side of the board, preferably on the same side of the board as the processor. To implement the SDRAMs on both sides of the board is possible, but the routing complexity and the number of PCB layers required is significantly increased.

Figure 2-5 shows the topology of the CK net class, and Figure 2-6 shows the topology for the corresponding ADDR_CTRL net class. The fly-by routes have been broken into segments to simplify the length matching analysis. Care must be taken to avoid excessive length error accumulation with this method.

Segments A1 and A2 comprise the lead-in section. Segment AT is the track to the termination at the end of the net. Segments A3 are the routed track between the stubs that branch off to each SDRAM. For topologies with fewer SDRAMs, remove an A3 segment for each SDRAM not present. Length matching requirements for the routing segments are detailed in Table 2-6.

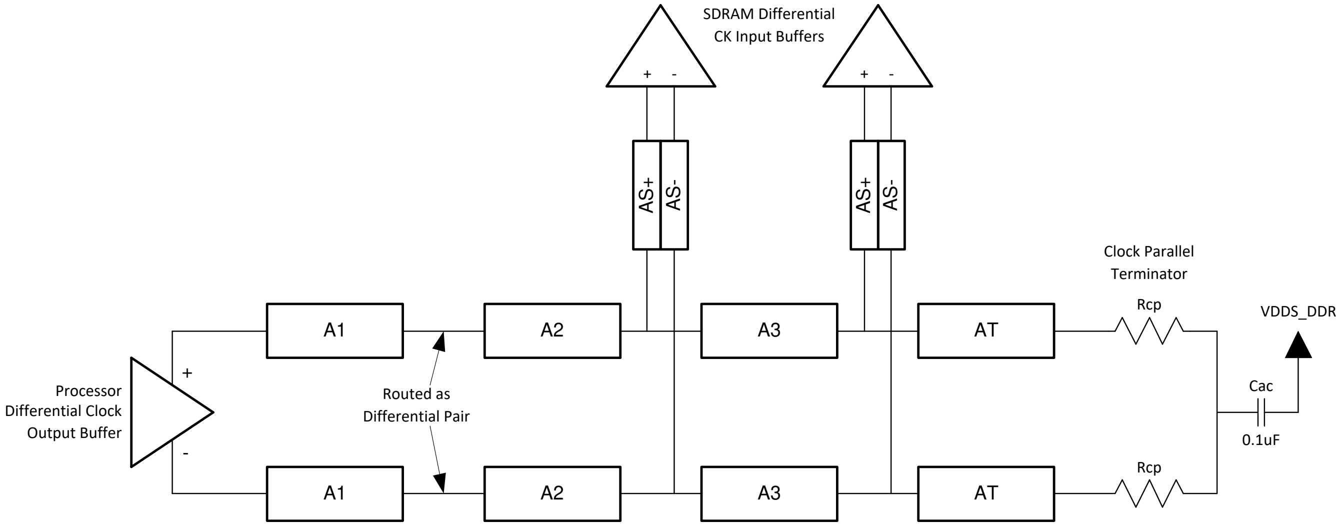


Figure 2-5. CK Topology for Two DDR4 SDRAM Devices

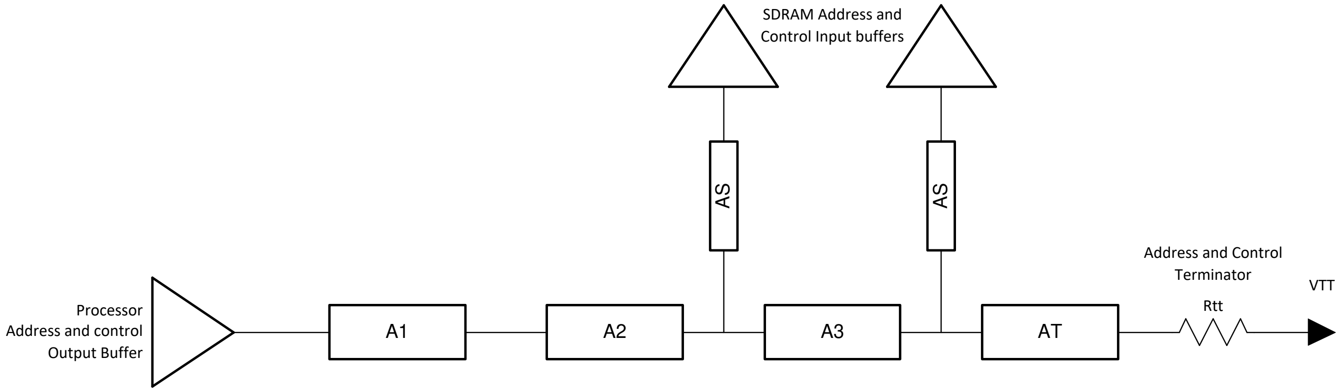


Figure 2-6. ADDR_CTRL Topology for Two DDR4 SDRAM Devices

The previous figures show the circuit topology such that the track lengths can be managed and the routed track length matching rules can be followed. The next two figures again show the routing for the CK and ADDR_CTRL routing groups depicted from the perspective of tracks routed on the PCB.

Figure 2-7 shows the CK group routing for two SDRAM devices. The fly-by routing is made clear in this figure. The DDR0_CK0 and DDR0_CK0_n tracks (the CK routing group) are routed as a differential pair from the processor to the SDRAM at the end that contains BYTE0 data. This differential pair routing then proceeds to the other SDRAM and ends with the AC termination to VDDS_DDR. The routing also includes the routing stubs for both DDR0_CK0 and DDR0_CK0_n at each SDRAM.

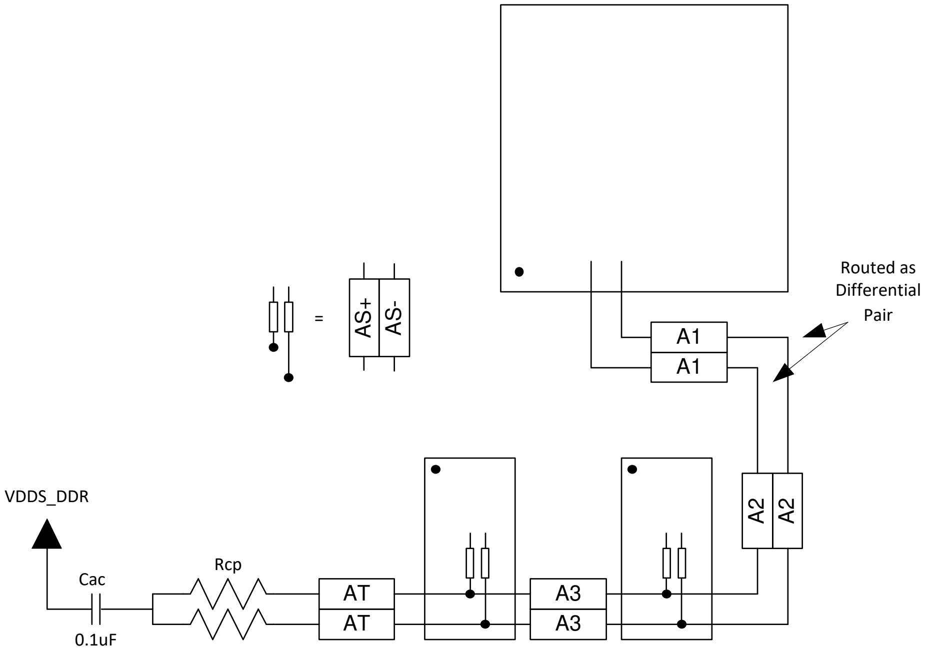


Figure 2-7. CK Routing for Two DDR4 SDRAM Devices

Figure 2-8 shows the ADDR_CTRL routing for two SDRAM devices. These are also routed in a fly-by manner along the same path because the ADDR_CTRL routing group is length-matched to the CK routing group.

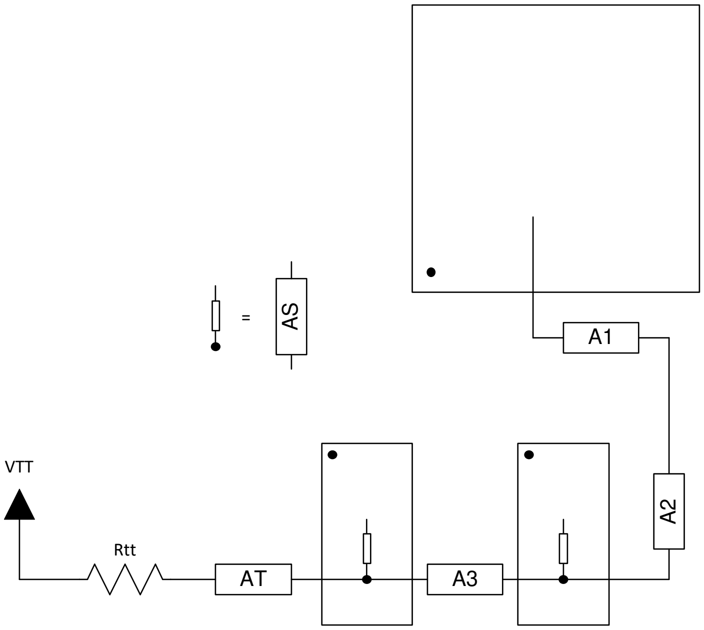


Figure 2-8. ADDR_CTRL Routing for Two DDR4 SDRAM Devices

The absolute order is not significant. The fly-by routing that starts at the processor can also route down to the SDRAM containing the last byte of data (or whichever SDRAM that is opposite in the row from the one containing the BYTE0 data). The fly-by routing then proceeds to the other SDRAM as discussed above, until routing to VTT through the Rtt termination after the BYTE0 SDRAM.

Minimize layer transitions during routing. If a layer transition is necessary, then this transition to a layer using the same reference plane is preferable. If this cannot be accommodated, then make sure there are nearby stitching vias to allow the return currents to transition between reference planes when both reference planes are ground or VDDS_DDR. Alternately, make sure there are nearby bypass capacitors to allow the return currents to transition between reference planes when one of the reference planes is ground and the other is VDDS_DDR. This must occur at every reference plane transition. The goal is to minimize the size of the return current path thus minimizing the inductance in this path. Lack of these stitching vias or capacitors results in impedance discontinuities in the signal path that increase crosstalk and signal distortion.

2.15 Data Group Topologies and Routing Guidance

Regardless of the number of DDR4 devices implemented, the data line topology is always point-to-point. Minimize layer transitions during routing. If a layer transition is necessary, then transition to a layer using the same reference plane. If this cannot be accommodated, then make sure there are nearby ground vias to allow the return currents to transition between reference planes. The goal is to provide a low inductance path for the return current. Also, to optimize the length matching, TI recommends routing all nets within a single data routing group on one layer where all have the exact same number of vias and the same via barrel length.

DQSP and DQSN lines are point-to-point signals routed as a differential pair. Figure 2-9 shows the DQS connection topology.

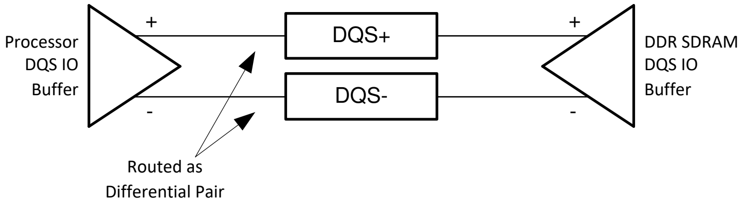


Figure 2-9. DDR4 DQS Topology

DQ and DM lines are point-to-point signals routed singled-ended. Figure 2-10 shows the DQ and DM connection topology.

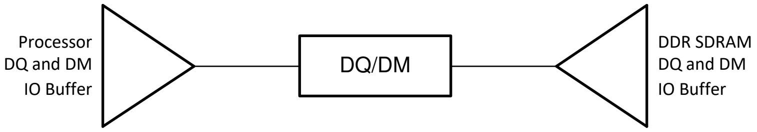


Figure 2-10. DDR4 DQ/DM Topology

Similar to the figures above for the CK and ADDR_CTRL routes, Figure 2-11 and Figure 2-12 show an example of the PCB routes for a DQS routing group and the associated data routing group nets.

The routing example shows DQS0P and DQS0N, which are routed as a differential pair from the processor to the SDRAM that contains Byte 0. This is implemented as a point-to-point routed differential pair without any board terminations. There are no stubs allowed on these nets of any kind. All test access probes must be in line without any branches or stubs. Similar DQS pair routing exists from the processor to each SDRAM for the byte lanes implemented.

Figure 2-12 shows a routing example for a single net in the Byte 0 routing group. The DQ and DM nets are routed single-ended and are also point-to-point without any stubs or board terminations. Point-to-point routes exist for each of the DQ and DM nets implemented.

The DQ and DM nets are routed along the same path as the DQSP and DQSN pair for that byte lane, so that the nets can be length matched to the DQS pair.

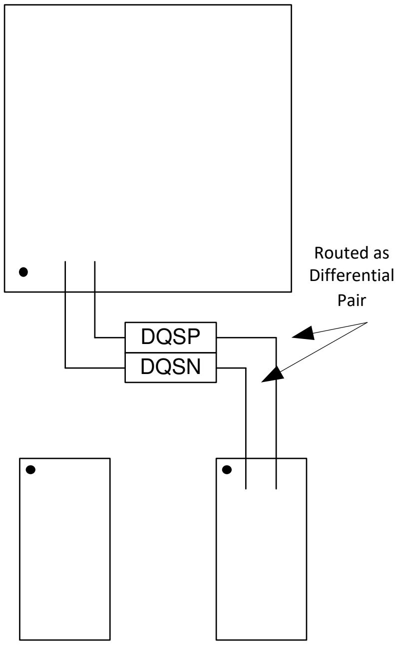


Figure 2-11. DQS Routing to Two DDR4 SDRAM Devices

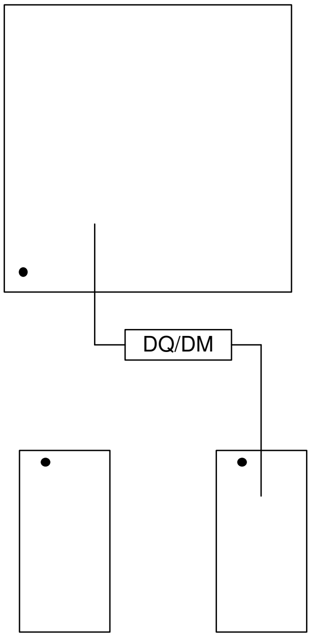


Figure 2-12. DQ/DM Routing to Two DDR4 SDRAM Devices

2.16 CK and ADDR_CTRL Routing Specification

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin for the ADDR_CTRL nets. Thus, this skew must be controlled. Routed PCB track has a delay proportional to the length. Thus, the delay skew must be managed through matching the lengths of the routed tracks within a defined group of signals. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and the associated clock pair, DDR0_CK0 and DDR0_CK0_n. Consider Z-axis delays (VIAs) with accurate stackup information during analysis.

2.16.1 CACLM - Clock Address Control Longest Manhattan Distance

A metric to establish a maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting the points with only horizontal or vertical track segments. A reasonable limit to the trace route length is to the Manhattan distance plus some margin. CACLM is this limit and is defined as the Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR4 memories, the maximum possible Manhattan distance can be determined given the placement of these parts. This is from this distance that this rule-of-thumb limit on the lengths of the routed track for the CK and ADDR_CTRL routing groups is determined.

There is a likelihood that the longest CK and ADDR_CTRL Manhattan distance is for Address Input A13 on the DDR4 SDRAM device because A13 is at the farthest corner in the placement. Assuming A13 is the longest, calculate CACLM as the sum of CACLMY(A13) + CACLMX(A13) + 300 mils. The extra 300 mils allows for routing past the first DDR4 SDRAM and returning up to reach pin A13. Use this as a guideline for the upper limit to the length of the routed traces from the processor to the first SDRAM.

2.16.2 CK and ADDR_CTRL Routing Limits

Table 2-6 lists the limits for the individual segments that comprise the routing from the processor to the SDRAM. These segment lengths coincide with the CK and ADDR_CTRL topology diagram shown previously in Figure 2-5 and Figure 2-6. By matching the length for the same segments of all signals in a routing group, the signal delay skews are controlled.

Recall that the CK and ADDR_CTRL nets route along the same path for each segment. This simplifies the length matching. The skew limits for the CK group compare the length of DDR0_CK0P to the length of DDR0_CK0N**.** Then the skew limits for the ADDR_CTRL group nets are compared to the CK group nets.

Most PCB layout tools can be configured to generate reports to assist with this validation. If this cannot be generated automatically, this must be generated and verified manually.

Table 2-6 also lists skew limits for the full routes from the processor to each SDRAM. This must be checked in addition to the skew limits in the individual sections to verify that there is not accumulating error in the layout.

To use length matching (in mils) instead of time delay (in ps), multiply the time delay (in ps) limit by 5. The microstrip routes propagate faster than stripline routes. A standard practice when using length matching is to divide the microstrip length by 1.1 to achieve a compensated length to normalize the microstrip length with the stripline length and to align with the delay limits provided. This is called velocity compensation (see Section 1.5).

Table 2-6. CK and ADDR_CTRL Routing Specifications

Number	Parameter	MIN	TYP	MAX	UNIT
1	A1+A2 length			500 (1)	ps (12)
2	A1+A2 skew ADDR_CTRL to CK (4)			3	ps
4	A3 skew ADDR_CTRL to CK (4)			3	ps
3	A3 length			125	ps
5	A1+A2 skew DDR0_CK0 to DDR0_CK0_n			0.4	ps
6	A3 skew DDR0_CK0 to DDR0_CK0_n			0.4	ps
7	AS length		5 (1)	17	ps
8	AS skew		1.3 (1)	3	ps
9	AS+/AS- length		5	17	ps
10	AS+/AS- skew			0.4	ps
11	AT length (3)		75		ps
12	AT skew ADDR_CTRL to CK (4)		14		ps
13	AT skew DDR0_CK0 to DDR0_CK0_n			0.4	ps
14	Total DDR0_CK0 to DDR0_CK0_n skew from processor to each SDRAM (2)			0.8	ps
15	Total CK to ADDR_CTRL skew from processor to each SDRAM (2)			4	ps
16	Vias per trace (11)			3(1)	vias

Table 2-6. CK and ADDR_CTRL Routing Specifications (continued)

Number	Parameter	MIN	TYP	MAX	UNIT
17	Via count difference[11]			1[10]	vias
18	Center-to-center CK to other DDR4 trace spacing[5]	4w			
19	Center-to-center ADDR_CTRL to other DDR4 trace spacing[5]	4w			
20	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing[5]	3w			
21	CK center-to-center spacing[6] [7]	See notes below			
22	CK spacing to other net[5]	4w			
23	Rcp[8]	Zo-1	Zo	Zo+1	Ω
24	Rtt[8] [9]	Zo-5	Zo	Zo+5	Ω

(1) Max value is based upon conservative signal integrity approach. This value can be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(2) This is the combined length from the processor to the SDRAM. This must be computed for each SDRAM to make sure that the segment matching does not result in accumulated error. The first SDRAM is A1 + A2 + AS, computed for each signal. The 2nd SDRAM is A1 + A2 + A3 + AS, computed for each signal.
(3) While this length can be increased for convenience, the length needs to be minimized.
(4) ADDR_CTRL net class relative to the CK net class.
(5) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length (only near endpoints).
(6) CK spacing set to make sure of proper differential impedance.
(7) The user must control the impedance so that inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing must be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo, on that layer.
(8) Source termination (series resistor at driver) is specifically not allowed.
(9) Termination values must be uniform across the net class.
(10) Via count difference can increase by 1 only if there is accurate 3-D modeling of the signal flight times. This includes accurately modeled signal propagation through vias and has been applied to make sure all segment skew maximums are not exceeded.
(11) Count vias individually from processor to each SDRAM.
(12) PCB track length shown as ps is a normalized representation of length. 1ps can be equated to 5 mils as a simple transformation. This is stripline equivalent length where velocity compensation must be used for all segments routed as microstrip track.

2.17 Data Group Routing Specification

Skew within the DQS, and DQ and DM net classes directly reduces setup and hold margin for the DQ and DM nets. Thus, this skew must be controlled. Routed PCB track has a delay proportional to the length. Thus, the length skew must be managed through matching the lengths of the routed tracks within a defined group of signals. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and the associated clock pair, DQSP, and DQSN. Consider Z-axis delays (VIAs) with accurate stackup information during analysis.

2.17.1 DQLM - DQ Longest Manhattan Distance

As with CK and ADDR_CTRL, a reasonable trace route length is to within a percentage of the Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 16-bit interface, there are two DQLMs, DQLM0 and DQLM1.

Note

TI does not require nor recommend to match the lengths across all byte lanes. Length matching is only required within each byte.

Given the DQS, DQ, and DM pin locations on the processor and the DDR4 memories, the maximum possible Manhattan distance can be determined given the placement. From this distance, that and the upper limit on the lengths of the transmission lines for the data bus can be established. Unlike the CACLM, there is no margin added to the DQLMn limits. These limits are simply the sum of the horizontal and vertical distances for the longest pin to pin route for that byte group.

2.17.2 Data Group Routing Limits

Table 2-7 contains the routing specifications for DQS, DQ, and DM routing groups. Each byte lane is routed and matched independently.

To use length matching (in mils) instead of time delay (in ps), multiply the time delay (in ps) limit by 5. The microstrip routes propagate faster than stripline routes. A standard practice when using length matching is to divide the microstrip length by 1.1, to achieve a compensated length to normalize the microstrip length with the stripline length and to align with the delay limits provided (see Section 1.5).

Table 2-7. Data Group Routing Specifications

Number	Parameter	MIN	MAX	UNIT
DRS31	BYTE0 length		500	ps (10)
DRS32	BYTE1 length		500	ps
DRS36	DQSn+ to DQSn- skew		0.4	ps
DRS37	DQSn to DQn skew (2) (3)		2	ps
DRS38	Vias per trace		2 (1)	vias
DRS39	Via count difference		0 (9)	vias
DRS310	Center-to-center BYTEn to other DDR4 trace spacing (5)	4		w (4)
DRS311	Center-to-center DQn to other DQn trace spacing (6)	3		w (4)
DRS312	DQSn center-to-center spacing (7) (8)	See notes below		
DRS313	DQSn center-to-center spacing to other net	4		w (4)

(1) Max value is based upon conservative signal integrity approach. This value can be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(2) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.
(3) Each DQS pair is length matched to the associated byte.
(4) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length (only near endpoints).
(5) Other DDR4 trace spacing means other DDR4 net classes not within the byte.
(6) This applies to spacing within the net classes of a byte.
(7) DQS pair spacing is set to make sure of proper differential impedance.
(8) The user must control the impedance so that inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing needs to be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo, on that layer.
(9) Via count difference can increase by 1 only if accurate 3-D modeling of the signal flight times. This includes accurately modeled signal propagation through vias and this has been applied to make sure that DQn skew and DQSn to DQn skew maximums are not exceeded.
(10) PCB track length shown as ps is a normalized representation of length. 1ps can be equated to 5 mils as a simple transformation. This is stripline equivalent length where velocity compensation must be used for all segments routed as microstrip track.

2.18 Bit Swapping

2.18.1 Data Bit Swapping

Data bit (DQx) and Data Mask (DM) swapping within a byte (for example, swapping D2 with D3) is allowed, but data bit DQx/DM swapping across bytes (for example, swapping D4 and D13) is not allowed. This data bit swapping within a byte is only possible when not using CRC.

Swapping byte lanes (for example, swapping byte 0 and 1) is allowed. When swapping bytes, all of the associated signals of the byte (DQx, DQSx, and DM) must be swapped together.

Software configuration changes in the DDR Configuration Tool (*https://dev.ti.com/sysconfig*) are not necessary for normal device functionality when swapping data signals with DDR4

2.18.2 Address and Control Bit Swapping

Bit swapping of the address or control bits is not allowed with DDR4, as this breaks functionality.

3 LPDDR4 Board Design and Layout Guidance

3.1 LPDDR4 Introduction

LPDDR4 is an SDRAM device specification governed by the JEDEC standard JESD209-4, *Low Power Double Data Rate 4 (LPDDR4)*. This standard strives to reduce power and improve signal integrity by implementing a lower voltage I/O power rail, employing ODT on the command and address bus, and reducing the overall width of the command and address bus, among other features. Unlike other DDR types, LPDDR4 has been organized into 16-bit channels. Refer to the device data sheet and the *DDR Subsystem (DDRSS)* chapter in the AM62x, AM62Lx Technical Reference Manual for lists of features and not supported features.

The following sections detail the routing specification and layout guidelines for an LPDDR4 interface.

3.2 LPDDR4 Device Implementations Supported

LPDDR4 supports many different implementation topologies. However, the devices only support a single 16-bit channel for LPDDR4. SDRAMs with additional channels and/or dies can be implemented but the additional channels or dies are unconnected and not used. Table 3-1 lists the only supported LPDDR4 device combination.

Table 3-1. Supported LPDDR4 SDRAM Combinations

LPDDR4 SDRAM Count	Channels	Die	Ranks(CS signals)	LPDDR4 Channel Width	DDRSS data width	Schematic	Max Addressable Range
1	1	1	1(CS0_n)	16	16	Figure 3-1	2GBytes

Note

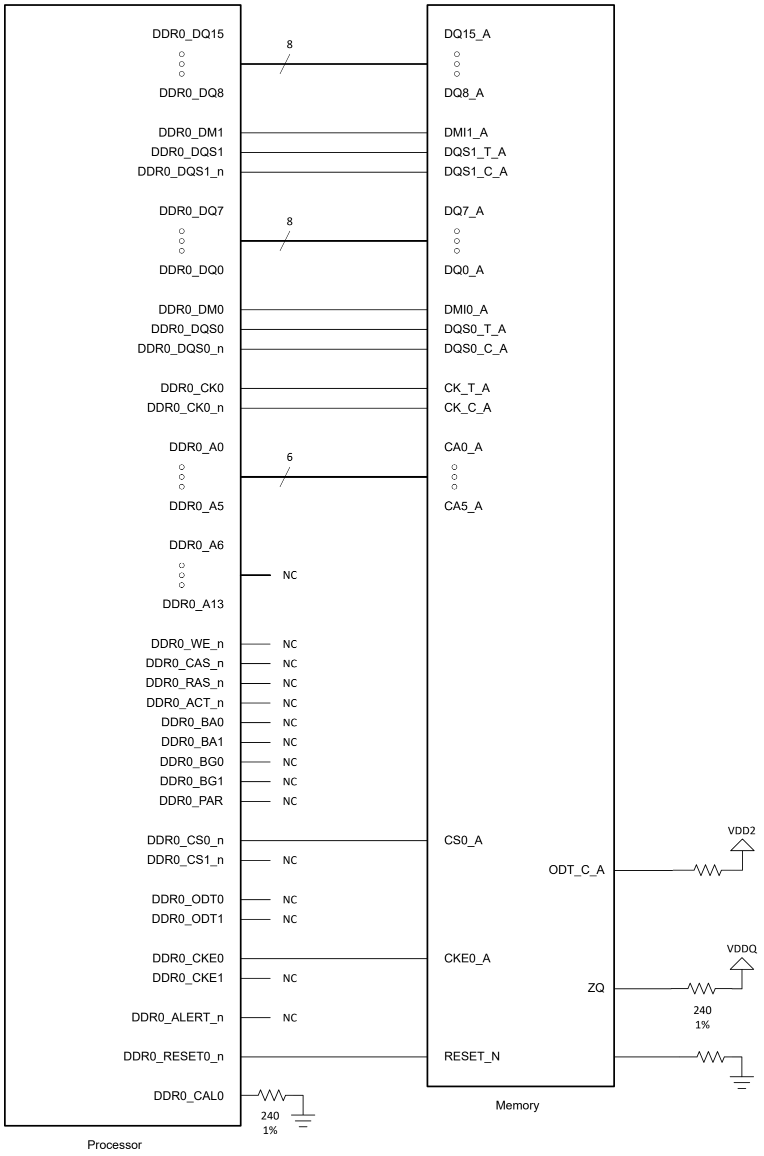
ECC is supported on the LPDDR4 interface. Unlike traditional ECC interfaces, which require dedicated memory pins and devices, ECC is supported inline. The ECC system impact is in interface bandwidth and overall memory density, as ECC data is stored alongside non-ECC data. Max addressable range is reduced if ECC is enabled. See device TRM for more details.

Note

Data bus routing must be point to point between the processor and the memory, and cannot be split on the board. Thus, dual-rank LPDDR4 designs are only possible when using one channel of an LPDDR4 dual channel, dual rank device. If more than 2GBytes is needed, consider using DDR4.

3.3 LPDDR4 Interface Schematics

As stated above, LPDDR4 supports many different implementation topologies but the device only supports a single 16-bit channel for LPDDR4. Figure 3-1 illustrates the supported 16-bit, single-rank, single-channel LPDDR4 implementation. SDRAMs with additional channels or dies can be used but the additional channels or dies are unconnected and not used.



1. An external 240Ω ±1% resistor must be connected between the DDR0_CAL0 pin and VSS. The maximum power dissipation for the resistor is 5.2mW. No external voltage must be applied to the DDR0_CAL0 pin. Tolerance of ±1% required throughout life of component or product.
2. RESET_n shall have an external 10k pull-down resistor to control RESET low until the DDR controller drives the signal. RESET_n has no length matching requirement.

Figure 3-1. 16-Bit, Single-Rank, Single Channel LPDDR4 Implementation

3.4 Compatible JEDEC LPDDR4 Devices

Table 3-2 shows the parameters of the JEDEC LPDDR4 devices compatible with this interface.

Table 3-2. Compatible JEDEC LPDDR4 Devices

Number	Parameter	MIN	MAX	UNIT
1	Data rate (1) (2)		1600	MT/s
2	Channel bit width	x16	x16	Bits
3	Channels	1	1	-
4	Ranks	1	1	-
5	Die	1	1	-
6	Device count	1	1	-

(1) Refer to the device data sheet for supported data rates.
(2) SDRAMs in faster speed grades can be used, provided the SDRAMs are properly configured to operate at the supported data rates. Faster speed grade SDRAMs can have faster edge rates, which can affect signal integrity. SDRAMs with faster speed grades must be validated on the target board design.

3.5 Placement

Figure 3-2 shows the required placement for the processor and the LPDDR4 device. The dimensions for this figure are defined in Table 3-3. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space.

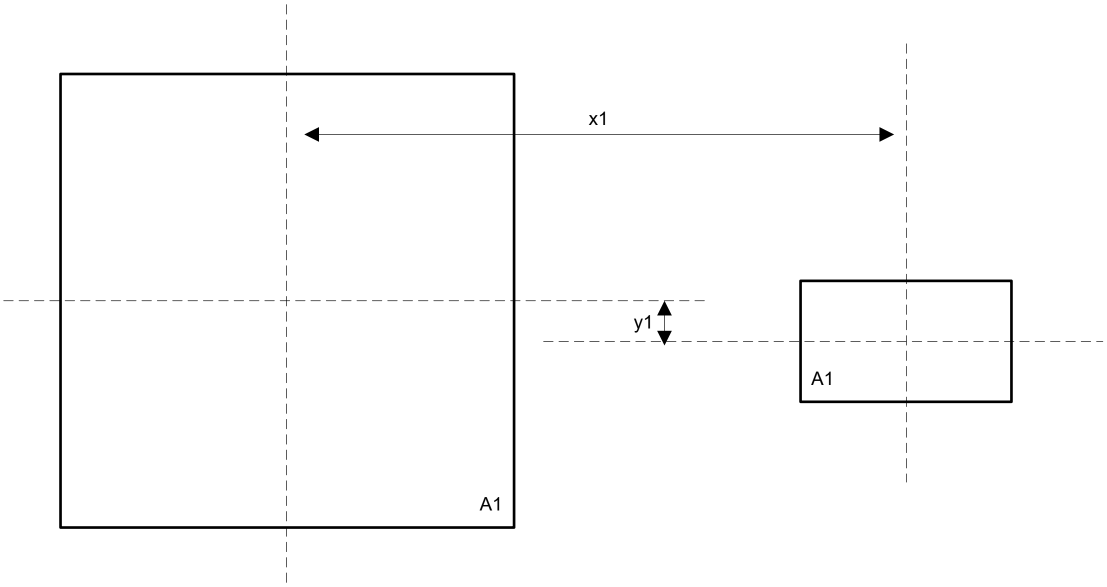


Figure 3-2. LPDDR4 Placement Specification

Table 3-3. LPDDR4 Placement Parameters

Number	Parameter	MIN	MAX	UNIT
1	x1		2000	Mils
2	y1		1000	Mils

3.6 LPDDR4 Keepout Region

The region of the PCB used for LPDDR4 circuitry must be isolated from other signals. The LPDDR4 keepout region is defined for this purpose and is shown in Figure 3-3. The size of this region varies with the placement and DDR routing. Non-LPDDR4 signals must not be routed on the DDR signal layers within the LPDDR4 keepout region. Non-LPDDR4 signals can be routed in this region only if the signals are routed on other layers separated from the DDR signal layers by a ground layer. No breaks are allowed in the reference ground layers in this region. In addition, a solid VDDS_DDR power plane must exist across the entire keepout region.

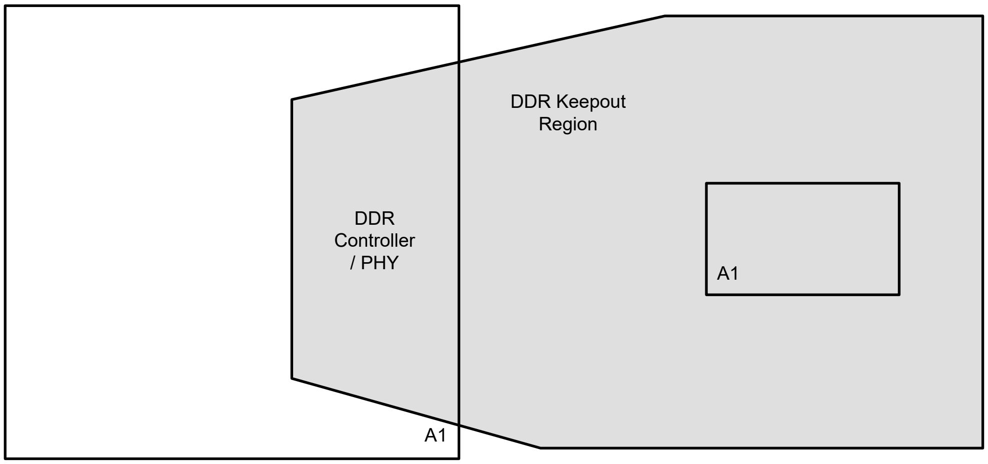


Figure 3-3. LPDDR4 Keepout Region

3.7 LPDDR4 DBI

DBI is recommended to reduce supply/ground noise and to improve the data eye. Therefore the DDR Subsystem Configuration Tool enables Write DBI as a default for LPDDR4 configurations.

3.8 Net Classes

Routing rules are applied to signals in groups called net classes. Each net class contains signals with the same routing requirements. This simplifies the implementation and compliance of these routes. Table 3-4 lists the clock net classes for the LPDDR4 interface. Table 3-5 lists the signal net classes, and associated clock net classes, for signals in the LPDDR4 interface. These net classes are then linked to the termination and routing rules that follow.

Table 3-4. Clock Net Class Definitions

Clock Net Class	Processor Pin Names
CK0	DDR0_CK0 / DDR0_CK0_n
DQS0	DDR0_DQS0 / DDR0_DQS0_n
DQS1	DDR0_DQS1 / DDR0_DQS1_n

Table 3-5. Signal Net Class Definitions

Signal Net Class	Associated Clock Net Class	Processor Pin Names
ADDR_CTRL	CK0	DDR0_A[5:0], DDR0_CS0_n, DDR0_CS1_n, DDR0_CKE0, DDR0_CKE1
BYTE0	DQS0	DDR0_DQ[7:0], DDR0_DM0
BYTE1	DQS1	DDR0_DQ[15:8], DDR0_DM1

3.9 LPDDR4 Signal Termination

LPDDR4 memories have software configurable on-die termination for the data group nets. The DDR subsystem also contains software configurable on-die termination for the address / control group nets. Thus, termination is not required on any DDR signals for an LPDDR4 configuration.

3.10 LPDDR4 VREF Routing

LPDDR4 memories generate VREFCA and VREFDQ internally for the address and command bus and data bus, respectively. Similarly, the DDR PHY also provides the reference voltage for the data group nets during reads. Thus, unlike DDR3 and DDR4, VREF does not need to be generated on the board, and there is no required VREF routing for an LPDDR4 configuration.

3.11 LPDDR4 VTT

Unlike DDR3 and DDR4, there is no required termination on the PCB of the address/control bus of an LPDDR4 configuration. All termination is handled internally (on-die). Thus, VTT does not apply for LPDDR4.

3.12 CK0 and ADDR_CTRL Topologies

The CK0 and ADDR_CTRL net classes are routed similarly, and are length matched from the DDR controller in the processor to the LPDDR4 SDRAM to minimize skew between the signals and make sure that the ADDR_CTRL signals are properly sampled at the SDRAM. The CK0 net class requires more care because the CK0 runs at a higher transition rate and is differential. The CK0 and ADDR_CTRL topologies are point-to-point.

Figure 3-4 shows the topology of the CK0 net class, and Figure 3-5 shows the topology for the corresponding ADDR_CTRL net classes. Length matching requirements for the routing segments are detailed in Table 3-6.

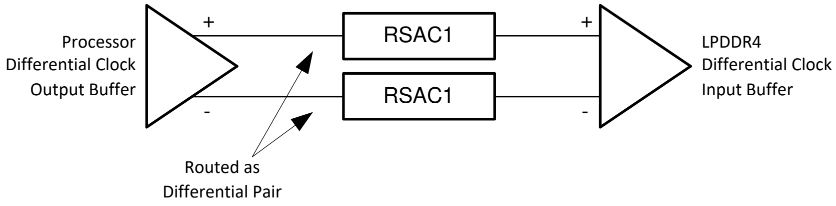


Figure 3-4. LPDDR4 CK0 Topology

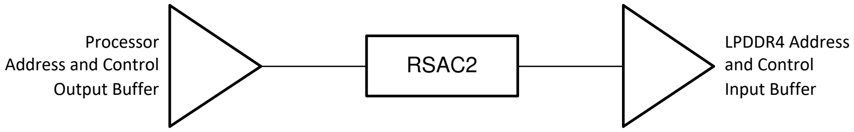


Figure 3-5. LPDDR4 ADDR_CTRL Topology

Minimize layer transitions during routing. If a layer transition is necessary, then transition to a layer using the same reference plane. If this cannot be accommodated, then make sure there are nearby stitching vias to allow the return currents to transition between reference planes when both reference planes are ground or VDDS_DDR. Alternately, make sure there are nearby bypass capacitors to allow the return currents to transition between reference planes when one of the reference planes is ground and the other is VDDS_DDR. This must occur at every reference plane transition. The goal is to minimize the size of the return current path thus minimizing the inductance in this path. Lack of these stitching vias or capacitors results in impedance discontinuities in the signal path that increase crosstalk and signal distortion.

There are no stubs or terminations allowed on the nets of the CK0 and ADDR_CTRL routing group topologies. All test and probe access points must be in line without any branches or stubs.

3.13 Data Group Topologies

The data line topology is always point-to-point for LPDDR4 implementations, and is separated into two different byte routing groups. Minimize layer transitions during routing. If a layer transition is necessary, then transitioning to a layer using the same reference plane is better. If this cannot be accommodated, then make sure there are nearby ground vias to allow the return currents to transition between reference planes (within ± 250 mils of transition vias). The goal is to provide a low inductance path for the return current. To optimize the length matching, TI recommends routing all nets within a single data routing group (that is, DQS, DQ, DM) together on the same layer or layers where all nets have the exact same number of vias and the same via barrel length. Microstrip routing can be used to implement DDR routing, but doing so provides lower EMI immunity and signal integrity at high data rates. The designer needs to evaluate system requirements carefully to determine that the desired product requirements can be met. High-speed DQ and DQS, DQSn routing on microstrip layers requires special care and DFM consideration because of more variation in signal propagation. Signals from the entire byte group must be routed together.

DQSP and DQSN lines are point-to-point signals routed as a differential pair. Figure 3-6 illustrates the DQSP and DQSN connection topology.

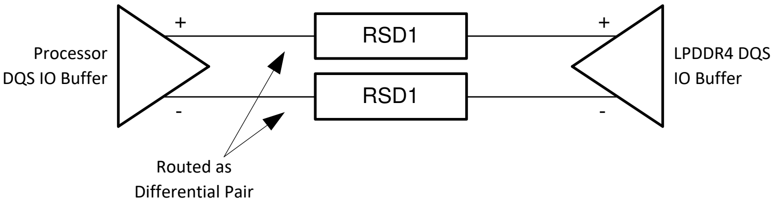


Figure 3-6. LPDDR4 DQS Topology

DQ and DM lines are point-to-point signals routed as single-ended. Figure 3-7 illustrates the DQ and DM connection topology.

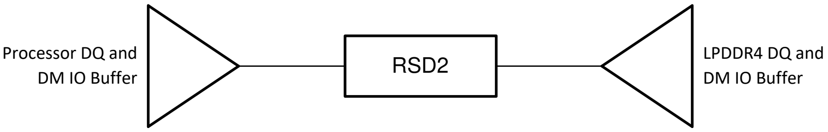


Figure 3-7. LPDDR4 DQ/DM Topology

There are no stubs or termination allowed on the nets of the data group topologies. All test and probe access points must be in line without any branches or stubs.

3.14 CK0 and ADDR_CTRL Routing Specification

Skew within the CK0 and ADDR_CTRL net classes directly to reduce setup and hold margin for the ADDR_CTRL nets. Thus, this skew must be controlled. Per-bit deskew capability within the PHY substantially loosens the skew tolerance requirements. The skew budgets in Table 3-6 include total delay from SoC die pad to DRAM pin. (that is, delay of SOC package and PCB). Package delays are provided in Additional Information: Package Delays. The designer is free to length match using smaller tolerance than the values shown in Table 3-6. The routed PCB track has a delay proportional to the length. Thus, the delay skew must be managed through matching the lengths of the routed tracks within a defined group of signals. The only way to practically match lengths on a PCB is to lengthen the shorter traces. Consider Z-axis delays (VIAs) with accurate stackup information during analysis.

Table 3-6 lists the limits for the individual segments that comprise the routing from the processor to the SDRAM. These segment lengths coincide with the CK0 and ADDR_CTRL topology diagram shown previously in Figure 3-4 and Figure 3-5. By matching the length for the same segments of all signals in a routing group, the signal delay skews are controlled. Most PCB layout tools can be configured to generate reports to assist with this validation. If this cannot be generated automatically, then this must be generated and verified manually.

Table 3-6. CK0 and ADDR_CTRL Routing Specifications

Number	Parameter	MIN	TYP	MAX	UNIT
LP4_ACRS1	Propagation delay of net class CK0 (RSAC1)			450(1)	ps
LP4_ACRS2	Propagation delay of net class ADDR_CTRL (RSAC2)			450(1)	ps
LP4_ACRS3	Skew within net class CK0 (Skew of DDR0_CK0 and DDR0_CK0_n) (RSAC1)			0.75(2) (3)	ps
LP4_ACRS6	Skew across ADDR_CTRL and CK0 clock net classes, relative to propagation delay of CK0 net class (RSAC1 - RSAC2)(4)	-312.5(3) (5)		312.5(3) (5)	ps
LP4_ACRS7	Vias per trace			3(1)	vias

Table 3-6. CK0 and ADDR_CTRL Routing Specifications (continued)

Number	Parameter	MIN	TYP	MAX	UNIT
LP4_ACRS8	VIA Stub Length		20		Mils
LP4_ACRS9	Via count difference			1(6)	vias
LP4_ACRS10	Center-to-center CK0 to other LPDDR4 trace spacing	5w(7)			
LP4_ACRS11	Center-to-center ADDR_CTRL to other LPDDR4 trace spacing	5w(7)			
LP4_ACRS12	Center-to-center ADDR_CTRL to self or other ADDR_CTRL trace spacing	3w(7)			
LP4_ACRS13	CK0 center-to-center spacing(8)	See note below			
LP4_ACRS14	CK0 spacing to non-DDR net	5w(7)			

(1) Max value is based upon conservative signal integrity approach. FR4 material assumed with Dk ≃ 3.7 - 3.9 and Df ≃ 0.002. This value can be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(2) Recommendation for PCB layout tool design. Required to be verified by simulation(9), confirm JEDEC defined Vix_DQS_ratio (20%) and Vix_CK_ratio (25%) are satisfied, also confirm good eye margins.
(3) Consider the delays from SOC die pad to the DRAM pin (that is, delays of SOC package and delays of PCB up to the DRAM pin. DRAM package delays are omitted). Refer to Additional Information: Package Delays.
(4) Recommend routing net classes CK0 and ADDR_CTRL on same signal layer for better skew control.
(5) Simulation(9) must be performed and the delay report analyzed to make sure delays are within the limit. Delay reports from PCB layout tools use a simplified calculation based on a constant propagation velocity factor. TI recommends initially delay matching in PCB layout tool to a target less than 20% of the limit.
(6) Via count difference can increase by 1 only if accurate 3-D modeling of the signal flight times. This includes accurately modeled signal propagation through vias; this has been applied to make sure all segment skew maximums are not exceeded.
(7) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length (only near endpoints). Spacing minimums can be relaxed if simulations(9) accurately capture crosstalk between neighboring victim and aggressor traces and show good margin. Consider also VIA spacing. Signals with adjacent VIAs near SOC must not also have adjacent VIAs near the DRAM.
(8) P to N spacing set to make sure of proper differential impedance. The designer must control the impedance so that inadvertent impedance mismatches are not created. Generally speaking, center-to center spacing must be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo, on that layer. Refer to impedance targets in Table 1-1
(9) Simulation refers to a power-aware IBIS Signal Integrity (SI) simulation. Simulate across process, voltage, and temperature (PVT). Refer to LPDDR4 Board Design Simulations

3.15 Data Group Routing Specification

Skew within the Byte signal net class directly reduces the setup and hold margin for the DQ and DM nets. Thus, as with the ADDR_CTRL signal net class and associated CK0 clock net class, this skew must be controlled. Per-bit deskew capability within the PHY substantially loosens the skew tolerance requirements. The skew budgets in Table 3-7 include total delay from SoC die pad to DRAM pin. (that is, delay of SOC package and PCB). Package delays are provided in Additional Information: Package Delays. The designer is free to length match using smaller tolerance than the values shown in Table 3-7. The routed PCB track has a delay proportional to the length. Thus, the length skew must be managed through matching the lengths of the routed tracks within a defined group of signals. The only way to practically match lengths on a PCB is to lengthen the shorter traces. Consider Z-axis delays (VIAs) with accurate stackup information during analysis.

Note

TI does not require nor recommend to match the lengths across all byte lanes. Length matching is only required within each byte.

Table 3-7 contains the routing specifications for the Byte0 and Byte1 routing groups. Each signal net class and the associated clock net class is routed and matched independently.

Table 3-7. Data Group Routing Specifications

Number	Parameter	MIN	TYP	MAX	UNIT
LP4_DRS1	Propagation delay of net class DQSx (RSD1)			450(1)	ps
LP4_DRS2	Propagation delay of net class BYTEx (RSD2)			450(1)	ps
LP4_DRS3	Difference in propagation delays of CK0 pair and each DQS pair. (RSAC1 - RSD1) (2)	0(3) (4)		3(3) (4)	tCK
LP4_DRS4	Skew within net class DQSx. Skew of DDR0_DQSx and DDR0_DQSx_n (RSD1)			1.5(4) (6)	ps
LP4_DRS5	Skew across DQSx and BYTEx net classes. (Skew of RSD1 and RSD2) (7)			150(3) (4)	ps

Table 3-7. Data Group Routing Specifications (continued)

Number	Parameter	MIN	TYP	MAX	UNIT
LP4_DRS6	Difference in propagation delays of shortest DQ/DM bit in BYTEx and respective DQSx. (RSD2 - RSD1)(8)	-49(3) (4) (5)			ps
LP4_DRS7	Vias Per Trace			2(1)	vias
LP4_DRS8	VIA Stub Length		40		Mils
LP4_DRS9	Via Count Difference			0(9)	vias
LP4_DRS10	RSD1 center-to-center spacing (between different clock net classes)	5w(10)			
LP4_DRS11	RSD1 center-to-center spacing (within clock net class)(11)	See note below			
LP4_DRS12	RSD2 center-to-center spacing (between different signal net classes/bytes)	5w(10)			
LP4_DRS13	RSD2 center-to-center spacing (to self or within signal net class)	3w(10)			

(1) Max value is based upon conservative signal integrity approach. FR4 material assumed with Dk ≃ 3.7 - 3.9 and Df ≃ 0.002. This value can be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(2) Propagation delay of CK0 pair must be greater than propagation delay of each DQS pair.
(3) Simulation(12) must be performed and the delay report analyzed to make sure delays are within the limit. Delay reports from PCB layout tools use a simplified calculation based on a constant propagation velocity factor. TI recommends initially delay matching in PCB layout tool to a target less than 20% of the limit.
(4) Consider the delays from SOC die pad to the DRAM pin (that is, delays of SOC package and delays of PCB up to the DRAM pin. DRAM package delays are omitted). Refer to Additional Information: Package Delays.
(5) Recommend that the propagation delay of DQS is shorter than all DQx within a byte. If that is not possible, then LP4_DRS6 specifies that a DQ can be shorter by at most 49ps.
(6) Recommendation for PCB layout tool design. Required to be verified by simulation(12), confirm JEDEC defined Vix_DQS_ratio (20%) and Vix_CK_ratio (25%) are satisfied, also confirm good eye margins.
(7) Skew matching is only done within a byte including DQS. Skew matching across bytes is neither required nor recommended.
(8) Propagation delay of the shortest DQ, DM bit in BYTEx Signal Net Class is recommended to be greater than the propagation delay of the respective DQSx.
(9) VIA count difference can increase by 1 only if accurate 3-D modeling of the signal flight times. This includes accurately modeled signal propagation through VIA. This has been applied to make sure skew maximums are not exceeded.
(10) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length (only near endpoints). Spacing minimums can be relaxed if simulations(12) accurately capture crosstalk between neighboring victim and aggressor traces and show good margin. Consider VIA spacing. Signals with adjacent VIAs near SOC must not also have adjacent VIAs near the DRAM.
(11) DQS pair spacing is set to make sure of proper differential impedance. For example, the P to N spacing set is to make sure of proper differential impedance. The designer must control the impedance so that inadvertent impedance mismatches are not created. Generally speaking, center-to center spacing must be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo, on that layer. Refer to impedance targets in Section 1.3.
(12) Simulation refers to a power-aware IBIS Signal Integrity (SI) simulation. Simulate across process, voltage, and temperature (PVT).

3.16 Byte and Bit Swapping

All address and control signals must be routed from the DDR controller to the LPDDR4 memory as described in the diagrams in LPDDR4 Interface Schematics. Address and control signals cannot be swapped with other signals. Data bit (DQx) and Data Mask (DM) swapping within a byte (for example, swapping D2 with D3) is allowed, but data bit DQx/DM swapping across bytes (for example, swapping D4 and D13) is not allowed.

Swapping byte lanes within a channel (for example, swapping byte 0 and 1) is allowed. When swapping bytes, all of the associated signals of the byte (DQx, DQSx, and DM) must be swapped together.

Use the DDR Subsystem Register Configuration Tool in SysConfig (*https://dev.ti.com/sysconfig*) to describe how the bits are swapped. Check the README link in the tool for detailed instructions.

4 LPDDR4 Board Design Simulations

This section is intended to provide an overview of the basic system-level board extraction, simulation, and analysis methodologies for high-speed LPDDR4 interfaces (information specific to DDR4 comes in a later revision of this document). This is an essential step to make sure the PCB design meets all the requirements to operate the targeted speeds.

4.1 Board Model Extraction

Note

This section contains various information from J7 devices and board designs. The specific details only apply to J7 board designs, but are provided here as an examples for AM62x, AM62Lx board designs. Consult the data sheet for device specifications.

The board level extraction guidelines listed below are intended to work in any EDA extraction tool and are not tool-specific. This is important to follow the steps outlined in Section 4.2 through Section 4.4 immediately after completing touchstone model extractions. The design must be checked with these steps prior to running IBIS simulations.

1. For DDR extractions, extract power (VDDS_DDR/VDDQ) and signal nets together in a 3D-EM solver.
2. Use wide-band models. TI recommends to extract from DC to at least until 6x the Nyquist frequency (for example, for LPDDR4-3733 extract the model at least until 11.2GHz).
3. Check the board stack-up for accurate layer thickness and material properties.
    a. TI recommends to use Djordjevic-Sarkar models for the dielectric material definition.
4. Use accurate etch profiles and surface roughness for the signal traces across all layers in the stack-up.
5. If the board layout is cut prior to extraction (to reduce simulation time), then define a cut boundary that is at least 0.25 inch away from the signal and power nets.
6. Check the via padstack definitions.
    a. Make sure that the non-functional internal layer pads on signal vias are modeled the same way the pads are fabricated.
    b. These non-functional internal layer pads on signal vias are not recommended by TI.
7. Use Spice/S-parameter models (typically available from the vendor) for modeling all passives in the system.

4.2 Board-Model Validation

The extracted board models need to be checked for the following properties:

- Passivity: This makes sure that the board model is a passive network and does not generate energy.
- Causality: This makes sure that the board model obeys the causal relationship (output follows input).

These checks can be performed in any standard EDA simulator or extraction engine.

4.3 S-Parameter Inspection

Once the extracted S-parameters have been verified as causal and passive, the S-parameter plots must be inspected. TI recommends to check for the following:

- Insertion Loss: The single-ended insertion loss is recommended to stay within 0 to 10dB up to 3 times the Nyquist frequency of operation. For example, if the target frequency is 8Gbps (4GHz Nyquist), the single-ended insertion loss must stay under 10dB up to 12GHz.
- Return Loss: The single-ended return loss is recommended to be less than 15dB up to 3 times the Nyquist frequency.
- Near and Far end crosstalk (FEXT/NEXT): The FEXT and NEXT are recommended to be under 25dB for frequencies up to 3 times the Nyquist frequency.

The S-Parameter inspection plots are not pass or fail tests, but rather more of a guide to check if the design has a reasonable chance of performing a the required level.

4.4 Time Domain Reflectometry (TDR) Analysis

As a lot of the design fixes are targeted towards maintaining uniform trace impedance, an important analysis method used in assessing the quality of the design is the Time Domain Reflectometry (TDR) analysis. This plots the impedance of a trace as a function of length, as shown in Figure 4-1.

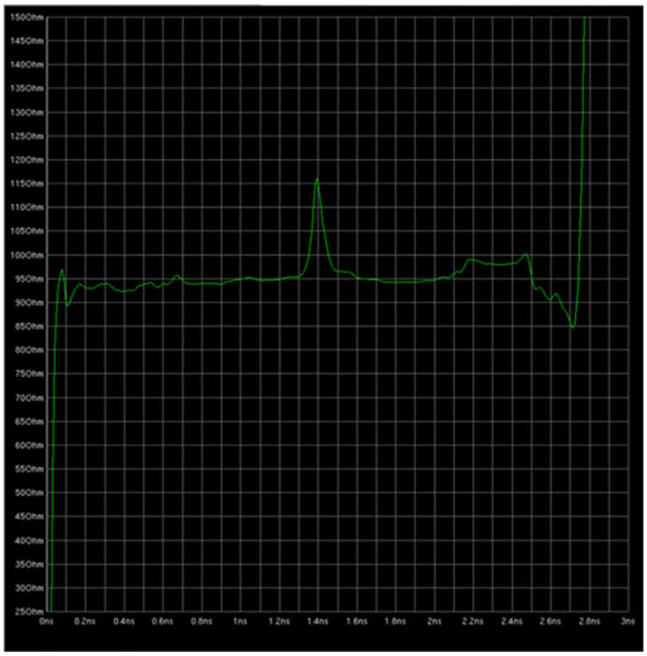


Figure 4-1. TDR Plot Example With Impedance Mismatch

As shown in Figure 4-1, the TDR plot highlights impedance discontinuities in the trace from one end to the other. This method depends on a reflected waveform from the far-end of the trace. The delay in the plot corresponding to a particular point in the trace actually corresponds to 2 times the distance of that point from the source, owing to the round trip time. This needs to be factored in for assessing the source of impedance discontinuities.

The TDR plot can be generated by reading in the S-parameter models generated by the extraction tool and assessing them in *Time-Domain* mode. A standard EDA simulator such as HyperLynx can perform this function. TI recommends to optimize the design to within a ± 5% deviation from the nominal trace impedance.

The TDR plots are not pass or fail tests, but rather is more of a guide to check if the design has a reasonable chance of performing a the required level.

4.5 System Level Simulation

The methodology for validating the DDR interface is outlined in this section. LPDDR4 interfaces, as defined in the JEDEC specification, uses eye masks defined at a target BER (Bit Error Rate) to determine pass or fail for signal integrity. This is essential to perform channel simulations using IBIS models to generate the signal eye diagrams at the targeted BER. These are introduced for memory interfaces starting from LPDDR4

4.5.1 Simulation Setup

Set up the system-level schematic in the simulator by connecting the SOC IBIS model, board model, power supplies, DRAM package model, and DRAM IBIS model. A typical system-level DDR schematic is shown in Figure 4-2.

Note

Be cautious of the DRAM configuration (number of dies in the package, number of ranks, and number of channels) while setting up the system schematic. Be cautious that the DRAM configuration can also include on-die decoupling circuit.

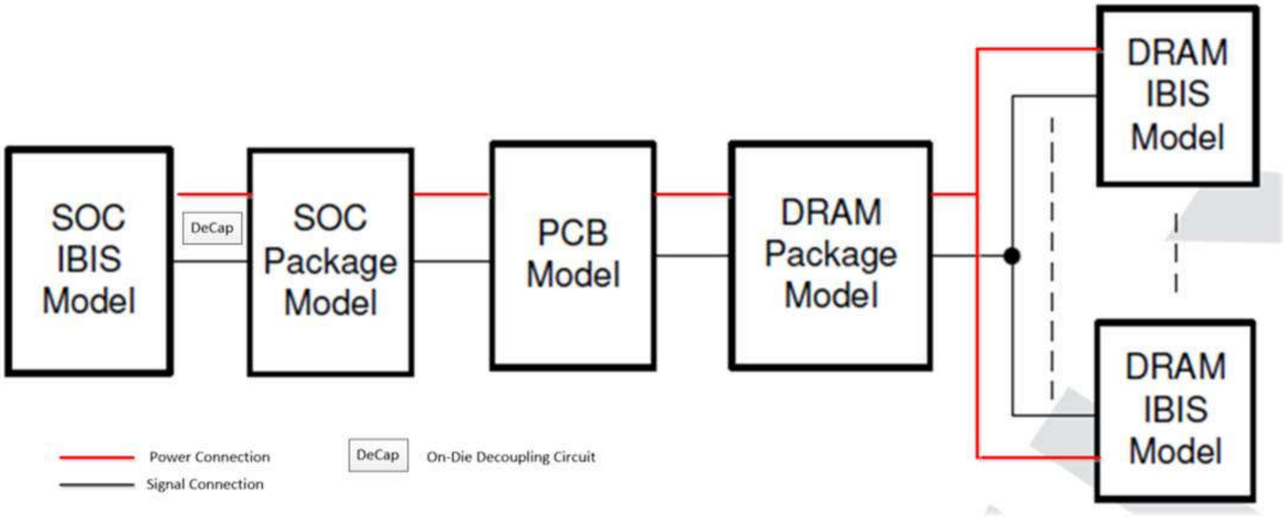


Figure 4-2. Typical System-Level DDR Schematic

- LPDDR4 simulations require power-aware IBIS models for the controller and the memory along with a simulator that supports channel simulations for DDR interfaces.
- SPICE-based transistor-level simulations cannot be used for generating BER signal eyes. Use a simulator that can handle power-aware IBIS simulations and can run channel simulations for the DDR interface.
- IBIS models reduce simulation time with minimal loss in accuracy compared with SPICE-based transistor-level simulations. IBIS models starting from version 5.0 are power-aware models which enables Simultaneous Switching Output (SSO) noise simulations. The TI IBIS model is a power-aware IBIS model.
- Use SPICE models to accurately model the on-die decoupling capacitance on the DDR supply net for both controller and DRAM. This makes sure of accurate power noise and Power Supply Induced Jitter (PSIJ) estimation in DDR simulations. The on-die decoupling capacitance information for the DRAM can be obtained from the DRAM vendor.
- Use SPICE or S-parameter files to model the DRAM package. This can be requested from the DRAM vendor. EBD models are not recommended.
- Note that inside the SoC IBIS model, there is a section for the package that contains an RLC matrix for all signal and power nets including DDR. TI recommends to use the SoC IBIS model, not the SOC package S-parameter model. When using SoC IBIS model, make sure to check the *Package Parasitics* (or equivalent parameter in the simulation tools) and use the *Package Model* model type which contains fully coupled L/C information on a per pin basis (denoted in the IBIS file as *[Package Model] am62_pkg*).

- AM62x, AM62Lx model for the on-die decoupling capacitance on the DDR supply net:
  - Data

```
******************************************
* On-die Decoupling circuit for AM62x,
                    AM62Lx (DIE_VDDS_DDR to VSS)
******************************************
* Notes:
* Includes on-die decoupling for all DDR signals
*
* This subcircuit must be added across the AM62x,
                    AM62Lx IBIS model's
* DIE_VDDS_DDR and VSS pins
*
******************************************
* x_decouple DIE_VDDS_DDR vss_die AM62x,
                    AM62Lx_ondie_decoupling_alldq
******************************************
.SUBCKTAM62x,
                    AM62Lx_ondie_decoupling_alldq DIE_VDDS_DDR vss_die
Cvddq_c  DIE_VDDS_DDR DIE_VDDS_DDR_c 1.324741e-9
Rvddq_c  vss_die DIE_VDDS_DDR_c 25.0036612e-3
.ENDS
```

  - Address/Command

```
******************************************
* On-die Decoupling circuit for AM62x,
                    AM62Lx (DIE_VDDS_DDR to VSS)
******************************************
* Notes:
* Includes on-die decoupling for all DDR signals
*
* This subcircuit must be added across the AM62x,
                    AM62Lx IBIS model's
* DIE_VDDS_DDR and VSS pins
*
******************************************
* x_decouple DIE_VDDS_DDR vss_die AM62x,
                    AM62Lx_ondie_decoupling_alldq
******************************************
.SUBCKTAM62x,
                    AM62Lx_ondie_decoupling_alldq DIE_VDDS_DDR vss_die
Cvddq_c  DIE_VDDS_DDR DIE_VDDS_DDR_c 4.335517e-9
Rvddq_c  vss_die DIE_VDDS_DDR_c 25.0036612e-3
.ENDS
```

4.5.2 Simulation Parameters

This is important to configure the simulation to exercise the system to real, but worst case parameters.

- Use the worst-case bit pattern to excite the system. The simulator is able to generate the worst-case bit pattern based on channel characterization.
- Select the controller and DRAM models (sets the drive strength, ODT, VOH levels, and so forth) from the IBIS files which work best for the system.
  - This is typically an iterative process.
  - Every system is unique and the best settings for these parameters can vary from system to system.

Table 4-1. Example Data Write ODI/ODT Optimization

Pkg Byte	Board	ODI Ω	ODT Ω	Total EW Margin (ps)	Total EH Margin (mV)B
B3	J7 370HR 10L Ref B3, No BD	40	40	50.28	15.66
B3	J7 370HR 10L Ref B3, No BD	40	48	27.62	11.76
B3	J7 370HR 10L Ref B3, No BD	40	40	33.52	2.92
B3	J7 370HR 10L Ref B3, No BD	48	48	1.54	0.86

- Data bus and address bus ODT and drive strength values can be set independently. As an example, the J7 EVM board (which supports LPDDR4 at similar speeds) used 40Ω ODT for data read and writes and 80Ω for CA bus. Drive strength of 40ohms for data read and write and CA.
  - Data READ Controller model - lpddr4_odt_40, lpddr4_odt_40_diff.
  - Data WRITE Controller model - lpddr4_ocd_40p_40n, lpddr4_ocd_40p_40n_diff.
  - CA/CLK Controller model - lpddr4_ocd_40p_40n, lpddr4_ocd_40p_40n_diff.
- Set up the channel simulation parameters. These typically consists of the data rate, ignore time/bits, minimum number of bits, bit sampling rate, BER floor, number of bits for display, types of BER eyes (voltage and/or timing), and target BER.
  - To determine the minimum number of bits one can run a series of channel simulations with different number of bits. The BER signal eye (and margins) tend to converge after a certain minimum number of bits. This helps determining the minimum number of bits to be used for the system.
  - Run channel simulations to generate the eye diagrams at LBER of -16.
- Run channel simulations with basic power settings at different PVT corners. TI recommends to run the simulations at least at the SSHT and FFLT corners.

4.5.3 Simulation Targets

Once the simulation successfully completes, generate the DDR analysis reports from the simulation tool. There are several different parameters to be verified, detailed in this section. Each parameter is pass or fail, meaning each must meet the specified target to make sure the design has sufficient margin to operate at the target data rates.

Use the appropriate JEDEC Vref parameters (Vref_min, Vref_max, Vref_step, and Vref_set_tol) and mask parameters (shape, height, width).

4.5.3.1 Eye Quality

The Vix_DQS ratio and Vix_CK ratio for data write and CA bus simulations are to be verified, at the DRAM pin/BGA. Figure 4-3 from the JEDEC specification explains how to measure the Vix ratio, as well as define the ration requirements.

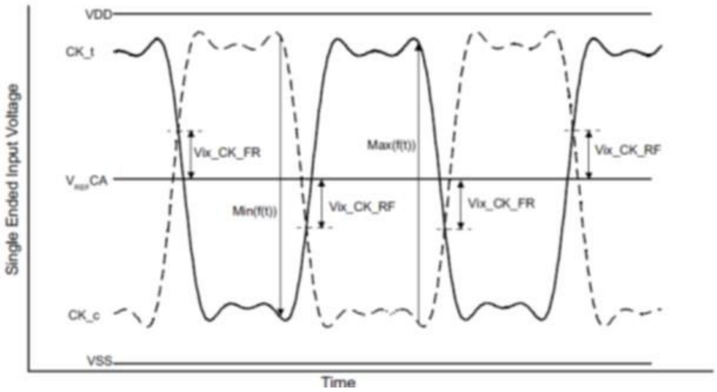


Figure 4-3. Vix_CK and Vix_DQS Ratio for Eye Quality

Table 4-2. Vix_CK and Vix_DQS Ratio for Eye Quality

Symbol	Data Rate						Unit	Note
	1600/1867		2133/2400/3200		3733/4266			
Vix_CK_ratio	-	25	-	25	-	25	%	(1), (2)
Vix_DQS	-	20	-	20	-	20	%	(1), (2)

(1) Vix_CK_Ratio is defined by the equation: Vix_CK_Ratio = Vix_CK_FR|Min(f(t))|
(2) Vix_CK_Ratio is defined by the equation: Vix_CK_Ratio = Vix_CK_RF|Min(f(t))|

4.5.3.2 Delay Report

The required interconnect delays for DQ, DQS, CA, and CLK are listed in Section 3.14 and Section 3.15. The values listed as *Typical* are only recommendations. Any minimum or maximum value is a requirement. One key requirement is to make sure the CK delay is greater than any DQS delay - refer to LP4_DRS3 in Section 3.15. DQSx delays are recommended to be less than the DQ and DM delays in the respective BYTEx - refer to LP4_DRS6 in Section 3.15.

Consider the delays of the complete system from SOC die pad, through the PCB, to the pins of the memory package. For example, to satisfy skew within net class DQSx and skew within net class CK0, the P and N differential trace lengths on the PCB need to offset any delay mismatching within the package. Refer to LP4_DRS4 in Section 3.15 and to LP4_ACRS3 in Section 3.14. Refer to the respective package delays in Section 5.

4.5.3.3 Mask Report

The minimum jitter and noise margins are to be captured with respect to the eye masks. This masks are data rate dependent, and includes:

- Data read eye mask at the SOC die pad for functionality testing.
- Data write eye mask (JEDEC spec) at the DRAM pin/BGA for compliance testing.
- CA bus eye mask (JEDEC spec) at the DRAM pin/BGA for compliance testing.

There is at least two sets of eye diagrams generated by the simulator:

- Vref set to the best Vref of the byte offset by the Vref_set_tol in the positive direction (Vref_set_tol is defined in JEDEC spec).
- Vref set to the best Vref of the byte offset by the Vref_set_tol in the negative direction.

The system-level margins are the worst case noise and jitter margins from all eye diagram measurements listed above (across SSHT and FFLT corners). For all waveforms captured at the DRAM device, margins must be calculated at both the BGA pin and the DRAM pad.

Table 4-3. LPDDR4 Eye Mask Definitions/Requirements

Parameter	Mask Shape	LPDDR4-1600	LPDDR4-3200	LPDDR4-3733
CA eye mask TcIVW	Rectangular (1)	0.3 UI	0.3 UI (1)	(2)
CA eye mask VcIVW	Rectangular (1)	175mV	155mV (1)	(2)
Write eye mask TdIVW	Rectangular (1)	0.22 UI	0.25 UI (1)	(2)
Write eye mask VdIVW	Rectangular (1)	140mV	140mV (1)	(2)
Read eye mask TdIVW	Diamond	0.42 UI	0.61 UI	0.66 UI
Read eye mask VdIVW	Diamond	140mV	140mV	140mV

(1) Copied from JEDEC specification: Low Power Double Date Rate 4 (LPDDR4).
(2) For details, contact the DRAM vendor.

Figure 4-4 through Figure 4-6 show the eye mask definitions translated to eye diagrams within captured waveforms.

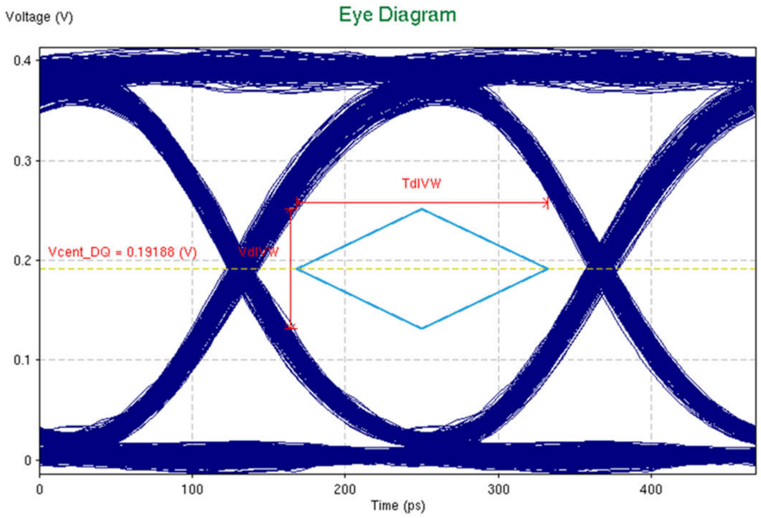


Figure 4-4. Example Simulated LPDDR4-4266 Read Eye With Diamond-Shaped Eye Mask

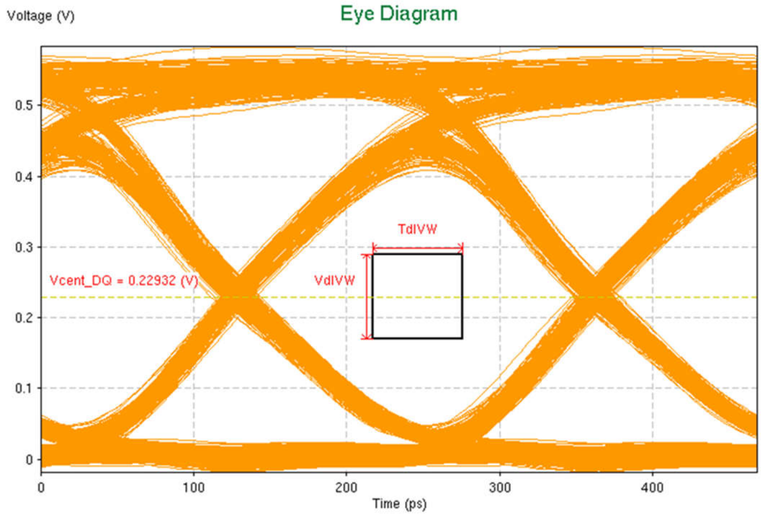


Figure 4-5. Example Simulated LPDDR4-4266 Write Eye With Rectangular JEDEC Eye Mask

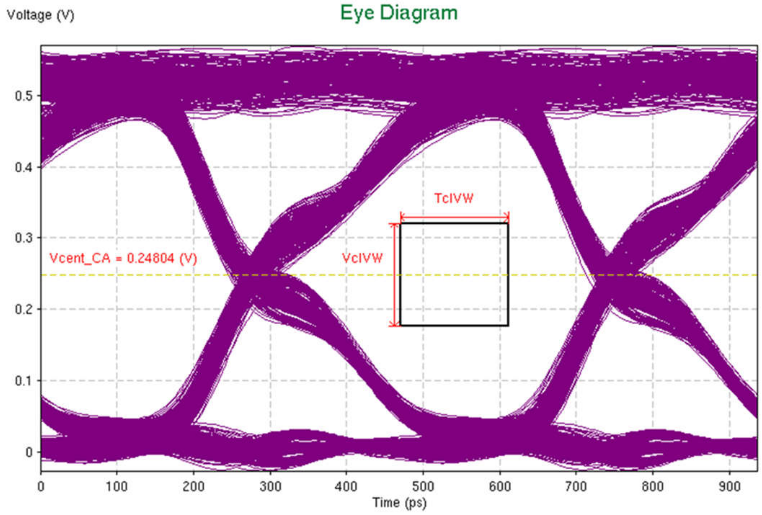


Figure 4-6. Example Simulated LPDDR4-4266 CA Eye With Rectangular JEDEC Eye Mask

4.6 Design Example

4.6.1 Stack-Up

These guidelines recommend a 8- or 6-layer PCB stack-up for full device entitlement. Below are 8- and 6-layer example stack-ups:

- Designs using FR4 products like 370HR are supported, but also recommend higher speed materials like ISOLA I-Speed (or equivalent) for increased margin. IT180A is also another material to help with cost vs. performance tradeoffs
- These examples routes all data groups on layer 3. While this minimizes the via travel and, therefore, reduces via-to-via coupling, but leaves a longer via stub.
- These examples routes all CA signals on the bottom layer.

Table 4-4. Example 8-layer PCB Stackup for LPDDR4 (PROC124 AM62x LP SK EVM)

Layer No	Stackup	Routing Plan Highest Priorities and Layer
	Solder mask	
1	TOP - SIG/PWR	BGA breakouts, GND, DRAM decoupling capacitors
2	GND	Solid GND reference plane
3	SIG/PWR	LPDDR4 Data, VDD1_LPDDR4_1V8, LVCMOS escape
4	PWR	VDD_LPDDR4 (under SOC and LPDDR4), SOC_DVDD1V8, VDDA_1V8
5	PWR	VDD_CORE, SOC_DVDD3V3, VCC_3V3_SYS, VPP_1V8, VDDA_1V8_OSC
6	SIG	LVCMOS escape
7	GND	Solid GND reference plane
8	BOTTOM - SIG/PWR	LPDDR4 CA, LVCMOS escape, SOC decoupling capacitors, GND, DRAM decaps
	Solder mask	

Table 4-5. Example 6-layer PCB Stackup for LPDDR4 (PROC181 AM62Lx EVM)

Layer No	Stackup	Routing Plan Highest Priorities and Layer
	Solder mask	
1	TOP - SIG/PWR	BGA breakouts, VDD_LPDDR4 to DRAM, VDD_LPDDR4 bulk capacitors
2	GND	Solid GND reference plane
3	SIG/PWR	LPDDR4 Data, LVCMOS escape, SOC_DVDD3V3, SOC_DVDD1V8, VDDA_1V8
4	PWR	VDD_CORE, VDD_LPDDR4 (under SOC and LPDDR4), VDDA_1V8
5	GND	Solid GND reference plane
6	SIG/PWR	LPDDR4 CA, LVCMOS escape, SOC/DRAM decoupling capacitors, VDD1_LPDDR4_1V8, DRAM test points
	Solder mask	

4.6.2 Routing

The examples below from a J7 design show the LPDDR4 Clock and CA routing on an example 10-layer PCB design. The clock is routed differentially with target impedance of 70Ω. For the T-branch to match the impedance of the trace, the impedance needs to be doubled. This can create challenges, as the higher impedances can be difficult to achieve in some PCB stackups. The CA signals are routed targeting 35Ω, with the T-branch at two times the source impedance.

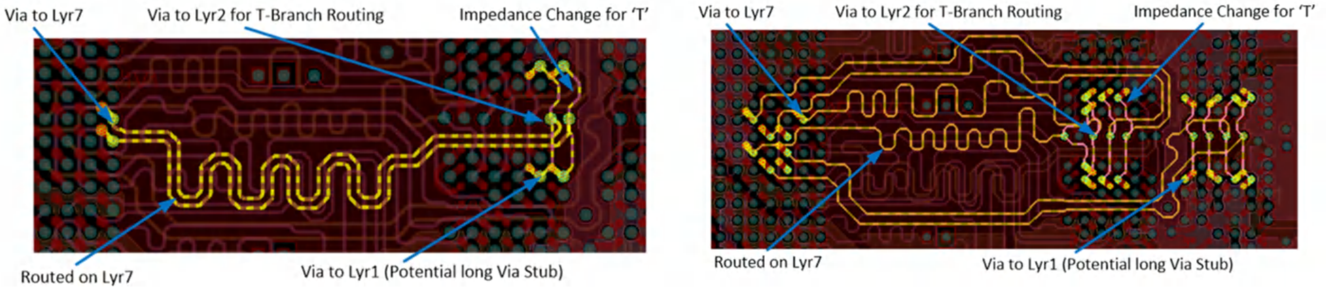


Figure 4-7. Example LPDDR4 Clock and CA Routing

On the same 10 layer reference design, the data groups are routed on layers 2 and 4. The upper layers are used due to the minimum via travel, which minimized the via inductance and via-to-via coupling. Because the data signals are point-to-point, T-branch routing is not required.

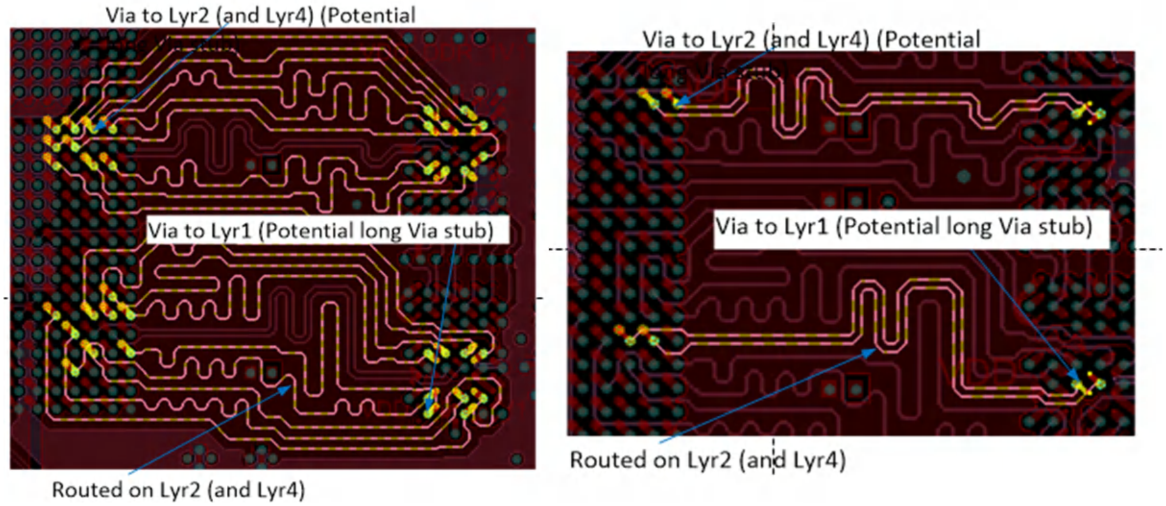


Figure 4-8. Example LPDDR4 Data Bytes and DQSs Routing

Table 4-6. LPDDR4 Performance Impact on Routing Layer (Read at pad)

Routing Layer	Via Type	Back Drilling	EW Margin (ps)	EH Margin (mV)
L1, L12	PTH	No	-7.10	56.72
L1, L12	PTH	Yes	-4.86	55.71
L1, L3	PTH	No	5.70	40.29
L1, L3	PTH	Yes	8.37	34.54

Table 4-7. LPDDR4 Performance Impact on Routing Layer (Write at pad)

Routing Layer	Via Type	Back Drilling	EW Margin (ps)	EH Margin (mV)
L1, L12	PTH	No	17.42	39.22
L1, L12	PTH	Yes	20.04	41.93
L1, L3	PTH	No	27.66	41.37
L1, L3	PTH	Yes	27.76	48.63

4.6.3 Model Verification

Before simulating, TI recommends to verify the models. One verification method described is the impedance plot (or impedance scan). The impedance scans for a 10 layer design are provided.

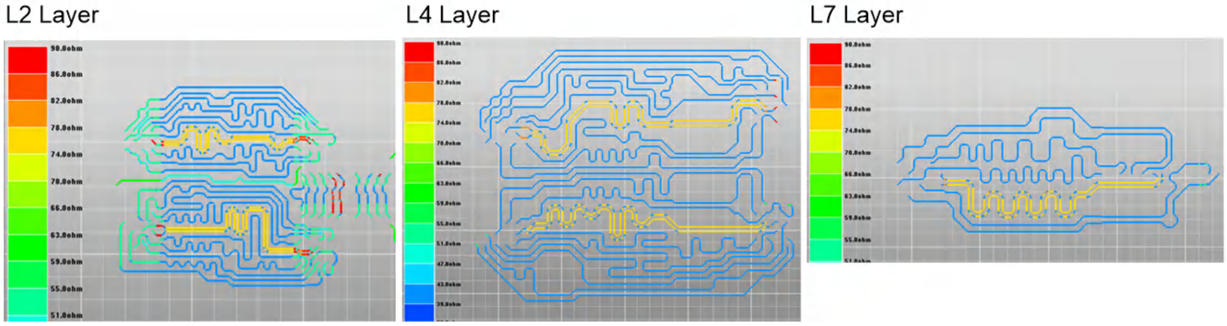


Figure 4-9. Example LPDDR4 Trace Impedance Scan

Table 4-8. Example LPDDR4 Trace Impedance Summary for Data

Layer	DDR Bus	DQ SE Impedance (Ω)	DQS/CLK Difference Impedance (Ω)
L2	B1 and B3	40.9	77.7
L2	CA	51.7	101.4
L4	B0 and B2	41.1	77.7
L7	CA	41.1	77.7

For CK and CA signals, the goal is to have the branch segment equal to two times the impedance of the feed trace. Note, this is common for the PCB to limit the achievable impedances. Simulations show users if the compromises are acceptable.

Table 4-9. Example LPDDR4 Trace Impedance Summary for CA

Board	CA Feed Impedance (Ω)	CA Branch Impedance (Ω)	CA Branch Target (Ω)	Impedance Mismatch (Ω)
Initial Design	49.1	59.6	98 (49x2)	19.3
Final Design	41.1	51.7	82 (41x2)	15.3

The simulation results show the improvement made by closer matching the impedances to the targets.

Table 4-10. Example LPDDR4 Simulation Results From Improved Trace Impedance

Board	Total Eye Width Margin (ps)	Total Eye Height Margin (ps)
Initial Design	58.00	14.00
Final Design	124.68	48.08

4.6.4 Simulation Results

The simulation results are provided for the LPDDR4 interface from a 10 layer design. These simulation targets must be met to make sure the design operates at the desired level of performance.

CA simulations need to be verified at the DRAM pin or BGA. This includes:

- Vix_CK ratio (JEDEC).
- Jitter and noise margins with respect to the eye mask (JEDEC).
- Peak-peak power noise.

At DRAM Pin:

Jitter/Noise Eye Margins

Vix_CA Ratio

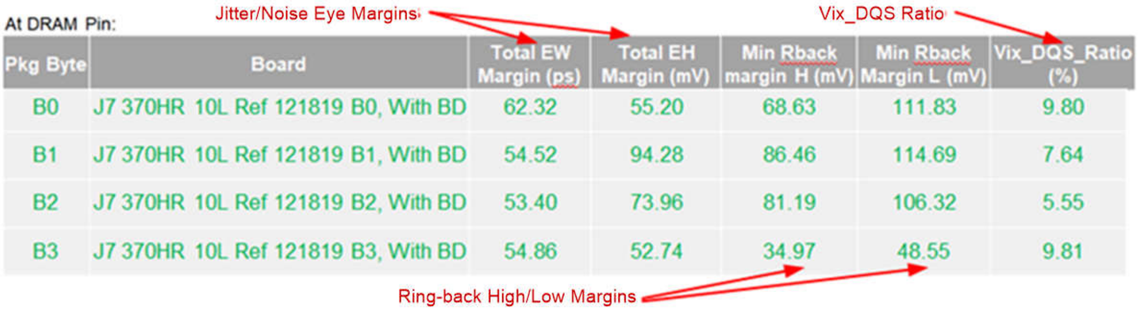
Package	Board	Total EW Margin (ps)	Total EH Margin (mV)	Min Rback Margin H (mV)	Min Rback Margin L (mV)	Vix_CK Ratio (%)
J7 SCK 1207	J7 370HR 10L Ref 121819 ACC, No BD, Slwave	182.04	68.50	89.43	25.50	16.81

Ring-back High/Low Margins

Figure 4-10. LPDDR4 Simulation Results for CA

Data write simulations need to be verified at both the DRAM BGA pin and the DRAM pad. This includes:

- Vix_CK ration (JEDEC).
- Jitter and noise margins with respect to the eye mask (JEDEC).
- Peak-peak power noise.



At DRAM Pin:

Jitter/Noise Eye Margins

Vix_DQS Ratio

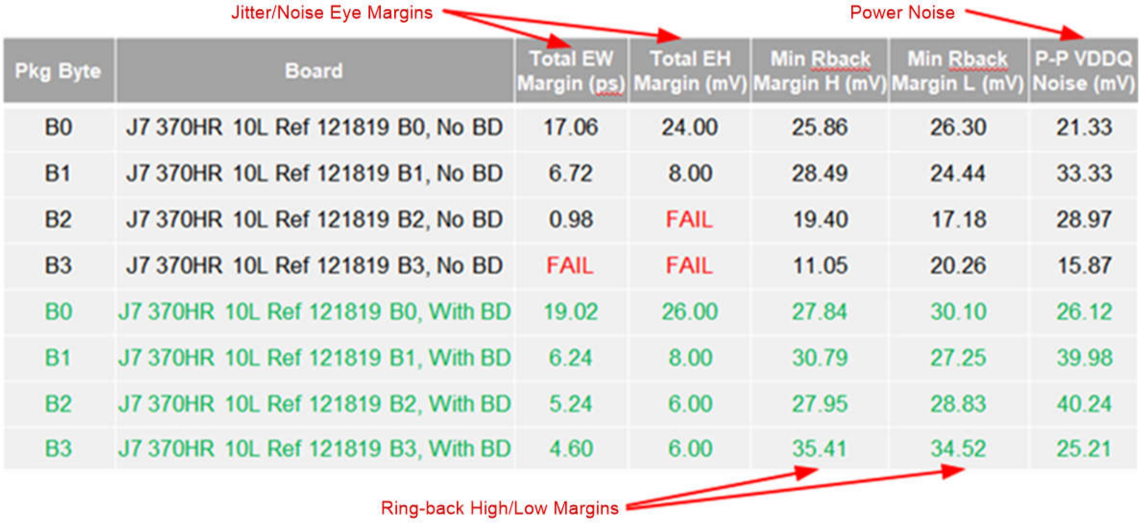
Pkg Byte	Board	Total EW Margin (ps)	Total EH Margin (mV)	Min Rback margin H (mV)	Min Rback Margin L (mV)	Vix_DQS_Ratio (%)
B0	J7 370HR 10L Ref 121819 B0, With BD	62.32	55.20	68.63	111.83	9.80
B1	J7 370HR 10L Ref 121819 B1, With BD	54.52	94.28	86.46	114.69	7.64
B2	J7 370HR 10L Ref 121819 B2, With BD	53.40	73.96	81.19	106.32	5.55
B3	J7 370HR 10L Ref 121819 B3, With BD	54.86	52.74	34.97	48.55	9.81

Ring-back High/Low Margins

Figure 4-11. LPDDR4 Simulation Results for Write

Data read simulations need to be verified at SOC. This includes:

- Jitter and noise margins with respect to the eye mask.
- Peak-peak power noise.



Jitter/Noise Eye Margins

Power Noise

Pkg Byte	Board	Total EW Margin (ps)	Total EH Margin (mV)	Min Rback Margin H (mV)	Min Rback Margin L (mV)	P-P VDDQ Noise (mV)
B0	J7 370HR 10L Ref 121819 B0, No BD	17.06	24.00	25.86	26.30	21.33
B1	J7 370HR 10L Ref 121819 B1, No BD	6.72	8.00	28.49	24.44	33.33
B2	J7 370HR 10L Ref 121819 B2, No BD	0.98	FAIL	19.40	17.18	28.97
B3	J7 370HR 10L Ref 121819 B3, No BD	FAIL	FAIL	11.05	20.26	15.87
B0	J7 370HR 10L Ref 121819 B0, With BD	19.02	26.00	27.84	30.10	26.12
B1	J7 370HR 10L Ref 121819 B1, With BD	6.24	8.00	30.79	27.25	39.98
B2	J7 370HR 10L Ref 121819 B2, With BD	5.24	6.00	27.95	28.83	40.24
B3	J7 370HR 10L Ref 121819 B3, With BD	4.60	6.00	35.41	34.52	25.21

Ring-back High/Low Margins

Figure 4-12. LPDDR4 Simulation Results for Read

The simulations results for read includes two sets for data, black and green. The black shows the design failed, as several bytes failed to meet the eye margins. The green is the simulation results of the same design, but with back-drilling the via stubs applied.

5 Additional Information: Package Delays

The package delays provided in this appendix are measured from SOC die pad to SOC package pin. The skew limits specified in Table 3-6 and Table 3-7 are measured from SOC die pad to DRAM package pin (including these delays inside the SOC package). The designer can sum these package delays with the PCB delays for each net when checking for compliance with the skew limits. Simulations of the propagation delays are then required to confirm the delays satisfy the requirements.

PROCESSOR PIN NAME	AM62x ALW PACKAGE DELAY (ps)	AM62x AMC PACKAGE DELAY (ps)	AM62Lx ANB PACKAGE DELAY (ps)	NET CLASS	DESCRIPTION
DDR0_A0	21.00	28.55	13.44	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A1	19.94	26.82	15.17	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A2	16.13	26.60	10.20	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A3	11.28	26.33	19.40	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A4	11.62	26.52	22.22	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A5	20.98	26.43	15.29	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A6	17.04	33.55	18.29	ADDR_CTRL	Used with DDR4
DDR0_A7	19.08	31.69	6.79	ADDR_CTRL	Used with DDR4
DDR0_A8	21.55	34.42	15.59	ADDR_CTRL	Used with DDR4
DDR0_A9	13.33	34.25	19.06	ADDR_CTRL	Used with DDR4
DDR0_A10	10.71	32.94	12.39	ADDR_CTRL	Used with DDR4
DDR0_A11	9.00	27.28	12.31	ADDR_CTRL	Used with DDR4
DDR0_A12	9.33	29.79	18.92	ADDR_CTRL	Used with DDR4
DDR0_A13	23.19	31.52	20.24	ADDR_CTRL	Used with DDR4
DDR0_ACT_n	7.98	32.68	17.13	ADDR_CTRL	Used with DDR4
DDR0_ALERT_n	17.37	32.54	-	N/A	Used with DDR4
DDR0_BA0	19.81	26.29	15.83	ADDR_CTRL	Used with DDR4
DDR0_BA1	21.85	27.00	17.80	ADDR_CTRL	Used with DDR4
DDR0_BG0	15.30	27.61	9.85	ADDR_CTRL	Used with DDR4
DDR0_BG1	17.09	26.62	12.79	ADDR_CTRL	Used with DDR4
DDR0_CAS_n	11.81	26.42	20.78	ADDR_CTRL	Used with DDR4
DDR0_CK0	23.03	34.72	27.15	CK0	Used with LPDDR4 and DDR4
DDR0_CK0_n	21.28	33.13	20.98	CK0	Used with LPDDR4 and DDR4
DDR0_CKE0	20.94	29.26	20.75	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_CKE1	13.68	31.10	-	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_CS0_n	7.80	28.47	16.09	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_CS1_n	18.29	35.18	-	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_DM0	13.95	35.06	31.18	BYTE0	Used with LPDDR4 and DDR4
DDR0_DM1	19.07	28.18	20.84	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ0	16.90	37.82	16.79	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ1	14.21	29.20	20.41	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ2	20.40	31.14	28.20	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ3	17.67	28.54	25.53	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ4	23.82	38.78	18.77	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ5	21.95	32.97	18.96	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ6	24.74	35.55	23.02	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ7	24.31	33.64	21.21	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ8	23.28	34.75	17.35	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ9	18.16	32.35	18.46	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ10	19.18	32.72	20.21	BYTE1	Used with LPDDR4 and DDR4

PROCESSOR PIN NAME	AM62x ALW PACKAGE DELAY (ps)	AM62x AMC PACKAGE DELAY (ps)	AM62Lx ANB PACKAGE DELAY (ps)	NET CLASS	DESCRIPTION
DDR0_DQ11	17.78	37.01	26.20	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ12	20.45	35.22	16.41	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ13	16.68	32.03	14.95	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ14	24.67	29.99	20.07	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ15	21.39	26.31	22.73	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQS0	27.23	40.21	23.77	DQS0	Used with LPDDR4 and DDR4
DDR0_DQS0_n	27.39	40.92	24.48	DQS0	Used with LPDDR4 and DDR4
DDR0_DQS1	21.74	39.71	23.32	DQS1	Used with LPDDR4 and DDR4
DDR0_DQS1_n	22.68	41.12	22.39	DQS1	Used with LPDDR4 and DDR4
DDR0_ODT0	29.40	29.31	13.32	ADDR_CTRL	Used with DDR4
DDR0_ODT1	18.45	30.02	-	ADDR_CTRL	Used with DDR4
DDR0_PAR	25.10	28.63	-	ADDR_CTRL	Used with DDR4
DDR0_RAS_n	10.64	28.63	11.54	ADDR_CTRL	Used with DDR4
DDR0_RESET0_n	31.66	32.77	19.01	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_WE_n	15.43	31.72	18.49	ADDR_CTRL	Used with DDR4

6 Summary

This application note describes how to plan, route, and simulate a PCB for successful LPDDR4 or DDR4 operation on AM62x, AM62Lx processor designs. Specifications are provided for the clock and address or control signal group and data group topologies. Designing to these metrics helps to achieve a board layout with first-pass success. The LPDDR4 simulation section of this application note documents a procedure for confirming an LPDDR4 layout meets the requirements for a robust system before board fabrication. The topics of board model extraction, drive-strength and termination optimization, system-level simulation, and eye mask minimums are presented with examples from actual board designs.

7 References

- Texas Instruments, AM62x Starter Kit User's Guide
- Texas Instruments, AM62x Low-Power SK EVM User’s Guide
- Texas Instruments, AM62L EVM User’s Guide

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2024) to Revision C (March 2025) **Page**

- Added information for AM62Lx.......... 1
- Added specified minimum processor HS bypass capacitor count and capacitance.......... 6
- Added note that AM62Lx does not support dual-rank.......... 8
- Added note to *16-Bit, Single-Rank DDR4 Implementation Using x16 SDRAM* figure.......... 9
- Added note to *16-Bit, Dual-Rank DDR4 Implementation Using x8 SDRAMs* figure.......... 11
- Added examples to clarify bit swaps.......... 21
- Added note to *16-Bit, Single-Rank, Single Channel LPDDR4 Implementation* figure.......... 22
- Added clarification and examples for the PCB need to offset delay mismatching.......... 35
- Changed Jacinto, AM62Ax, and AM62Px stackup info with AM62 and AM62L EVMs stackup info.......... 37
- Added AM62Lx ANB package delays.......... 42

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