参考資料

Design Guide: TIDA-010080

5G テレコム整流器向け、500W、高効率 (94.5% 超)、アナログ制御 AC/DC のリファレンス・デザイン

概要

このコンパクトな高効率リファレンス・デザインは、48V DC、500W を出力するもので、5G のテレコム電源と産業用 AC/DC 電源をターゲットにしています。この回路は、UCC28180 デバイスをベースとするフロントエンド連続導通モード (CCM) 力率補正 (PFC) 回路と、その後段にあって UCC256403 をベースとした絶縁型 DC/DC コンバータ向けの堅牢な LLC 段で形成されています。高効率のニーズを満たすために、UCC24624 を使用して同期整流を処理しています。このリファレンス・デザインは、UCC28911 (高電圧 MOSFET を内蔵) による補助電源フライバックを使用しています。このリファレンス・デザインは 94.5% のピーク効率を実現しているため、システムは強制冷却を使わずに動作できます。このシステム全体は、30% 負荷で 12% 未満、50% 負荷で 8% 未満、100% 負荷で 5.5% 未満と THD が小さく、負荷過渡特性も優れています。

特長

- ピーク効率:94.5% (V_{AC} = 230V)
- CCM PFC とハーフブリッジ LLC を採用 (UCC28180、UCC256403)
- 低 THD:30% 負荷で 12% 未満、50% 負荷で 8% 未満
- 100% 負荷で 5.5% 未満
- 高力率 (PF):0.95 超 (30%～100% 負荷、高ライン電圧時)
- 優れた負荷過渡性能:1% 未満
- レギュレーション
- 受動的冷却

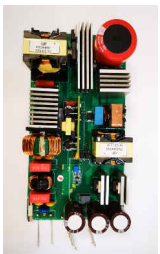
アプリケーション

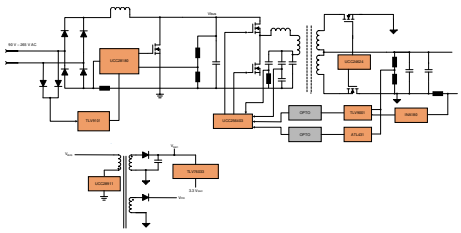
- 商用テレコム整流器
- 産業用 AC/DC
- 商用バッテリ・チャージャ

リソース

TIDA-010080	デザイン・フォルダ
UCC28180、UCC256403	プロダクト・フォルダ
UCC24624、INA180	プロダクト・フォルダ
TLV9101、TLV9001	プロダクト・フォルダ
UCC28911、TLV760	プロダクト・フォルダ
ATL431	プロダクト・フォルダ

TI の TI E2E™ サポート・エキスパートにお問い合わせください。





1 System Description

This compact, high-efficiency AC/DC reference design has a 48-V DC, 500-W output at 230 V_{AC}. The circuit consists of a front-end continuous conduction mode (CCM) power factor correction (PFC) circuit based on the UCC28180 device, followed by a robust LLC stage for an isolated DC/DC converter based on the UCC256403. For high-efficiency needs, synchronous rectification is done with the UCC24624. This design uses an auxiliary power supply flyback with the UCC28911 which has an internal high-voltage MOSFET (HV MOS). This design enables 94.5% peak efficiency and allows the system to work without forced cooling. This design has low THD, with 30% load at < 12%, 50% load at < 8%, 100% load at < 5.5%, and good load transient performance.

1.1 Key System Specifications

表 1-1 displays the key system specifications.

表 1-1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage		90	230	265	VAC
Frequency		47	50	63	Hz
OUTPUT CONDITIONS					
Output voltage		44	48	52	V
Output current	V_O = 48-V		10.5		A
Line regulation	V_O = 48 V			0.5	%
Load regulation	V_O = 48 V			0.5	%
Output voltage ripple	V_O = 48 V, Peak-Peak			500	mV
Output power (nominal)				500	W
SYSTEM CHARACTERISTICS					
Efficiency	V_{IN} = 230-V_{AC} RMS and full load at 48-V output		94.5		%
	V_{IN} = 115-V_{AC} RMS and full load at 48-V output		92		%
Protections	Output overcurrent		Latch		
	Output overvoltage		AR		
Operating ambient	Open frame	–10	25	55	°C
Standards and norms	Power line harmonics (THD)	IEC 61000-3-2 Class A			
	Conducted emissions	EN 55022 Class B			
	EFT	As per IEC 61000-4-4			
	Surge	As per IEC 61000-4-5			
Board form factor (FR4 material, 2 layer)	Length × Width × Height	185 × 95 × 38			mm

2 System Overview

2.1 Block Diagram

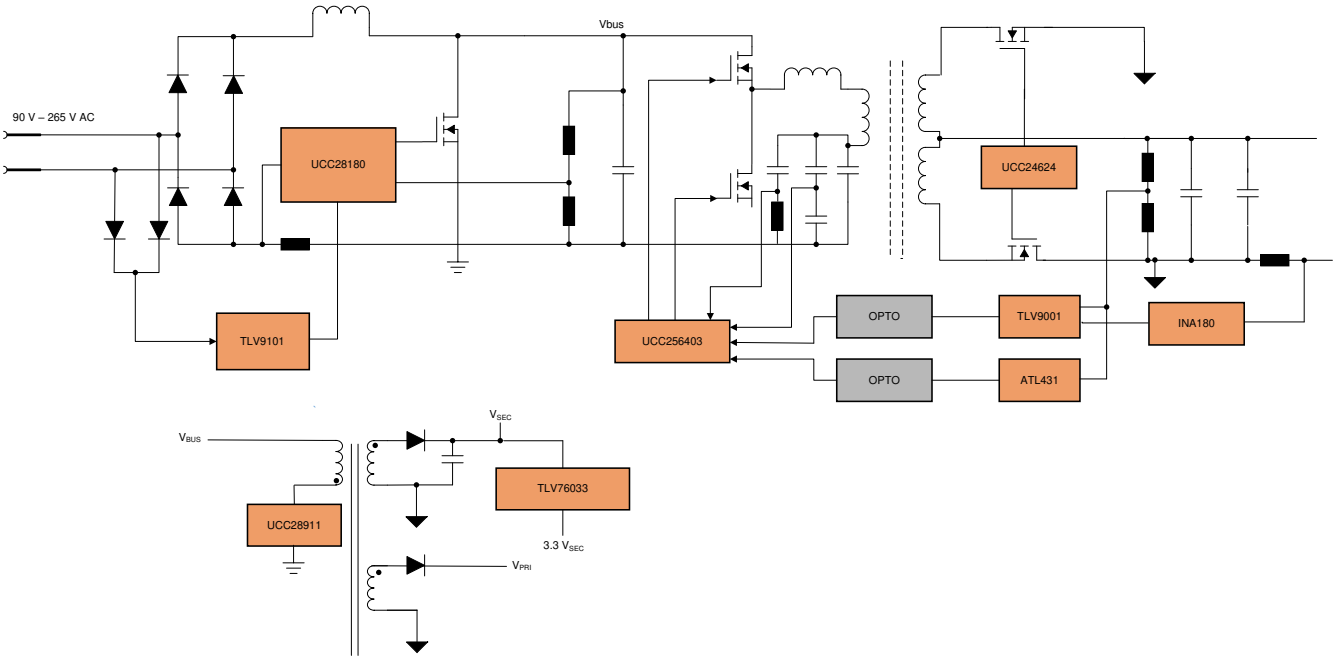


図 2-1. TIDA-010080 System Block Diagram

2.2 Design Consideration

This design targets high-efficiency low-cost applications for small cell 5G telecom rectifiers as well as industrial power, which require natural cooling applications. The design is demonstrated with TI CCM PFC controller UCC28180 plus LLC controller UCC256403 together with UCC24624 synchronous rectifier to achieve high efficiency, and meanwhile maintain simple and easy design.

2.3 Highlighted Products

The following highlighted products are used in this reference design. These sections also highlight the key features for selecting the devices for this reference design. For the complete details of these highlighted devices, see the respective product data sheet.

2.3.1 UCC28180

The UCC28180 is a high-performance, continuous conduction mode (CCM), 8-pin programmable frequency power factor correction (PFC) controller. The wide and programmable operating frequency of the controller provides flexibility to design at a high frequency to optimize the components. The UCC28180 uses trimmed current loop circuits to achieve less than a 5% THD from a medium-to-full load (50% to 100%). A reduced current sense threshold enables the UCC28180 device to use a 50% smaller shunt resistor, resulting in lower power dissipation while maintaining low THD. The UCC28180 also consists of an integrated fast gate driver, with a drive of 2-A source current and –1.5-A sink current, which eliminates the need for an external gate driver. The UCC28180 device also has a complete set of system protection features that greatly improves reliability and further simplifies the design:

- Soft overcurrent
- Cycle-by-cycle peak current limit
- Output overvoltage
- VCC undervoltage lockout (UVLO) protection
- Open pin protections (ISENSE and VSENSE pins)

2.3.2 UCC25640X

An LLC resonant converter is one of the most widely used topologies for implementing medium- to high- power, isolated, DC/DC power stages in industrial power supplies. These converters are popular due to their ability to achieve soft-switching (ZVS turn on) for the high-voltage MOSFET and hence improving the overall efficiency of the system. The UCC25640x is a fully featured LLC controller. The UCC25640x includes a range of features designed to make LLC converter operation well controlled and robust. The part aims to unburden the LLC designer and allow mainstream applications to benefit from efficiency advantages of the LLC topology. This device uses hybrid hysteretic control to provide best-in-class line and load transient response. The control effort is approximately linear proportional to the average input current in one cycle. The control makes the open loop transfer function a first-order system so that it is very easy to compensate. The system is always stable with proper frequency compensation. Ensure that the LLC converter does not enter capacitive (ZCS) region during the low input voltage condition; otherwise, it could make damage to the system.

The UCC25640x with its ZCS avoidance feature can ensure that the system does not enter the ZCS region under all operating conditions and hence ensures the safety of the system. Apart from this, the power supplies typically need a tunable input or output voltage with a wide range. The UCC25640x provides a wide operating frequency range from 35 kHz to 1MHz to make it easier to design a wide output voltage range using an LLC converter. Its wide frequency range can reduce the PFC bulk capacitor required to meet the holdup time requirement in the industrial power supplies. With the integrated high- voltage gate drive, X-Cap discharge function, and additional output OVP, the UCC256401x reduces the amount of external discreet components required to implement a high-efficiency industrial PSU.

2.3.3 UCC24624

The UCC24624 high-performance synchronous rectifier (SR) controller is dedicated for LLC resonant converters to replace the lossy diode output rectifiers with SR MOSFETs and improve the overall system efficiency. Two independent SR control channels are integrated into the single package to minimize the external components and allow for easy PCB layout.

The UCC24624 SR controller uses drain-to-source voltage sensing method to achieve on and off control of the SR MOSFET. Proportional gate drive is implemented to extend the SR conduction time, minimize the body diode conduction time, and improve efficiency. To compensate for the offset voltage caused by the SR parasitic inductance, the UCC24624 implements an adjustable positive turn-off threshold to accommodate different SR MOSFET packages. The UCC24624 has a built-in 450-ns minimum on-time blanking and a fixed 650-ns minimum off-time blanking to avoid SR false turn-on and -off. The UCC24624 also integrates a two-channel interlock function that prevents the two SRs from being on at the same time.

With the built-in standby mode detection based on average switching frequency, the UCC24624 enters the sleep mode automatically without using external components. The low standby mode current of 175 µA supports meeting modern no-load standby power requirements such as CoC and DoE regulations.

With a 1.5-A peak source and 4-A peak sink driving capability, the UCC24624 is able to support LLC converters up to 1-kW. With 230-V voltage-sensing pins and a 26-V maximum VDD rating, it can be directly used in converters with an output voltage of up to 26 V. The internal clamp allows the controller to support a 36-V output voltage easily by adding an external current limiting resistor on VDD.

2.3.4 INA180

The INA180, INA2180, and INA4180 (INAx180) current sense amplifiers are designed for cost optimized applications. These devices are part of a family of current-sense amplifiers (also called current shunt monitors) that sense voltage drops across current-sense resistors at common-mode voltages from –0.2 V to +26 V, independent of the supply voltage. The INAx180 integrate a matched resistor gain network in four, fixed-gain device options: 20 V/V, 50 V/V, 100 V/V, or 200 V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift. All these devices operate from a single 2.7-V to 5.5-V power supply. The single-channel INA180 draws a maximum supply current of 260 µA; whereas, the dual-channel INA2180 draws a maximum supply current of 500 µA, and the quad channel draws a maximum supply current of 900 µA. The INA180 is available in a 5-pin, SOT-23 package with two different pin configurations. The INA2180 is available in 8-pin, VSSOP and WSON packages. The INA4180 is available in a 14-pin, TSSOP package. All device options are specified over the extended operating temperature range of –40°C to +125°C.

2.3.5 TLV760

The TLV760 is an integrated linear-voltage regulator featuring operation from an input as high as 30 V. The TLV760 has a maximum dropout of 1.2 V at the full 100-mA load across operating temperature. Standard packaging for the TLV760 is the 3-pin SOT23 package. The TLV760 is available in 3.3 V, 5 V, 12 V and 15 V. The SOT-23 packaging of the TLV760 series allows the device to be used in space-constrained applications. The TLV760 is a small size alternative to LM78Lxx series and similar devices. The TLV760 is designed to bias digital and analog circuits in applications that are subject to voltage transients and spikes up to 30 V — for example, appliances and automation applications. The device has robust internal thermal protection, which protects itself from potential damage caused by conditions like short to ground, increases in ambient temperature, high load, or high dropout events.

2.3.6 TLV9001

The TLV900x family includes single (TLV9001), dual (TLV9002), and quad-channel (TLV9004) low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. This op amp provides a cost-effective solution for space-constrained applications where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the TLV900X is 500 pF, and the resistive open loop output impedance makes stabilization easier with much higher capacitive loads. This op amp is designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications. The robust design of the TLV900X simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions. Micro-size packages, such as SOT-553 and WSON, are offered, along with industry- standard packages such as SOIC, MSOP, SOT-23, and TSSOP packages.

2.3.7 TLV9101

The TLV910x family (TLV9101, TLV9102, and TLV9104) is a family of 16-V general purpose operational amplifiers. This family offers excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±300 µV, typ), low offset drift (±0.5 µV/°C, typ), and 1.1-MHz bandwidth. Wide differential and common-mode input-voltage range, high output current (±80 mA), high slew rate (4.5 V/µs), low power operation (120 µA, typ) and shutdown functionality make the TLV910x a robust, low-power, high-performance operational amplifier for industrial applications. The TLV910x family of op amps is available in microsize packages, as well as standard packages, and is specified from –40°C to 125°C.

2.3.8 UCC28911

The UCC28910 and UCC28911 are high-voltage flyback switchers that provide output voltage and current regulation without the use of an optical coupler. Both devices incorporate a 700-V power FET and a controller that process operating information from the flyback auxiliary winding and power FET to provide a precise output voltage and current control. The integrated high-voltage current source for start up that is switched off during device operation, and the controller current consumption is dynamically adjusted with load. Both enable the very low stand-by power consumption. Control algorithms in the UCC28910 and UCC28911, combining switching frequency and peak primary current modulation, allow operating efficiencies to meet or exceed applicable standards. Discontinuous conduction mode (DCM) with valley switching is used to reduce switching losses. Built-in protection features help to keep secondary and primary component stress levels in check across the operating range. The frequency jitter helps to reduce EMI filter cost.

2.3.9 ATL431

The ATL431 and ATL432 are three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and industrial temperature ranges. The output voltage can be set to any value between Vref (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.05 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies. The ATL43x has > 20 × improvement cathode current range over its TL43x predecessor. It also is stable with a wider range of load capacitance types and values. ATL431 and ATL432 are the exact same parts but with different pinouts and order numbers. The ATL43x is offered in two grades, with initial tolerances (at 25°C) of 0.5%, 1%, for the B and A grade, respectively. In addition, low output drift vs temperature ensures consistent voltage regulation over the entire temperature range. The ATL43xxI

devices are characterized for operation from –40°C to +85°C, and the ATL43xxQ devices are characterized for operation from –40°C to +125°C.

2.4 System Design Theory

This reference design provides a universal AC, mains-powered, 500-W nominal output at 48 V. This design is derating to 300 W at a low line 115 V_{AC}. The UCC28180 controls a PFC boost front end, while the UCC256403 LLC resonant half-bridge converts the PFC output to an isolated 48 V. The total system efficiency is 94.5% with a 230-V_{AC} input and over 92.5% with a 115-V_{AC} input at full load. In addition, several protections are embedded into this design, which include input undervoltage protection and output short-circuit protection. Low EMI, high efficiency, a high power factor, and a reliable power supply are the main focus of this design for targeted applications.

2.4.1 PFC Stage Design

The CCM boost PFC is a popular choice for the 500-W design because of the low number of components and cost. This design, with the UCC28180, operates at a fixed frequency in CCM and requires minimal external components for high-wattage PFC implementation which helps reduce the cost. The design process and component selection for this design are illustrated in the following sections.

2.4.1.1 Design Parameters

表 2-1 shows the design goal parameters for the PFC stage.

表 2-1. Design Parameters for PFC Stage

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
INPUT					
AC line input voltage	V_{AC_high}	90	230	265	VAC
Input frequency	f_{LINE}	47	50	63	Hz
OUTPUT					
Output voltage	V_{blk}		390		VDC
Output power	P_{DCBUS}		515.4		W
Line regulation				5	%
Load regulation				5	%
Power factor	PF		0.99		
Holdup time	t_{holdup}			20	ms
Minimum switching frequency	f_{SW}		65		kHz
Targeted efficiency	η_{PFC}		98		%

2.4.1.2 Current Calculation

The input fuse, bridge rectifier, and input capacitor are selected based on the input current calculations. First, determine the maximum average output current, Iout(max), allowing for an overload to 110% of maximum load power.

$$I_{out(max)} = \frac{110\% \times P_{out}}{V_{bus}} = \frac{110\% \times 500\ W}{390} = 1.41\ A \quad (1)$$

The PFC stage is 500 W at high-line input at 180 V to 265 V and is derating to 300 W at low-line input at 90 V to 127 V. The maximum input RMS line current, Iin_rms(max), is calculated with minimum input voltage, the efficiency and power factor initial assumptions, allowing for an overload to 110% of maximum load power.

$$I_{in\_rms(max)} = \frac{110\% \times P_{out}}{V_{in(min)} \times \eta_{PFC} \times PF} = 6.3\ A \quad (2)$$

The maximum input peak current is:

$$I_{in\_pk(max)} = \sqrt{2} \times I_{in\_rms(max)} = 8.9\ A \quad (3)$$

The maximum input average current is:

$$I_{in\_avg(max)} = \frac{2}{\pi} \times I_{in\_pk(max)} = 5.66\,A \quad (4)$$

2.4.1.3 Bridge Rectifier

The maximum input AC voltage is 265-V AC. For safety, the voltage rating of the bridge must be at least

600 V. The input bridge rectifier must have an average current capability that exceeds the input average current, Iin_ave(max). The bridge rectifier also carries the full inrush current as the bulk capacitor charges when the line is connected. The amplitude and duration of this current is difficult to determine in advance because it depends on parameters that are hard to predict.

2.4.1.4 Boost Inductor Design

To dimension the boost inductor, first calculate the maximum-allowed ripple current. The maximum ripple current is observed at the lowest input voltage and maximum load. Assuming a maximum 30% ripple in the inductor current gives a ripple current of:

$$I_{ripple(max)} = 0.3 \times I_{in\_pk(max)} = 2.67\,A \quad (5)$$

The maximum duty cycle is:

$$D_{max} = \frac{V_{out} - V_{in\_peak(min)}}{V_{out}} = 0.674 \quad (6)$$

The minimum boost inductor value is calculated from the maximum duty cycle:

$$L_{PFC} \geq \frac{V_{blk} \times D_{max} \times (1 - D_{max})}{f_{swpfc} \times I_{ripple(max)}} = 460\ \mu H \quad (7)$$

The boost inductor must be able to support a maximum current of:

$$I_{L\_pk(max)} = I_{in\_pk(max)} + \frac{I_{ripple(max)}}{2} = 10.2\ A \quad (8)$$

2.4.1.5 Switching MOSFET

The drain source breakdown voltage of the switching MOS is ≥ 600 V. The drain-to-source RMS current through the MOS is calculated as:

$$I_{ds(max)} = \frac{P_{out}}{\sqrt{2} \times V_{in(min)}} \times \sqrt{2 - \frac{16 \times \sqrt{2} \times V_{in(nim)}}{3\pi \times V_o}} = 4.71\ A \quad (9)$$

The key specifications of the MOS that must be taken into consideration are:

- Low $R_{DS(on)}$ for reducing the conduction loss
- Low Qg for fast turnon and turnoff in the hard switching in this topology
- Low output capacitance for reducing the switching loss

2.4.1.6 Boost Diode

The output diode must have a blocking voltage that exceeds the output overvoltage of the converter and an average current that exceeds Iout(max). In CCM PFC topology, the boost diode undergoes hard turnoff and hence suffers from reverse recovery loss. To reduce the reverse recovery loss, it is better to select an ultra-fast diode or silicon-carbide diode. Silicon-carbide diodes have no reverse recovery loss, but the cost is higher than silicon ultra-fast diodes.

2.4.1.7 Output Capacitor

The value of the output capacitor is determined by two factors. One is that the value must be large enough to provide the required holdup time. The other is that the value must be large enough to keep the ripple at twice the line frequency within the required limits. The holdup time required in this design is 20 ms. Substituting the known values in 式 10, the minimum Cout is:

$$C_{out} \geq 2 \times P_{out} \times \frac{T_{holdup}}{V_{out(max)}^2 - V_{out(min)}^2} = 294\ \mu F \tag{10}$$

2.4.1.8 Sense Resistor

To accommodate the gain of the non-linear power limit, the sense resistor, RSENSE, is sized such that it triggers the soft overcurrent at 10% higher than the maximum peak inductor current using the minimum soft overcurrent threshold of the ISENSE pin, VSOC, of ISENSE equal to 0.259 V.

$$R_{sense} = \frac{V_{soc(min)}}{1.2 \times I_{L(max)}} = 0.021\ \Omega \tag{11}$$

2.4.2 LLC Stage Design

LLC topology has been widely used in telecom and server power supplies. LLC topology can get a wide gain range by changing the frequency. LLC topology usually applies to generation of a constant output voltage for a wide-input DC voltage range or generation of a variable output voltage for a constant input DC voltage. The wider the frequency range is, the more different the LLC design is. The DC/DC stage in this design must support 20-ms holdup time. LLC topology can achieve both ZVS for the primary MOSFET and ZCS for the secondary diode under resonant frequency. Considering efficiency, the converter is designed to operate at a frequency slightly lower than resonance frequency at full load.

1. Select the Transformer

   The transformer can be built or purchased from Wurth. The detail specifications are found on the Wurth website with P/N 750344508.
2. Select the Resonant Inductor

   The resonant inductor can be built or purchased from Wurth. The detail specifications are found on Wurth website with P/N 750344650/

   Inductor Terminal AC voltage can be expressed as the following:

$$V_{Lr} = \omega \times L_R \times I_r = 39\ V \tag{12}$$

3. Select the Resonant Capacitor

   This capacitor carries the full-primary current at a high frequency. A low dissipation factor part is needed to prevent overheating in the part.

   The AC voltage across the resonant capacitor is given by its impedance times the current.

$$V_{CR} = \frac{I_r}{\omega \times C_R} = 125\ V \tag{13}$$

$$V_{CR(rms)} = \sqrt{\left(\frac{V_{IN(max)}}{2}\right)^2 + V_{CR}^2} = 240.1\ V \quad (14)$$

$$V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2} \times V_{CR} = 382\ V \quad (15)$$

$$V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2} \times V_{CR} = -32\ V \quad (16)$$

4. Select the Primary Side MOSFETs

   Each MOSFET detects the input voltage as its maximum applied voltage. Choose the MOSFET voltage rating to be 1.5 times of the maximum bulk voltage.

$$V_{DS} = 1.5 \times V_{IN(max)} = 615\ V \quad (17)$$

   Choose the MOSFET current rating to be 1.1 times of the maximum primary side RMS current.

$$I_D = 1.1 \times I_r = 4.74\ A \quad (18)$$

   For the LLC power stage working in ZVS, the turn-on losses can be neglected. The choice of MOSFET must be based on $R_{DS(on)}$ and Coss. Optimizing the Coss helps in minimizing the dead time required for achieving ZVS, thereby minimizing duty cycle loss. The feature that optimizes the adaptive dead time of the UCC256403 helps in maximizing the duty cycle, thereby improving efficiency.

5. Select the Secondary Side MOSFETs

   The secondary-side rectifier voltage rating is determined by:

$$V_{DS\_sec} = 1.2 \times 2 \times V_{OUT\_max} = 115\ V \quad (19)$$

   The current rating of the secondary-side MOSFET is determined by:

$$I_{D\_sec} = \frac{\sqrt{2}I_{SEC}}{2} = 8.2\ A \quad (20)$$

   This reference design uses 150-V MOS with its low $R_{DS(on)}$ (7.6 mΩ) and Qg (21 nC). The very low $R_{DS(on)}$ helps in reducing the overall loss in the synchronous rectifier.

2.4.2.1 Design Parameters

表 2-2 shows the design parameters for the LLC stage.

表 2-2. Design Parameters for LLC Stage

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
INPUT					
Input voltage	V_{INDC}	290	390	410	VDC
OUTPUT					
Output voltage	V_{OUT}	42	48	54	VDC
Max output power	P_{OUT}			500	W
Nominal switching frequency	f_{SWNOM}		100		kHz
Line regulation			1		%

表 2-2. Design Parameters for LLC Stage (continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Load regulation			1		%
Targeted efficiency			97		%

2.4.2.2 Determining Mg

The transformer turns ratio is determined by 式 21:

$$n = \frac{\frac{V_{DCIN\_nom}}{2}}{V_{OUT}} = 4.1 \tag{21}$$

From the specifications, the nominal values for input voltage and output voltage are 390 V and 48 V, respectively, so the turns ratio can be calculated as:

$$n = \frac{\frac{390}{2}}{48} = 4.1 \tag{22}$$

2.4.2.3 LLC Gain Range M_{g_min} and M_{g_max}

M_{g_min} and M_{g_max} can be determined by using 式 23 and 式 24, respectively:

$$M_{g\_min} = n \times \left(\frac{V_{OUT\_min}}{\frac{V_{DCIN\_max}}{2}} \right) = 0.937 \tag{23}$$

$$M_{g\_max} = n \times \left(\frac{V_{OUT\_max}}{\frac{V_{DCIN\_min}}{2}} \right) = 1.32 \tag{24}$$

2.4.2.4 Determine Equivalent Load Resistance of Resonant Network

To determine the equivalent load resistance at nominal and peak load under nominal output voltage and peak output voltage, use 式 25:

$$R_E = \frac{8 \times n^2}{\pi^2} \times \left(\frac{V_{OUT_{nom}}}{I_{OUT_{nom}}} \right) = \frac{8 \times 4^2}{\pi^2} \times \left(\frac{48}{10.45} \right) = 59.6\ \Omega \tag{25}$$

2.4.2.5 Select L_M/L_R Ratio (L_N) and Q_E

L_N is the ratio between the magnetizing inductance and the resonant inductance.

$$L_N = \frac{L_M}{L_R} \tag{26}$$

Q_E is the quality factor of the resonant tank.

$$Q_E = \frac{\sqrt{\frac{L_R}{C_R}}}{R_E} \tag{27}$$

Selecting L_N and Q_E values must result in an LLC gain curve, as shown in 図 2-2, that intersects with Mg_{min} and Mg_{max} traces. The peak gain of the resulting curve must be larger than Mg_{max}.

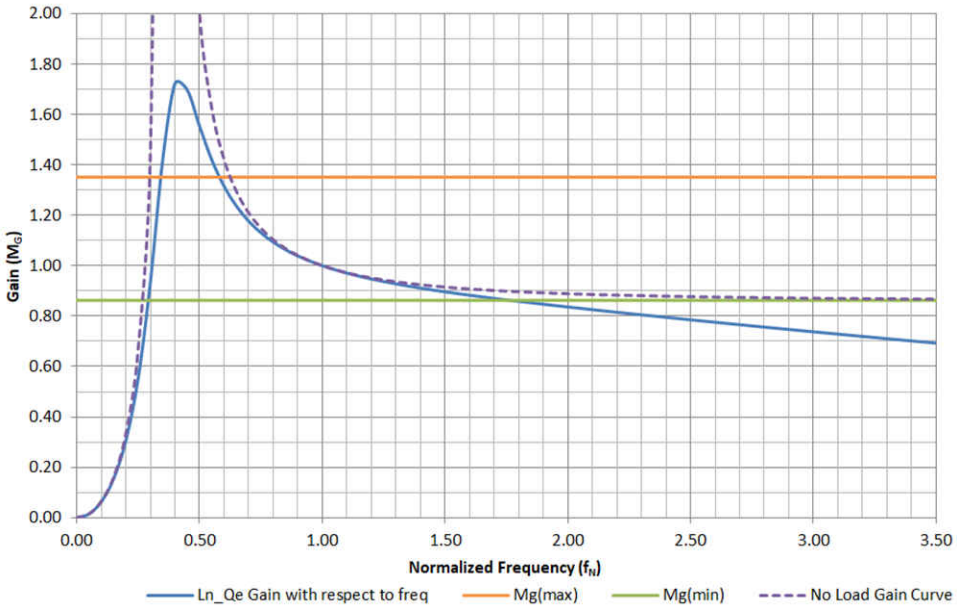


図 2-2. LLC Gain Curve for Selected L_N and Q_E

The relationship between MG_{peak} and Q_E with respect to L_N is shown in 図 2-3:

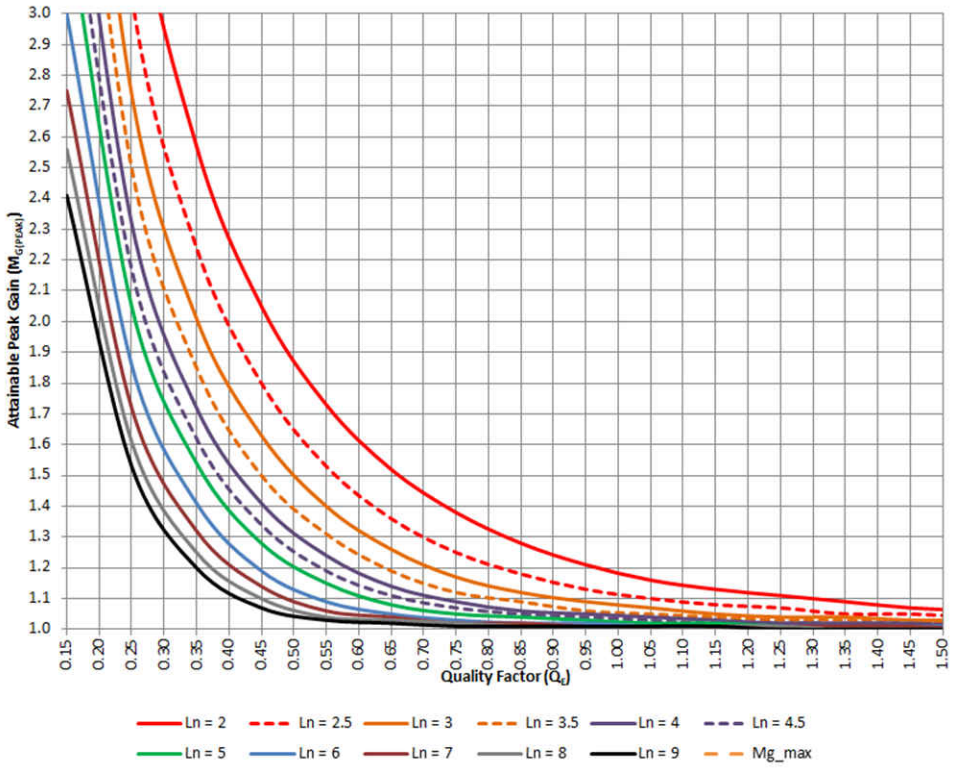


図 2-3. MG_{peak} and Q_E With Respect to L_N

2.4.2.6 Switching Frequency

The wide switching frequency of the UCC256403 is from 35 kHz to 1 MHz, which makes this reference design more flexible. To ensure that the temperature rise of the LLC stage is not too high, reduce the loss of the transformer, inductor, and power MOS. The resonant frequency is chosen to be 100 kHz for the consideration of magnetic loss and switching loss.

$$f_0 = 100\ kHz \tag{28}$$

$$C_R = \frac{1}{2\pi \times Q_E \times f_0 \times R_E} = 98\ nF \tag{29}$$

$$L_R = \frac{1}{(2\pi \times f_0)^2 \times C_R} = 26\ \mu H \tag{30}$$

$$L_M = L_N \times L_R = 6 \times 26\ \mu H = 155\ \mu H \tag{31}$$

After the preliminary parameters are selected, find the closest actual component value that is available, recheck the gain curve with the selected parameters, and then run the time domain simulation to verify the circuit operation. This results in the following resonant tank parameters:

$$C_R = 0.1\ \mu F \tag{32}$$

$$L_R = 26\ \mu H \tag{33}$$

$$L_M = 155\ \mu H \tag{34}$$

Based on the final resonant tank parameters, the resonant frequency can be calculated as follows:

$$f_0 = \frac{1}{2\pi \times \sqrt{C_R \times L_R}} = 98.7 \text{ kHz} \quad (35)$$

2.4.2.7 LLC Primary-Side Currents

式 36 shows the LLC Primary-side current:

$$I_{pri} = \frac{\pi}{2\sqrt{2}} \times \frac{I_O}{n} = 2.9 \text{ A} \quad (36)$$

The RMS magnetizing current at $f_{SW(min)}$ is determined by:

$$I_m = \frac{2\sqrt{2}}{\pi} \times \frac{n \times V_{OUT}}{2\pi \times f_{SW(min)} \times L_M} = 3.22 \text{ A} \quad (37)$$

The current of the resonant circuit is determined by:

$$I_r = \sqrt{I_m^{\ 2} + I_{pri}^{\ 2}} = 3 = 4.33 \text{ A} \quad (38)$$

This calculation is also the primary winding current of the transformer at $f_{SW(min)}$.

2.4.2.8 LLC Secondary-Side Currents

The total secondary-side RMS load current is the current referred from the primary-side current to the secondary side.

$$I_{sec} = n \times I_{pri} = 11.5 \text{ A} \quad (39)$$

Because the secondary side of the transformer has a center-tapped configuration, this current is split equally into two transformer windings on the secondary side. The current of each winding is then calculated as:

$$I_{SW} = \frac{\sqrt{2} \times I_{sec}}{2} = 8.16 \text{ A} \quad (40)$$

The corresponding half-wave average current is:

$$I_{savg} = \frac{\sqrt{2} \times I_{sec}}{\pi} = 5.2 \text{ A} \quad (41)$$

2.4.2.9 LLC Output Capacitors

The LLC converter topology does not require an output filter, although a small second-stage filter inductor can be useful in reducing peak-to-peak output noise. Assuming that the output capacitors carry the full wave output current of the rectifier, the capacitor ripple current rating is:

$$I_{RECT} = \frac{\pi}{2\sqrt{2}} \times I_O = 11.5 \text{ A} \quad (42)$$

The RMS current rating of the capacitor is:

$$I_{C(out)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times I_O\right)^2 - I_O^2} = 5.02\ A \tag{43}$$

The ripple current rating for a single capacitor may not be sufficient, so multiple capacitors are often connected in parallel.

$$ESR_{max} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)} \times \sqrt{2}} = 15\ m\Omega \tag{44}$$

2.4.2.10 BLK Pin Voltage Divider

The BLK pin senses the LLC input voltage and determines when to turn on and off the LLC converter. Different versions of the UCC25640 have different BLK thresholds. Choose the bulk startup voltage at 360 V, then the BLK resistor divider ratio can be calculated:

$$K_{BLK} = \frac{V_{BUSON}}{3.05\ V} = \frac{360}{3.05} = 118 \tag{45}$$

The desired power consumption of the BLK pin resistor is P_{BLKsns} = 10 mW. The total value of the BLK sense resistor is given by:

$$R_{BLKsns} = \frac{V_{IN(nom)}^2}{P_{BLK(sns)}} = \frac{390^2}{0.01} = 15.21\ \ M\Omega \tag{46}$$

The lower BLK divider resistor value is given by:

$$R_{BLKlower} = \frac{R_{BLKsns}}{K_{BLK}} = \frac{15.21\,M\Omega}{118} = 129\ k\Omega \tag{47}$$

The higher BLK divider resistor value is given by:

$$R_{BLKUPPER} = R_{BLKsns} - R_{BLKlower} = 15.1\,M\Omega \tag{48}$$

2.4.2.11 Current Sense Circuit (ISNS Pin)

The ISNS pin sets the overcurrent protection level. OCP1 is peak current protection level; OCP2 and OCP3 are average current protection levels. The threshold voltages are 0.425 V, 0.56 V, and 4.03 V, respectively. Set the OCP3 level at 140% of full load. Thus, the sensed average input current level at full load is given by:

$$V_{ISNSfullload} = \frac{0.425\ V}{150\%} = 0.28V \tag{49}$$

The current sense ratio can then be calculated:

$$K_{ISNS} = \frac{V_{ISNSfullload}}{\frac{P_{OUT}}{\eta} \times \frac{1}{V_{DCBUS\_nom}}} = \frac{0.28\ V}{\frac{500\ W}{0.97} \times \frac{1}{390\ V}} = 0.214\ \Omega \tag{50}$$

Select a current-sense capacitor first because there are fewer high-voltage capacitor choices than resistors. C_{ISNS} = 330 pF Then calculate the required ISNS resistor value:

$$R_{ISNS} = \frac{K_{ISNS} \times C_R}{C_{ISNS}} = 65\ \Omega \tag{51}$$

2.4.2.12 Auxiliary PSU

This reference design has the additional auxiliary PSU to provide the bias power to the PFC, LLC, SR, and other logic circuits on the board. The converter is powered from the output of the PFC pre-regulator stage and must be able to start up prior to the PFC stage being operational. For this reason, the circuit is designed to operate over a wide input voltage, 100- to 450-V_{DC}. The flyback transformer has three output windings, which are isolated to each other.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Hardware

The following equipment is required for testing:

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multimeter
- Electronic load

3.2 Testing and Result

This section contains test set up and test result.

3.2.1 Test Setup

This section contains the test conditions and required equipment for testing.

3.2.1.1 Test Condition

The following conditions are required for testing:

- Input conditions: V_{IN}: 85-V to 265-V AC, set the input current limit to 8 A
- Output conditions: Electronic load, 0 V to 70 V, 800 W

3.2.2 Test Results

This section presents the test results for the reference design.

3.2.2.1 Efficiency and Regulation

This section displays the performance data and performance curves for the reference design.

3.2.2.1.1 Performance Data

This section shows the efficiency, power factor, THD, and load regulation results at 115-V and 230-V AC input conditions.

表 3-1 shows the data for V_{IN} = 115-V AC.

表 3-1. Efficiency and Regulation at 115-V AC

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	THD (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFF (%)	Load %
115.00	0.55	62.8	0.979	8.50	48.10	1.094	52.621	83.79	10%
115.00	1.03	113.2	0.992	5.50	48.05	2.091	100.473	88.76	20%
115.00	1.31	168.7	0.996	4.15	48.08	3.188	153.279	90.86	30%
115.00	1.93	218.9	0.997	3.56	48.05	4.170	200.369	91.53	40%
115.00	2.37	275.3	0.998	3.17	48.08	5.260	252.917	91.87	50%
115.00	2.85	326.6	0.999	3.00	48.08	6.260	300.981	92.16	60%
115.00	3.29	378.1	0.999	2.92	48.08	7.260	349.061	92.32	70%
115.00	3.73	435.6	0.999	2.88	48.08	8.350	401.468	92.16	80%
115.00	4.23	488.0	0.999	2.93	48.08	9.350	449.548	92.12	90%
115.00	4.67	545.7	0.997	2.98	48.06	10.450	502.227	92.03	100%

表 3-2 shows the data for V_{IN} = 230-V AC.

表 3-2. Efficiency and Regulation at 230-V AC

V_{INAC} (V)	I_{INAC} (A)	P_{INAC} (W)	PF	THD (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFF (%)	Load %
230.00	0.55	61.6	0.860	25.00	48.11	1.094	52.632	85.44	10%
230.00	1.03	110.9	0.948	14.50	48.06	2.091	100.493	90.62	20%
230.00	1.31	165.6	0.971	9.50	48.08	3.188	153.279	92.56	30%
230.00	1.93	214.8	0.979	7.65	48.06	4.170	200.410	93.30	40%
230.00	2.37	269.8	0.985	6.14	48.08	5.260	252.917	93.74	50%
230.00	2.85	319.6	0.988	5.34	48.08	6.260	300.981	94.17	60%
230.00	3.29	369.3	0.990	4.78	48.08	7.250	348.580	94.39	70%
230.00	3.73	424.4	0.992	4.34	48.08	8.350	401.468	94.60	80%
230.00	4.23	474.1	0.993	4.14	48.08	9.325	448.346	94.57	90%
230.00	4.67	529.9	0.994	3.91	48.06	10.420	500.785	94.51	100%

3.2.2.1.2 Performance Curves

図 3-1 through 図 3-6 show the graphs for efficiency, power factor, and THD, respectively.

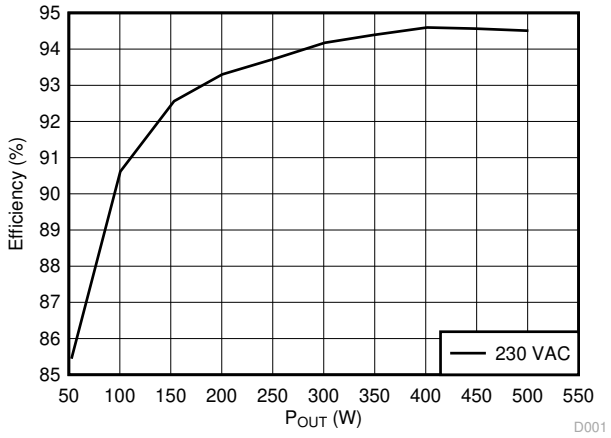


図 3-1. Efficiency at 230-V AC

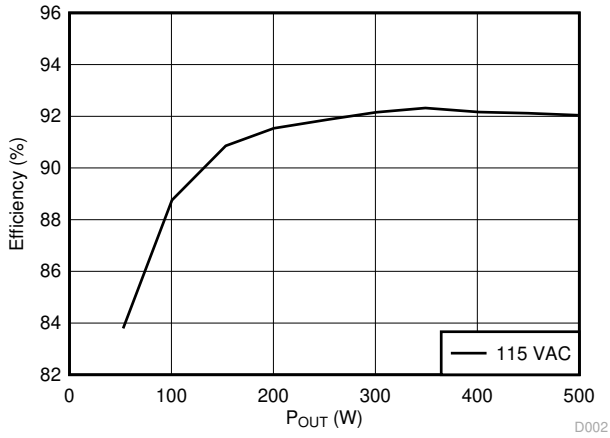


図 3-2. Efficiency at 115-V AC

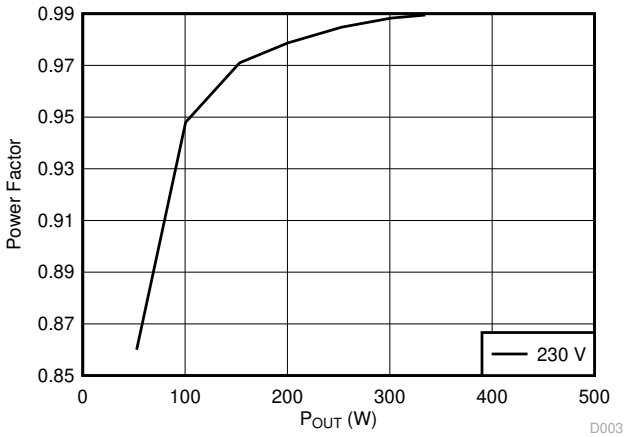


図 3-3. Power Factor at 230-V AC

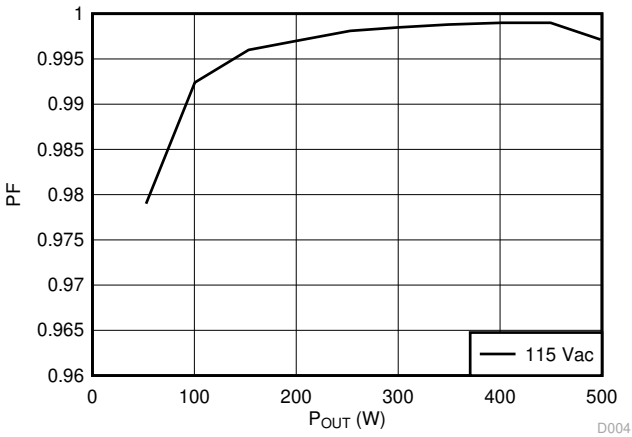


図 3-4. Power Factor at 115-V AC

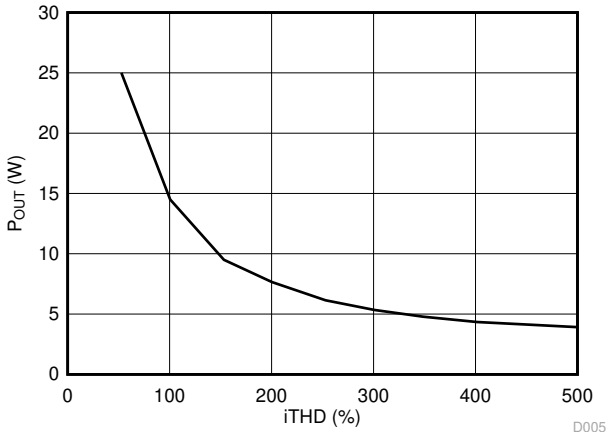


図 3-5. THD at 230-V AC

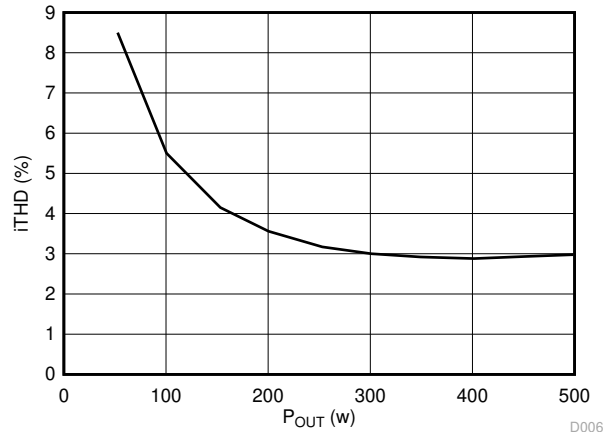


図 3-6. THD at 230-V AC

3.2.2.2 Switching Waveforms

This section displays the PFC stage, LLC stage, LLC secondary-side synchronous drive, input, start-up, dynamic load, and output ripple waveforms for the reference design.

3.2.2.2.1 PFC Stage Switching Waveforms

This section shows the PFC stage switching waveforms at an input voltage of 115-V AC and 230-V AC at different load conditions.

図 3-7 shows the PFC inductor current and switching node waveform at 230-V AC, 500 W.

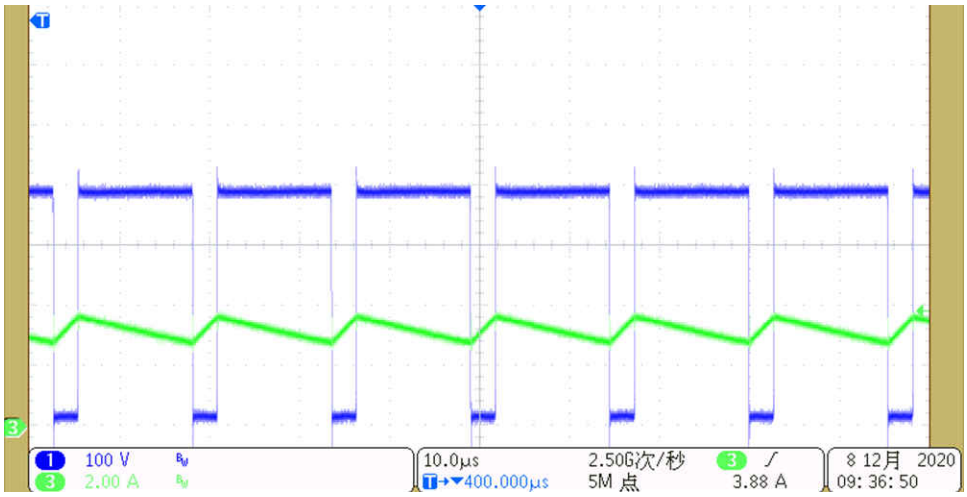


図 3-7. PFC Inductor Current and Switching Node Waveform at 230-V AC, 500 W

図 3-8 shows the PFC inductor current and switching node waveform at 115 V_{AC}, 500 W.

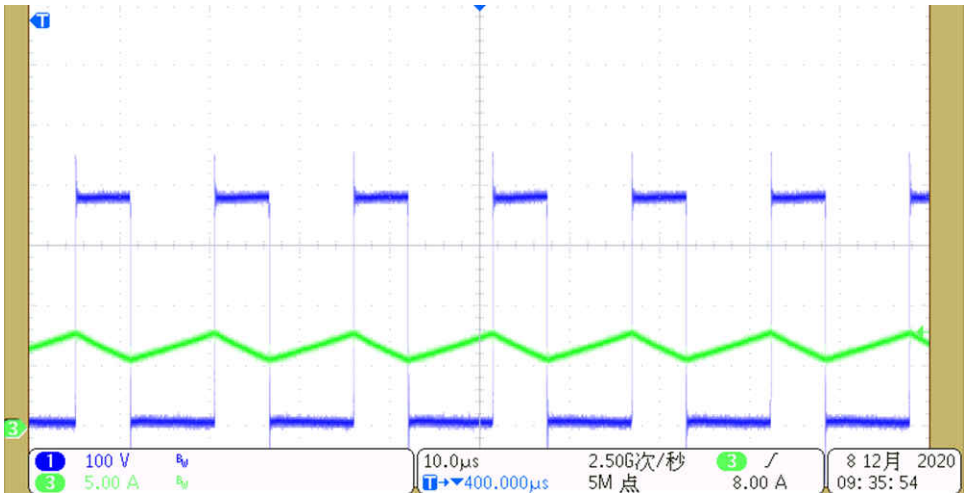


図 3-8. PFC Inductor Current and Switching Node Waveform at 115-V AC, 500 W

3.2.2.2.2 LLC Stage Switching Waveforms

This section shows the LLC-stage, primary-side switching waveforms at an output voltage of 24-V AC at different load conditions.

図 3-9 shows the low-side PWM and Resonant current at full load.

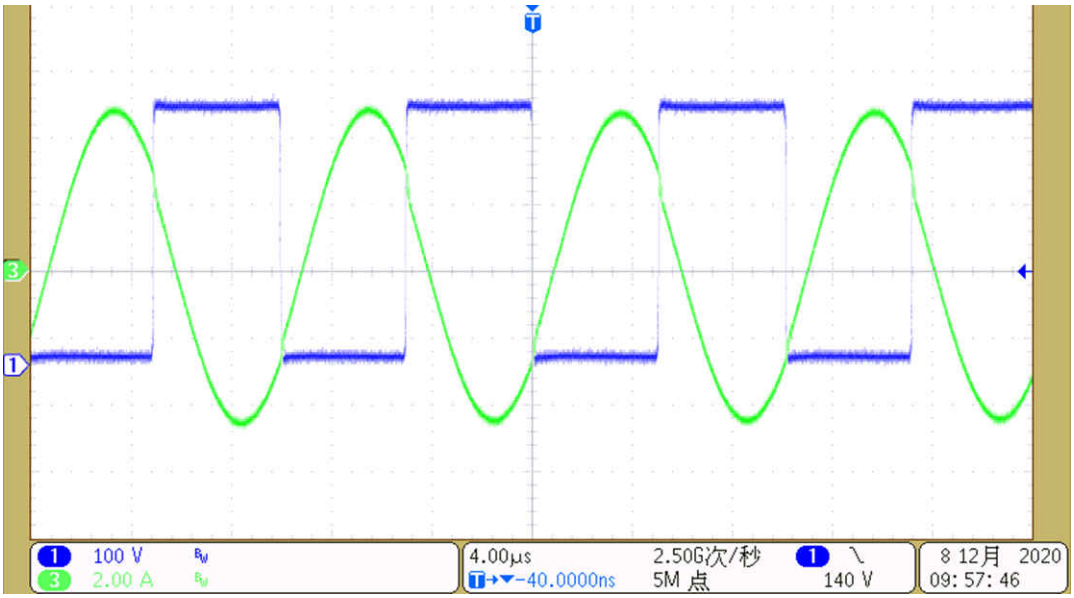


図 3-9. Low-Side PWM and Resonant Current at Full Load

3.2.2.2.3 LLC Secondary Side Synchronous Drive Waveform

The synchronous drive output waveforms and the resonant current are shown in the following figures.

図 3-10 shows the SR rectifier gate driver.

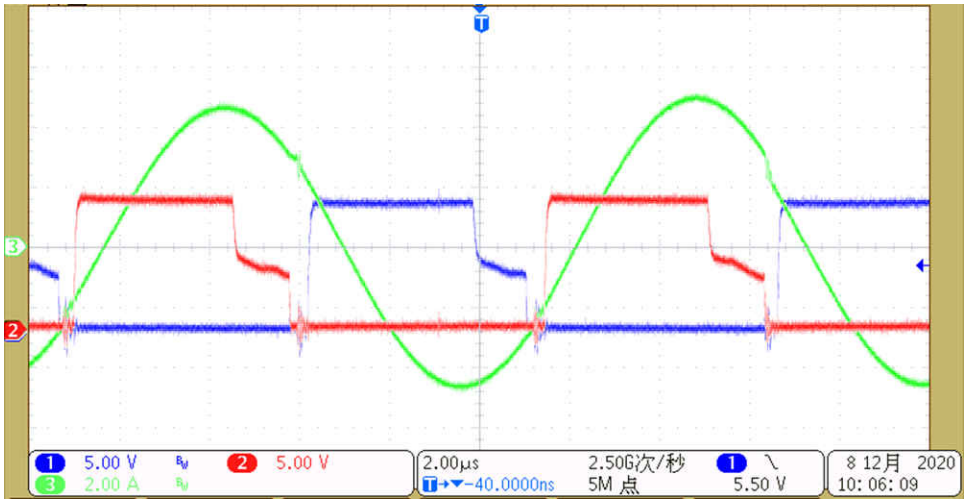


図 3-10. SR Rectifier Gate Driver

3.2.2.2.4 Input Waveforms

図 3-11 and 図 3-12 show the input current waveform at 230-V AC and 115-V AC at full load conditions, respectively.

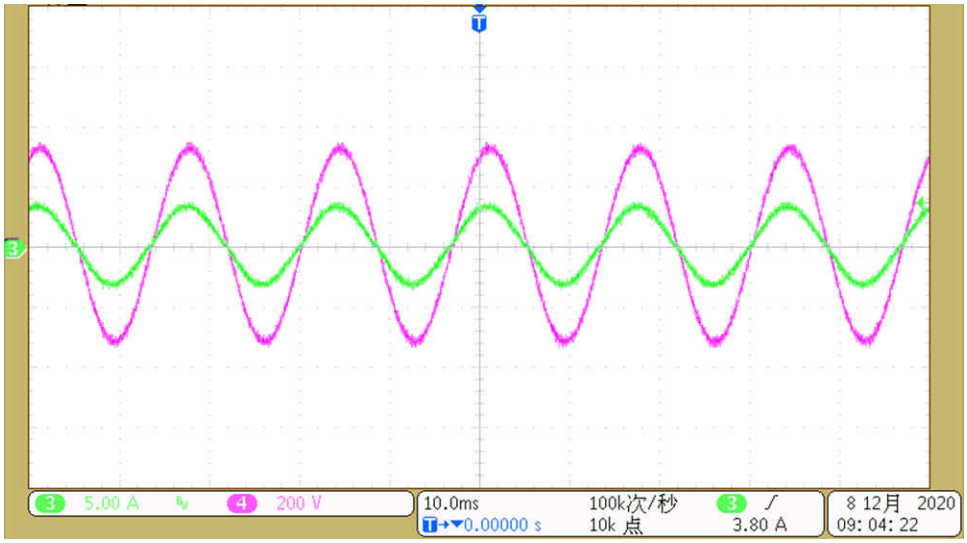


図 3-11. Input Voltage and Current at 230-V AC, 500 W

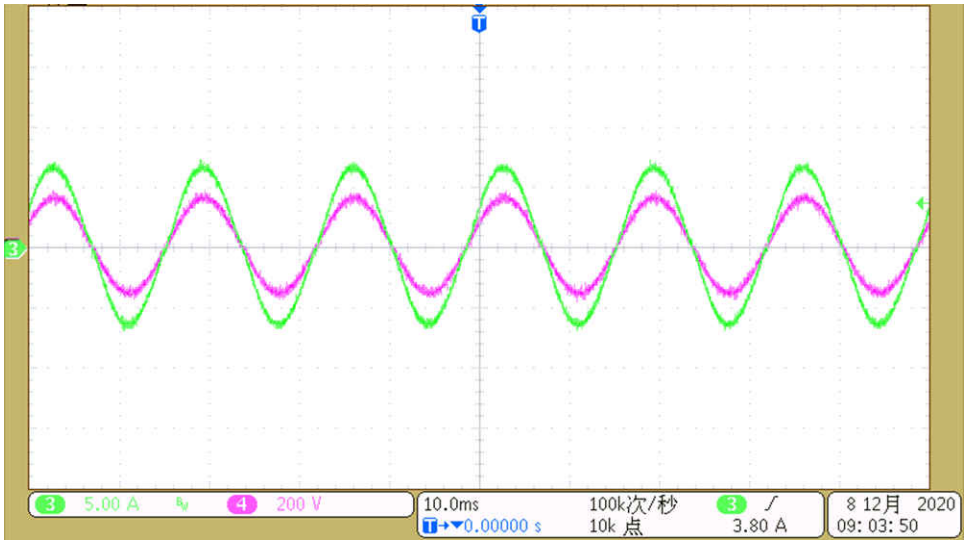


図 3-12. Input Voltage and Current at 115-V AC, 500 W

3.2.2.2.5 Start-up Waveforms

図 3-13 and 図 3-14 show the start-up waveform showing the 54-V output voltage and the input AC voltage at V_{INAC} = 230 V AC and V_{INAC} = 115 V AC, respectively.

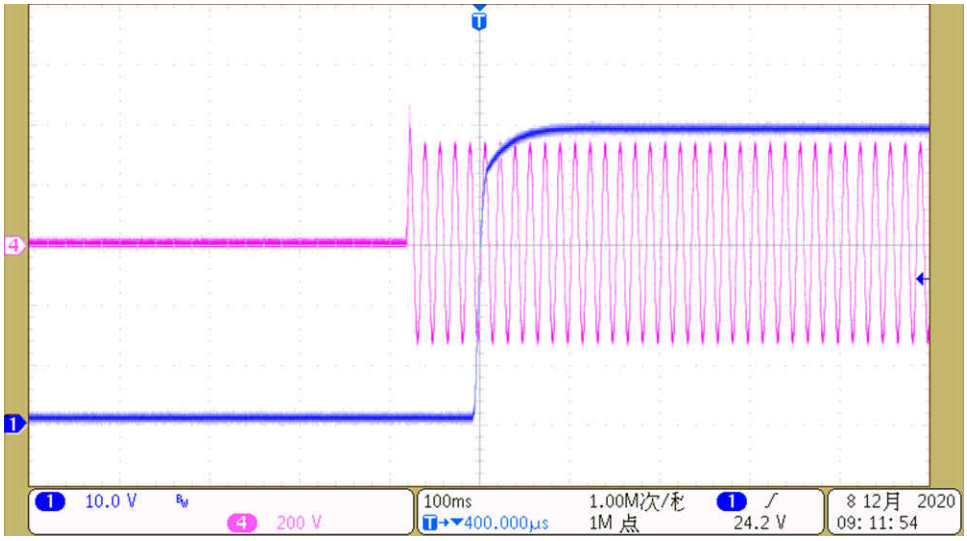


図 3-13. Start-up Waveform at V_{INAC} = 230 V_{AC} and 500 W

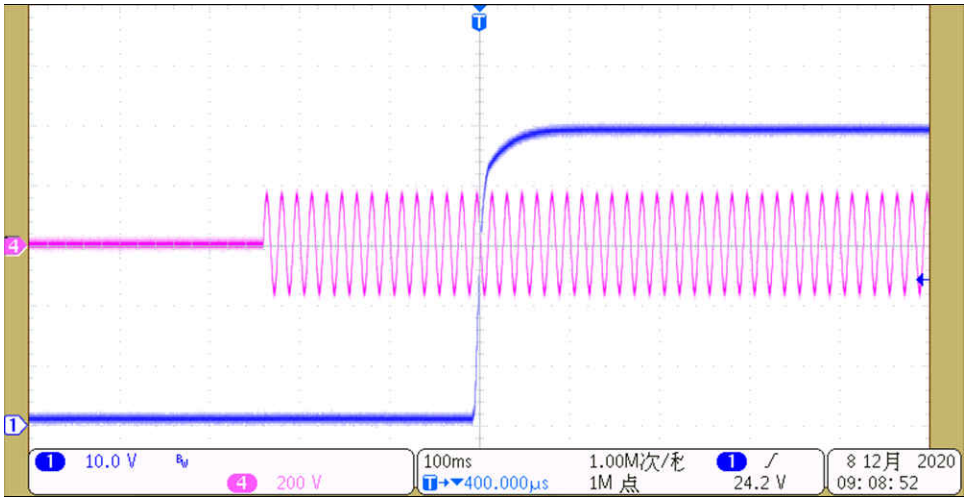


図 3-14. Start-up Waveform at V_{INAC} = 115 V_{AC} and 500 W

3.2.2.2.6 Dynamic Load Characteristics

Load transient performance is observed using an electronic load. The converter is operating at an input voltage of 230-V AC and an output voltage of 48-V DC.

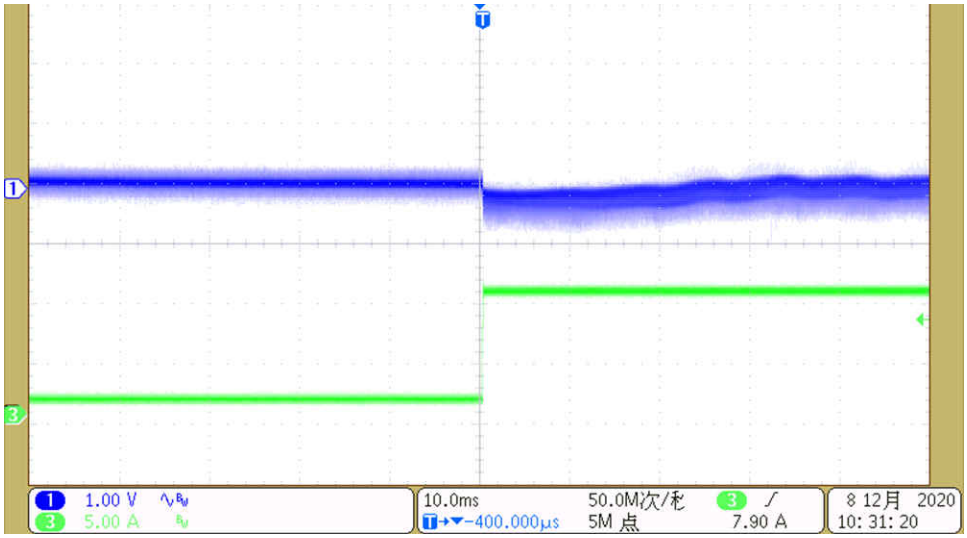


図 3-15. Transient Response From 10% to 90% Load

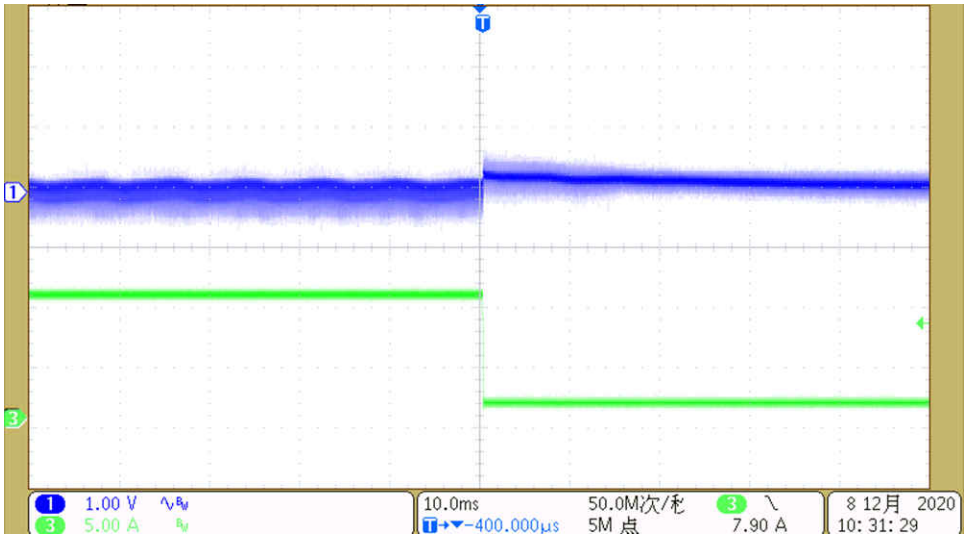


図 3-16. Transient Response From 90% to 10% Load

3.2.2.2.7 Output Ripple

図 3-17 shows the output voltage ripple at full load conditions at a 230-V AC input.

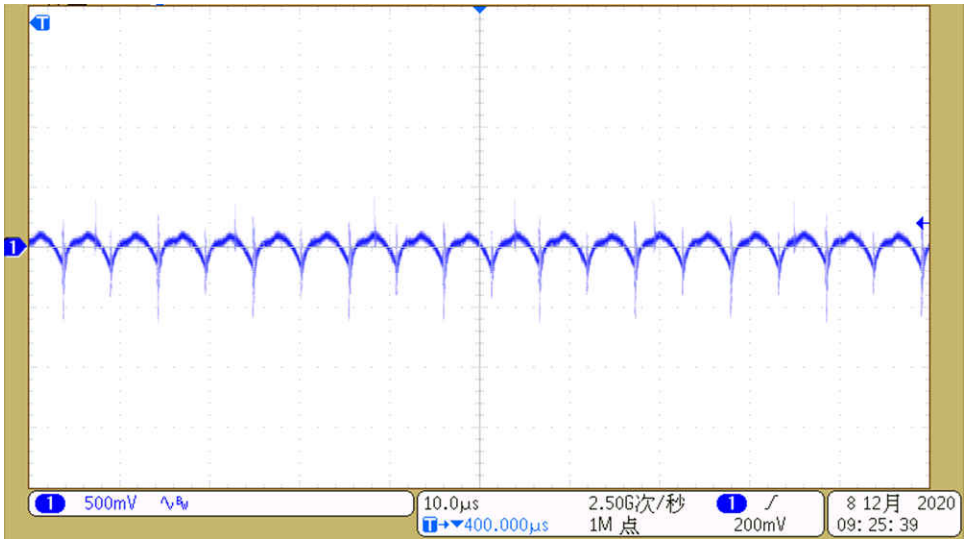


図 3-17. Output Ripple With 1000 W at V_{INAC} = 230 V_{AC}

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010080.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010080.

4.1.3 PCB Layout Recommendations

The key guidelines for routing power stage components follows:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents, on both the primary and secondary sides of the converter. This helps reduce EMI and improve converter overall performance.
- Keep traces with high dV/dt potential and high dI/dt capability away from or shielded from sensitive signals.
- Keep power ground and control ground separated for each power supply stage. If they are electrically connected, tie them together at one point near the DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, the layout must be symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher currents and become hotter.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device. Devices are intended for protection and hence must be routed with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current per IPC2152 as well as acceptable DC and AC impedances. Also, the traces must withstand the fault currents (such as short-circuit current) before the activation of electronic protection such as a fuse or circuit breaker.
- Determine the distances between various circuits according to the requirements of applicable standards such as the UL60950.
- Adapt thermal management to fit the end-equipment requirements.

4.1.4 Gerber Files

To download the Gerber files, see the design files at TIDA-010080.

4.1.5 Assembly Drawings

To download the Assembly Drawings files, see the design files at TIDA-010080.

4.2 Tools and Software

4.3 Documentation Support

1. Texas Instruments, *UCC28180 Programmable Frequency, Continuous Conduction Mode (CCM), Boost Power Factor Correction (PFC) Controller Data Sheet*
2. Texas Instruments, *UCC24624 Dual-Channel Synchronous Rectifier Controller for LLC Resonant Converters Data Sheet*
3. Texas Instruments, *UCC25640x LLC Resonant Controller with Ultra-Low Audible Noise and Standby Power Data Sheet*
4. Texas Instruments, *UCC28910, UCC28911 High-Voltage Flyback Switcher with Primary-Side Regulation and Output Current Control Data Sheet*

4.4 サポート・リソース

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5 About the Author

Max Wang is a Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the power delivery, industrial segment. Max earned his master of technology degree in power electronics from Zhejiang University.

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