SNx4AHC138 3-Line to 8-Line Decoders/Demultiplexers

1 Features

- Operating range 2V to 5.5V V_{CC}
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporate three enable inputs to simplify cascading and/or data reception
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22:
  - 2000V Human-Body Model (A114-A)
  - 1000V Charged-Device Model (C101)

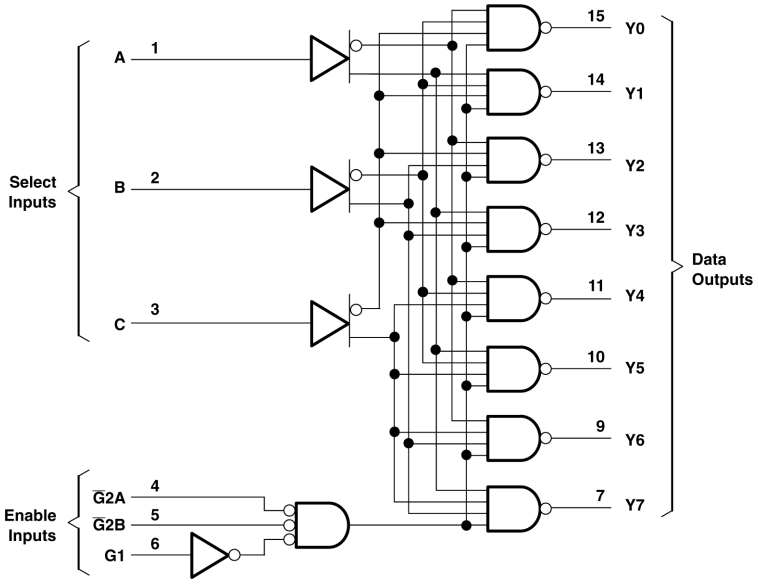
2 Description

The SNx4AHC138 decoders/demultiplexers are designed for high-performance memory-decoding and data-routing applications that require very short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

Device Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE (2)	BODY SIZE (3)
SN74AHC138	RGY (VQFN, 16)	4mm x 3.5mm	4mm x 3.5mm
	N (PDIP, 16)	19.3mm × 9.4mm	19.32mm x 6.35 mm
	D (SOIC, 16)	9.9mm × 6mm	9.90mm x 3.90mm
	NS (SOP, 16)	10.2mm x 7.8mm	10.20mm x 5.30mm
	DB (SSOP, 16)	6.2mm × 7.8mm	6.20mm x 5.30mm
	PW (TSSOP , 16)	5mm × 6.4mm	5.00mm x 4.40mm
	DGV (TVSOP, 16)	3.6mm x 6.4mm	3.6mm x 4.4mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

Table of Contents

3 Pin Configuration and Functions

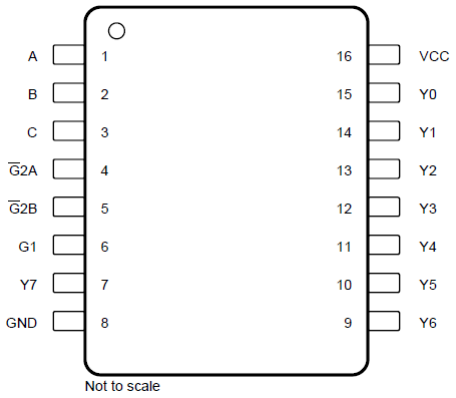


Figure 3-1. D, DB, DGV , N, NS , or PW Package, 16-Pin SOIC, SSOP, TVSOP, PDIP, SOP, or TSSOP (Top View)

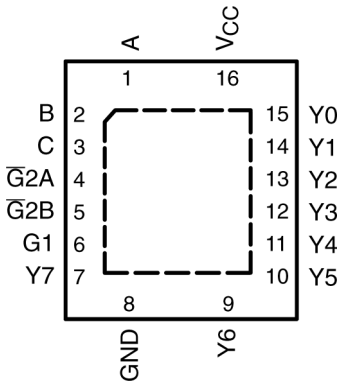
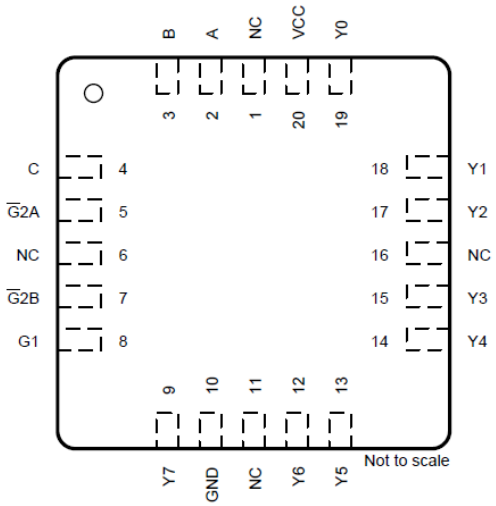


Figure 3-2. RGY Package, 16-Pin VQFN (Top View)



NC: No internal connection

Figure 3-3. FK Package, 20-Pin LCCC (Top View)

Table 3-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A_0	1	I	Address select 0
A_1	2	I	Address select 1
A_2	3	I	Address select 2
$\overline{G}_0$	4	I	Output strobe 0, active low
$\overline{G}_1$	5	I	Output strobe 1, active low
G_2	6	I	Output strobe 2
Y_7	7	O	Output 7
GND	8	G	Ground
Y_6	9	O	Output 6
Y_5	10	O	Output 5
Y_4	11	O	Output 4
Y_3	12	O	Output 3
Y_2	13	O	Output 2
Y_1	14	O	Output 1
Y_0	15	O	Output 0
V_{CC}	16	P	Positive supply
Thermal pad[2]			The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.
(2) WBQB package only.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I (2)	Input voltage range		−0.5	7	V
V_O (2)	Output voltage range		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0)		−20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54AHC138		SN74AHC138		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage			0 5.5		0 5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	mA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	mA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC[1]		SN74AHC138							UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		16							
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.8	82	120	67	64	135.9	39	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC138		SN74AHC138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50µA	2 V		0.1			0.1		0.1	V
		3 V		0.1			0.1		0.1	
		4.5 V		0.1			0.1		0.1	
	I_{OL} = 4 mA	3 V		0.36			0.5		0.44	
	I_{OL} = 8 mA	4.5 V		0.36			0.5		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V		±0.1			±1[1]		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V		4		40		40		µA
C_i	V_I = V_{CC} or GND	5 V	2	10					10	pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

4.5 Switching Characteristics: V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC138		SN74AHC138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	C_L = 15pF		8.2[1]	11.4[1]	1[1]	13[1]	1	13	ns
t_{PHL}					8.2[1]	11.4[1]	1[1]	13[1]	1	13	
t_{PLH}	G1	Any Y	C_L = 15pF		8.1[1]	12.8[1]	1[1]	15[1]	1	15	ns
t_{PHL}					8.1[1]	12.8[1]	1[1]	15[1]	1	15	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15pF		8.2[1]	11.4[1]	1[1]	13.5[1]	1	13.5	ns
t_{PHL}					8.2[1]	11.4[1]	1[1]	13.5[1]	1	13.5	
t_{PLH}	A, B, C	Any Y	C_L = 50pF		10	15.8	1	18	1	18	ns
t_{PHL}					10	15.8	1	18	1	18	
t_{PLH}	G1	Any Y	C_L = 50pF		10.6	16.3	1	18.5	1	18.5	ns
t_{PHL}					10.6	16.3	1	18.5	1	18.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50pF		10.7	14.9	1	17	1	17	ns
t_{PHL}					10.7	14.9	1	17	1	17	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.6 Switching Characteristics: V_{CC} = 5V ± 0.5V

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A= 25°C			SN54AHC138		SN74AHC138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	C_L = 15pF		5.7(1)	8.1(1)	1(1)	9.5(1)	1	9.5	ns
t_{PHL}					5.7(1)	8.1(1)	1(1)	9.5(1)	1	9.5	
t_{PLH}	G1	Any Y	C_L = 15pF		5.6(1)	8.1(1)	1(1)	9.5(1)	1	9.5	ns
t_{PHL}					5.6(1)	8.1(1)	1(1)	9.5(1)	1	9.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15pF		5.8(1)	8.1(1)	1(1)	9.5(1)	1	9.5	ns
t_{PHL}					5.8(1)	8.1(1)	1(1)	9.5(1)	1	9.5	
t_{PLH}	A, B, C	Any Y	C_L = 50pF		7.2	10.1	1	11.5	1	11.5	ns
t_{PHL}					7.2	10.1	1	11.5	1	11.5	
t_{PLH}	G1	Any Y	C_L = 50pF		7.1	10.1	1	11.5	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50pF		7.3	10.1	1	11.5	1	11.5	ns
t_{PHL}					7.3	10.1	1	11.5	1	11.5	

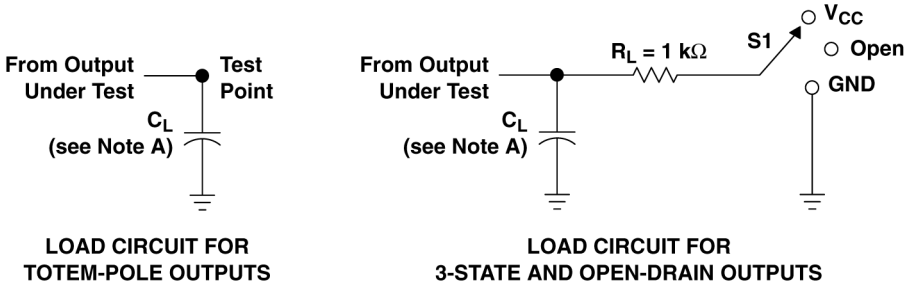
(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

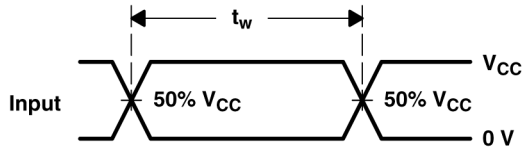
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	13	pF

5 Parameter Measurement Information

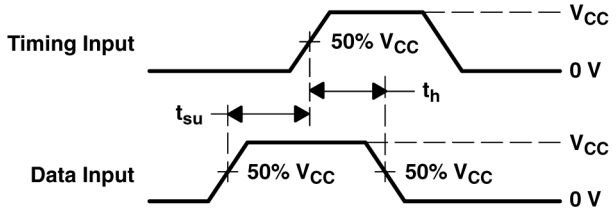


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

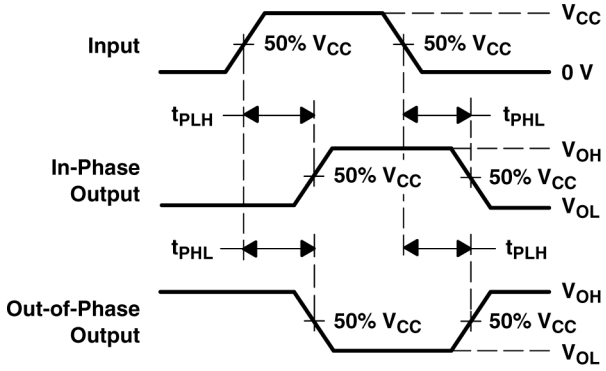
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



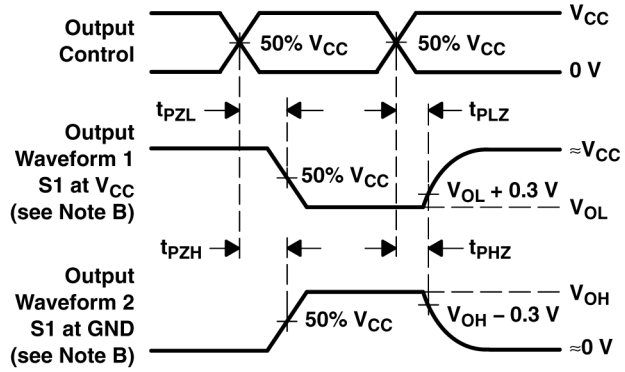
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

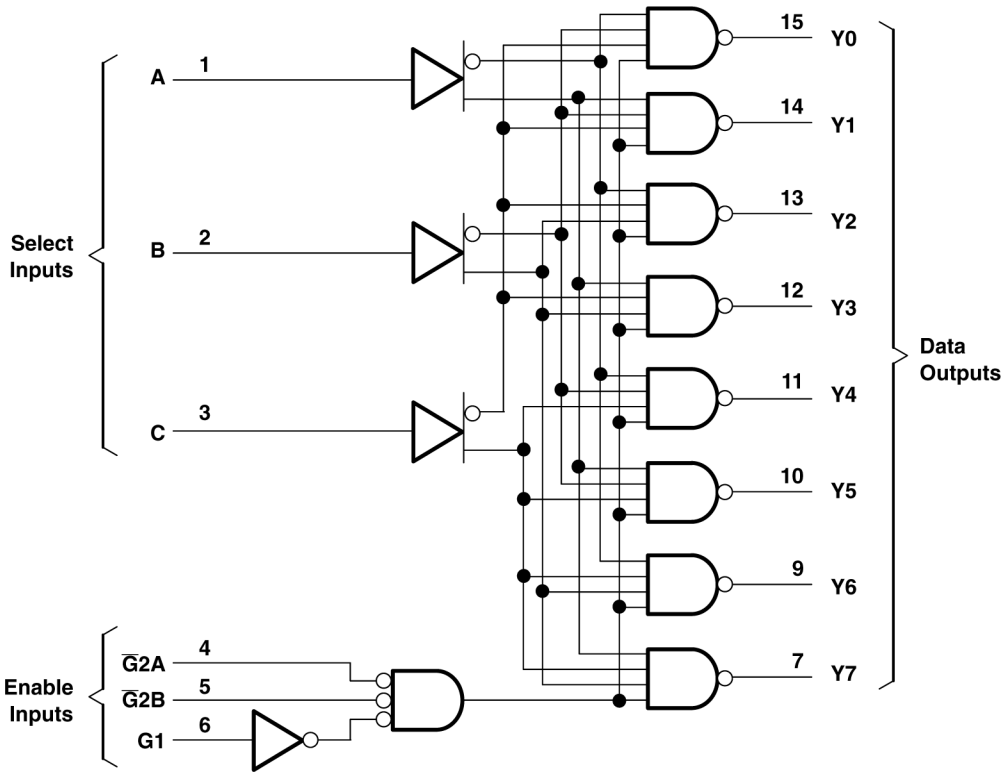
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

6 Detailed Description

6.1 Overview

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

6.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

6.3 Function Table

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

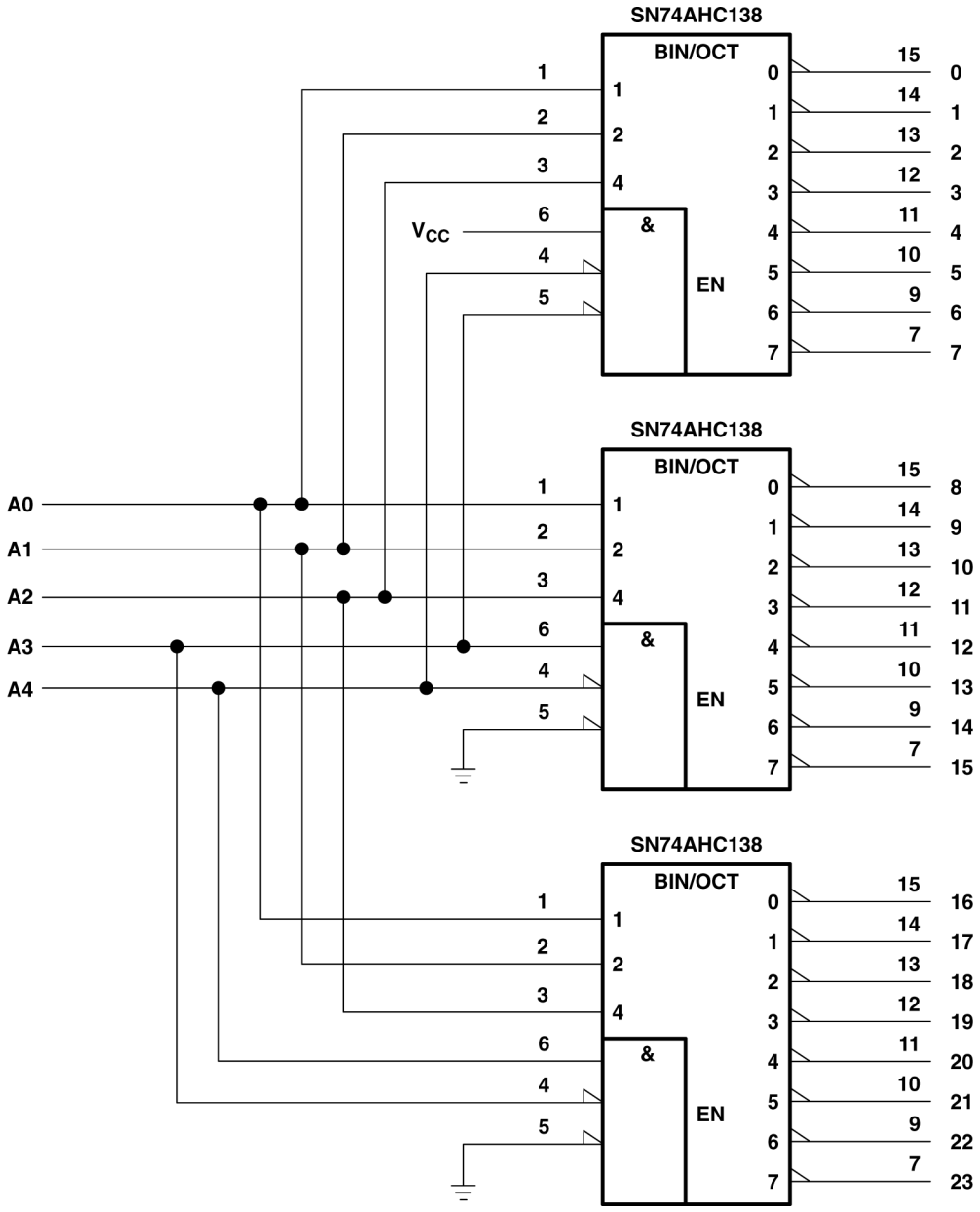


Figure 7-1. 24-Bit Decoding Scheme

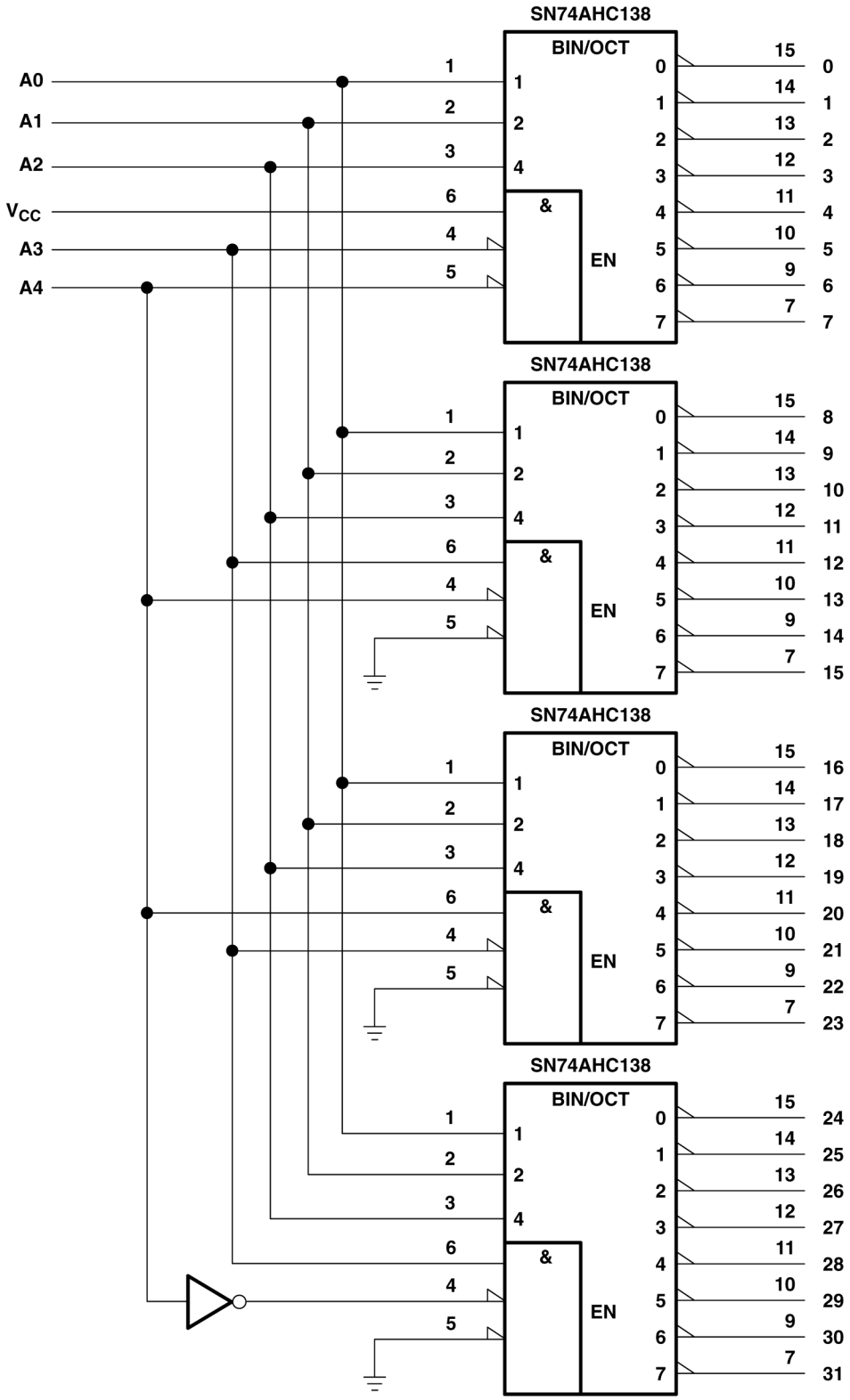


Figure 7-2. 32-Bit Decoding Scheme

7.2 Power Supply Recommendations

7.3 Layout

7.3.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

7.3.2 Layout Example

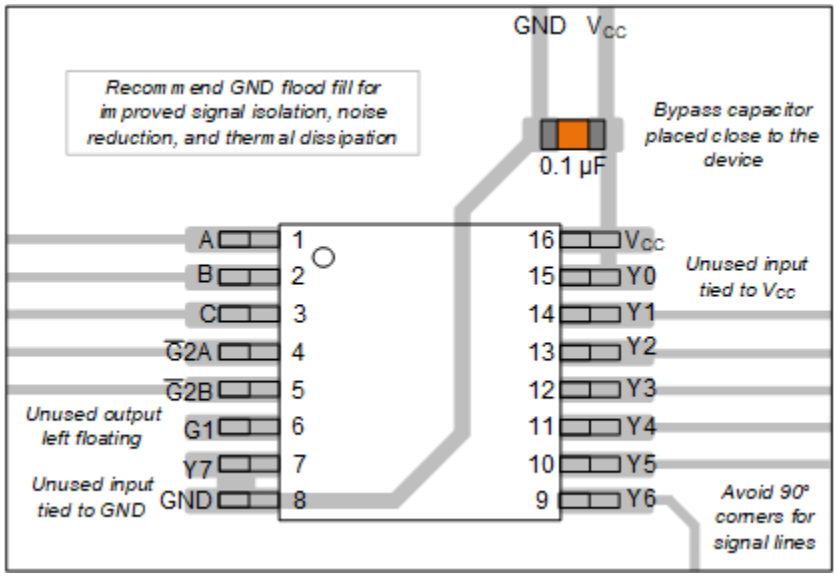


Figure 7-3. Example Layout for the SN74AHC138

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC138	Click here	Click here	Click here	Click here	Click here
SN74AHC138	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (April 2024) to Revision N (July 2024)	Page
• Updated thermal values for D package from RθJA = 73 to 93.8, all values in °C/W	6

Changes from Revision L (July 2003) to Revision M (April 2024)	Page
• Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

- Removed references to machine model.....1
- Updated thermal values for PW package from RθJA = 108 to 135.9, all values in °C/W 6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9851601Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601Q2A SNJ54AHC 138FK	Samples
5962-9851601QEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601QEA SNJ54AHC138J	Samples
5962-9851601QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601QFA SNJ54AHC138W	Samples
SN74AHC138D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	AHC138	
SN74AHC138DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA138	Samples
SN74AHC138DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA138	Samples
SN74AHC138DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC138	Samples
SN74AHC138N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC138N	Samples
SN74AHC138NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC138	Samples
SN74AHC138PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	HA138	
SN74AHC138PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA138	Samples
SN74AHC138RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HA138	Samples
SNJ54AHC138FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601Q2A SNJ54AHC 138FK	Samples
SNJ54AHC138J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601QEA SNJ54AHC138J	Samples
SNJ54AHC138W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601QFA SNJ54AHC138W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54AHC138, SN74AHC138 :

- Catalog : SN74AHC138
- Automotive : SN74AHC138-Q1, SN74AHC138-Q1
- Military : SN54AHC138

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

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