User's Guide TPS389006Q1EVM Multichannel Voltage Supervisor with *I*²*C*



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ABSTRACT

This user's guide describes the operational use of the TPS389006Q1EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS389006-Q1 Multichannel Overvoltage and Undervoltage I²C Programmable Voltage Supervisor and Monitor. This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

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1 Introduction

The TPS389006Q1EVM is an evaluation module (EVM) for the TPS389006-Q1 Multichannel Overvoltage and Undervoltage I²C Programmable Voltage Supervisor and Monitor. Test points are provided to give the user additional access, if needed, for oscilloscope or multi-meter measurements.

TPS389006Q1EVM comes with TPS389006004RTERQ1 pre-populated on pad U1 or depending on availability TPS389006Q1EVM can be fitted with socket J7 to house TPS389006004RTERQ1. This IC variant is configured for six integrated multichannel window inputs to monitor six distinct input voltage rails with two remote sense pins. The device also includes internal glitch immunity and noise filters to eliminate false resets resulting from erroneous signals. The TPS389006-Q1 device does not require any external resistors for setting overvoltage and undervoltage reset thresholds which optimizes and improves the reliability for safety systems.

I²C functionality gives flexibility in selecting thresholds, reset delays, glitch filters, and pin functionality. This device offers CRC error checking, sequence logging during turn ON or turn OFF, and a built-in ADC for voltage readouts to provide redundant error checking. In addition, TPS389006-Q1 offers a sync feature for tagging rails coming up. Rail tagging works across multiple instances of TPS389006-Q1 devices. If users need a different TPS389006-Q1 variant, the existing device must be removed from the board. The EVM board is designed to support all possible options by changing jumper configurations, such as the TPS389R0x-Q1 variant. TPS389006Q1EVM is capable of daisy-chaining, through 10-pin ribbon, up to three evaluation boards.



Figure 1-1. TPS389006Q1EVM Board Top





Figure 1-2. TPS389006Q1EVM Board Bottom

1.1 Related Documentation

Data sheet: TPS389006-Q1 Multichannel Overvoltage and Undervoltage I²C Programmable Voltage Supervisor and Monitor

1.2 TPS389006-Q1 Applications

- Advanced Driver Assistance System (ADAS)
- Sensor fusion

- Medical robotics
- Industrial robotics



2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TPS389006Q1EVM schematic, bill of materials (BOM), and layout.

2.1 TPS389006Q1EVM Schematic



Figure 2-1. TPS389006Q1EVM Main Schematic



Figure 2-2. TPS389006Q1EVM I²C Schematic with Buffers



2.2 TPS389006Q1EVM Bill of Materials

DESIGNATOR	QTY VALUE DESCRIPTION PACKAGE REFERENCE PART NUMBER		MANUFACTURER				
РСВ	1	LP051	Printed Circuit Board		TPS389006Q1EVM	Any	
C1, C6, C7, C8, C10	5	0.1µF	CAP, CERM, 0.1µF, 25V, +/- 10%, X5R, 0603	0603	CL10A104KA8NNNC	Samsung Electro- Mechanics	
C2, C3, C4, C5, C18	5	10µF	10µF ±10% 25V Ceramic Capacitor X7S 0805 (2012 Metric)	0805	C2012X7S1E106K125AC	TDK	
C9, C12, C14, C17, C27	5	1µF	CAP, CERM, 1µF, 16V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	0805	C0805C105K4RACAUTO	Kemet	
C11	1	0.1µF	CAP, CERM, 0.1µF, 50V, +/- 10%, X7R, 0603	0603	06035C104KAT2A	AVX	
C13, C15, C19(DNI), C20(DNI), C21(DNI), C22(DNI), C23(DNI), C24(DNI), C25(DNI), C26(DNI)	2	0.1µF	CAP, CERM, 0.1μF, 50V, +/- 10%, X7R, 0805 (C19 - C26 DO NOT POPULATE)	AP, CERM, 0.1µF, 50V, +/- 10%, X7R, 0805 (C19 - 0805 C0805C104K5RACTU 26 DO NOT POPULATE)		Kemet	
C16	1	10µF	10µF ±10% 10V Ceramic Capacitor X5R 0603 (1608 Metric)	citor X5R 0603 0603 C1608X5R1A106K080AC		TDK	
D1, D2	2	Super Red	LED, Super Red, SMD LED_0603 150060SS75000		Wurth Elektronik		
EN/ACT, MON1, MON2, MON3, MON4, MON5/ RS_4, MON6/RS_3, MON7, NIRQ, NSLEEP/, SYNC/NRST/MON8, SYNC_PD, TP6a, TP6b, TP6c, TP6d, TP_ADDR, TP_EXT, VDD	<pre>I/ACT, MON1, MON2, 19 Turret Terminal, Turret, TH, Triple K DN3, MON4, MON5/ 5_4, MON6/RS_3, DN7, NIRQ, NSLEEP/, NC/NRST/MON8, NC_PD, TP6a, TP6b, 6c, TP6d, TP_ADDR, EXT VDD</pre>		Keystone 1598-2	1598-2	Keystone		
GND1, GND2, GND3, GND4	4	Test Point (SMD)	Test Point, Miniature, SMT	Miniature, SMT	5019	Keystone	
H1, H2, H3, H4	4	Bumpon Pad	Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent SJ-5303 (CLEAR) Bumpon		3M	
J1, J2, J3	3	Terminal Block	Terminal Block, 5.08mm, 2x1, Brass, TH	Terminal Block, 5.08mm, 2x1, Brass, TH 2x1 5.08mm ED120/2DS Terminal Block		On-Shore Technology	
J4, J35, J36	3	Header	Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec	
J5, J6, J10, J11, J12, J13, J14, J15, J16, J17, J19, J20, J21, J22, J23, J24, J26, J27, J28, J29, J30, J31, J32, J33, J34, J37, J38, J39, J40	29	Header	Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec	
J7	1 ⁽¹⁾	Socket ⁽¹⁾	QFN CLAMSHELL 16 PIN RTE THRU HOLE WITH CENTER GND	16-Pin Socket	QFN-16(24)BT-0.5-01	Enplas	

Table 2-1. Bill of Materials

Table 2-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
J8, J18	2	Shrouded Header	Header (shrouded), 100mil, 5x2, Gold, TH	5x2 Shrouded header	5103308-1	TE Connectivity
Q1	1	MOSFET	MOSFET N-CH 20V, 0.1A, VMT3	SOT723	RUM001L02T2CL	ROHM Semiconductor
R1, R18, R19, R32	4	10kΩ	RES, 10.0kΩ, 1%, 0.1W, 0603	0603	RC0603FR-0710KL	Yageo
R2, R5, R20	3	10kΩ	RES, 10.0kΩ, 1%, 0.1W, 0603	0603	RCG060310K0FKEA	Vishay Draloric
R3(DNI)	0	10kΩ	RES, DNP, 1%, 0.1 W, 0603 (DO NOT POPULATE)	0603	RCG060310K0FKEA	Vishay Draloric
R4(DNI)	0	21kΩ	RES, DNP, 1%, 0.1 W, 0603 (DO NOT POPULATE)	0603	RC0603FR-0721KL	Yageo
R6, Rx	2	1Ω	1 Ohms ±1% 0.25 W, ¼ W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Pulse Withstanding Thick Film	0603	RCS06031R00FKEA	Vishay
R7, Ry	2	1kΩ	RES, 1.0kΩ, 5%, 0.125W, AEC-Q200 Grade 0, 0805	0805	ERJ-6GEYJ102V	Panasonic
R8	1	5.36kΩ	RES, 5.36 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF5361V	Panasonic
R9	1	16.2kΩ	RES, 16.2kΩ, 1%, 0.125W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF1622V	Panasonic
R10	1	26.7kΩ	RES, 26.7kΩ, 1%, 0.125W, AEC-Q200 Grade 0, 0805	0805 ERJ-6ENF2672V		Panasonic
R11	1	37.4kΩ	RES, 37.4kΩ, 1%, 0.125W, AEC-Q200 Grade 0, 0805	1%, 0.125W, AEC-Q200 Grade 0, 0805 ERJ-6ENF3742V		Panasonic
R12	1	47.5kΩ	δkΩ RES, 47.5kΩ, 1%, 0.125W, AEC-Q200 Grade 0, 0805 0805 ERJ-6ENF4752V		Panasonic	
R13	1	59kΩ	RES, 59kΩ, 1%, 0.125W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF5902V	Panasonic
R14	1 69.8kΩ RES, 69.8kΩ, 1%, 0.125W, AEC-Q200 Grade 0, 0805 ERJ-6		ERJ-6ENF6982V	Panasonic		
R15	1	80.6kΩ	RES, 80.6kΩ, 1%, 0.125W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF8062V	Panasonic
R16, R17, R29, R30	4	2.2kΩ	RES, 2.2kΩ, 5%, 0.1W, 0603	0603	RC0603JR-072K2L	Yageo
R21, R22, R23, R24, R25, R26, R27, R28	8	0Ω	RES, 0Ω, 5%, 0.125W, 0805	0805	RC0805JR-070RL	Yageo
R31	1	100Ω	RES, 100Ω, 5%, 0.125W, AEC-Q200 Grade 0, 0805	0805	ERJ-6GEYJ101V	Panasonic
SCL, SDA	2	Test Points	Test Point, Multipurpose, Purple, TH	Purple Multipurpose Test point	5129	Keystone
U1	0	IC	ASIL-D Multichannel Overvoltage and Undervoltage I2C Programmable Voltage Supervisor and Monitor	WQFN16	TPS389006004RTERQ1	ТІ
U2	1	IC	1A Low-Quiescent-Current Low-Dropout (LDO) Regulator, 1.2V, DRV0006A (WSON-6)	WSON-6	TLV75712PDRVR	TI

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DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
U3	1	IC	1A Low-Quiescent-Current Low-Dropout (LDO) Regulator, 1.8V, DRV0006A (WSON-6)	WSON-6	TLV75718PDRVR	ТІ
U4	1	IC	Dual-Channel, Low-Power Comparator with Integrated Reference	SON6	TLV4082DRYR	ТІ
U5, U6	2	IC	Automotive, Level-Shifting I ² C Bus Repeater, DGK0008A (VSSOP-8)	VSSOP-8 (DGK0008A)	TCA9517DGKRQ1	TI
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

Table 2-1. Bill of Materials (continued)

(1) Dependent on availability, if J7 is not available the U1 device is installed on the U1 pad.



2.3 Layout and Component Placement

Figure 2-3 and Figure 2-4 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 2-5 and Figure 2-6 show the top and bottom layouts, Figure 2-7 and Figure 2-8 show the top and bottom layers, and Figure 2-9 and Figure 2-10 shows the top and bottom solder masks of the EVM.

2.4 Layout



Figure 2-3. Component Placement—Top Assembly



Figure 2-4. Component Placement—Bottom Assembly



Figure 2-5. Layout-Top



Figure 2-6. Layout—Bottom

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3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent supply connection, but all grounds are connected on the board.

3.1 EVM Test Points

Table 3-1 lists the EVM test points as well as the functional descriptions. All TPS389006-Q1 pins have a corresponding test point on the EVM. These test points are located close to the pins for more accurate measurements. In addition to the test points listed below, the EVM also has four additional GND test points.

TEST POINT SILKSCREEN LABEL	FUNCTION	DESCRIPTION
MON1	Connection to MON1 pin	Allows the user to monitor voltage rail #1
MON2	Connection to MON2 pin	Allows the user to monitor voltage rail #2
MON3	Connection to MON3 pin	Allows the user to monitor voltage rail #3
MON4	Connection to MON4 pin	Allows the user to monitor voltage rail #4
MON5/RS_4	Connection to MON5 pin	Allows the user to monitor voltage rail #5
MON6/RS_3	Connection to MON6 pin	Allows the user to monitor voltage rail #6
MON7/RS_1/2	Connection to RS_1/2 pin	Allows the user to remote sense MON1 or MON2
SYNC/NRST/MON8	Connection to SYNC pin	SYNC pin indicates the number of monitored rails that have exited fault status and assigns tag values to each monitor voltage rail. Note when the TPS389R0x-Q1 device is utilized, the NRST signal is reported at this test pin.
SYNC_PD	Connection to SYNC_PD	Forcing the SYNC pin to toggle during test and increments an internal tag counter for each of the monitored channel (for debug purposes only)
ADDR	Connection to ADDR pin	Allows the user to measure the I ² C address voltage
NIRQ	Connection to NIRQ pin	Allows the user to monitor the interrupt (NIRQ) output
EN/ACT	Connection to ACT pin	Allows the user to set the ACT input to VDD or GND
SLEEP/ESM/WDI	Connection to SLEEP pin	Allows the user to set SLEEP input
SCL	Connection to SCL pin	Allows the user to monitor the clock signal input
SDA	Connection to SDA pin	Allows the user to monitor the data signal input
PEXT	External power supply	Allows the user to apply a power supply voltage that is not provided from the EVM
GND	GND for EVM	GND for EVM

Table 3-1. Test Points



3.2 EVM Jumpers

Table 3-2 lists the jumpers on the TPS389006Q1EVM. As ordered, the EVM has thirty-five (35) jumpers installed. Figure 3-1 is provided as visual aid.

JUMPER	JUMPER CONFIGUATION	DESCRIPTION
J1	VAUX	For connecting VAUX power to the EVM
J2	VDD	For connecting VDD power to the EVM
J3	GND	For connecting GND to the EVM
J4	Shunted (default) Pin 2 to Pin 3	For connecting ACT, NIRQ, and SLEEP to P1V8 or PEXT (Any external power)
J5 and J6	Open	For manually pulling down SLEEP and ACT pins to GND
J10, J11, J12, J13, J14, J15, J16, and J17	J15 shunted	Shunting any one of J10-J17 jumpers selects the I^2C address for TPS389006-Q1 IC on the EVM
J19, J20, and J21	Open	For connecting to the on-board I^2C buffer and pull-up voltage rail to either P1V8, PEXT or P1V2. Only shunt one of these jumpers at a time. Please remove the shunt of J22 when using one of these jumpers.
J22	Shunt	For connecting to the on-board, buffer I ² C and pull-up voltage rail to P3V3. During <i>daisy-chain</i> configuration, J22 needs to be shunted and J19, J20, and J21 needs to be open on the secondary EVMs.
J23	Shunted	Disables (U5) I ² C buffer
J24	Open	Connects PEXT to VAUX
J26 and J29	Shunted	Shunting both J26 and J29 bypasses the I ² C (U5) buffer for SDA and SCL signal lines
J27, J28, J30, and J31	Open	Shunting these jumpers buffers SCL and SDA I ² C signal lines by using the on-board (U5) buffer.
J32 and J33	Shunted	Shunting both J32 and J33 bypasses the I ² C (U6) buffer for SDA and SCL signal lines
J34	Shunted	Disables (U6) I ² C buffer
J35	Shunted (default) Pin 1 to Pin 2	SYNC pin is pulled up to P1V8. Note if TPS389R0x-Q1 variant is used, NRST is pulled up to P1V8 when using the described jumper placement.
J36	Shunted (default) Pin 2 to Pin 3	Input to one of (U4) comparators to indicate the SYNC pin has <i>tagged</i> a voltage rail that is not in a fault condition
J37, J38, J39, J40	Open	If multiple EVMs are connected in a <i>daisy-chain</i> configuration, then the following EVM boards needs to have J37, J38, J39, and J40 all shunted. By shunting these jumpers, VDD, VAUX, SYNC, and NIRQ signals is provided as inputs from the primary EVM board. Also, J22 needs to be shunted and J19, J20, and J21 needs to be open on the secondary EVMs during <i>daisy-chain</i> configuration.

· · · · · · · · · · · · · · · · · · ·	Fable 3-2 .	List	of On-	-board	Jumpers
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Figure 3-1. TPS389006Q1EVM Jumper Locations



4 EVM Setup and Operation

This section describes the functionality and operation of the TPS389006Q1EVM. Refer to the TPS389006-Q1 Multichannel Overvoltage and Undervoltage I²C Programmable Voltage Supervisor and Monitor data sheet for details on the electrical characteristics of the device.

The TPS389006Q1EVM comes with the TPS389006004RTERQ1 IC meaning the device is capable of monitoring up to six separate voltage rails. The EVM is capable of many different configurations to fully evaluate the functionality of all the TPS389006-Q1 device variants. The default jumper configuration of the TPS389006Q1EVM is mentioned in Table 3-2.

The TPS389006Q1EVM comes with USB to GPIO connector, I²C bus repeaters, comparators, two LDOs, socket and solder down footprints, the ability to monitor up to eight (8) voltage rails, the option to daisy-chain up to three EVMs at a time via 10-pin connector, jumper selectable I²C address, I²C pullup voltage options, and TPS389006004RTERQ1 IC. The TPS389006Q1EVM also provides the ability for each monitored rail to be voltage divided down by resistor dividers on each of the monitored and input lines. The user must choose appropriately sized resistors such that the divided voltage is above, below or within the window of the voltage threshold depending on the type of input sensing topology is setup for each monitored input channel. Consult the Device Threshold Table in the TPS389006-Q1 data sheet to verify proper voltage monitored values.

The TPS389006Q1EVM is designed to be daisy-chain where the primary board is connected to the USB to GPIO connector (J18) and the output connector (J8) provides VDD, VAUX, SYNC, SCL, SDA, NIRQ, and GND to the (J18) connector of the secondary board through a 10-pin ribbon cable. When the daisy-chain option is being used, jumpers on the secondary board (J19-J22 and J37-J40) must be configured properly or else possible damage to the IC or EVM can occur. Jumper settings of J19, J20, and J21 must be left open whereas J22, J37, J38, J39, and J40 need to be shunted with jumpers for proper setup of the secondary board during daisy-chain setup. Also, the I^2C rail voltage for the secondary board in the daisy-chain mode is defined as VI2CPULLUP = VAUX = 3.3V. See Figure 2-2 for reference.

Equipment needed for TPS389006Q1EVM evaluation:

- TPS389006Q1EVM
- TI's USB2GPIO interface adapter (with ribbon cable)
- Power Supply (3.3V)
- Multimeters
- Multi-channel Oscilloscope (review evaluation waveforms)
- Jumper Wires/Cables



4.1 Setup and GUI Installations

4.1.1 TPS389006Q1EVM Hardware Setup

Follow the steps below for TPS389006Q1EVM hardware setup:

- 1. Connect VAUX (J1) and VDD (J2) to 3.3V from the power supply.
- 2. Connect GND (J3) to ground from the power supply.
- 3. Make sure the jumpers are connected as per the guidelines in the Table 3-2.
- 4. Before allowing the output of the power supply to be engaged, check if the power supply voltage is set at 3.3V and the power supply output current is limited to 10mA.
- 5. Connect the TI's USB2GPIO USB interface adapter to J18 (USB2GPIO connector) using a 10-pin ribbon cable.
- 6. Connect the TI's USB2GPIO USB interface adapter to the USB port of the computer.
- 7. Connect any voltage supply rail that needs monitoring to any of the voltage monitoring inputs (MON1 MON8).
- 8. The description of the TPS389006Q1EVM connections can be found in Figure 4-1.



Figure 4-1. TPS389006Q1EVM Connection Description



4.1.2 TPS389006Q1EVM Software Setup

Follow the steps below for TPS389006Q1EVM GUI software installation:

- 1. Download the Fusion Digital Power Designer Platform GUI for TPS389006Q1EVM.
- 2. Open the downloaded file.
- 3. In the Welcome Wizard window, click Next.
- 4. Accept the license agreement and then click Next.



Figure 4-2. Setup License Agreement Window

5. The default destination folder works best. Click Next.

🔀 Setup - Fusion Digital Power Designer	_		×
Select Destination Location Where should Fusion Digital Power Designer be installed?			ð
Setup will install Fusion Digital Power Designer into the follo	wing fo	older.	
To continue, click Next. If you would like to select a different folder,	click B	rowse.	
rogram Files (x86)\Texas Instruments\Fusion Digital Power Designe	E	Browse	
At least 72.6 MB of free disk space is required.			
< Back Nex	t >	Ca	incel

Figure 4-3. Setup Destination Window



6. Click *Next* for the Select Start Menu Folder option.

👸 Setup - Fusion Digital Power Designer	_		×
Select Start Menu Folder Where should Setup place the program's shortcuts?			
Setup will create the program's shortcuts in the following St	art Me	enu folder.	
To continue, dick Next. If you would like to select a different folder,	click B	rowse.	
Texas Instruments Fusion Digital Power Designer		Browse	
Don't create a Start Menu folder			
< Back Nex	t >	Ca	incel

Figure 4-4. Setup Window - Start Menu Selection

7. There is no need to install additional options for this EVM. Click Next.

😽 Setup - Fusion Digital Power Designer		_		\times
Select Additional Tasks Which additional tasks should be performed?			Q	
Select the additional tasks you would like Set Power Designer, then click Next.	up to perform while	installing Fus	ion Digiti	al
Additional icons:				
🗹 Create a desktop icon				
🗹 Create a Quick Launch icon				
Other desktop shortcuts				
SMBus I2C SAA Debug Tool				
UCD9xxx Device GUI				
Additional Tasks:				
Add application directory to your system	PATH			
[< Back	Next >	Can	icel

Figure 4-5. Setup Window - Additional Tasks



8. Finally click Install to install the Fusion software.

ß	Setup - Fusion Digital Power Designer —		×
	Ready to Install Setup is now ready to begin installing Fusion Digital Power Designer on your computer.		Ð
	Click Install to continue with the installation, or click Back if you want to review change any settings.	or	
	Destination location: C:\Program Files (x86)\Texas Instruments\Fusion Digital Power Designer		^
	<	>	~
	< Back Install	Ca	ancel

Figure 4-6. Setup Installation Window

9. Click on *Finish* to complete the installation setup and launch the software.



Figure 4-7. Installation Complete Window



4.2 Quick Start to TPS389006Q1EVM GUI

Please follow the steps below precisely to quickly evaluate the TPS389006-Q1. In this quick start, the TPS389006Q1EVM is set up to monitor several power supply rails after the ACT pin is triggered.

- 1. Make the hardware connections and software installation described in Section 4.1 have been completed. Feel free to skip the GUI installation if the *Fusion Digital Power Designer* for TPS389006Q1EVM GUI has been installed already.
- 2. Power the EVM by turning on the power supply. Note that the voltage and current limits at the power supply is set at 3.3V and 10mA.
- 3. Once the TI's USB2GPIO USB interface adapter is connected to EVM and the laptop, launch the evaluation software *Fusion Digital Power Designer*.
- 4. Click on *I2C GUI* on the bottom right of GUI.

Fusion Di	igital F	,omsi	Desigi	191				
Version 7.6.	7.5 [202	21-08-12	2]					
to compatible PMBus	s devices wer your device.	e found. Plea	ise check that	t the serial cat	ble end of your	USB adapte	r is attached to your device and	
Scanning Mode:	Device	IDAndCod	eAndICDev	viceID				
USB Adapter Fir USB Adapter ID:	mware Vers SAA, Serial N	ion: 1.0. umber: 6353	11 37f9700000					
Bus Speed:	Packet B	Error Check	ing: ALE	RT Pullup:	2.2 kΩ	\checkmark		
🔾 100 kHz	Enable	led	CLO	CK Pullup:	2.2 kΩ	\checkmark		
• 400 kHz	🔿 Disat	oled	DAT	A Pullup:	2.2 kΩ	~		
Signals								
SMBALERT#:	ACK: High	. (Refresh					
Control Lines:	#1	#2	#3	#4	#5			
(click to set)	OHigh	🔘 High	🔘 High	OHigh	🔘 High		Refresh All	
	Low	 Low 	 Low 	Low	• Low			

Figure 4-8. Fusion Welcome Window



5. Click on Change Scan Mode to select TPS389xxx and then click OK.

🌵 Texas Instruments - Fusion D	igital Power Designer					. 🗆 🗙
File Tools						
Q Scan for TPS389xxx Change Si	an Mode 🕨 Start Polling	Polling Interval	1000 ms			
# Address 🛆 D	evice					1
					1	
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Timestamo	Message					
CopyLog ClearLog						Indude poling activities
Fusion Digital Power Designer v7.6.	7.5.Alpha (For WCM testing)) No Adapter		Not Saved		TEXAS INSTRUMENTS fusion digital power

Figure 4-9. Fusion Scan Window

🐌 Texas Instruments - Fusion Digital Power Designer									
File Tools									
λ San for TPS389ox Change San Mose ► Sant Polling Interval 1000 ms									
# Address 🛆 Device									
4) Device Scan Editor	. 🗆 🗙								
Set All Addesses To: Skp (TP5538:u05383) (TP5595xx (TP538700x (TP5388xx) XP53830) (TP Allow address zero (S842A50 TPS54xC2x								
1d 0x01 TP5389xxx 🕑 18d 0x12 TP5389xxx 💟 34d 0x22 TP5389xx 👽 50d 0x32 TP5389xx	✓ 66d 0x42 TPS389xxx ✓ 82d 0x52								
2d 0x02 TPS389xxx 🕑 19d 0x13 TPS389xxx 💟 35d 0x23 TPS389xxx 🗸 51d 0x33 TPS389xxx	✓ 67d 0x43 TPS389xxx ✓ 83d 0x53								
3d 0x03 TPS889xxx 💟 20d 0x14 TPS889xxx 💟 36d 0x24 TPS889xxx 💟 52d 0x34 TPS889xxx	✓ 68d 0x44 TPS389xxx ✓ 84d 0x54								
4d 0x04 TPS389xxx ♥ 21d 0x15 TPS389xxx ♥ 37d 0x25 TPS389xxx ♥ 53d 0x35 TPS389xxx	✓ 69d 0x45 TPS389Xxx ✓ 85d 0x55								
5d 0x05 TP\$389xxx 🗸 22d 0x16 TP\$389xxx V 38d 0x26 TP\$389xxx V 54d 0x36 TP\$389xxx	✓ 70d 0x46 TPS389xxx ✓ 86d 0x56								
6d 0x06 TPS389xxx 🗸 23d 0x17 TPS389xxx 🗸 39d 0x27 TPS389xxx 🗸 55d 0x37 TPS389xxx	✓ 71d 0x47 TPS389xxx ✓ 87d 0x57								
7d 0x07 TP5389xxx ✓ 24d 0x18 TP5389xxx ✓ 40d 0x28 TP5389xxx ✓ 56d 0x38 TP5389xxx	✓ 72d 0x48 TPS389x00x ✓ 88d 0x58								
8d 0x08 TPS389xxx ∨ 25d 0x19 TPS389xxx ∨ 41d 0x29 TPS389xxx ∨ 57d 0x39 TPS389xxx	✓ 73d 0x49 TPS389xxx ✓ 89d 0x59								
9d 0x09 TP\$889xxx 🗸 26d 0x1A TP\$889xxx 🗸 42d 0x2A TP\$889xxx 🗸 58d 0x3A TP\$889xxx	✓ 74d 0x4A TPS389xxx ✓ 90d 0x5A								
10d 0x0A 1P5389xxx ⊻ 27d 0x18 1P5389xxx ⊻ 43d 0x28 1P5389xxx ⊻ 59d 0x38 1P5389xxx	✓ 75d 0x48 1125389200x								
11d 0x08 TP5389xxx	✓ 76d 0x4C TP5389xxx ✓ 92d 0x5C								
13d 0x00 TF5389xxx 🗸 29d 0x10 TF5389xxx 🗸 45d 0x20 TF5389xxx 🗸 61d 0x30 TF5389xxx	✓ 77d 0x40 TP5389xxx ✓ 93d 0x5D								
14d 0x0E TPS389xxx ∨ 30d 0x1E TPS389xxx ∨ 46d 0x2E TPS389xxx ∨ 62d 0x3E TPS389xxx	✓ 78d 0x4E 1125389xxx ✓ 94d 0x5E								
15d 0x0F TPS389xxx 🗸 31d 0x3F TPS389xxx 🗸 47d 0x3F TPS389xxx V 63d 0x3F TPS389xxx	✓ 79d 0x4F TPS389xxx ✓ 95d 0x5F								
16d 0x10 TPS389xxx ✓ 32d 0x20 TPS389xxx ✓ 48d 0x30 TPS389xxx ✓ 64d 0x40 TPS389xxx	✓ 80d 0x50 TP5389xxx ✓ 96d 0x60								
17d 0x11 TPS389xxx	✓ 81d 0x51 TP5389xxx								
Fusion Digital Power Designer v7.6.7.5.Alpha (For WCM testing) No Adapter	TEXAS INSTRUMENTS fusion digital power								

Figure 4-10. Fusion Scan Selection Window

6. Scan for the TPS389006Q1EVM by clicking on Scan for TPS389xxx on top left of the window.

🗄 Texas	Instrument	- Fusion Digital Pov	ver Designer					. 🗆 🔀
File To	ols							
Q Scent	or TPS389xxx	Change Scan Mode	Start Polling	Polling Interval	1000	ms		
#	Address	△ Device						
Log								J
Timesta	10	Message						
Copy	.og Clea	rLog						Include polling activities
Fusion Di	gital Power De	signer v7.6.7.5.Alpha	(For WCM testing) No Adapter			Not Saved	TEXAS INSTRUMENTS fusion digital power

Figure 4-11. Fusion Scan Window - Scanning for TPS389006Q1EVM

7. Once the EVM is discovered, select Click to Configure.

🌵 Texas Instruments - I	usion Digital Power Designer				_ 0 🛛
File Tools					
Q Scan for TPS389xxx C	hange Scan Mode 🕨 Start Polling Polling Interval	1000 ms			
# Address	△ Device				i i
1 04h (4d)	TPS389004			Click to Configure	
Log					
	Mercane				1
14-24-52 440	Scanning LISB Adapter #1 at address 121d (TE	IS389yyyx) for devices			n
14-24-52 472	12CRead (Address 121d Cmd 0x00): NACK <	moty >			
14:24:52.498	Scanning LISB Adapter #1 at address 122d (TE	IS 389yox) for devices			
14:24:52.529	I2CRead (Address 122d, Cmd 0x00): NACK <	moty>			
14:24:52.558	Scanning USB Adapter #1 at address 123d (TF	S389xxx) for devices			
14:24:52.593	I2CRead (Address 123d, Cmd 0x00): NACK <e< th=""><th>empty></th><th></th><th></th><th></th></e<>	empty>			
14:24:52.620	Scanning US8 Adapter #1 at address 124d (TF	S389xxx) for devices			
14:24:52.655	I2CRead (Address 124d, Cmd 0x00): NACK <e< th=""><th>empty></th><th></th><th></th><th></th></e<>	empty>			
14:24:52.689	Scanning USB Adapter #1 at address 125d (TF	S389xxx) for devices			
14:24:52.727	I2CRead (Address 125d, Cmd 0x00): NACK <e< th=""><th>empty></th><th></th><th></th><th></th></e<>	empty>			
14:24:52.752	Scanning USB Adapter #1 at address 126d (TF	S389xxx) for devices			
14:24:52.781	I2CRead (Address 126d, Cmd 0x00): NACK <	empty>			
14:24:52.806	Found 1 device.				(III)
Copy Log Clear Lo					Include poling activities
Fusion Digital Power Design	ner v7.6.7.5.Alpha (For WCM testing) USB Adapter	v1.0.11 [PEC; 400 kHz]	Not Saved		TEXAS INSTRUMENTS fusion digital power

Figure 4-12. Fusion Scan Window - Scan for TPS389006Q1EVM Completed

8. Once the *Click to Configure* box has been selected, the Fusion Digital Power Device GUI for the TPS389006-Q1 appears as shown below. The GUI image shows the *General Config*, *Sequencing*, *Clear/ Reset*, *Telemetry*, and Polling (Plotting the monitored voltage rails) sub-windows.

Image: Class and the state st	anaral Confin	a) and					
Image: Down to ball Image: Down to ball<	- VMON_MISC (11h) INT_CONTROL (18h) Enable Interrupt (1Ch)	- VHON_C				6	
Image: Sector Sector Model (Sector Sector	Timestamp Overwrite Enable Register CRC ECC single error correction SEQ Overwrite Enable STRC ELLI+n-test-complete	PORCE	IRQ (NERQ pin is c NERQ pin is f	controlled by intern force asserted (low	pt registers faults	Monitor Comparator Offset Comparisations	Y Max 10.00 🕆 Y Min 0.00 🛧 🖌 Show dust info
	Require PEC PEC Builton test complete fai	FORCE	TINC O SYNC pin is c	controlled by seque forced asserted (lor	nce monitoring logic ()	Clear PROT1/PROT2 registers	Show value on pict Reg Coder - V +
Image: District (AD) Image: District (AD) <td>- Sequence Timeout (ASh & A6h) 25 - Tra 25 - Tra Tra Tra StQ REC CTL (Ach) - Record Start - SEQ ENTER ACK - TimeStarp ACK - SEQ ENTER ACK</td> <td>S.EP_P</td> <td>VR C Low Power (High Power (</td> <td>reduce monitoring, (full monitoring, sar</td> <td>OVHF and UVHF only) ie as ACTIVE state)</td> <td>Reset SYNC Counter</td> <td>READ_VING GAL C READ_VINA GAL C</td>	- Sequence Timeout (ASh & A6h) 25 - Tra 25 - Tra Tra Tra StQ REC CTL (Ach) - Record Start - SEQ ENTER ACK - TimeStarp ACK - SEQ ENTER ACK	S.EP_P	VR C Low Power (High Power (reduce monitoring, (full monitoring, sar	OVHF and UVHF only) ie as ACTIVE state)	Reset SYNC Counter	READ_VING GAL C READ_VINA GAL C
Signature Signature <t< td=""><td>− Palse Width Duration (A7b)</td><td>Telemetry</td><td></td><td></td><td></td><td>G</td><td></td></t<>	− Palse Width Duration (A7b)	Telemetry				G	
Non-wee of the (dis) Non-wee o	austrios	SINC_COUNT	0				8
States faced de States fac	HONA HONS HONE HON	READ_VIN	0.27	0.2 0.2	v 0.2V		
Name off action (dis) 1	ower ON Order (Boh : B3h) 1 ¥ 1 ¥ 1 ¥ 1 ¥	SEQ ON Order	0	0	0 0		
States Lation (200): 6.8.4) 1<	ower OFF Order (C0b : C3b)	SEQ OFF Orde	٥	0	0 0		
skey clor Outre (3b) 1	lega Exit Order (D0h : D3h)	SEQ EXS Order	0	0	0 0		
Alternative de	lean Fater (Infer (Fife - Fife)	SEQ BNS Orde	0	0	0 0		
Attract Table		SEQ Timestan	0.5	0 s 0	s 0 s		
Atlas Registra	terrupt Enable						
	Atage Range and Threshold	Status Regist	(D)			Q	
							2

Figure 4-13. Fusion Digital Power Device GUI - TPS389006Q1EVM (Image #1)

 The GUI image below continues to show the additional sub-windows that are in the GUI for the TPS389006-Q1. The GUI image includes the *Interrupt Enable*, *Voltage Range and Threshold*, *Status Registers*, and Polling (plotting the monitored voltage rails) sub-windows.



Figure 4-14. Fusion Digital Power Device GUI - TPS389006Q1EVM (Image #2)



10. The last GUI image below shows the last five registers in the Status Registers sub-window.

	ral Confin	INT_SEQ_ON (1Ah)	INT_SEQ_OFF (1Ch)	INT_SEQ_EXS (10h)	Y Max 20.00 [6] Y Ma 0.00 [6] (1)
		7 850	7 RSID	7 RSND	
Nume Num Nume Num Nume Nume N	uencing	6 RSVD	6 RSID	6 RSND	(
	rrupt Enable	5 RS/D	5 RSVD	5 RSVD	Aller and Aller and All Constants
	age Range and Threshold	4 RSVD	4 RSVD	4 RSVD	
····································	HONA HON3 HON2 HON1	3 SEQ_084 (03)	3 SEQ_OFF4 000	3 SEQ_EX54	S and water on her well case - S (4)
	roltage Scaling (1fh)	2 SEQ_ON3 (01)	2 SEQ_OFF3	2 SEQ_EX53	READ_VINI 0.40 3 READ_VIN2 0.41 3
1:Bachd (D, D), D,	1x ¥ 1x ¥ 1x ¥ 1x ¥	1 SEQ_ON2 (55)	1 SEQ_OFF2 55	1 SEQ_EXS2	READ_VING 0H2 COREAD_VIDH CHIL CO
mg mg <td< td=""><td>(hreshold (20h, 21h, 22h, 23h + (N-1)*0x10 where N is channel number)</td><td>0 StQ_001 (03</td><td>0 SEQ_OFF1 000</td><td>0 SEQ_EX51 003</td><td>10</td></td<>	(hreshold (20h, 21h, 22h, 23h + (N-1)*0x10 where N is channel number)	0 StQ_001 (03	0 SEQ_OFF1 000	0 SEQ_EX51 003	10
Windfield	W 0.200日 0.200日 0.200日 0.200日 V				
m m	gh Pass	THT STO THS (20b)	THE CONTROL (22b)	INT TEST (21b)	
	6/ 0.200 문 0.200 문 0.200 문 V	7 850	7 2500	7 850	
	64 0.200 ⊕ 0.200 ⊕ 0.200 ⊕ 0.200 ⊕ ν	6 820	6 890	6 RSVD	•
	W Pass (2) a match a match a match w	5 R940	\$ RSVD	5 RSVD	
	(vavid) (vavid) (vavid) (vavid) (vavid)	4 RSVD	4 CRC 000	4 RSVD	
0*** 1 0 1 0 1 0	Debounce (24h + (N-1)*0x10 where N is channel number)	3 SEQ_EN54 (03	3 NIRO	3 ECC_SEC	
W N	OV 0.1 V 0.1 V 0.1 V 0.1 V M	2 SEQ_ENS3 (33)	2 TSD 200	2 ECC_DED 000	
interregences prints (SS) (258 + 168 3 / 160 0 doers it is deament interregences prints (SS) (258 + 168 3 / 160 0 doers it is deament interregences prints (SS) (258 + 168 3 / 160 0 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 3 / 160 doers it is deament interregences prints (SS) (258 + 168 doers it is deament in	UV 0.1 V 0.1 V 0.1 V 0.1 V M	1 SEQ ENS2 (00	1 5700	1 LINST C 000	
Image: mark (a) (2 % (b) '1/bit) durit if a dataset aduated aduate) Image: mark (a) (2 % (b) '1/bit) durit if a dataset aduated aduate		0 510 [051 003	0.967	0 BIST 000	
Non- Non- <th< th=""><th>low Frequency Path G(s) (25h +(N-1)*0x10 where N is channel number)</th><th></th><th></th><th></th><th>4</th></th<>	low Frequency Path G(s) (25h +(N-1)*0x10 where N is channel number)				4
1 1 <th>1000 ¥ 1000 ¥ 1000 ¥ /dr</th> <th></th> <th></th> <th>1</th> <th></th>	1000 ¥ 1000 ¥ 1000 ¥ /dr			1	
1 1 <td></td> <td>WHON_STAT (308)</td> <td>151_100(318)</td> <td>OIT_SIAT(328)</td> <td></td>		WHON_STAT (308)	151_100(318)	OIT_SIAT(328)	
1 1 <td></td> <td>/ FALSARE</td> <td>7 KOID</td> <td>7 KSTD</td> <td></td>		/ FALSARE	7 KOID	7 KSTD	
1 1		S CT IND	s pre ste	s por	2
1 1 1 1 1 1 1 1 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 <td></td> <td>4 ST NRO</td> <td>4 ECC DED</td> <td>4 85/0</td> <td></td>		4 ST NRO	4 ECC DED	4 85/0	
2 1 <td></td> <td>3 ST ACTSLP</td> <td>3 815T VH</td> <td>3 11014</td> <td></td>		3 ST ACTSLP	3 815T VH	3 11014	
1 1 <td></td> <td>2 ST_ACTSHDN</td> <td>2 825T_NVM</td> <td>2 MONS</td> <td></td>		2 ST_ACTSHDN	2 825T_NVM	2 MONS	
0 0 0 857.4 0 1008 7 96.05.507 0 1000 7 96.05.607 0 1000 7 96.05.607 0 1000 1 96.05.607 1000 1 15.007 15.007 1 15.007 15.007 1 15.007 15.007 1 15.007 15.007 1 15.007 15.007 1 15.007 15.007 1 150.07,007 150.07,007 1 150.07,007 150.07,007 1 150.07,007 150.07,007		1 ST_SYNC	1 815T_L	1 MON2	0.00 00:00 00:00 00:0
No. No. <td></td> <td>0 RSVD</td> <td>0 8IST_A</td> <td>0 MON1</td> <td></td>		0 RSVD	0 8IST_A	0 MON1	
Stop_BitC_static_(bis) Stop_cons_static_(bis) F Stop_cons_static_(bis) Stop_cons_static_(bis)					
WDMET_ATA (19h) WDMET_ATA (19h) 1 WEL_ATA (19h) 2 MEL_ATA 4 MEL_MET_ATA 6 MEL_MET_ATA 7 MEL_ATA 8 MEL_MET_ATA 8 MEL_ATA 9 MELATA 9 MELATA 9 MELATA <td></td> <td></td> <td></td> <td></td> <td></td>					
2 MC_ACTIV 2 100 5 MS_ACTIV 100 100 4 MS_ACTIV 4 1500 5 MS_ACTIV 4 1500 1 MS_ACTIV 2 340,400 1 MS_ACTIV 2 340,400 2 MS_ACTIV 2 340,400 9 MS_ACTIV 0 940,400		SEQ_REC_STAT (34h)	SEQ_OW_STAT (35b)		
0 MQ_BEC_BTTL 0 0 0 1 SQL_ME_BTD 0 0 0 0 1 SQL_ME_BTD 0 0 0 0 0 1 SQL_ME_BTD		7 REC_ACTIVE	7 RSID		
1 100,00,000 2 100,00,000 2 100,00,000 2 100,00,000 2 100,000 2 100,000 3 100,000 4 100,000 5 100,000 6 100,000,000		6 SEQ_REC_BIT1	6 R5/ID		
- 1 15.000 AUT - 15.00 AUT - 1		5 SEQ_REC_BITO	\$ RSVD		
2 340,07,07 2 340,07,07 1 340,07 1 340,07		4 TS_RDY	1 15_0W		
1 Stage, Stage 2 Stage, Stage 3 Stage, Stage		3 550_00_007	5 5EQ_0M_0W		
			sto pr on		
		a sto the poy	0 SED ENS OW		
		· sto_bis_kor	· sugar ow		
		<		2	

Figure 4-15. Fusion Digital Power Device GUI - TPS389006Q1EVM (Image #3)



4.3 Example Operation of TPS389xxx-Q1

The example below shows a TPS389004-Q1 monitoring four voltage supply rails on the TPS389006Q1EVM. Please follow the steps in Section 4.1.1 and Section 4.1.2 before evaluating the TPS389004-Q1. In this example, the TPS389006Q1EVM is set up to monitor several power supply rails after the ACT pin is asserted. Below, Figure 4-16 shows how the TPS389006Q1EVM was setup to monitor four voltage supply rails.



Figure 4-16. TPS389006Q1EVM Monitoring Four Voltage Supply Rails

- 1. Connect the TPS389006Q1EVM VDD and VAUX inputs to a 3.3V external power supply. Note that the voltage and current limits of the power supply must be set at 3.3V and 10mA.
- Connect the TPS389006Q1EVM with TI's USB2GPIO USB Interface Adapter ribbon to J18 (USB2GPIO connector). Connect the USB plug from the USB Interface Adapter to the USB port of the computer. The TI USB Interface Adapter communicates to the TPS389004-Q1 IC via I²C protocols.
- 3. Verify that the jumper settings, highlighted in red in Figure 4-16, are set on the TPS389006Q1EVM.
- 4. Ground turret (MON7/RS_1/2).
- 5. Apply 0.8V to MON1, 1.0V to MON2, 1.8V to MON3, 3.3V to MON4 to the turrets of TPS389006Q1EVM.
- 6. Final Connections must look similar to Figure 4-16.
- 7. Open up the Fusion Digital Power Designer GUI on the computer and follow Section 4.2.
- 8. Once the EVM is discovered and *Click to Configure* has been selected, the GUI is similar to Figure 4-13, Figure 4-14, Figure 4-15.
- 9. Scroll to the bottom of the *Interrupt Enable* sub-window and enable all four monitoring inputs by clicking the empty boxes. The GUI image, Figure 4-17 below, shows all the monitoring inputs being selected in the highlighted *black-box*.
- 10. In the *Voltage Range and Threshold* sub-window, enter the undervoltage (UV) and overvoltage (OV) threshold values for the monitoring inputs. One thing to note, any monitoring inputs that are higher than 1.5V needs to select 4*x* in the *Voltage Scaling (1Fh)* field. The GUI image below, highlighted by a *yellow-box*, shows is described above.
- 11. Once steps 9 and 10 are completed, press *Write to Hardware* and the USB Interface Adapter communicates to the TPS389004-Q1 IC. Next, press *Start Polling* and both the Telemetry (shown in the highlighted orange-box) and the graphical waveform of the monitored inputs (shown in the highlighted red-box) is shown in the GUI.
- 12. If one of the monitored inputs senses a fault, then an interrupt indicator is displayed (illumination of a red LED) on the TPS389006Q1EVM. Also, one of the bit registers found in the *Status Registers* sub-window, highlighted in the green-box, also shows a fault in red color.



- 13. To clear the fault interrupt, press *Stop Polling*, go to the *Status Registers* sub-window, locate the red color fault interrupt and click on *CLR*. Then click on *Write to Hardware*. This procedure clears the fault interrupt and allows the device to continue to monitor the input channels.
- 14. Steps 8 through 13 refers to Figure 4-17 below.

	X Discard Changes	C Refresh All	Store to NVM	Restore from NVM Clear Fault	Stop Polling Cli	ok to disable Test Mi	de						
lou Device	ENS (19h)					^		ona orea o y interrupt registers radius	Monitor Comparator Offset	Y Max	50.00 🕀 Y Min	0.00 🕀 🗭	
	ENS (1Ah)						FORCE SYNC O SYNC pin is c	once asserted (low) controlled by sequence monitoring logic	Clear PROT1/PROT2 registers				e
sk Fil	ON (A1h)						SYNC pin is f O Low Power (reduce monitoring, OVHF and UVHF only)		Y Max	4.00 🐥 Y Min	0.00 🕀 🔽 Show chart i	info
	OFF (A2h)						SLEEP_PWR O High Power (full monitoring, same as ACTIVE state)	Reset SYNC Counter	READ_V	/IN1 0x40 🚫 REA	D_VIN2 0x41 🚷	
	ENS (A3h) ENS (A4h)									READ_N	/IN3 0x42 🔞 REA	D_VIN4 0x43 🔇	
		U U	U			s	INC_COUNT 1			4			
ble	Monitoring (1Eh)	2	~				MON4	MON3 MON2 MON1					
-	1.41 1.11					s	EQ.ON Order 1	1.84 V 1.02 V 0.815 V 1 1 1		3.2			
Kange al	na i nresnola MON4 MO	13 MON2	MONI	1		s	EQ OFF Order 0	0 0 0					
ige Scalii	ng (1fh)	v 1v	• 1• 1	T		s	SQ ENS Order 0	0 0 0					
shold (20	0h, 21h, 22h, 23h + (N	1)*0x10 where	N is channel				EQ Timestamp SE-OS s 5	E-05 s 5E-05 s 5E-05 s		2.4-			
UV	2.50 💭 1.50	0.600	0.600 🤤	Ξv		6	atus Registers						
ov	4.00 🕀 2.20	1.200	1.000 🔅	V		E E	INT_SRC (10h)	INT_MONITOR (11h)	INT_UVHF (12h)	1.6			1.84
UV ISS	2.50 🕀 1.50	0.600	0.600 🕀	Ψ			7 OTHER 6 RSVD	7 SEQ_ON 6 Bit6	7 RSVD 6 RSVD				
ov	4.00 🕀 2.20	1.200 🕀	1.000 🕀) v			5 RSVD	5 SEQ_EXS	5 RSVD				1.02
ince (24	4h + (N-1)*0x10 when	e N IS Channel P	umber)				4 RSVD 3 RSVD	4 SEQ_ENS 3 OV LE	4 RSVD 3 UV HF4 00	0.8-			0.82
ov	0.1 🛛 0.1	0.1	0.1	√ µs			2 TEST	2 OV_HF	2 UV HE3				
UV	0.1 🔟 0.1	0.1	0.1	v us			1 CONTROL	1 UV_LF	1 UV HF2				
Frequenc	cy Path G(s) (25h + (N	1)*0x10 where	N is channel	number)			0 MONITOR	0 UV_HF	0 UV_HF1 (0	25:40 26:00	26:20 2	26:40 27:00
	1000	1000	1000	1									

Figure 4-17. TPS389006Q1EVM GUI Setup for Monitoring Four Voltage Supply Rails

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

C	hanges from Revision B (July 2023) to Revision C (August 2024)	Page
•	Added TPS389R0x-Q1 variant throughout document	3
•	Updated SYNC/NRST/MON8 behavior when using TPS389R0x-Q1	12
•	Updated J36 configuration when using TPS389R0x-Q1	13



С	hanges from Revision A (May 2023) to Revision B (August 2023)	Page
•	Changed the OPN to TPS389006004RTERQ1 from TPS389006Q1 in Section 1	3
•	Added statement clarifying the availability of socket J7 in Section 1	3
•	Added table note to clarify availability of J7	7
•	Changed the OPN to TP\$389006004RTERQ1 from TP\$389006Q1 in Section 4	15

C	hanges from Revision * (February 2022) to Revision A (May 2023)	Page
•	Changed the OPN to TPS389006004RTERQ1 from TPS389006Q1 in TPS389006Q1EVM Main S	chematic .5

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WARNING

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
- 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

- 3.3 Japan
 - 3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に 輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

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- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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- 3.4 European Union
 - 3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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