

EVM User's Guide: F29H85X-SOM-EVM

F29H85X controlSOM Evaluation Board



Description

F29H85X-SOM-EVM is an evaluation and development board for TI C2000™ MCU series of F29H85x and F29P58x devices. Its system-on-module design with three 120-pin high-speed/high-density connectors is ideal for initial evaluation and prototyping. An [XDS110ISO-EVM](#) debug probe is required for evaluation of the F29H85X-SOM-EVM, and can be purchased separately.

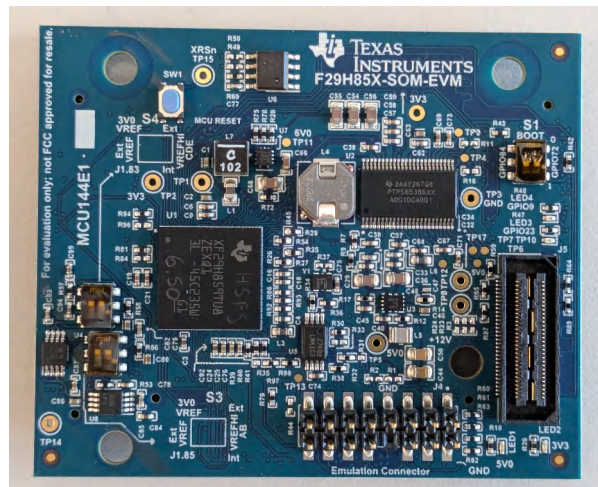
Get Started

1. Order the F29H85X controlSOM evaluation board (EVM).
2. Order the XDS110 plug-in board ([XDS110ISO-EVM](#)) and any optional adapter and base board hardware.

3. Download the latest Code Composer Studio™ [Theia](#) integrated development environment (IDE) and [MCU_SDK_F29H85x](#) software development kit.
4. Read the Quick Start Setup chapter in this user's guide to get started!

Features

- Three 120-pin controlSOM high-speed/high-density connectors
- Analog I/O, digital I/O and JTAG signals at board interface
- Power management IC for safety applications
- Free download of [Code Composer Studio Theia IDE](#)
- Free download of [MCU_SDK_F29H85x](#) for device drivers and example projects



F29H85X-SOM-EVM

1 Evaluation Module Overview

1.1 Introduction

The F29H85X-SOM-EVM evaluation module is a development platform which can be used to evaluate the performance of F29H85x and F29P58x devices in automotive and industrial applications. The EVM's system-on-module architecture includes all the power, reset, and clock logic needed to operate the F29H85x device.

This 360-pin controlSOM is intended to provide a well-filtered robust design that is capable of working in most environments. This document provides the hardware details of the F29H85X controlSOM and explains the functions, locations of jumpers, and connectors present on the board. Also included in this guide are instructions on how to start developing software applications on the controlSOM.

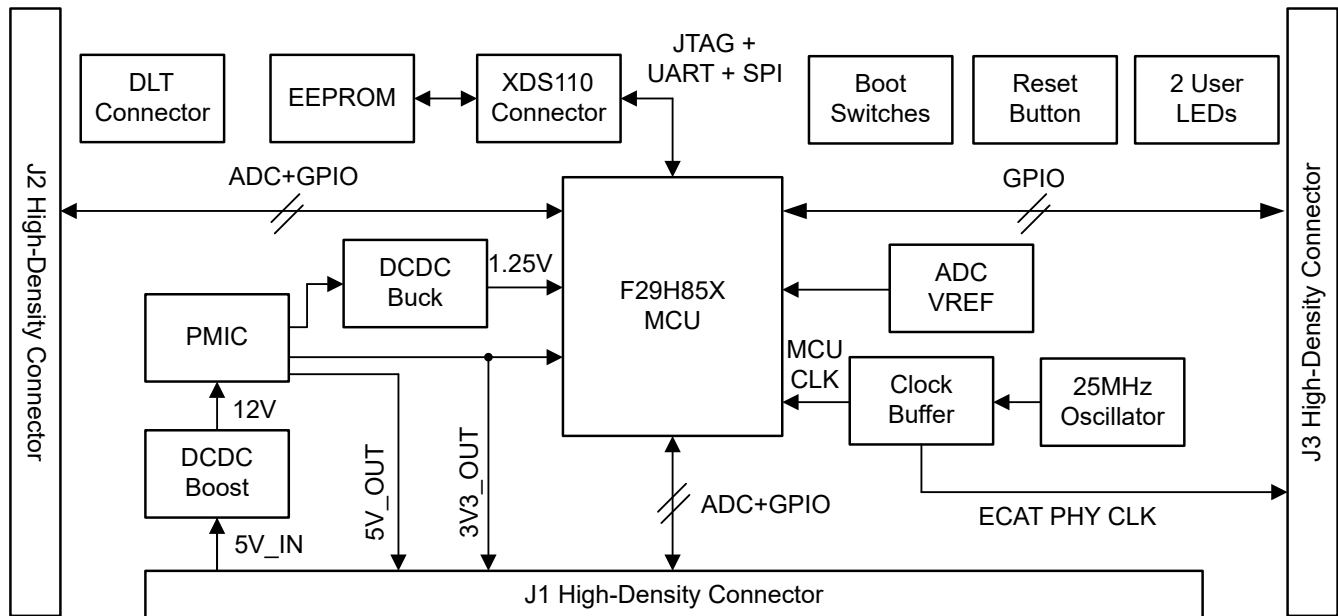


Figure 1-1. F29H85X-SOM-EVM Block Diagram

1.2 Kit Contents

The following items are included in the F29H85X-SOM-EVM kit:

- MCU144 board that includes the F29H850TU9TZEXR device
- Quick-start guide detailing the steps needed to quickly set up the EVM for use

The following items are not included in the kit:

- (Required) [XDS110ISO-EVM](#) debug probe needed to provide debug connectivity to the controlSOM
- (Optional) [HSEC180ADAPEVM](#) adapter board which is used to interface the controlSOM to any hardware designed for the C2000 controlCARD standard
- (Optional) [TMDSHSECDOCK](#) baseboard docking station which provides header-pin access to key signals on the controlSOM

1.3 Specification

The F29H85X-SOM-EVM is designed to explore the functionality of F29H85x and F29P58x microcontrollers. The controlSOM can be treated as a good reference design and is not intended to be a complete customer design. Full compliance to safety, EMI/EMC, and other regulations are left to the designer of the customer's system.

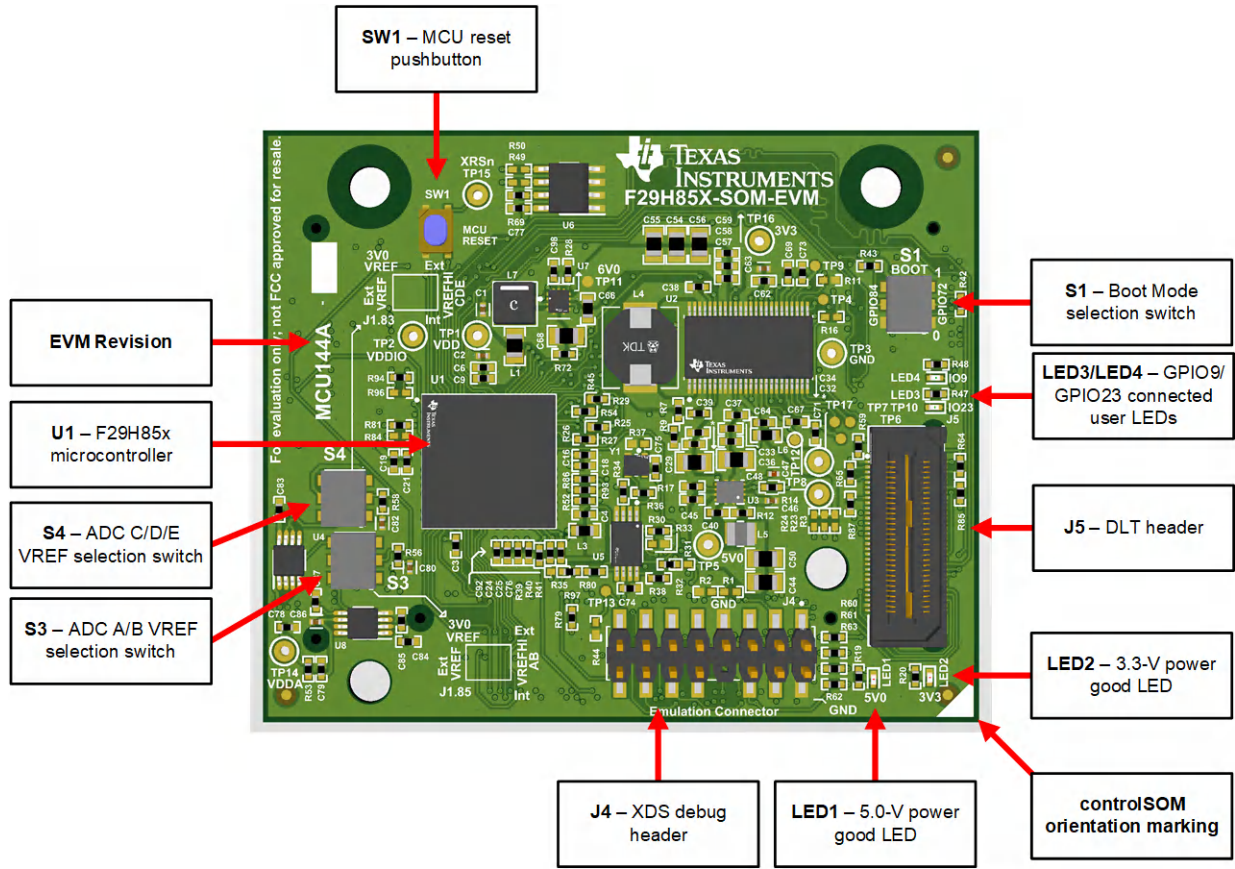


Figure 1-2. Key Components on the controlSOM - Front

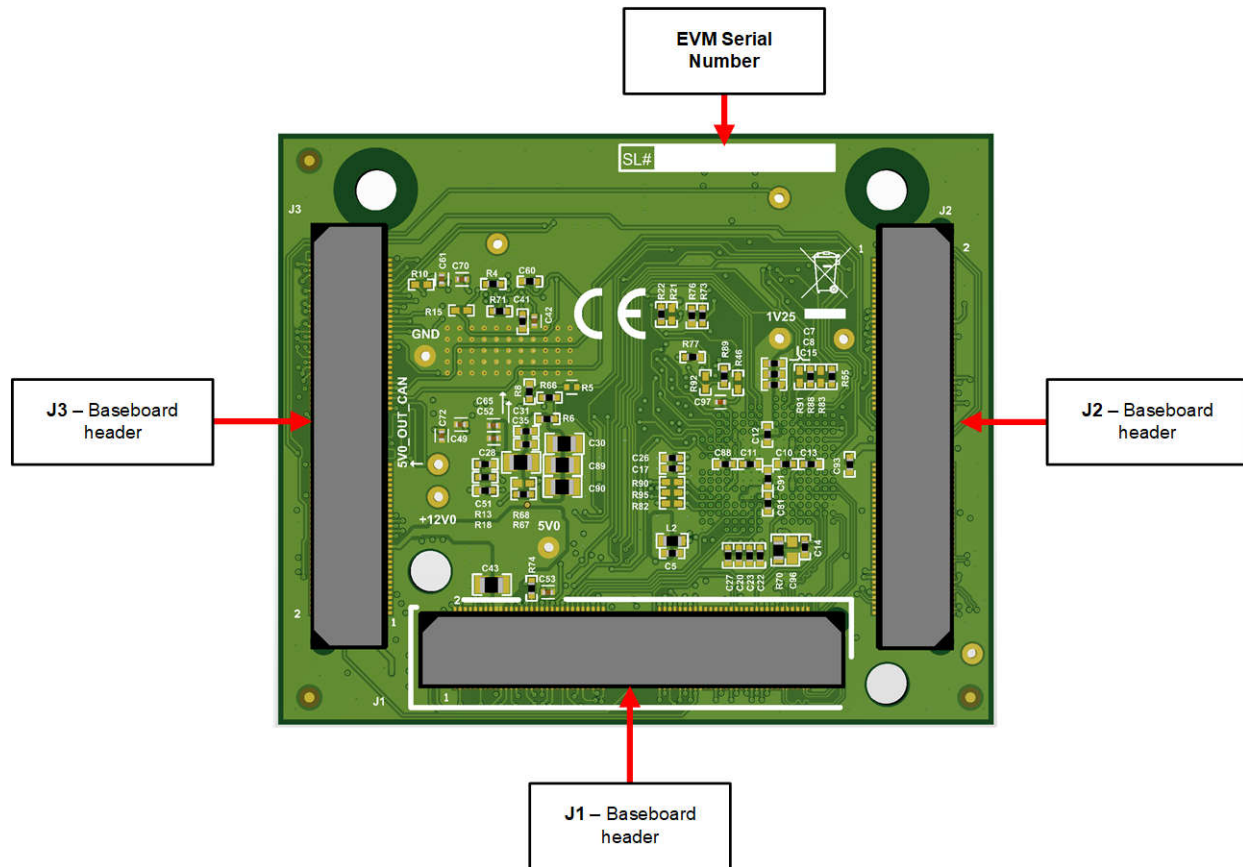


Figure 1-3. Key Components on the controlSOM - Back

1.4 Device Information

The F29H85x and F29P58x devices are members of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

These include such applications as:

- Electrical vehicles and transportation
- Motor control
 - Traction inverter motor control
 - HVAC motor control
 - Mobile robot motor control
- Solar inverters
 - Central inverter
 - Micro inverter
 - String inverter
- Digital power
- Industrial motor drives
- EV charging infrastructure

For a full list of device features, refer to the [F29H85x and F29P58x Real-Time Microcontrollers](#) data sheet and the [F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual](#).

2 Hardware

2.1 Quick Start Setup

The controlSOM supports three different configurations. Each configuration enables a different evaluation setup.

WARNING

When the controlSOM is used in a high-voltage setup, the user is responsible to confirm that the voltages and isolation requirements are identified and understood prior to energizing the board or simulation. When energized, the controlSOM or components connected to the controlSOM cannot be touched.

2.1.1 Configuration 1: Stand-alone Configuration

The stand-alone configuration can be used for most software development use cases which do not require the controlSOM to interface to other hardware. An XDS110 debug-probe ([XDS110ISO-EVM](#)) is required for this configuration. Power is provided to the controlSOM through XDS110 debug-probe. The XDS110 debug-probe is sold separately.

In this configuration, Code Composer Studio™ [Theia](#) connects to the controlSOM via JTAG and enables software development. The XDS110 debug-probe also enumerates a virtual COM port (VCP) for communication with the MCU via UART.

Follow these steps to enable this configuration:

1. Collect the required equipment:
 - a. F29H85x controlSOM ([F29H85X-SOM-EVM](#))
 - b. XDS110 isolated debug probe ([XDS110ISO-EVM](#))
 - c. USB Type-C® cable
2. Verify the switch settings are correct on each EVM.
 - a. [F29H85X-SOM-EVM](#):
 - i. Use S1 to select the desired boot mode.
 - ii. Use S3/S4 to select the desired ADC voltage reference mode.
 - b. [XDS110ISO-EVM](#): No switch configuration is necessary.
3. Connect the [XDS110ISO-EVM](#) to connector J1 of the controlSOM.
4. Connect the USB cable into connector J5 on the XDS110 isolated debug probe. The XDS110 isolated probe and the controlSOM are powered on.
5. Verify the power status LEDs (LED1 and LED2) on the controlSOM are turned on.
6. The controlSOM is ready for use. Follow the steps in [Software](#) to get started developing software.

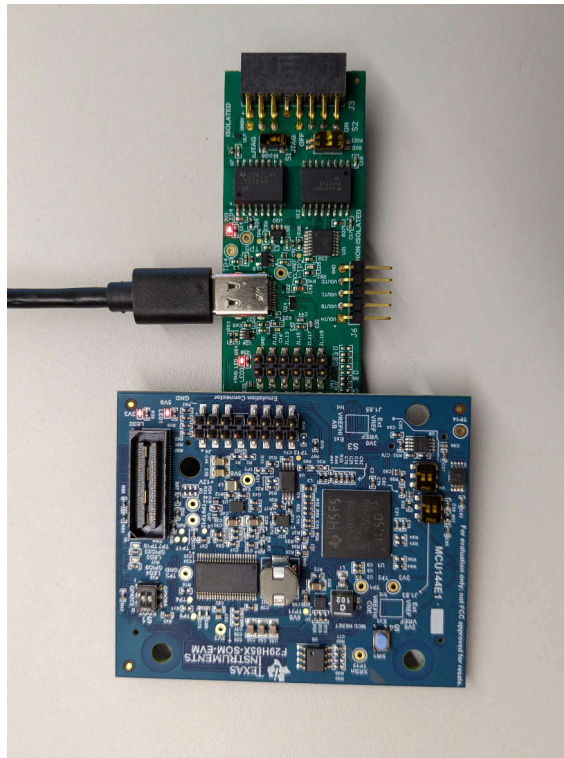


Figure 2-1. Stand-alone Configuration

In the stand-alone configuration, the 12-pin prototype header (J2) on the XDS110ISO-EVM provides access a few ADC and GPIO pins on the F29H85x device. [Table 2-1](#) lists the ADC and GPIO pins which can be accessed on this prototype header.

Table 2-1. XDS110ISO-EVM Prototype Header (J2) Pinout

MCU Signal	SOM Standard	Pin	Pin	SOM Standard	MCU Signal
GND	GND	12	11	GND	GND
GPIO5	J1.5	10	9	J1.11	GPIO2
GPIO4	J1.7	8	7	J1.13	GPIO1
GPIO3	J1.9	6	5	J1.15	GPIO0
A7/E25/GPIO225/ CMP9P/CMP2N	J1.118	4	3	J1.117	A1/C25/CMP7P/ CMP4N
A6/E24/GPIO224/ CMP2P/CMP12N	J1.120	2	1	J1.119	A0/DACOUT1/C24/ CMP4P/CMP9P

2.1.2 Configuration 2: C2000 controlCARD Backward Compatibility Configuration

The backward compatibility configuration is used for cases which require the controlSOM to interface to a C2000 controlCARD compatible baseboard or docking station. A HSEC adapter board ([HSEC180ADAPEVM](#)) is required for this configuration. Power is provided to the controlSOM through the baseboard. An emulation debug-probe such as the [XDS110ISO-EVM](#) is required to provide debug connectivity to the MCU. The HSEC adapter board and XDS110 debug-probe are sold separately.

In this configuration, Code Composer Studio™ [Theia](#) connects to the controlSOM via JTAG and enables software development. The XDS110 debug-probe also enumerates a virtual COM port (VCP) for communication with the MCU via UART.

Multiple prototype headers on the HSEC adapter board provide access to many of the MCU ADC and GPIO signals for prototyping (refer to the [HSEC adapter board user guide](#) for more details).

Follow these steps to enable this configuration:

1. The following equipment is required:
 - a. F29H85x controlSOM ([F29H85X-SOM-EVM](#))
 - b. HSEC-180 adapter board ([HSEC180ADAPEVM](#))
 - c. C2000 controlCARD compatible baseboard or HSEC-180 docking station ([TMDSHSECDOCK](#))
 - d. XDS110 isolated debug probe ([XDS110ISO-EVM](#))
 - e. 2 USB Type-C cables
 - f. (Optional) DC 5V power supply
2. Verify the switch settings are correct on each EVM.
 - a. [F29H85X-SOM-EVM](#):
 - i. Use S1 to select the desired boot mode.
 - ii. Use S3/S4 to select the desired ADC voltage reference mode.
 - b. [XDS110ISO-EVM](#):
 - i. S1 selects JTAG mode – set to JTAG mode.
 - ii. S2 enables UART/SPI connection – set to ON mode.
3. Attach the controlSOM to the HSEC-180 adapter board.
4. Ensure the controlSOM is correctly oriented. The J1 header on the controlSOM should connect with the J1 header on the HSEC-180 adapter board.
5. Insert the HSEC-180 adapter board into the baseboard or [TMDSHSECDOCK](#) docking station.
6. Connect the [XDS110ISO-EVM](#) into the connector J7 of the HSEC-180 adapter board.
7. Connect the USB cable into connector J5 on the XDS110 isolated debug probe. The XDS110 isolated probe is powered on.
8. Connect a USB cable into the connector J17 on the [TMDSHSECDOCK](#).
9. Flip S1 to the *USB-ON* position on the [TMDSHSECDOCK](#).
10. Verify the power status LEDs (LED1 and LED2) on the controlSOM are turned on.
11. The controlSOM is ready for use. Follow the steps in [Software](#) to get started developing software.

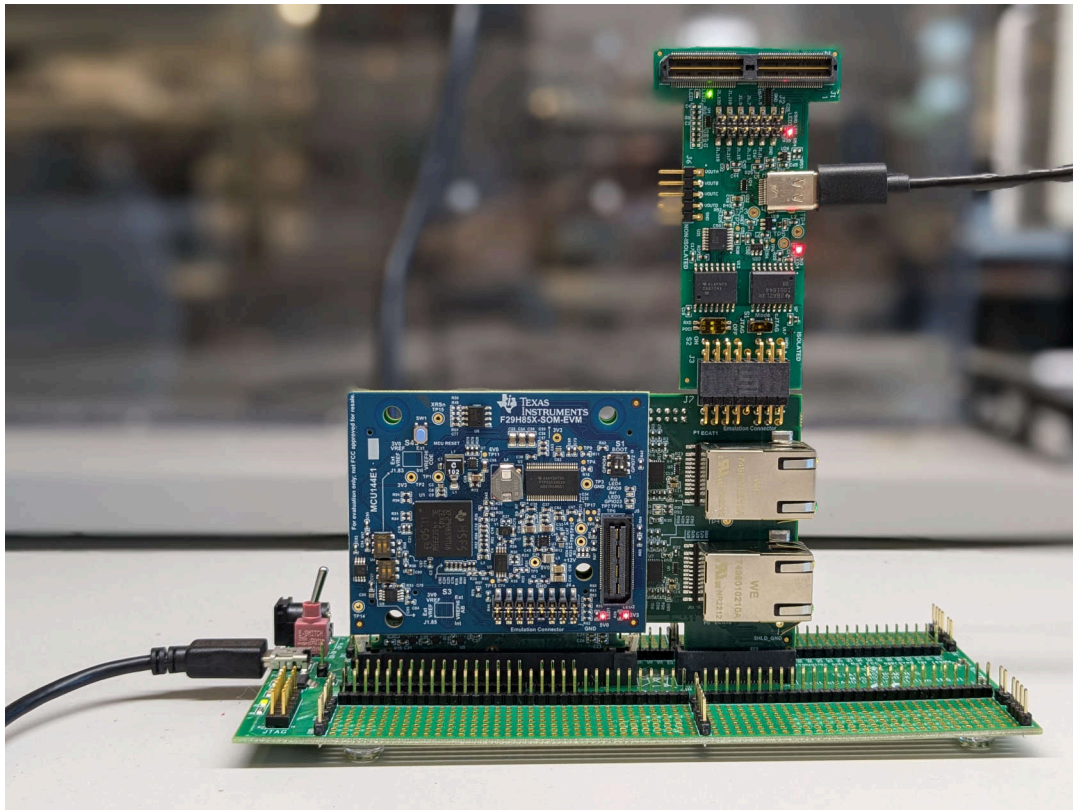


Figure 2-2. C2000 controlCARD Backward Compatibility Configuration

2.1.3 Configuration 3: Baseboard Configuration

The baseboard configuration is used for to interface the controlSOM directly to a compatible baseboard or docking station. Power is provided to the controlSOM through the baseboard. An emulation debug-probe such as the [XDS110ISO-EVM](#) is required to provide debug connectivity to the MCU. The XDS110 debug-probe and baseboard are sold separately.

In this configuration, Code Composer Studio™ [Theia](#) connects to the controlSOM via JTAG and enables software development. The XDS110 debug-probe also enumerates a virtual COM port (VCP) for communication with the MCU via UART.

Follow the steps in the baseboard user guide to enable this configuration.

1. The following equipment is required:
 - a. F29H85x controlSOM ([F29H85X-SOM-EVM](#))
 - b. C2000/Sitara controlSOM compatible base board
 - c. XDS110 isolated debug probe ([XDS110ISO-EVM](#))
 - d. 1 USB Type-C cable
2. Verify the switch settings are correct on each EVM.
 - a. [F29H85X-SOM-EVM](#):
 - i. Use S1 to select the desired boot mode.
 - ii. Use S3/S4 to select the desired ADC voltage reference mode.
 - b. [XDS110ISO-EVM](#):
 - i. S1 selects JTAG mode – set to JTAG mode.
 - ii. S2 enables UART/SPI connection – set to ON mode.
3. Set up the base board per its user guide instructions.
4. Attach the F29H85x ControlSOM to the base board.
5. Ensure the controlSOM is correctly oriented. The J1 header on the controlSOM should connect with the J1 header on the base board.
6. Connect the [XDS110ISO-EVM](#) into the XDS Debug Header (J4) of the controlSOM.

7. Connect the USB cable into connector J5 on the XDS110 isolated debug probe. The XDS110 isolated probe and the controlSOM are powered on.
8. Provide power to the base board per its user guide instructions.
9. Verify the power status LEDs (LED1 and LED2) on the controlSOM are turned on.
10. The controlSOM is ready for use. Follow the steps in [Software](#) to get started developing software.

2.2 Design Details

2.2.1 Power Tree

The controlSOM receives power from the 5V input on the high-density connectors. This 5V input is boosted to 12V, which serves as the input to the TPS65386x-Q1 PMIC. The PMIC and buck converter on the board generate all the voltage rails required on the controlSOM. All power supply sequencing and voltage monitoring is handled by the PMIC. Refer to [Section 2.3](#) for specific requirements on the 5V input to the controlSOM. [Figure 2-3](#) details the power tree of the F29H85x controlSOM.

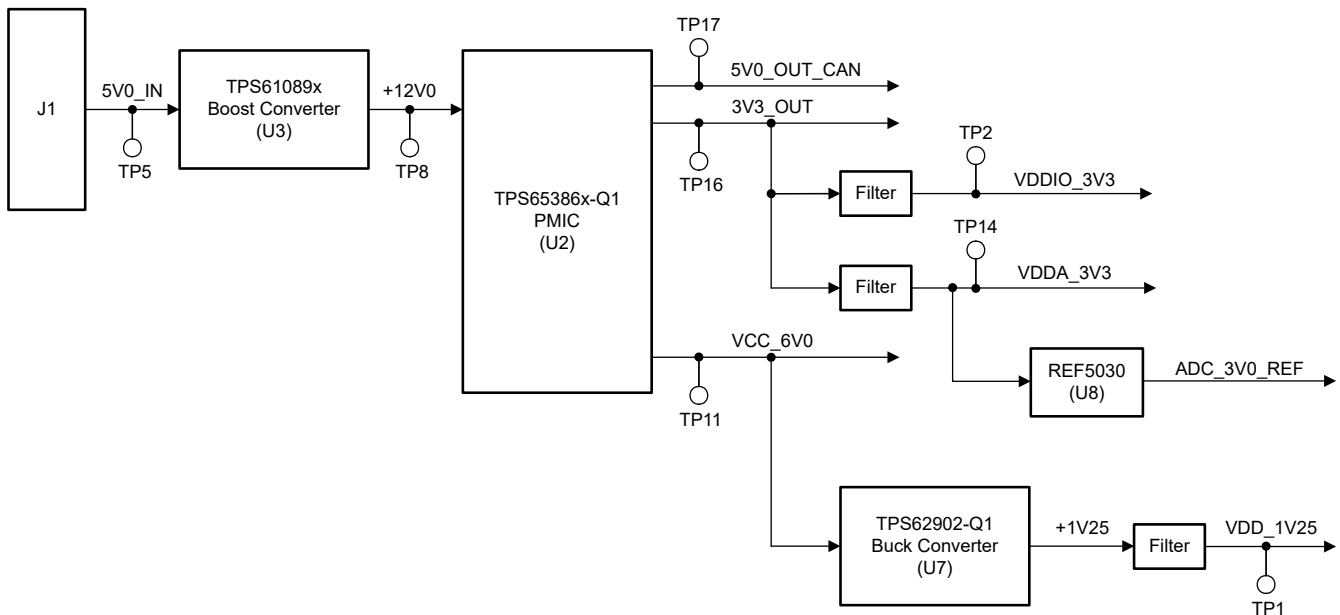


Figure 2-3. F29H85x controlSOM Power Tree

The controlSOM has two voltage rail outputs which can be used to power logic on a compatible-baseboard. These voltage rail outputs are available on the high-density connectors. [Table 2-2](#) describes each output and their maximum current rating.

Table 2-2. F29H85x controlSOM Voltage Rail Outputs

controlSOM Voltage Rail	Voltage Output (V)	Maximum Current Rating (mA)
3V3_OUT	3.3	200
5V0_OUT_CAN	5.0	200

2.2.2 Clocking

On the F29H85X-SOM-EVM, a BAW oscillator (Y1) provides a 25MHz CMOS clock that is used by the F29H85x device. This clock can also be used as a source for the ECAT_PHY0_CLK and ECAT_PHY1_CLK outputs of the controlSOM. Figure 2-4 details the clock tree of the F29H85x controlSOM.

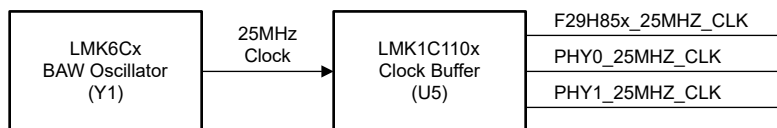


Figure 2-4. F29H85x controlSOM Clock Tree

The F29H85x device clock can be monitored through the GPIO219/XCLKOUT pin. This pin is connected to TP13 on the board. The XCLKOUT feature must be enabled through software. For more information on XCLKOUT, refer to the [F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual](#).

2.2.3 Reset

The F29H85x device reset input (XRSn) is controlled by the following sources on the controlSOM:

- **PMIC:** The PMIC will assert the XRSn pin during power up and power down. Also, when the safety features of the PMIC are enabled, the PMIC will assert the XRSn pin during a SAFE state.
- **Push button:** A push-button (SW1) on the board allows the user to manually trigger a reset on the F29H85x device.
- **Baseboard:** The XRSn pin is connected to the baseboard headers. Logic on a baseboard can be used to trigger an F29H85x device reset.
- **DLT header:** The XRSn pin is connected to the DLT header (J5). Advanced debug probes have the capability to assert the F29H85x device reset.

2.2.4 Board ID EEPROM

An I2C EEPROM is included on the controlSOM to store board identification (ID) information. The board ID is accessed by an XDS110ISO-EVM to identify the hardware during a debug session. This I2C EEPROM is not accessible by the F29H85x device.

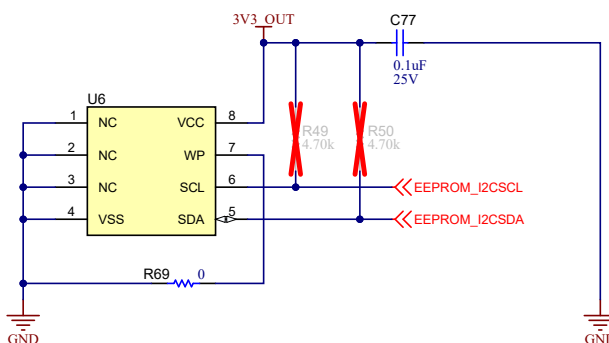


Figure 2-5. Board ID EEPROM

2.3 Power Requirements

The F29H85x controlSOM board is powered through the 5V0_IN inputs on the high-density baseboard connectors. The board supports voltage input ranges of 5V and 3A of current.

External Power Supply or Accessory Requirements

- Nominal output voltage: 5 VDC
- Maximum output current: 3A
- Efficiency level V

Note

TI recommends using an external power supply or power accessory that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, and so on.

2.4 Configuration Options

The F29H85x controlSOM can be configured through multiple switches and resistor options. The controlSOM configuration must be verified before starting software development.

2.4.1 Boot Mode Selection

Switch S1 is used to configure the device boot mode.

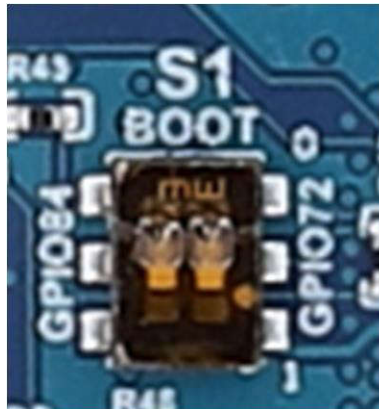


Figure 2-6. Boost Mode Selection Switch (S1)

Table 2-3. Boot Mode Selection

GPIO72	GPIO84	Boot Mode
0	0	Boot from parallel GPIO
0	1	Boot from UART / Wait Mode
1	0	Boot from CAN
1	1	Boot from Flash

2.4.2 ADC Voltage Reference Selection

Switch S3 and S4 are used to configure select the voltage reference for mode VREFHIAB and VREFHICDE, respectively.

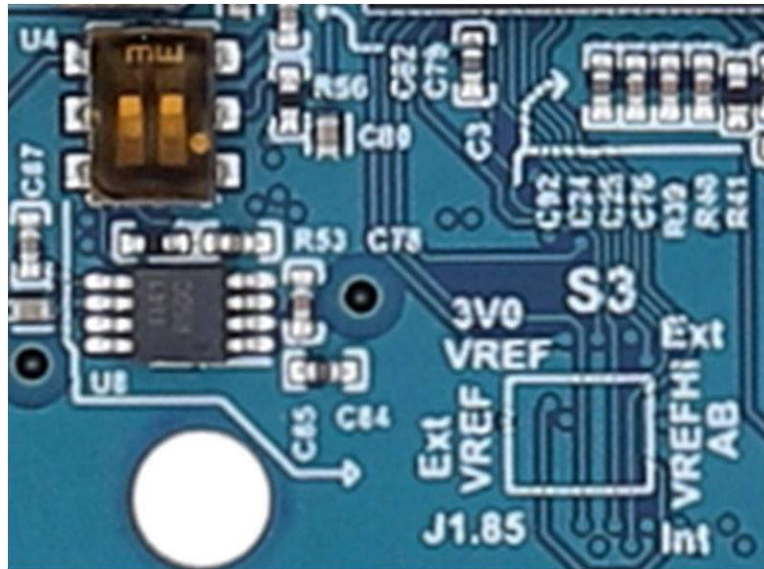


Figure 2-7. ADCA/ADCB VREF Mode Switch (S3)

Table 2-4. ADCA/ADCB VREF Mode Selection

POS1	POS2	VREFHIAB Source
DOWN	X	Internal VREF
UP	DOWN	External VREF from J1.85 pin
UP	UP	On-board 3.0V reference

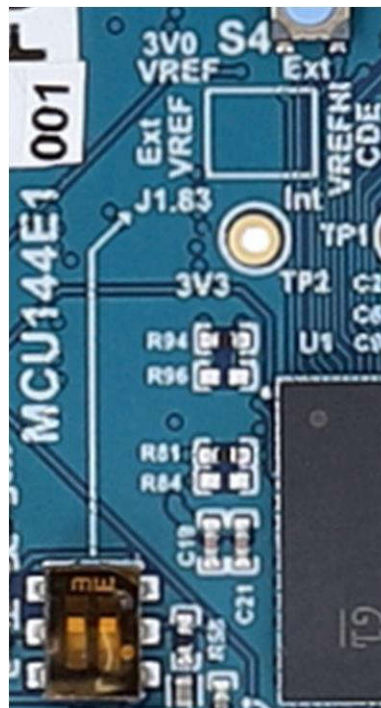


Figure 2-8. ADCC/ADCD/ADCE VREF Mode Switch (S4)

Table 2-5. ADCC/ADCD/ADCE VREF Mode Selection

POS1	POS2	VREFHICDE Source
DOWN	X	Internal VREF
UP	DOWN	External VREF from J1.83 pin
UP	UP	On-board 3.0V reference

2.4.3 MCAN-A Boot Support

An optional resistor configuration is included on the F29H85x controlSOM to enable use of MCAN-A function the high-density connector J1. By default, J1.35/37 pins support the MCAN-D pin multiplex option. Through a resistor modification, the MCAN-A function can be brought on these J1 pins. This enables use of the MCAN-A boot feature. Refer to the [F29H85x and F29P58x Real-Time Microcontrollers](#) data sheet for more information on MCAN-A boot.

When the MCAN-A function is enabled on J1 through resistor modification, EtherCAT functionality is not supported.

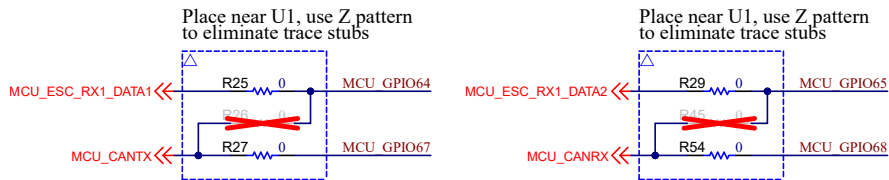


Figure 2-9. MCAN-A Boot Selection Resistors

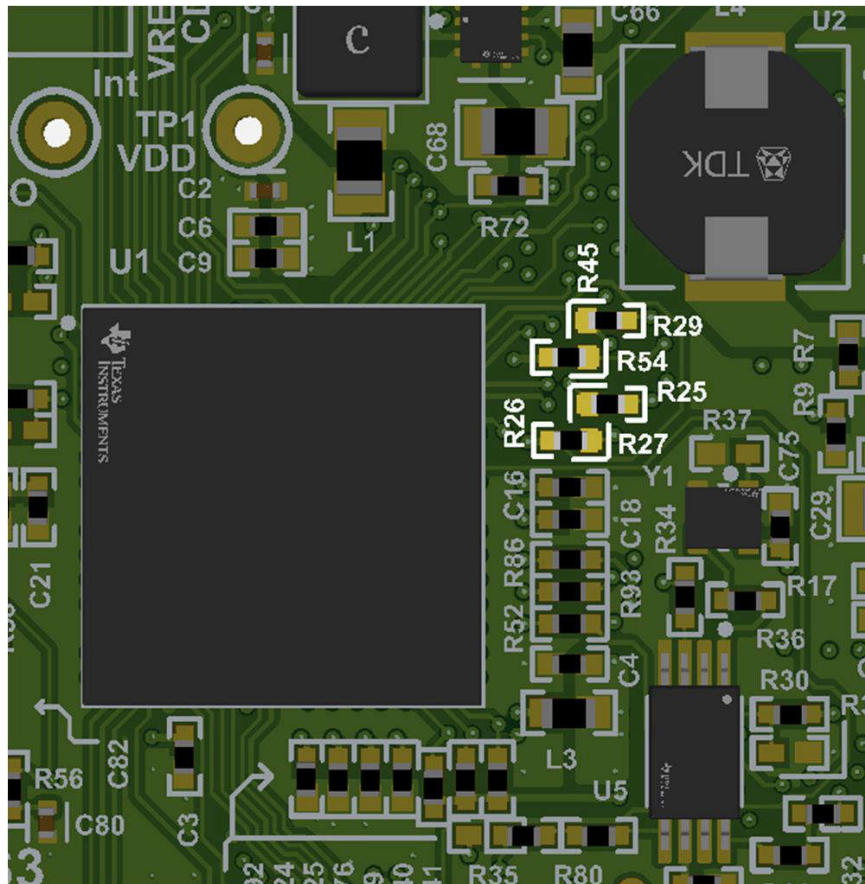


Figure 2-10. MCAN-A Boot Selection Resistor Locations

Table 2-6. EtherCAT/MCAN-A Boot Function Support

Mode	J1.35/37	J3.80/82	Resistor Configuration
EtherCAT support (default)	GPIO67/68 (MCAN-D)	GPIO64/65 (EtherCAT)	Populate R25/R27 and R29/R54 with 0-ohm resistor, remove R26/R45.
MCAN-A support	GPIO64/65 (MCAN-A)	No connection. EtherCAT not supported	Populate R26/R45 with 0-ohm resistor, remove R25/R27 and R29/R54.

2.4.4 FSI DLT Support

An optional resistor configuration is included on the F29H85x controlSOM to enable use of multiple FSI pins for data logging through the data, logging, and trace (DLT) header (J5). Table 2-7 lists all the FSI pins which can be connected to the DLT header. By default, these FSI pins are connected to the J1/J3 high-density connectors for baseboard use; they are not connected to the DLT header. To connect these FSI pins to the DLT header, follow the instructions on Table 2-8.

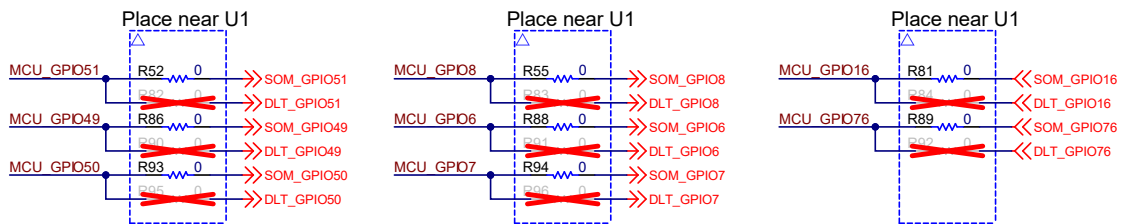


Figure 2-11. FSI DLT Selection Resistors

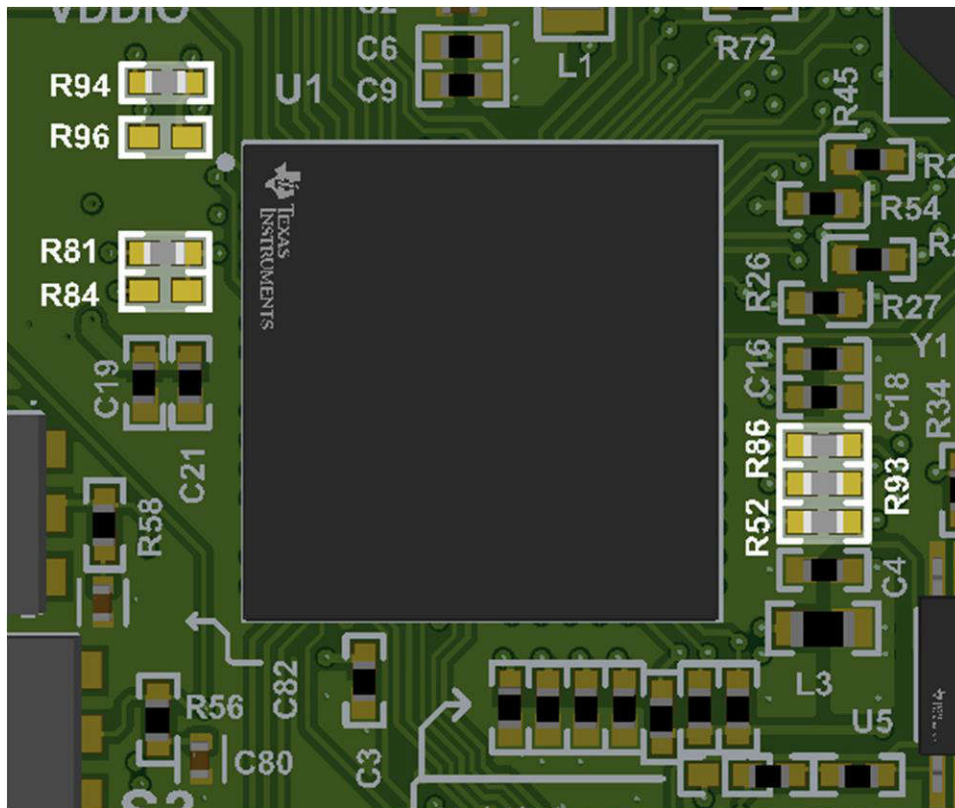


Figure 2-12. FSI DLT Selection Resistor Locations (Top)

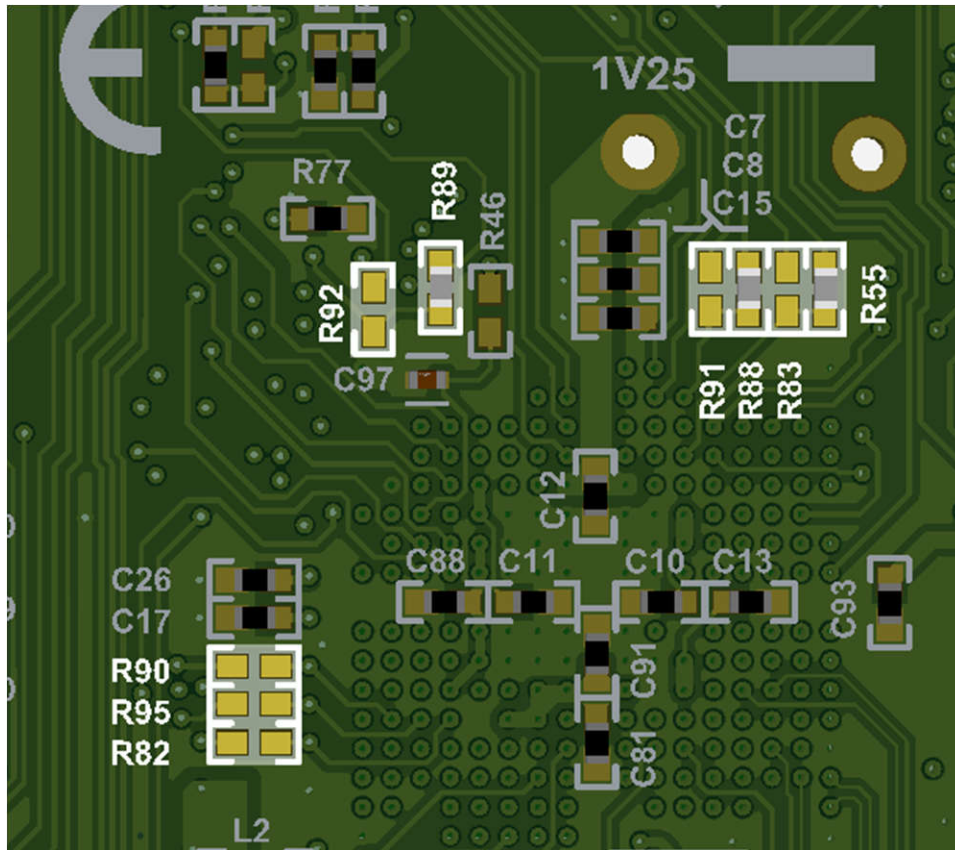


Figure 2-13. FSI DLT Selection Resistor Locations (Bottom)

Table 2-7. FSI Pins Used for DLT Support

GPIO	Function
GPIO51	FSITXA_CLK
GPIO49	FSITXA_D0
GPIO50	FSITXA_D1
GPIO8	FSITXB_CLK
GPIO6	FSITXB_D0
GPIO7	FSITXB_D1
GPIO16	FSIRXC_CLK
GPIO76	FSIRXC_D0

Table 2-8. FSI GPIO Baseboard/DLT Header Connection

Mode	Resistor Configuration
FSI pins connected to J1/J3 Baseboard Headers (default)	Populate all 0-ohm resistors on R52, R86, R93, R55, R88, R94, R81, and R89. Remove all resistors on R82, R90, R95, R83, R91, R96, R84, and R92.
FSI GPIOs connected to DLT Header	Remove all resistors on R52, R86, R93, R55, R88, R94, R81, and R89. Populate all 0-ohm resistors on R82, R90, R95, R83, R91, R96, R84, and R92.

2.4.5 EtherCAT PHY Clock Selection

The controlSOM provides two EtherCAT PHY clock outputs, ECAT_PHY0_CLK and ECAT_PHY1_CLK. By default, these clocks are sourced from a 25MHz BAW oscillator (Y1). These clocks can also be sourced from the ESC_PHY_CLK on the F29H85x device. An optional resistor configuration is included source for the EtherCAT PHY clocks from the GPIO54/ESC_PHY_CLK output on the F29H85x device. To enable this option, follow the instructions on [Table 2-9](#). Refer to the [F29H85x and F29P58x Real-Time Microcontrollers](#) data sheet for more information on ESC_PHY_CLK.

Table 2-9. EtherCAT PHY Clock Source Selection

Mode	Resistor Configuration
On-board LVC MOS 25MHz oscillator (Y1) (default)	Populate all 0-ohm resistors on R32 and R97. Remove all resistors on R31 and R35.
Device ESC_PHY_CLK (GPIO54)	Remove all resistors on R32 and R97. Populate all 0-ohm resistors on R31 and R35.

2.5 Header Information

The F29H85X-SOM-EVM can be interfaced to a compatible baseboard through three 120-pin high-density connectors. These connectors provide access to a number pins on the F29H85x device and other signals. For a complete pinout of these connectors, refer to the [F29H85X-SOM-EVM design files](#).

2.5.1 Baseboard Headers (J1, J2, J3)

The F29H85x-SOM-EVM conforms to the C2000/Sitara MCU controlSOM standard. Three baseboard headers, J1, J2, and J3, are supported for interfacing to compatible baseboards. Refer to the [F29H85X-SOM-EVM design files](#) for a complete pinout of these headers.

J1, J2, J3 header information:

- Part number: QSH-060-01-L-D-A
- Manufacturer: Samtec
- Maximum insertion cycles: 500

2.5.2 XDS Debug Header (J4)

The XDS debug header (J4) provides debug access to the F29H85X-SOM-EVM. This header is used when the controlSOM is used in [Section 2.1.1](#). The XDS debug header is compatible with the [XDS110ISO-EVM](#). [Table 2-10](#) provides a pinout of the J4 header.

CAUTION

The XDS debug header (J4) is only compatible with the [XDS110ISO-EVM](#). Do not plug in any other debug probe directly into this header. See [Section 2.8](#) for information on using other debug probes with the controlSOM.

Table 2-10. XDS Debug Header (J4) Pinout

EVM Connection	Function	Pin	Pin	Function	EVM Connection
VSYS_3V3_LDO1	IO_TGT_V	1	2	GND	GND
TMS	MCU_TMS	3	4	MCU_TCK	TCK
TDI	MCU_TDI	5	6	MCU_TDO	TDO
GND	GND	7	8	KEY	NC
UART0_RXD	MCU_SCI_RX	9	10	MCU_SCI_TX	UART0_TXD
I2C0_SDA	EE_I2CSDA	11	12	EE_I2CSCL	I2C0_SCL
SPI3_CLK	DAC_SPI_SCLK	13	14	DAC_SPI_PICO	SPI3_D0

Table 2-10. XDS Debug Header (J4) Pinout (continued)

EVM Connection	Function	Pin	Pin	Function	EVM Connection
SPI3_D1	DAC_SPI_POCI	15	16	DAC_SPI_PTE	SPI3_CS0

2.5.3 DLT Header (J5)

The debugging, log, and trace header (J5) provides *alternate* debug access to the F29H85X-SOM-EVM. A debugging tool compatible with the MIPI-60 emulation and trace header standard is required to use this feature. [Table 2-11](#) provides a pinout of the J5 header.

J5 header information:

- Part number: QSH-030-01-L-D-A
- Manufacturer: Samtec
- Maximum insertion cycles: 500

A resistor modification is required to enable FSI pin connection to the DLT header. See [Section 2.4.4](#) for more information.

Table 2-11. DLT Header (J5) Pinout

EVM Connection	Function	Pin	Pin	Function	EVM Connection
3V3_OUT via 100-ohm resistor	VREF_DEBUG	1	31	TRC_DATA[0][7]	
TMS	TMS/TMSC	2	32	TRC_DATA[0][27] or TRC_DATA[1][7]	
TCK	TCK	3	33	TRC_DATA[0][8]	
GPIO223	TDO/EXTA	4	34	TRC_DATA[0][28] or TRC_DATA[1][8]	
GPIO222	TDI/EXTB	5	35	TRC_DATA[0][9]	
XRSn	nRESET	6	36	TRC_DATA[0][29] or TRC_DATA[1][9]	
TCK	RTCK/EXTC	7	37	TRC_DATA[0][10] or TRC_DATA[3][0]	
	nTRST_PD	8	38	TRC_DATA[0][30] or TRC_DATA[1][10] or TRC_DATA[2][0]	GPIO16 (FSIRX_CLK)
	nTRST/EXTD	9	39	TRC_DATA[0][11] or TRC_DATA[3][1]	
	EXTE/TRIGIN	10	40	TRC_DATA[0][31] or TRC_DATA[1][11] or TRC_DATA[2][1]	GPIO76 (FSIRX_D0)
	EXTF/TRIGOUT	11	41	TRC_DATA[0][12] or TRC_DATA[3][2]	
3V3_OUT via 100-ohm resistor	VREF_TRACE	12	42	TRC_DATA[0][32] or TRC_DATA[1][12] or TRC_DATA[2][2]	GPIO8 (FSITX0_CLK)
	TRC_CLK[0]	13	43	TRC_DATA[0][13] or TRC_DATA[3][3]	
	TRC_CLK[1]	14	44	TRC_DATA[0][33] or TRC_DATA[1][13] or TRC_DATA[2][3]	GPIO6 (FSITX0_D0)

Table 2-11. DLT Header (J5) Pinout (continued)

EVM Connection	Function	Pin	Pin	Function	EVM Connection
GND via 0- ohm resistor	Target Presence Detect	15	45	TRC_DATA[0][14] or TRC_DATA[3][4]	
GND	GND	16	46	TRC_DATA[0][34] or TRC_DATA[1][14] or TRC_DATA[2][4]	GPIO7 (FSITX0_D1)
	TRC_DATA[0][0]	17	47	TRC_DATA[0][15] or TRC_DATA[3][5]	
	TRC_DATA[1][0] or TRC_DATA[0][20]	18	48	TRC_DATA[0][35] or TRC_DATA[1][15] or TRC_DATA[2][5]	
	TRC_DATA[0][1]	19	49	TRC_DATA[0][16] or TRC_DATA[3][6]	
	TRC_DATA[1][1] or TRC_DATA[0][21]	20	50	TRC_DATA[0][36] or TRC_DATA[1][16] or TRC_DATA[2][6]	
	TRC_DATA[0][2]	21	51	TRC_DATA[0][17] or TRC_DATA[3][7]	
	TRC_DATA[1][2] or TRC_DATA[0][22]	22	52	TRC_DATA[0][37] or TRC_DATA[1][17] or TRC_DATA[2][7]	GPIO51 (FSITX1_CLK)
	TRC_DATA[0][3]	23	53	TRC_DATA[0][18] or TRC_DATA[3][8]	
	TRC_DATA[1][3] or TRC_DATA[0][23]	24	54	TRC_DATA[0][38] or TRC_DATA[1][18] or TRC_DATA[2][8]	GPIO49 (FSITX1_D0)
	TRC_DATA[0][4]	25	55	TRC_DATA[0][19] or TRC_DATA[3][9]	
	TRC_DATA[1][4] or TRC_DATA[0][24]	26	56	TRC_DATA[0][39] or TRC_DATA[1][19] or TRC_DATA[2][9]	GPIO50 (FSITX1_D1)
	TRC_DATA[0][5]	27	57	GND	GND
	TRC_DATA[1][5] or TRC_DATA[0][25]	28	58	GND	GND
	TRC_DATA[0][6]	29	59	TRC_CLK[3]	
	TRC_DATA[1][6] or TRC_DATA[0][26]	30	60	TRC_CLK[2]	

2.6 Push Buttons

The F29H85x controlSOM includes the push button shown on [Table 2-12](#).

Table 2-12. Push Button Description

Push Button	Function
SW1	MCU reset (XRSn)

2.7 User LEDs

The two Green LEDs are available on the controlSOM for software use. These LEDs are connected to GPIOs on the F29H85x device. Setting the GPIO low will turn on the LED, and setting the pin high will turn off the LED.

LED	GPIO
LED3	GPIO23
LED4	GPIO9

2.8 Debug Information

This section describes frequently asked questions about the F29H85X-SOM-EVM.

- Can other programming and debug tools (such as an XDS200 debug probe) be used with the controlSOM?
 - Yes, when the controlSOM is paired with the [HSEC180ADAPEVM](#) adapter board and the [TMDSHSECDOCK](#) baseboard docking station, a debug probe such as the XDS200 can be used. Also, an XDS560v2 debug probe with a MIPI-60 connector can connect directly to the DLT header (J5) on the controlSOM.
- Why can't I connect to the controlSOM in Code Composer Studio?
 - Ensure there is power on the controlSOM by verifying that LED1 (5.0V input) and LED2 (3.3V output) are on.
 - Check that power is being delivered to the F29H85x device by probing TP1 (VDD, 1.25V), TP2 (VDDIO, 3.3V), and TP14 (VDDA, 3.3V).
 - Check that the F29H85x device is out of reset by probing TP15. This test point should read close to 3.3V when the device is out of reset.
 - If using [Section 2.1.2](#) or [Section 2.1.3](#), check that the [XDS110ISO-EVM](#) is configured for full JTAG mode. Switch S1 on the [XDS110ISO-EVM](#) should be set to the JTAG setting.
 - Ensure that the target configuration is set up to use full JTAG mode. Open the Target Configuration file (.ccxml) in Code Composer Studio. Click on the Advanced tab and select "JTAG (1149.1), SWD and cJTAG are disabled" from the "JTAG/SWD/cJTAG Mode" drop-down. Alternatively, a working target configuration file is included in all the F29 SDK examples. This file can be used without modifications.

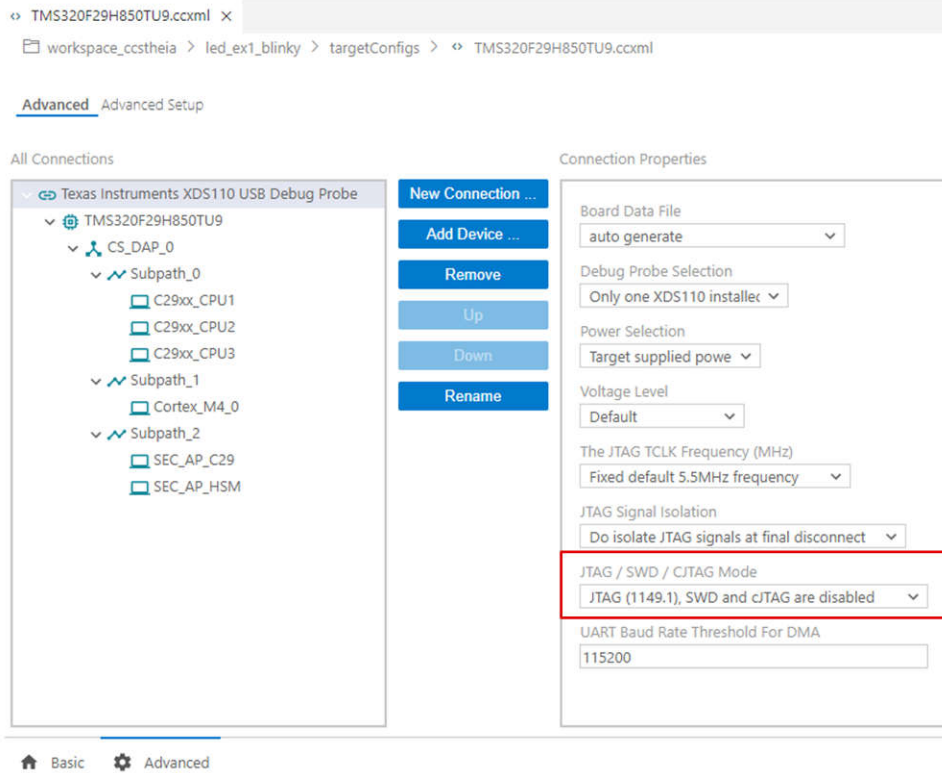


Figure 2-14. Target Configuration Advanced Options

2.9 Test Points

The F29H85x controlSOM includes multiple test points to aid in hardware debug. [Table 2-13](#) includes a list of the test points available on the controlSOM.

Table 2-13. Test Point Description

Test Point	Test Point Name	Description
TP1	VDD_1V25	Filtered MCU VDD supply
TP2	VDDIO_3V3	Filtered MCU VDDIO supply
TP3	GND	Ground reference
TP4	COMP2_OUT	PMIC comparator output (COMP2_OUT)
TP5	5V0_IN	Board 5V input
TP6	CFG_VOUT1	PMIC configurable LDO output (PLDO1_OUT)
TP7	PMIC_GPIO_1	PMIC GPIO1 pin
TP8	+12V0	Board 12V supply
TP9	CFG_VOUT2	PMIC configurable LDO output (LDO2_OUT)
TP10	COMP1_OUT	PMIC comparator output (COMP1_OUT)
TP11	VCC_6V0	PMIC 6V output (BB_OUT)
TP12	CFG_VOUT3	PMIC configurable LDO output (LDO3_OUT)
TP13	MCU_ERRORSTS	MCU GPIO19/ERRORSTS output
TP14	VDDA_3V3	Filtered MCU VDDA supply
TP15	MCU_XRSn	MCU reset (XRSn) pin
TP16	3V3_OUT	PMIC 3.3V output (LDO1_OUT)

Table 2-13. Test Point Description (continued)

Test Point	Test Point Name	Description
TP17	5V0_OUT_CAN	Filtered 5V output for CAN transceivers

2.10 Best Practices

Electrostatic Discharge (ESD) Compliance

Components installed on the product are sensitive to electrostatic discharge (ESD). TI recommends this product be used in ESD controlled environment. This includes a temperature or humidity controlled environment to limit the buildup of ESD. TI recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

Assumed Operating Conditions

This kit is assumed to run at standard room conditions. Standard ambient temperature and pressure (SATP) with moderate-to-low humidity is assumed.

3 Software

3.1 Software Description

The F29H85x software development kit ([MCU_SDK_F29H85x](#)) is a cohesive set of development tools for F29H85x real-time controllers. The SDK includes device-specific drivers, bit-field header files for device registers, and peripheral examples. Also included in the SDK are math, DSP, and control libraries.

3.2 Software Installation

Follow these steps to install the F29H85x SDK:

1. Download the latest version of [MCU_SDK_F29H85x](#)
2. Start the installer and follow the prompts to complete the installation
 - a. It is recommended to install the SDK in the 'C:\ti' folder
3. Review the release notes and other documentation included with the SDK

3.3 Software Development

[Code Composer Studio \(CCS\) Theia](#) is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. [CCS Theia](#) is used to develop and debug embedded applications on the F29H85x controlSOM.

Follow these steps to install TI's [CCS Theia](#):

1. Download the latest version of [CCS Theia](#)
2. Start the installer and follow the prompts to complete the installation
 - a. It is recommended to install [CCS Theia](#) in the 'C:\ti' folder
3. Review the release notes and other documentation included with [CCS Theia](#)

3.4 Developing an Application

A sample application can be built, loaded, and ran on the EVM once the [MCU_SDK_F29H85x](#) and [CCS Theia](#) have been installed.

Follow these steps to load a simple LED blinking example on the F29H85x controlSOM:

1. Set the controlSOM in flash boot mode
 - a. Set switch S1 (GPIO84) to 1
 - b. Set switch S1 (GPIO72) to 1
2. Set up the controlSOM and XDS110ISO-EVM in Stand-alone configuration (see [Section 2.1.1](#))
3. Power on the EVMs
4. Launch [CCS Theia](#)
5. Go to "File -> Import Project(s)"
6. Click "Browse.." and navigate to the path below, then click "Select Folder":
 - a. C:\ti\mcu_sdk_f29h85x_X_XX_XX_XX_\examples\driverlib\single_core\led\led_ex1_blinky
7. Select the "led_ex1_blinky" project from the "Discovered Projects" list and click "Finish" to import the project into the workspace
8. Right-click on the project name and select "Build Configurations -> CPU1_FLASH"

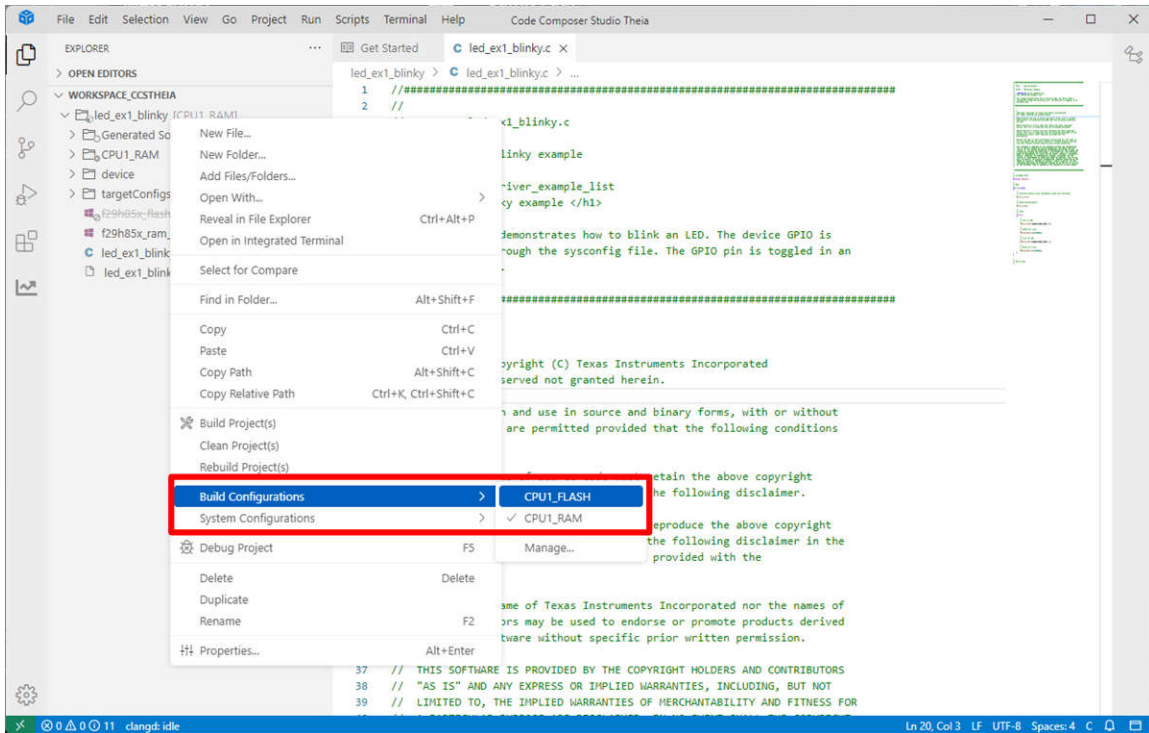


Figure 3-1. Build Configuration Selection

- Right-click on the project name and select "Debug Project (F5)". This builds the project, executes the "post build sequence for FLASH configuration", and launches the target configuration.

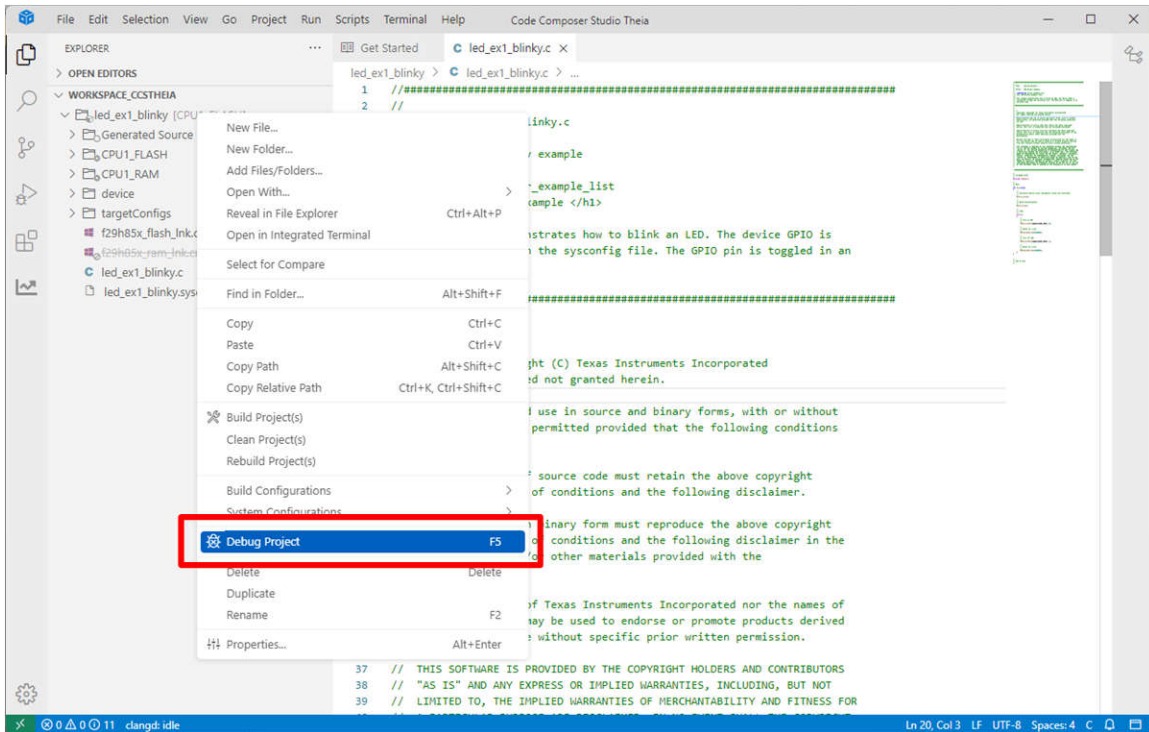


Figure 3-2. Debug Project Selection

- Select "Texas Instruments XDS110 USB Debug Probe_0/C29xx_CPU1" as the core
- Navigate to Debug (left side of screen) and select the blue play button to run the example

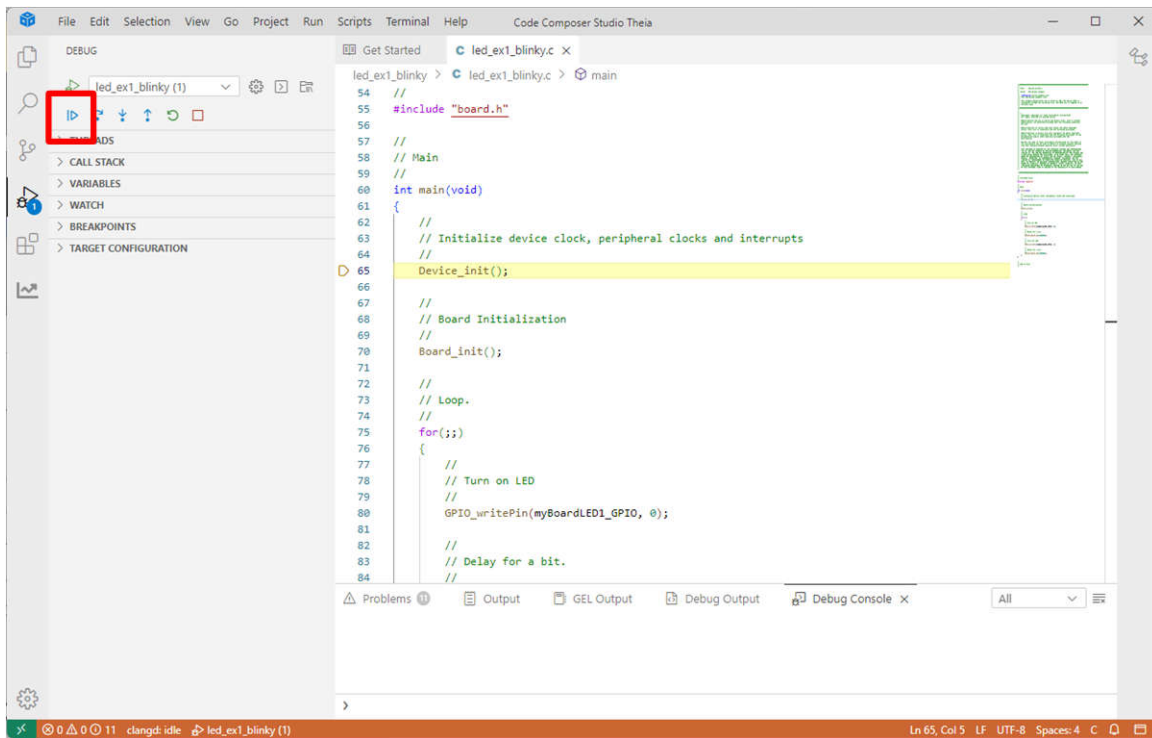


Figure 3-3. Run Selection

12. Observe the LED blinking on the controlSOM

4 Hardware Design Files

4.1 Schematics

The board schematic can be found in the [F29H85X-SOM-EVM design files](#).

4.2 PCB Layouts

The board layout source files are included in the [F29H85X-SOM-EVM design files](#).

4.3 Bill of Materials (BOM)

The BOM is included in the [F29H85X-SOM-EVM design files](#).

5 Additional Information

5.1 Known Hardware or Software Issues

This section describes the known exceptions to the EVM functional specification (advisories). This section also contains EVM usage notes. Usage notes describe situations where the EVM's behavior may not match the presumed or documented behavior.

5.1.1 EVM Usage Notes

Parallel I/O Boot Can Cause Watchdog Timer Timeout if No Host Is Connected to EVM

Revisions Affected: All

Use of parallel I/O boot can lead to a watchdog timer timeout if a host does not drive the host control lines. The timeout will cause the F29H85x device to reset.

The boot mode switch (S1) on the EVM should not be set to parallel I/O boot unless a host is present to drive the host control lines.

Refer to the [F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual](#) for more information on parallel boot.

Device GPIOs Dedicated to PMIC SPI Bus Should Be Used for SPI Function If Used On Baseboard

Revisions Affected: All

The F29H85x device and the PMIC on the controlSOM are connected via SPI bus. The SPI bus is used by the device to configure the PMIC and also, when enabled, to service the PMIC's watchdog. The SPI bus GPIOs are also connected to the SPI standard location on J1, see [Table 5-1](#) for more information. Note that the SPI_STE pin is not connected to any of the baseboard headers.

Care must be taken when using these GPIOs on a baseboard since these GPIOs will toggle when the F29H85x device communicates with the PMIC via SPI. It is recommended to always use these pins for SPI function on a baseboard.

Table 5-1. PMIC SPI Bus GPIOs

SPI Pin	GPIO	J1 Connection
PICO	GPIO91	J1.75
POCI	GPIO92	J1.77
CLK	GPIO93	J1.79
PTE	GPIO94	Not connected to J1

Limited Functionality On Early EVM Revisions

Revisions Affected: MCU144E1-001

Initial builds of the F29H85X-SOM-EVM are assembled with early samples of the F29H85x microcontroller (MCU). These MCU samples have the following limitations:

- Flash is not supported: early F29H85x devices do not support internal flash. All microcontroller code must be loaded to and executed from internal RAM.
- Incorrect package marking: early F29H85x devices have an incorrect package label. The correct package label is F29H850TU9.
- Internal oscillator (INTOSC2) defaults to 6MHz: in early F29H85x devices INTOSC2 is untrimmed and defaults to 6MHz.

F29H85X-SOM-EVMs built with these early F29H85x MCU samples are labeled as *MCU144E1-001*.

5.1.2 EVM Advisories

MCU fault state possible when on-board 25MHz clock is enabled

Revisions Affected: MCU144E1 (all assemblies), MCU144A-001

The on-board 25MHz clock can be used to clock the F29H85x MCU. However, when this clock is used, clock glitches can be induced in the device which can lead to a fault state. See the [F29H85x and F29P58x Real-Time MCUs Silicon Errata](#) for more information.

To work around this issue, the on-board 25MHz clock must be disabled by removing R30 and populating R33 with a 10k Ω resistor. Furthermore, the internal oscillators (INTOSC1 or INTOSC2) of the MCU must be used as the main clock source.

The INTOSC frequency accuracy must be carefully considered for certain peripherals and applications.

The workaround for this issue has been implemented on all *MCU144E1-003* and *MCU144A-001* assemblies.

MCU Reset can cause PMIC to shut down MCU power supplies

Revisions Affected: MCU144A-001

The PMIC continually monitors the MCU reset signal (XRSN) through its NRST pin. The PMIC NRST read-back circuit compares the external logic level on the NRST pin with the internally applied NRST logic level. If this read-back circuit detects a difference between these two logic levels, the device sets the NRST read-back error. An NRST read-back error can cause the PMIC to enter a safe state during which the MCU supplies are turned off.

A reset initiated through the on-board reset switch (SW1) or a software reset initiated by the MCU can inadvertently trigger a PMIC NRST read-back error and cause the MCU supplies to shut down. The PMIC's NRST read-back feature has been effectively disabled on *MCU144A-001* assemblies by disconnecting the NRST pin from the MCU XRSN pin.

ADC VREFHIAB and VREFHICDE incorrectly shorted together when S3 and S4 are both set to internal VREF mode

Revisions Affected: MCU144E1 (all assemblies)

Switch S3 and S4 are used to specify the VREF mode for the VREFHIAB and VREFHICDE pins of the F29H85x microcontroller.

The VREFHIAB and VREFHICDE pins are incorrectly shorted together when internal VREF mode is selected on both S3 and S4. Refer to [Section 2.4.2](#) for more information on S3 and S4.

A hardware modification is required to workaround this issue:

- Set S3/S4 for external mode
- Remove R53/C79
- Remove R57/C95

With this change, the board will not drive any voltage on VREFHI pins. The ADCs can be used in internal VREF mode.

Incorrect voltage on VREFHIAB and VREFHICDE pins when external VREF mode is selected

Revisions Affected: MCU144E1 (all assemblies)

Switch S3 and S4 are used to select the VREF mode for the VREFHIAB and VREFHICDE pins of the F29H85x microcontroller.

An incorrect voltage on the VREFHIAB and VREFHICDE will be observed when external VREF mode is selected.

A hardware modification is required to work around this issue:

- Replace R53 and R57 on the on the board with 0 Ω resistors.
- Remove C78, C79, C94, and C95

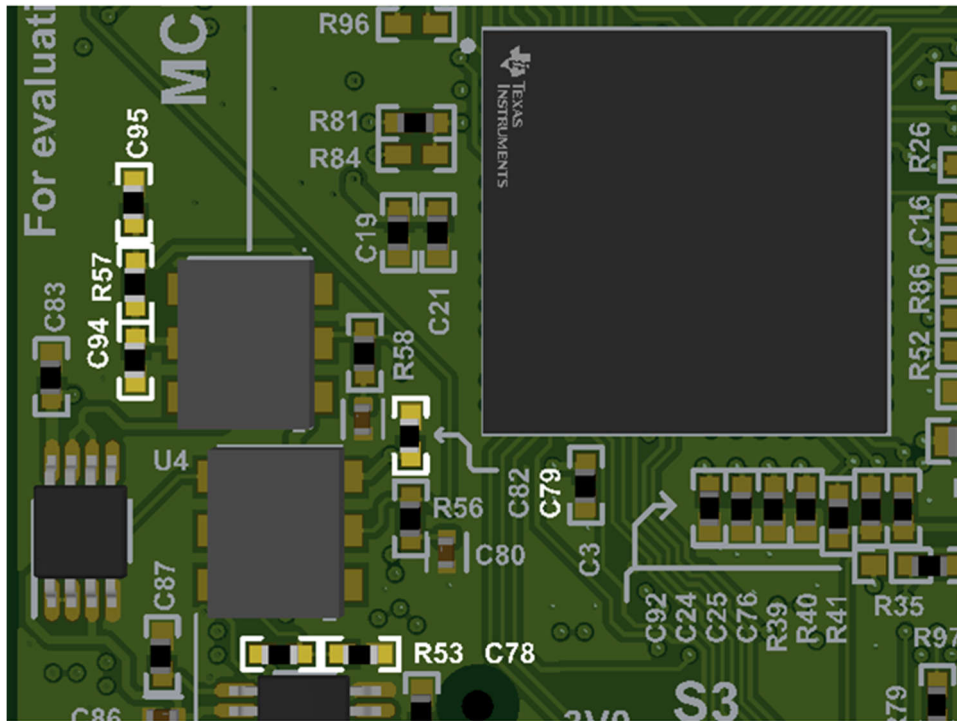


Figure 5-1. Component Location For ADC VREF Modification

Refer to [Section 2.4.2](#) for more information on S3 and S4.

Incorrect power-up sequence for VDD and VDDIO/VDDA MCU rails

Revisions Affected: MCU144E1-001

The *F29H85x and F29P58x Real-Time Microcontrollers* data sheet specifies that the VDD rail should be powered-on after the VDDIO/VDDA rails have powered-on.

The power-management IC (PMIC) is programmed to bring up the VDD and VDDIO/VDD rails together. This incorrect power supply sequence can cause the MCU XRSn pin to remain asserted on some EVMs after power-on. On these boards, Code Composer Studio cannot connect to the MCU.

The hardware modification shown below is required to work around this issue.

- Remove R22, R75, R78
- Add R1 and R2 as shown
 - R1 = 10.7K (1%) R2 = 5760 (1%)
- Add blue wire between R1, R2, and U7.5 as shown in [Figure 5-2](#).

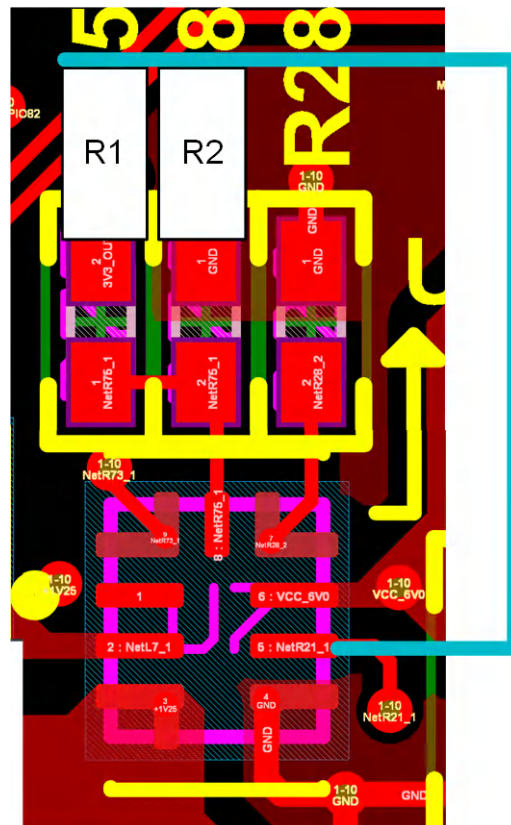


Figure 5-2. Hardware Modification for Power-Up Advisory

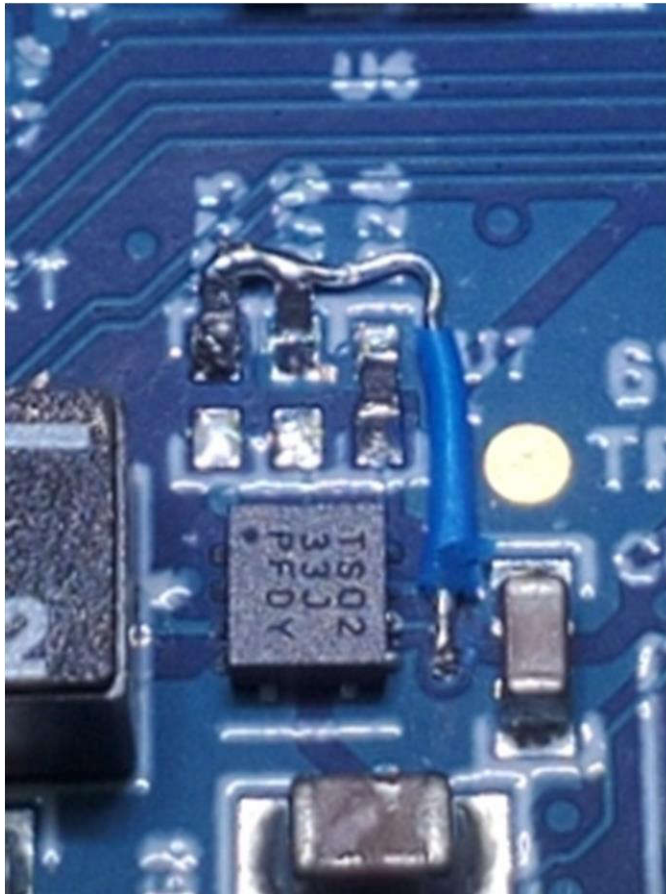


Figure 5-3. Completed Modification for Power-Up Advisory

This hardware modification has been implemented on all *MCU144E1-002* and *MCU144E1-003* assemblies.

FSI signals on the data logging and trace connector (J5) may interfere with some advanced debuggers

Revisions Affected: MCU144E1 (all assemblies)

The data logging and trace (DLT) header (J5) includes various FSI signals for data logging.

The locations of these FSI signals on J5 may interfere with some advanced debuggers such as the XDS560v2.

By default, the FSI signals are not connected to the DLT header (J5). Resistor modification is required to enable connection of the FSI signals to the DLT header.

Refer to [Section 2.4.4](#) for more information on FSI signal support for DLT header.

5.2 Trademarks

C2000™ and Code Composer Studio™ are trademarks of Texas Instruments.

USB Type-C® is a registered trademark of USB Implementers Forum.

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6 References

- HSEC180 adapter board for system-on-module (SOM)-based platforms ([HSEC180ADAPEVM](#))
- XDS110 isolated plug-in board for C2000 and Sitara controlSOMs ([XDS110ISO-EVM](#))
- HSEC180 controlCARD baseboard docking station ([TMDSHSECDOCK](#))
- Texas Instruments, [F29H85x and F29P58x Real-Time Microcontrollers](#) data sheet
- Texas Instruments, [F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual](#)
- [Code Composer Studio Integrated Development Environment \(IDE\)](#)
- [MCU-SDK-F29H85x Development Kit](#)

7 Revision History

Changes from November 5, 2024 to December 18, 2024 (from Revision A (November 2024) to Revision B (December 2024))

	Page
• <i>EVM Advisories</i> section: Changed section title from <i>MCU144E1 Known Hardware Issues</i> to <i>EVM Advisories</i>	27
• <i>EVM Advisories</i> section: Added "MCU fault state possible when on-board 25MHz clock is enabled" advisory.....	27
• <i>EVM Advisories</i> section: Added "MCU Reset can cause PMIC to shut down MCU power supplies" advisory.....	27
• <i>EVM Advisories</i> section: Added "Revisions Affected" to each advisory.....	27
• <i>EVM Advisories</i> section: Updated "Incorrect power-up sequence for VDD and VDDIO/VDDA MCU rails" advisory by changing "This hardware modification has been implemented on all MCU144E1-002 assemblies" to "This hardware modification has been implemented on all MCU144E1-002 and MCU144E1-003 assemblies".....	27

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないものご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。日本テキサス・イ

ンスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 <https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html>

3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4. *EVM Use Restrictions and Warnings:*
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 *Safety-Related Warnings and Restrictions:*
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
 - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
 5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
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 - 6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.
 - 6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.
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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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