TLC6C5712-Q1 12-Channel, Full-Diagnostic, Constant-Current-Sink LED Driver With 8-Bit Dot Correction

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H3A
  - Device CDM ESD Classification Level C4B
- 12 Power DMOS-Transistor Output Channels
  - Maximum Constant Current up to 75 mA, Programmable through External Resistor
  - Maximum Output Voltage up to 7 V
  - Maximum Dropout Voltage:
    - 0.75 V at 50 mA per Channel
    - 1.2 V at 75 mA per Channel
- Excellent Output Constant-Current Accuracy:
  - Channel-Channel Difference: < ±3% (Max.)
  - Device-Device Difference: < ±3% (Max.)
  - 8-Bit, 256-Step Linear Dot Correction for Each Channel
- Flexible External PWM Dimming Support
  - 6 PWM Inputs With Frequency Supervision
  - Programmable Channel Mapping Capability through SPI
- Protection and Diagnostics
  - Adjacent-Pin Short Detection
  - Open-Load, Short-to-GND, Shorted-LED, Detection for Both Activated and Deactivated State
  - Thermal Prewarning and Shutdown
  - Open-Drain Error Retorting
  - LED Weak Supply Diagnostics
  - Reference Resistor Open or Short Detection and Protection
  - SPI Register Lock for Content Protection
  - Force Error for SPI Integrity Diagnostics
- Small and Thermally Effective 28-Pin HTSSOP PowerPAD™ Package

2 Applications

- Cluster Tell-Tale Indicators
- Panel and Button Backlighting
- Bar-Graph LEDs
- Shifter PRNDL Indicators
- Sequential Turn Indicators

3 Description

In automotive cluster and other safety-critical LED driver applications, the performance demand for multi-channel LED is increasing to achieve consistency of LED brightness and color temperature. System-level safety considerations require detection capability for various fault scenarios and thus increase system complexity.

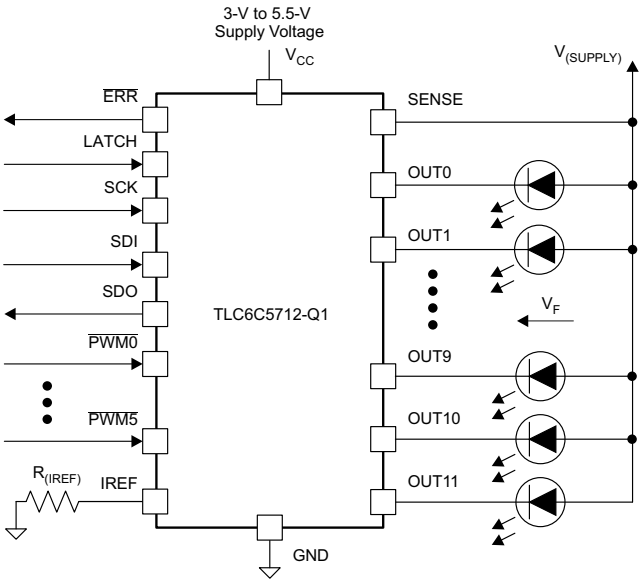
The TLC6C5712-Q1 device is a 12-channel constant-current-sink LED driver. The precision output current with 8-bit dot correction makes the TLC6C5712-Q1 device a perfect solution to correct LED brightness and color temperature variation. Advanced protection and diagnostics for each component improve system-level robustness and ease safety-oriented design. Six PWM inputs with programmable mapping support different LED color-dimming configurations and provide a high dimming ratio. A 16-bit serial-peripheral interface (SPI with diagnostics supports multiple devices in a daisy chain and eases the system-level design.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC6C5712-Q1	HTSSOP (28)	4.40 mm × 9.70 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2014) to Revision A	Page
• Released the full version of the data sheet	1

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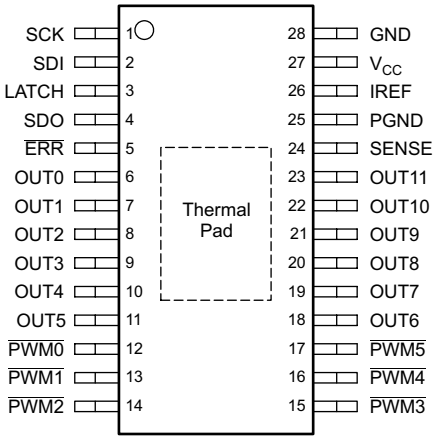
5 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP PowerPAD Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{ERR}}$	5	O	Error output, open-drain output, active-low
GND	28	—	Device ground
IREF	26	I	Connect an external resistor to GND for setting the full-scale current.
LATCH	3	I	Latch enable
OUT0	6	O	Open-drain output
OUT1	7	O	Open-drain output
OUT2	8	O	Open-drain output
OUT3	9	O	Open-drain output
OUT4	10	O	Open-drain output
OUT5	11	O	Open-drain output
OUT6	18	O	Open-drain output
OUT7	19	O	Open-drain output
OUT8	20	O	Open-drain output
OUT9	21	O	Open-drain output
OUT10	22	O	Open-drain output
OUT11	23	O	Open-drain output
PGND	25	—	Ground for output power
$\overline{\text{PWM0}}$	12	I	PWM dimming input 0
$\overline{\text{PWM1}}$	13	I	PWM dimming input 1
$\overline{\text{PWM2}}$	14	I	PWM dimming input 2
$\overline{\text{PWM3}}$	15	I	PWM dimming input 3
$\overline{\text{PWM4}}$	16	I	PWM dimming input 4
$\overline{\text{PWM5}}$	17	I	PWM dimming input 5
SCK	1	I	SPI clock
SDI	2	I	Serial-data input
SDO	4	O	Serial-data output
SENSE	24	I	Sense input (LED supply-voltage monitor)
V_{CC}	27	I	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range. Voltages referenced with respect to GND (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Input voltage	V_{CC}	–0.3	7	V
	IREF, LATCH, $\overline{PWMx}$, SCK, SDI	–0.3	V_{CC}	
	SENSE	–0.3	10	
Output voltage	ERR open-drain output	–0.3	7	V
	OUTx power DMOS drain-to-source voltage	–0.3	10	
	SDO	–0.3	V_{CC}	
Ground	PGND	–0.3	0.3	V
Operating ambient temperature, T_A		–40	125	°C
Operating junction temperature, T_J		–40	150	°C
Storage temperature range, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured relative to GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	V
			Corner pins (1, 14, 15, and 28)	±750	

(1) AEC Q100-002 indicates HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply input voltage		3		5.5	V
V_I	Input voltage	LATCH, $\overline{PWMx}$, SCK, SDI, SDO	0		5.5	V
		ERR, SENSE	0		7	
V_O	Output voltage	OUTx for x = 0 to 11	0.5		7	V
V_{IL}	Input logic-low voltage	LATCH, $\overline{PWMx}$, SCK, SDI	0.28 V_{CC}	0.3 V_{CC}	0.33 V_{CC}	V
V_{IH}	Input logic-high voltage	LATCH, $\overline{PWMx}$, SCK, SDI	0.38 V_{CC}	0.4 V_{CC}	0.43 V_{CC}	V
T_A	Ambient operating temperature		–40		125	ºC
T_J	Junction operating temperature		–40		150	ºC

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6.4 Thermal Information

THERMAL METRIC(1)		TLC6C5712-Q1 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC}, PGND, GND)						
I_{CC}	Supply current	V_{CC} = 5 V, PWM = H, R_{REF} = 20.5 kΩ	3		4.5	mA
		V_{CC} = 3.3 V	2.5		4	
$V_{(POR-rising)}$	Power-on reset voltage, rising	Rising threshold	2.6	2.7	2.8	V
$V_{(POR-falling)}$	Power-on reset voltage, falling	Falling threshold	2.4	2.5	2.6	V
$V_{(POR-hyst)}$	POR threshold hysteresis			0.2		V
LOGIC INPUTS ($\overline{PWMx}$, SDI, LATCH, SCK)						
$V_{(HYS)}$	Input logic hysterisis	V_{CC} = 5 V or 3.3 V		0.1 V_{CC}		V
I_{lkg}	Input leakage current	V_I = V_{CC}	–1		1	µA
R_{PU}	PWM pullup resistance		105	150	230	kΩ
CONTROL OUTPUTS (ERR, IREF, SDO)						
$V_{(ERR)}$	ERR pin open-drain voltage drop	$I_{(ERR)}$ = 4 mA, V_{CC} = 3.3 V–5 V			0.1 V_{CC}	V
$I_{lkg(ERR)}$	ERR leakage current	$V_{(ERR)}$ = 5 V			3	µA
$V_{(IREF)}$	IREF voltage	$R_{(IREF)}$ = 20.5 kΩ	1.204	1.229	1.254	V
$V_{OH(SDO)}$	SDO output-high voltage	$I_{(SDO)}$ = –4 mA	0.9 V_{CC}			V
$V_{OL(SDO)}$	SDO output-low voltage	$I_{(SDO)}$ = 4 mA			0.1 V_{CC}	V
OUTPUT STAGE (OUTx)						
$I_{(OUTx,max)}$	Constant output current	$V_{(OUTx)}$ = 0.75 V, $R_{(IREF)}$ = 12.2 kΩ, Dot correction = 255		50		mA
		$V_{(OUTx)}$ = 1.2 V, $R_{(IREF)}$ = 8.13 kΩ, Dot correction = 255		75		
$I_{(OUTx,min)}$	Minimum current-sink capability	$V_{(OUTx)}$ = 0.75 V, R_{REF} = 12.2 kΩ, dot correction = 255	0.15	0.165	0.18	mA
$I_{(OUTx,default)}$	Constant output current	$V_{(OUTx)}$ = 0.75 V, reference fault detected, Dot correction = 255	7.5	10	14	mA
$V_{(OUT,min)}$	Minimum output voltage	V_{CC} = 3.3 V, $R_{(IREF)}$ = 12.2 kΩ, dot correction = 255			0.75	V
		V_{CC} = 5 V, $R_{(IREF)}$ = 12.2 kΩ, dot correction = 255			0.5	
		V_{CC} = 5 V, $R_{(IREF)}$ = 8.13 kΩ, dot correction = 255			1.2	
DNL	Output-current dot-correction differential nonlinearity	V_{CC} = 5 V, $R_{(IREF)}$ = 12.2 kΩ, (50-mA maximum output current)	–0.6		0.6	mA
		V_{CC} = 5 V, $R_{(IREF)}$ = 61 kΩ, (10-mA maximum output current)	–0.08		0.08	
$\Delta I_{(OUTx)}$	Output current absolute error percentage	$V_{(OUTx)}$ = 0.75 V, $R_{(IREF)}$ = 12.2 kΩ (50 mA), dot correction = 255	–3%		3%	
		$V_{(OUTx)}$ = 0.75 V, $R_{(IREF)}$ = 20.5 kΩ (30 mA), dot correction = 255	–3%		3%	
		$V_{(OUTx)}$ = 0.75 V, $R_{(IREF)}$ = 61 kΩ (10 mA), dot correction = 255	–7.5%		7.5%	
		$V_{(OUTx)}$ = 1.2 V, $R_{(IREF)}$ = 8.13 kΩ (75 mA), dot correction = 255	–3%		3%	

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Electrical Characteristics (continued)

T_A = 25°C, over recommended operating conditions (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta I_{(OUT\_VOUT)}$	Output current dependency on OUTx voltage	$V_{(OUTx)}$ = 0.75 V, $R_{(IREF)}$ = 12.2 kΩ (50 mA), $\Delta I_{(OUT\_VOUT)} = (I_{(OUT\_7V)} - I_{(OUT\_1V)} / I_{(IDEAL)}) \times 100$	–0.5%		0.5%	
$K_{(OUT)}$	Ratio of output current to IREF current, $K = I_{(OUTx)} / I_{(IREF)}$	Dot correction = 255		500		mA/mA
$I_{lkg(OUTx)}$	Output leakage current	*[CH_EN_MASKx]* = 1, *[DIS_OFF_FAULT_DIAG]* = 1, $V_{(OUTx)}$ = 6.7 V, $V_{(SENSE)}$ = 7 V, T_A = 125°C			0.5	µA
$I_{lkg(SENSE)}$	Leakage current at SENSE pin	V_{CC} = 0, $V_{(SENSE)}$ = 5 V			10	µA
$I_{(IREF\_octh)}$	IREF resistor open-circuit detection threshold	V_{CC} = 5 V	4.5		15	µA
$I_{(IREF\_octh,hyst)}$	IREF resistor open-circuit detection-threshold hysteresis	V_{CC} = 5 V		2		µA
$I_{(IREF\_scth)}$	IREF resistor short-circuit detection threshold	V_{CC} = 5 V	160		260	µA
$I_{(IREF\_scth,hyst)}$	IREF resistor short-circuit detection-threshold hysteresis	V_{CC} = 5 V		20		µA
$I_{(OUT\_PULLUP)}$	Channel pullup current during deactivated state	V_{CC} = 5 V, $V_{(OUTx)}$ = 1 V		50		µA
PROTECTION CIRCUITS						
$V_{(WLS)}$	Weak LED supply-detection threshold voltage	*[WLS_TH]* = 0	4.1	4.2	4.3	V
$V_{(WLS\_hyst)}$	Weak LED supply hysteresis	*[WLS_TH]* = 0		0.1		V
$V_{(WLS\_OPT)}$	Weak LED supply detection-threshold voltage	*[WLS_TH]* = 1	2.7	2.77	2.85	V
$V_{(WLS\_hyst\_OPT)}$	Weak LED supply hysteresis	*[WLS_TH]* = 1		0.1		V
$V_{(SC\_th)}$	Short circuit-to-$V_{(SENSE)}$ detection threshold, voltage difference between V(SENSE) and V(OUTx)		0.5	0.7	0.9	V
$V_{(SC\_hyst)}$	Short circuit-to-$V_{(SENSE)}$ detection hysteresis			0.1		V
$V_{(OC\_th)}$	Open-circuit detection threshold		0.1	0.2	0.3	V
$V_{(OC\_hyst)}$	Open-circuit-detection hysteresis			0.05		V
$T_{(TSD)}$	Thermal-shutdown junction temperature		150	165		ºC
$T_{(HYS)}$	Thermal shutdown or warning junction temperature hysteresis			15		ºC
$T_{(PTW)}$	Pre-thermal warning junction-temperature threshold		125	135	150	ºC

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6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
$f_{(SCK)}$	Clock frequency, cascade operation		1	10	MHz
$t_{c(SCK)}$	SCK cycle time	100			ns
$t_{w(LAH)}$, $t_{w(WLAH)}$	Pulse duration, LATCH	380			ns
$t_{w(CKH)}$, $t_{w(WCKH)}$	SCK high pulse duration	50			ns
$t_{w(CKL)}$, $t_{w(WCKL)}$	SCK low pulse duration	50			ns
$t_{w(SEW)}$, $t_{w(WDI)}$	SDI high and low pulse duration	150			ns
$t_{su(SEST)}$	SDI setup time prior to SCK rise	75			ns
$t_{h(SEHD)}$	SDI hold time after SCK rise	75			ns
t_r	Output rise time (SCK)			50	ns
t_f	Output fall time (SCK)			50	ns

6.7 Switching Characteristics

T_A = –40°C to 105°C, V_{CC} = 3 V to 5.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCK)}$	Clock frequency	Cascade operation			10	MHz
$t_{d(LAH)}$	Latch switching delay				3000	ns
$t_{pd(SOH)}$	SDO propagation delay time (L to H)				1000	ns
$t_{pd(SOL)}$	SDO propagation delay (H to L)				3000	ns
$t_{pd(LAOL)}$	High to low propagation delay time (LATCH – OUT)			750	3000	ns
$t_{pd(CKLAH)}$	Low-to-high propagation delay time (SCK – LATCH)		200			ns
$t_{pd(CKDOH)}$	Low-to-high propagation delay time (SCK – SDO)			30	75	ns
$t_{pd(CKDOHL)}$	High-to-low propagation delay time (SCK – SDO)			30	75	ns
$t_{r(o)}$	Rise time, outputs (OFF) SDO				50	ns
$t_{f(o)}$	Fall time, outputs (ON) SDO				50	ns
$t_{d(PWM\_ON)}$	Output delay time from PWMx to $I_{(OUTx)}$	PWMx falling threshold from 0.4 V_{CC} to $I_{(OUTx)}$ rising threshold 10% of $I_{(OUTx,max)}$	0.09	0.13	0.2	µs
$t_{d(PWM\_OFF)}$	Output delay time PWMx to I_{OUTx}	PWMx rising threshold from 0.4 V_{CC} to $I_{(OUTx)}$ falling threshold 90% of $I_{(OUTx,max)}$	0.09	0.13	0.2	µs
t_r	Output rise time	Default slew rate, rise time from 10% to 90% current, 30-pF loading capacitance			0.3	µs
		With slow-slew-rate register option, rise time from 10% to 90% current, 30-pF loading capacitance			0.8	
t_f	Output fall time	Default slew rate, fall time from 90% to 10% current, 30-pF loading capacitance			0.3	µs
		With slow-slew-rate register option, fall time from 90% to 10% current, 30-pF loading capacitance			0.8	
$t_{(DEG)}$	Output open or short degllitch time		1	2	3	µs
$t_{(REF\_DEG)}$	Reference open or short deglitch time			100		µs
$t_{(PWM)}$	PWM edge detection timer	Timer length for PWM edge detection	17	20	23	ms

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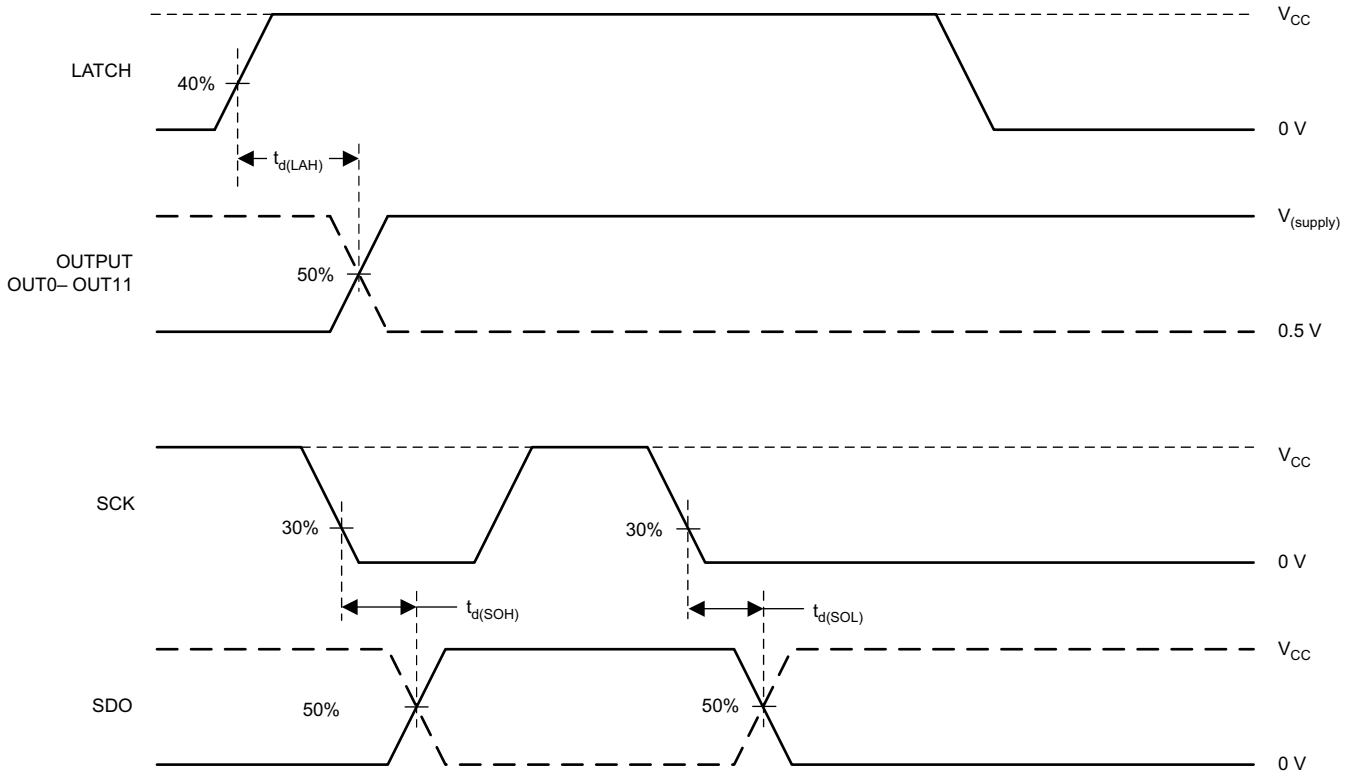

Figure 1. Input Signal Timing Diagram Showing Absolute Minimal Timing

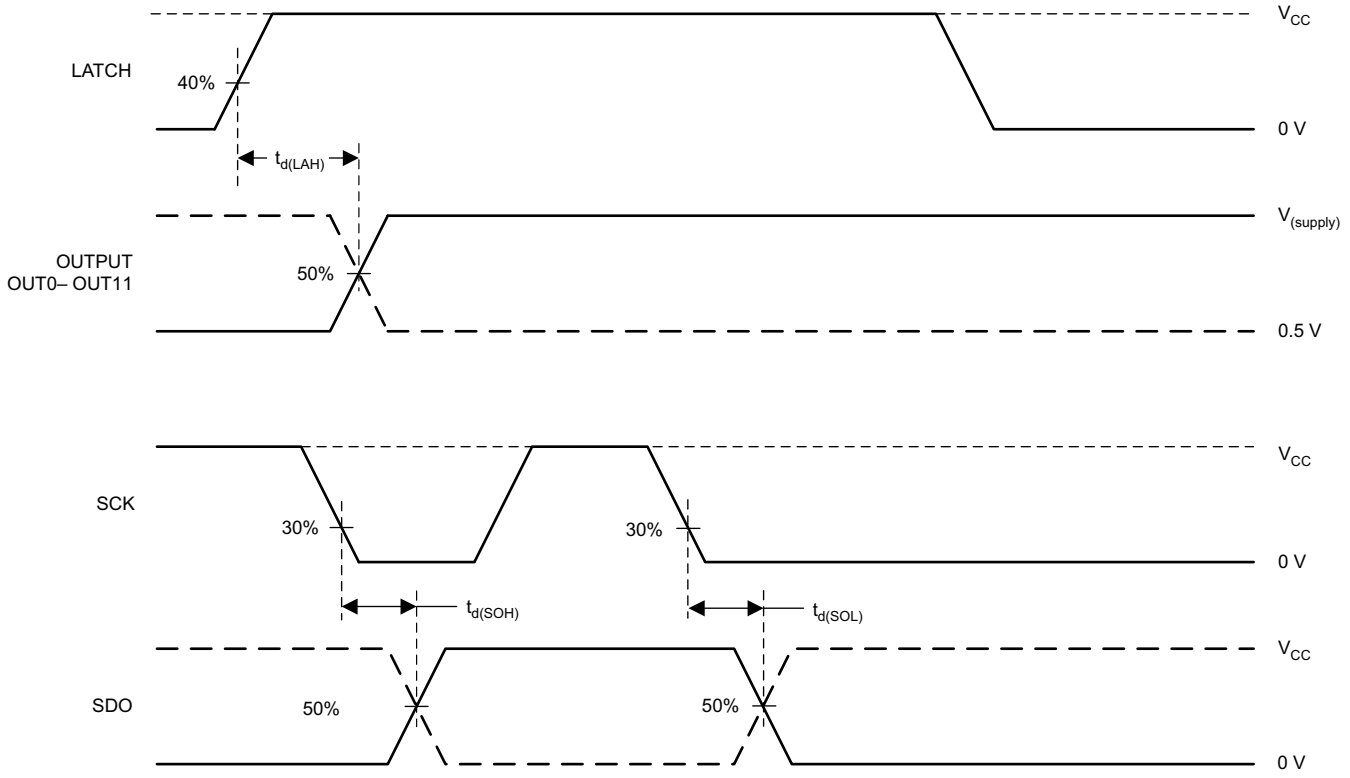

Figure 2. Output Signal Delay Time

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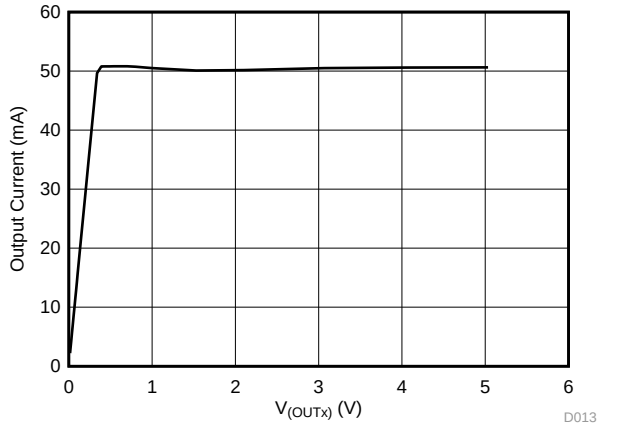
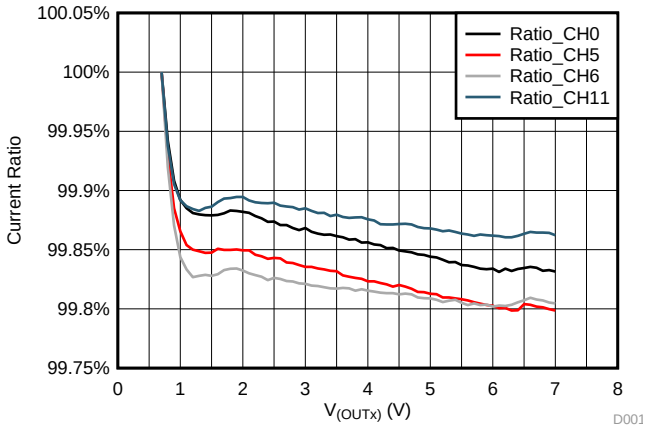
6.8 Typical Characteristics



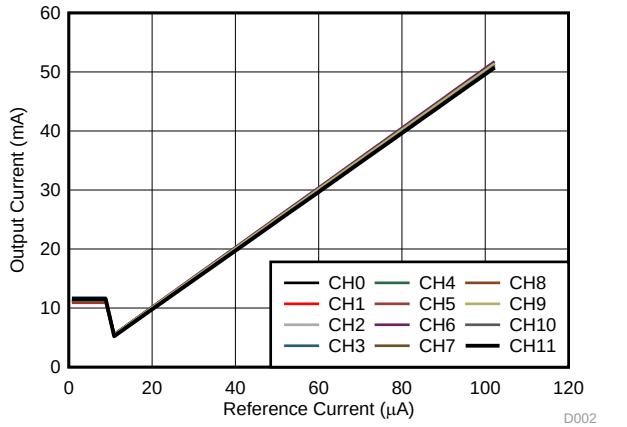
V_{CC} = 3.3 V $R_{(IREF)}$ = 12.2 kΩ T_A = 25ºC
Dot correction = 255

Figure 3. Output Current vs Output Voltage



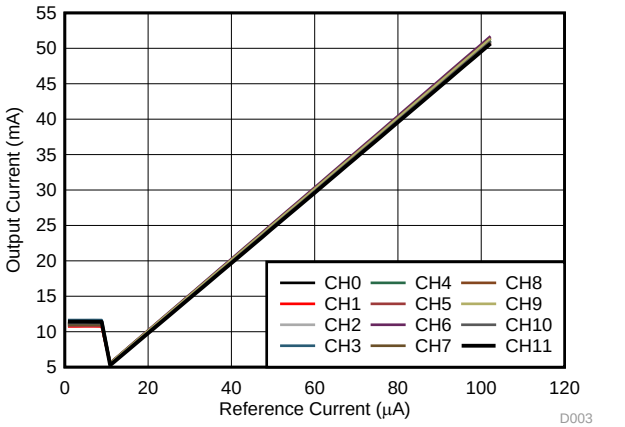
V_{CC} = 5.5 V T_A = 25ºC $R_{(IREF)}$ = 12.2 kΩ
Dot correction = 255

Figure 4. Output Current Ratio vs Output Voltage



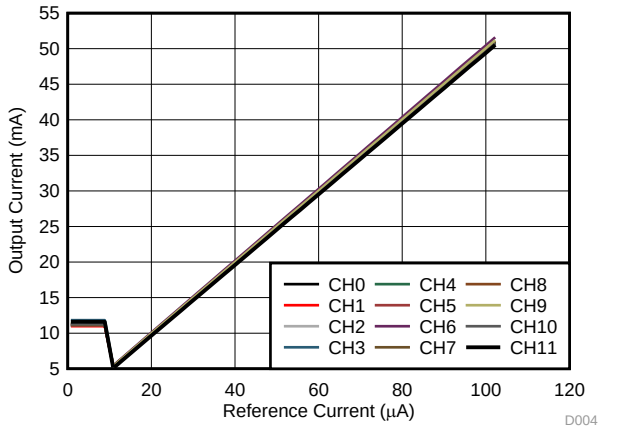
V_{CC} = 5.5 V T_A = 25ºC Dot correction = 255

Figure 5. Output Current vs Reference Current



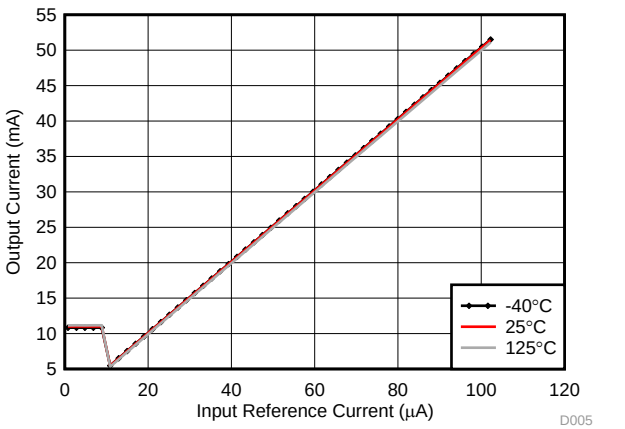
V_{CC} = 5.5 V T_A = –40ºC Dot correction = 255

Figure 6. Output Current vs Reference Current



V_{CC} = 5.5 V T_A = 125ºC Dot correction = 255

Figure 7. Output Current vs Reference Current



V_{CC} = 5.5 V Channel = IOUT5 Dot correction = 255

Figure 8. Output Current vs Reference Current

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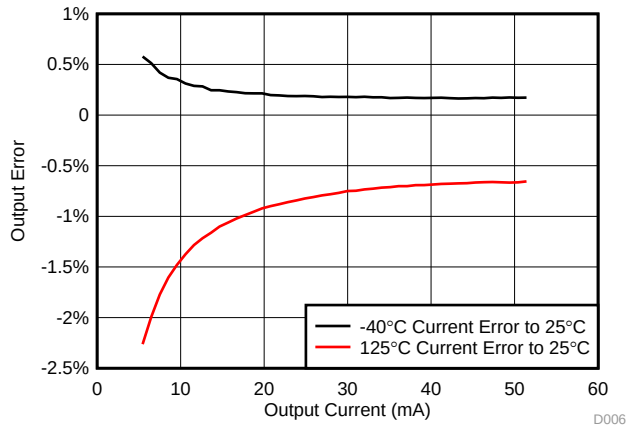
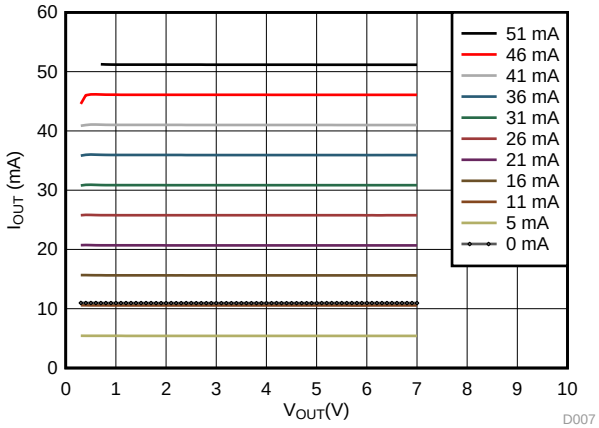
Typical Characteristics (continued)



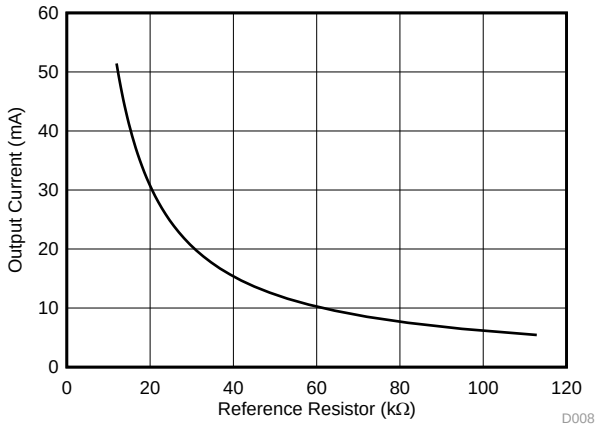
V_{CC} = 5.5 V T_A = 25ºC Dot correction = 255

Figure 9. Output Temperature Error vs Output Current



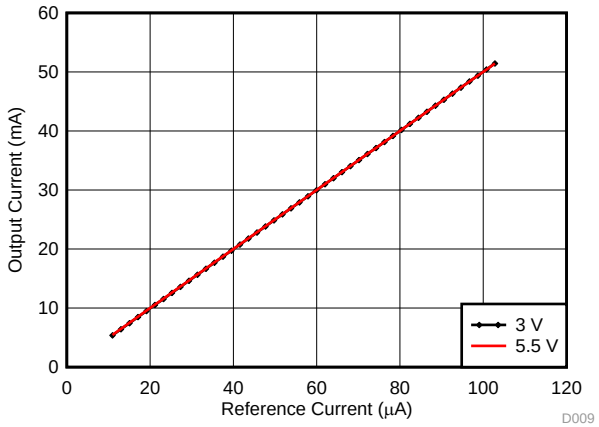
V_{CC} = 5.5 V T_A = 25ºC Dot correction = 255

Figure 10. Output Current vs Output Voltage



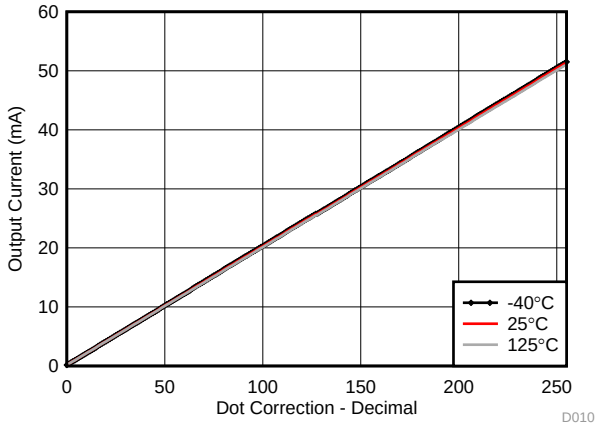
V_{CC} = 5.5 V V_O = 0.7 V Dot correction = 255
T_A = 25ºC

Figure 11. Output Current vs Reference Resistor



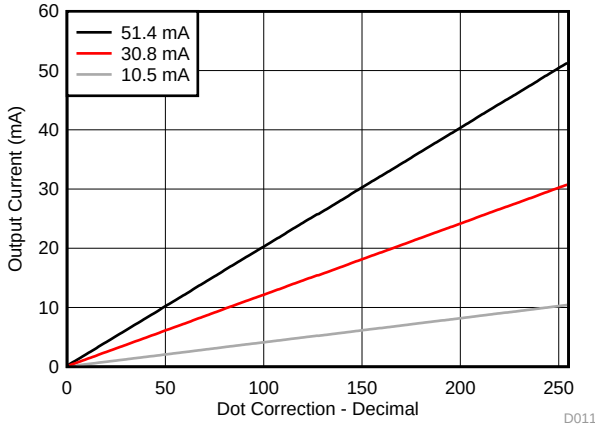
V_O = 0.7 V T_A = 25ºC Dot correction = 255

Figure 12. Output Current vs Reference Current



V_O = 0.7 V I_O = 51.4 mA

Figure 13. Output Current vs Dot Correction



V_O = 0.7 V T_A = 25ºC

Figure 14. Output Current vs Dot Correction

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7 Detailed Description

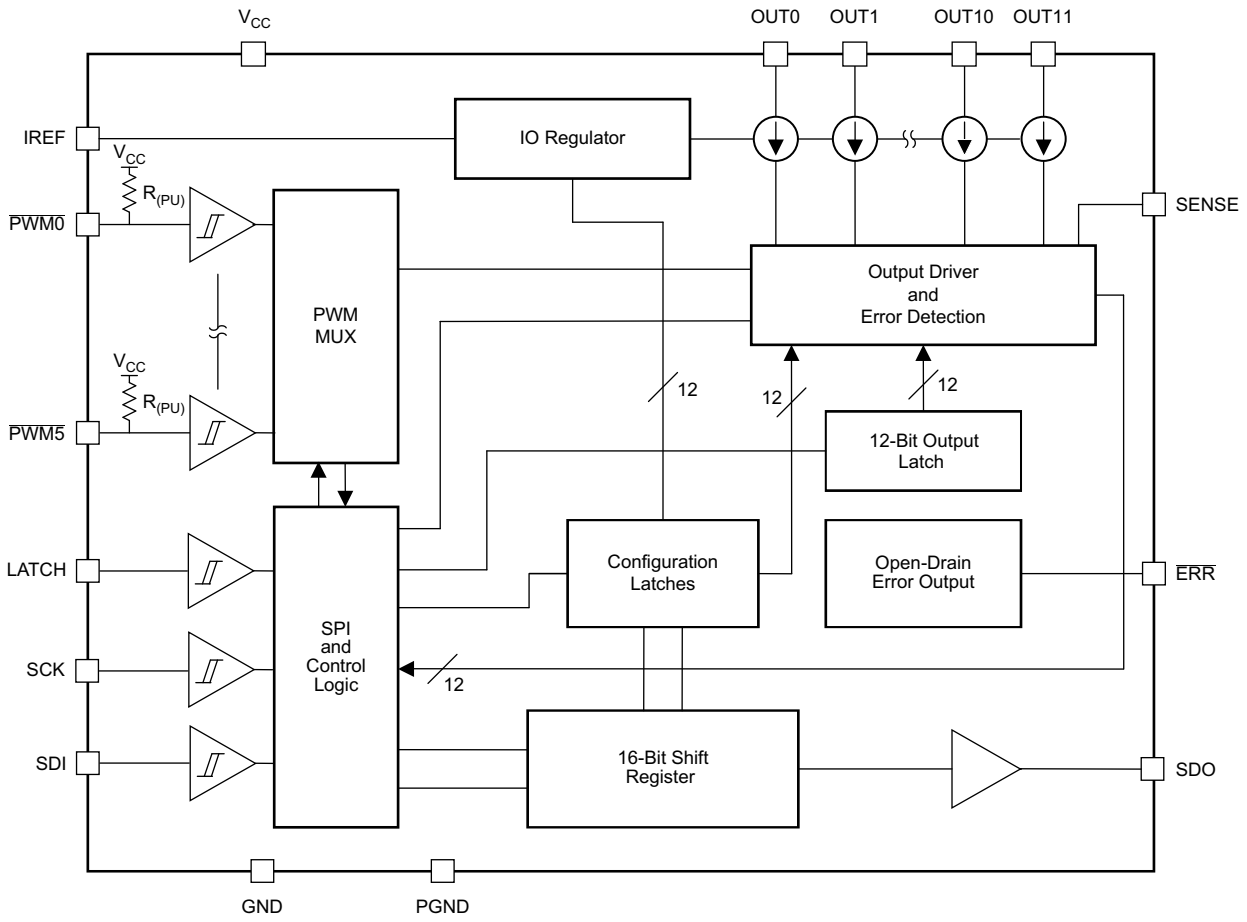
7.1 Overview

The TLC6C5712-Q1 device is a 12-channel constant-current-sink LED driver. At the TLC6C5712-Q1 output stage, 12 regulated current channels provide uniform and constant current for driving LEDs within a wide range of forward-voltage variations.

Users can adjust output current from 10 mA to 75 mA through an external resistor, $R_{(IREF)}$, which provides flexibility in controlling the light intensity of the LEDs. The maximum constant-current value (full-scale range) of all 12 channels is set by a single external resistor. The current of each individual output can be programmed in 256 linear steps, allowing further calibration. The design of the TLC6C5712-Q1 device supports up to 7 V at the output ports. The serial communication interface is designed for high-throughput data transmission with cascaded devices. The device has six PWM input channels and 12 output channels that can be mapped arbitrarily to any of the 6 PWM inputs.

The TLC6C5712-Q1 device has advanced diagnostics, LED open-load detection, shorted-LED detection, short-circuit to ground detection, reference resistor open and short protection, PWM input-frequency supervision, adjacent-pin short diagnostics, thermal pre-warning and thermal protection. LED open-and-short and output short-to-ground detection is available even when an LED channel is off. The diagnostic functions and errors can be activated or de-activated individually by functions or channels. Users can configure the open-drain error output to signalize various types of errors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power-On Reset (POR)

The device supports two types of POR, start-up or UVLO POR and software POR, with software reset capability.

7.3.1.1 Start-Up or UVLO POR

When power is applied to V_{CC}, or when V_{CC} is undervoltage ($V_{CC} < V_{(POR)}$), an internal power-on reset (POR) holds the TLC6C5712-Q1 device in a reset condition with the following conditions until V_{CC} reaches VPOR. During RESET:

- The device cannot receive data.
- The SDO pin is held LOW, so the device cannot transmit data.
- The $\overline{\text{ERR}}$ open-drain output is pulled down.

During POR, communication between the controller and the device is lost. Any data transmitted during this period is lost. The state machine inside the device is undefined. After POR, the reset status is released, the TLC6C5712-Q1 registers and SPI state machine are re-initialized to default states (see the *Default* column in Table 2). [POR_ERR_FLAG] is set to HIGH during start-up or UVLO POR.

7.3.1.2 Software POR

A software reset command (<*SOFTWARE_POR*>) resets all internal register settings to default values. The command executes on a LATCH rising edge. All fault bits and diagnostic status are cleared and set to their default values. The <*SOFTWARE_POR*> command also executes the RESET_STATUS] command. The [POR_ERR_FLAG] bit in the <READ_STATUS0> register is set to HIGH on a software POR.

7.3.1.3 Reset POR

Either start-up or a UVLO POR or a software POR sets [POR_ERR_FLAG] to HIGH. when the device enters POR status, the [POR_ERR_FLAG] bit is latched HIGH. To clear the [POR_ERR_FLAG], a *RESET_POR* command must be issued.

If [POR_ERR_FLAG] is set either by start-up, UVLO, or software, and the device is not in any UVLO state, [POR_ERR_FLAG] is latched and does not block any operation.

7.3.1.4 POR Masking

[POR_ERR_FLAG] reporting to the $\overline{\text{ERR}}$ output can be masked by the [POR_MASK] bit. If a POR event happens when [POR_MASK] is set HIGH, POR events do not trigger the $\overline{\text{ERR}}$ output, and [POR_ERR_FLAG] is set HIGH.

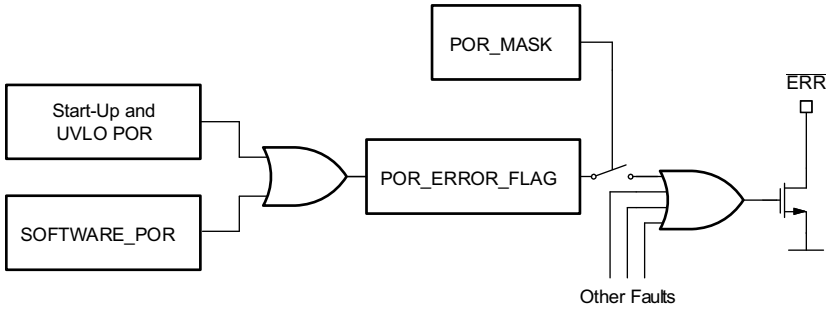


Figure 15. POR Error Report Topology

See the following addresses in Table 2: 61h, 62h, 63h, and A2h.

7.3.2 Error Feedback

The TLC6C5712-Q1 device supports an active-low open-drain output for error information through the $\overline{\text{ERR}}$ pin for the MCU error-monitor interrupt. If any FLAG bit is set to HIGH in the <READ_STATUS0> register, and is not masked by a corresponding mask bit in the <WRITE_ERROR_MASK> register, the $\overline{\text{ERR}}$ pin pulls low to indicate an ERROR scenario. The MCU should immediately execute the error monitor routine.

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Feature Description (continued)

7.3.2.1 Recovery From Error

When any fault occurs, all FAULT information can be read in separate FAULT registers, for example, <READ_OPEN_FAULT0>. When the error condition recovers, the register information is still latched and the $\overline{ERR}$ pin remains low until the fault is masked or the *RESET_STATUS* command has been issued. However, if the error condition still exists after issuing the *RESET_STATUS* command, the $\overline{ERR}$ pin pulls low again and the corresponding FAULT register is set HIGH.

7.3.2.2 RESET_STATUS Command

The *RESET_STATUS* command clears all flags in the following registers:

<READ_ADJSHORT0>
<READ_ADJSHORT1>
<READ_SHORT_FAULT0>
<READ_SHORT_FAULT1>
<READ_SHORT_GND_FAULT0>
<READ_SHORT_GND_FAULT1>
<READ_OPEN_FAULT0>
<READ_OPEN_FAULT1>
<READ_PWM_FAULT>
<READ_STATUS0>, **excluding** the [POR_ERR_FLAG] bit.

As mentioned in the POR section, only the *RESET_POR* command can clear the [POR_ERR_FLAG] bit.

[POR_ERR_FLAG] bit: Read only (R) bit. HIGH: A POR error has occurred. To reset this flag, issue a *RESET_POR* command.

[POR_MASK] bit: Read and write (R/W) bit. HIGH: A POR error is stored in the [POR_ERR_FLAG] bit and is not reported to $\overline{ERR}$.

RESET_POR: A command to reset [POR_ERR_FLAG].

SOFTWARE_POR: A command to generate a POR. It also clears STATUS flags.

See the following addresses in Table 2: 62h, 9Ah through A2h, A8h, and A9h.

7.3.3 PWM Input

The TLC6C5712-Q1 device has six $\overline{PWM}$ inputs with independently configurable mapping to modulate any of the 12 channels for external PWM dimming. A PWM monitor can be used to supervise $\overline{PWM}$ input-signal integrity.

7.3.3.1 PWM Dimming

PWM dimming is supported on all 12 channels by six $\overline{PWM}$ inputs. The input $\overline{PWMx}$ signal is active-low. Due to the minimal pulse duration needed for diagnostics, at 200 Hz the minimum achievable duty cycle is 0.1%, or 5 µs minimal on-time. Similarly, the maximum achievable duty cycle is 99.2%, or 40 µs minimum off-time. The setting of this boundary allows enough time for diagnostic functions. In the case of 0% or 100% PWM, diagnostics are not reported.

7.3.3.2 PWM Monitor

Independent **rising-edge** triggered timers are implemented as PWM monitors for each $\overline{PWMx}$ input channel. when the timer length reaches the threshold t_{PWM}, *[PWM_FAULTx]* is set to HIGH. If the corresponding masking register [PWM_FAULT_MASKx] is also set HIGH, the fault is stored in [PWM_FAULTx] and is not reported to the [ANY_PWM_FAULT_FLAG] register. [ANY_PWM_FAULT_FLAG] is set to HIGH and the $\overline{ERR}$ pin is pulled LOW if any of the PWM monitors reported a fault and the mask register [PWM_MASK] is disabled. The PWM rising edge resets the timer and restarts counting from 0. For 0% or 100% PWM, the [PWM_FAULTx] registers should be independently masked for each PWMx input via the [PWM_FAULT_MASKx] registers.

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Feature Description (continued)

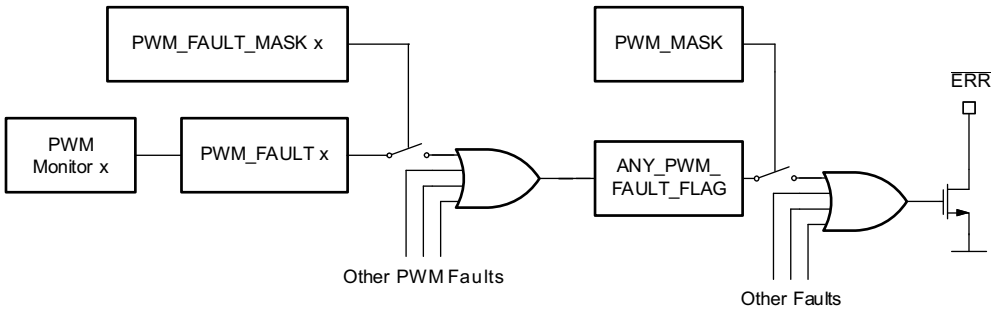

Figure 16. PWM Fault Report Topology

After being set HIGH, [PWM_FAULTx] FAULT_PWMx is latched even if the corresponding PWM input toggling has recovered. The *RESET_STATUS* command must be issued to clear the [ANY_PWM_FAULT_FLAG] bit.

7.3.3.3 PWM Mapping

Each of the 12 output channels has a 3-bit [PWM_MAP_CH] field to assign to one $\overline{\text{PWMx}}$ input. All output channels are assigned to $\overline{\text{PWM0}}$ by default. Table 1 lists the mapping for each $\overline{\text{PWMx}}$ input..

Table 1. $\overline{\text{PWMx}}$ Mapping

BIT 2	BIT 1	BIT 0	$\overline{\text{PWMx}}$
0	0	0	$\overline{\text{PWM0}}$
0	0	1	$\overline{\text{PWM1}}$
0	1	0	$\overline{\text{PWM2}}$
0	1	1	$\overline{\text{PWM3}}$
1	0	0	$\overline{\text{PWM4}}$
1	0	1	$\overline{\text{PWM5}}$
1	1	0	$\overline{\text{PWM0}}$
1	1	1	$\overline{\text{PWM0}}$

7.3.3.4 PWM MAP Register Lock

To avoid unintended modification of the <PWM MAPx> registers, the <PWM MAPx> registers can be locked via the *LOCK_MAP* command and unlocked via the *UNLOCK_MAP* command. For details, see the *Register Protection* feature.

See the following addresses in Table 2: 40h through 45h, 60h, 62h, 66h through 68h, 6Ch, A0h through A3h, A6h, and A7h.

[PWM_MAP_CH] field:	R/W. 3 bits. Mapping output channel PWM source to $\overline{\text{PWMx}}$ input.
[PWM_FAULT_MASKx] bit:	R/W. Active-high. Mask the PWM fault flag $\overline{\text{PWMx}}$.
[PWM_MASK] bit:	R/W. Active-high. Disable the ANY_PWM_FAULT_FLAG from reporting to $\overline{\text{ERR}}$.
[PWM_FAULTx] bit:	R only. Active-high. HIGH: PWM monitor timer has triggered for $\overline{\text{PWMx}}$.
[ANY_PWM_FAULT_FLAG] bit:	R only. Active-high. HIGH: One or more $\overline{\text{PWMx}}$ inputs have triggered the PWM monitor.
[SLOW_SLEW_RATE] bit:	R/W. Active-high. HIGH: Slow slew rate.

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7.3.4 Constant-Current Output

The TLC6C5712-Q1 device has 12 constant-current output channels. An external resistor, $R_{(IREF)}$, sets the maximum current of all channels globally. The current of each channel is individually configurable by independent 8-bit current digital-to-analog converters to support dot-correction capability, also known as calibration capability. Dot correction can be used to calibrate out brightness differences introduced by LED bin-to-bin differences or plastic transmittance variation by software instead of manually selecting matching resistors.

7.3.4.1 Global Current Reference

Maximum channel output current (dot-correction register [OUTPUT_DC_CHx] is set at full range, FFh) is globally set by reference resistor $R_{(IREF)}$. The $V_{(IREF)}$ voltage biases external reference resistor $R_{(IREF)}$, generating reference current $I_{(IREF)}$. $I_{(IREF)}$ is sensed and amplified by the ratio of $K_{(OUT)}$ as the maximum output current. Choose the external resistor $R_{(IREF)}$ value using Equation 1, based on maximum current $I_{(OUT,MAX|DC=255}$.

$$R_{(IREF)} = \frac{V_{(IREF)}}{I_{(OUT)max\,|\,Dot\ Correction\,=\,255}} \times K_{(OUT)} \quad (1)$$

7.3.4.2 Current Reference Monitor and Protection

The TLC6C5712-Q1 device implements a current-reference monitor for current-reference resistor open-and-short diagnostic and protection. The device monitors the current $I_{(IREF)}$ flowing out of the IREF pin. If $I_{(IREF)}$ is higher than $I_{(IREF\_scth)}$, a reference-short condition is asserted, limiting the $I_{(IREF)}$ output current for short protection. If the $I_{(IREF)}$ current is smaller than $I_{I(IREF\_octh)}$, a reference-open condition is asserted.

To maintain output function when the IREF resistor is in a short or open condition, device switches to a fail-safe current source. In fail-safe mode, the maximum output current is defined as $I_{(OUTx\_default)}$. when the external fault condition is removed, the external resistor sets the $I_{(IREF)}$ current.

$$I_{(IREF)} = \frac{V_{(IREF)}}{R_{(IREF)}} \quad (2)$$

To avoid switching into default current unintentionally, the device implements a digital deglitch filter on the reference open and short diagnostics. The filter length is defined as $t_{(REF\_deg)}$. On assertion of the reference open-or-short fault, the [REF_FAULT_FLAG] bit is set. The [REF_MASK] bit can be used to mask the reference fault output to the $\overline{ERR}$ pin. If [REF_MASK] is enabled, a reference fault is not reported to the $\overline{ERR}$ output. If [REF_MASK] is enabled, a reference fault is not reported to the $\overline{ERR}$ output. Clearing the [REF_FAULT_FLAG] bit requires issuing the *RESET_STATUS* command.

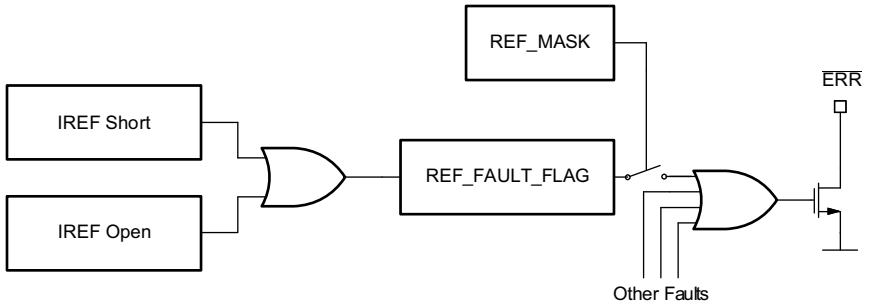

Figure 17. Reference Fault Report Topology

7.3.4.3 Channel Activation Control

[CH_ON_MASKx] are the channel activation mask bits which control each channel output ACTIVATED-DEACTIVATED. Logic LOW stands for channel ACTIVATED status.

DEACTIVTING a channel output does not clear the diagnostics registers.

7.3.4.4 Individual Dot Correction Control

Each channel has an internal 8-bit linear-current digital-to-analog converter for individual dot correction control. The 8-bit [OUTPUT_DC_CHx] fields are used to control DAC output current according to Equation 3. Note that the minimum current is 1 / 256 of $I_{OUT,MAX}$. If absolutely zero current is required in some scenarios, the channel can be disabled by setting the corresponding channel-enable [CH_ON_MASKx] bit HIGH.

$$I_{(OUT)} = I_{(OUT)}max \times \frac{\text{Dot Correction} + 1}{256} \quad (3)$$

7.3.4.5 Output Slew-Rate Adjustment

To accommodate different slew rate requirements for EMC optimization, the [SLOW_SLEW_RATE] bit is provided. Setting [SLOW_SLEW_RATE] HIGH makes both the rising and falling times, t_r and t_f, longer.

7.3.4.6 Register Lock

To avoid unintended modification of registers, the [OUTPUT_DC_CHx] fields can be locked with the *LOCK_CORR* command and unlocked with the *UNLOCK_CORR* command. The *[CH_ON_MASKx]* bits can be locked with the *LOCK_MASK* command and unlocked with the *UNLOCK_MASK* command. For details, see the *Register Protection* section.

7.3.4.7 Deactivated-Channel Internal Pullup

To avoid floating outputs on a deactivated channel, optional pullup current to the SENSE node $I_{(OUT\_PULLUP)}$ is provided. The pullup current is disabled by default and can be enabled by setting the [DIS_PULL_UP_CHx] bit HIGH.

See the following addresses in Table 2: 46h through 43h, 69h, 6Ah, 6Dh, 6Eh, and 86h through 93h.

[OUTPUT_DC_CHx] field:	R/W. 8-bit. Dot correction current DAC setting register for channel x.
[CH_ON_MASKx]:	R/W. HIGH: Channel output disabled; LOW: Channel output enabled

7.3.5 Advanced Diagnostics

The TLC6C5712-Q1 device supports a variety of diagnostic features, including:

- Pre-thermal warning and thermal shutdown protection
- LED short-to-supply detection
- LED short-to-GND detection
- LED open-load detection
- Deactivated-channel LED-open or -short detection
- Weak-LED-supply detection
- Adjacent-pin short detection
- Reference resistor open or short detection and protection
- PWM frequency monitor

7.3.5.1 Pre-Thermal Warning and Thermal Shutdown Protection

When the junction temperature exceeds the pre-thermal-warning threshold $T_{(PTW)}$, [PRE_TSD_FLAG] in the <READ_STATUS0> register is set HIGH to signal the pre-thermal warning. The $\overline{ERR}$ open-drain output is also pulled down. The microcontroller should respond to the fault warning and take actions to prevent junction temperature rising.

If junction temperature continues to rise and exceeds thermal-shutdown threshold $T_{(TSD)}$, the overtemperature fault bit [TSD_FLAG] in the <READ_STATUS0> register is set HIGH to signal thermal shutdown, the $\overline{ERR}$ open-drain output is also pulled down, and all output channels are turned off for protection.

[PRE_TSD_FLAG] and [TSD_FLAG] are latched when triggered. To clear either of the flags, issue the *RESET_STATUS* command.

[TSD_FLAG] is latched after having been set. After the die temperature falls below $T_{(TSD)} – T_{(HYS)}$, the LED outputs are activated using the previous settings without re-initializing.

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The flag bits can be individually masked by [PRE_TSD_MASK] and [TSD_MASK]. [PRE_TSD_MASK] prevents the $\overline{\text{ERR}}$ open-drain output. [TSD_MASK] prevents the $\overline{\text{ERR}}$ open-drain output and thermal shutdown of all channels. Even if the faults are masked, the fault status can still be read in the registers.

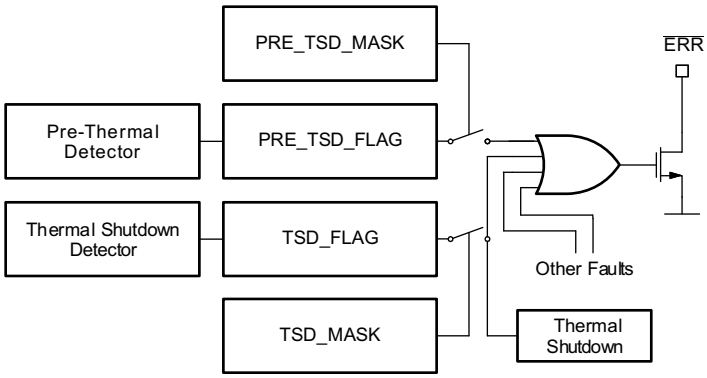

Figure 18. Thermal Fault Report Topology

7.3.5.2 LED Short-to-Supply Detection

The device has independent LED short-to-supply detection for each channel. Whether the channel PWM source is HIGH or LOW, the voltage difference between the SENSE and OUTx pins is monitored.

If an LED short to the supply is detected, the [SHORT_FAULT_CHx] bit of the channel is set HIGH and the [ANY_SHORT_FLAG] bit is set HIGH The [ANY_SHORT_FLAG] also pulls down the $\overline{\text{ERR}}$ open-drain output.

The LED short-to-supply fault does not disable the corresponding channel output. when the fault condition is removed, the LED should resume normal operation. Fault conditions are latched in the [SHORT_FAULT_CHx] bits. To clear the [SHORT_FAULT_CHx] bits, issue the *RESET_STATUS* command.

The [SHORT_FAULT_CHx] bits can be masked independently for each channel by the [SHORT_MASK_CHx] bits. when the [SHORT_MASK_CHx] bit of any channel is set HIGH, the short-to-supply fault on the specific channel is not reported to [ANY_SHORT_FLAG].

7.3.5.3 LED Short-to-GND Detection

The TLC6C5712-Q1 device is able to distinguish an LED short-to-GND condition from an LED open-detection condition by having an internal pullup current to the SENSE node. The pullup is enabled during the PWM OFF state or channel-deactivated state.

If an LED short-to-GND is detected, the [SG_FAULT_CHx] bit for the channel is set HIGH, and the [ANY_SHORT_FLAG] bit is also set HIGH. [ANY_SHORT_FLAG] also pulls down the $\overline{\text{ERR}}$ open-drain output.

An LED short-to-GND fault does not disable the corresponding channel output. when a fault condition is removed, the LED should resume normal operation. Fault conditions are latched in the [SG_FAULT_CHx] fault bits. Issue a *RESET_STATUS* command to clear the [SG_FAULT_CHx] fault bits.

The [SG_FAULT_CHx] channel-fault bits can be masked independently by [SG_MASK_CHx]. when the [SG_MASK_CHx] bit of any channel is set HIGH, the short-to-GND fault on the specific channel is not reported to [ANY_SHORT_FLAG].

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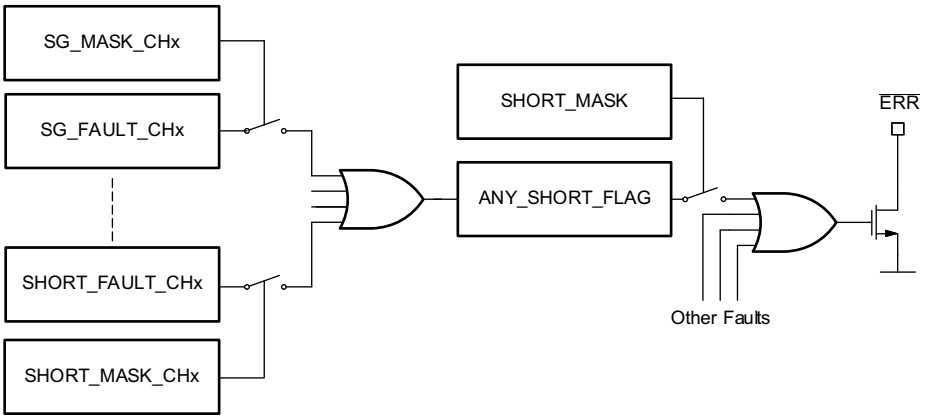

Figure 19. Short Fault Report Topology

7.3.5.4 LED Open-Load Detection

The device has independent LED open-load detection for each channel. If an LED open-load condition is detected, the [OPEN_FAULT_CHx] bit for the channel is set HIGH, and the [ANY_OPEN_FLAG] bit also is set HIGH. [ANY_OPEN_FLAG] also pulls down the $\overline{\text{ERR}}$ open-drain output.

An LED open-load fault does not disable the corresponding channel output. when a fault condition is removed, the LED should resume normal operation. Fault conditions are latched in the [OPEN_FAULT_CHx] fault bits. Issue a *RESET_STATUS* command to clear the [OPEN_FAULT_CHx] fault bits.

The [OPEN_FAULT_CHx] channel-fault bits can be masked independently by the [OPEN_MASK_CHx] bits. when the [OPEN_MASK_CHx] bit of any channel is set HIGH, the open-load fault on the specific channel is not reported to the [ANY_OPEN_FLAG] bit.

[ANY_OPEN_FLAG] is the indicator for open-load detectors. [ANY_OPEN_FLAG] can be masked by [OPEN_MASK] to avoid pulling down the $\overline{\text{ERR}}$ open-drain output.

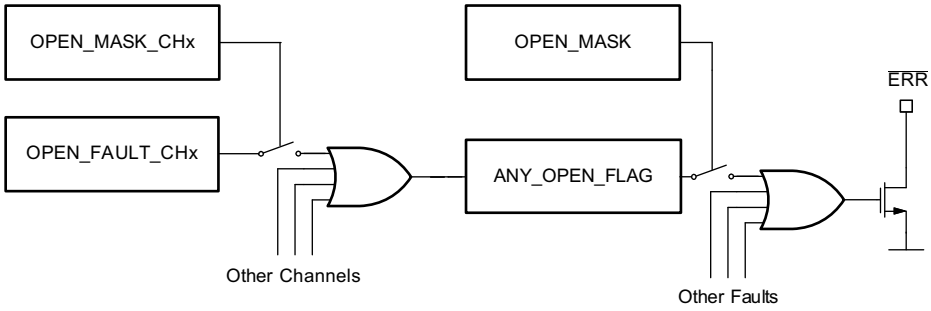

Figure 20. Open Fault Report Topology

7.3.5.5 Deactivated-Channel LED Open or Short Detection

Deactivating a channel by setting [CH_ON_MASKx] automatically enables detection of an off-state LED open load, short to the supply, or short to GND. If a fault is detected when the pullup is enabled, the respective fault register is set and the $\overline{\text{ERR}}$ open-drain output is pulled down.

To clear the fault, issue the *RESET_STATUS* command, the same as for activated-state diagnostics. The fault-masking mechanism is also the same as for activated-state diagnostics.

If an application allows absolutely no current during the channel disabled state, disable the off-state LED open-or-short detection feature using the [DIS_OFF_FAULT_DIAG] bit.

There is a provision for pulling each channel up to SENSE to avoid a floating node during off-state. This function can be enabled by setting the [DIS_PULL_UP_CHx] bit to HIGH. If any [DIS_PULL_UP_CHx] bit is set HIGH, the [DIS_PULL_UP_FLAG] bit is also set HIGH.

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7.3.5.6 Weak LED Supply (WLS) Detection

The TLC6C5712-Q1 device provides weak-LED-supply detection to avoid reporting false faults due to supply failure. Implementation of weak-LED-supply detection is by monitoring the $V_{(SENSE)}$ voltage using the internal threshold voltage $V_{(WLS)}$ as a reference.

The default threshold $V_{(WLS)}$ is set for a 5-V supply. If a 3.3-V LED supply is needed, the threshold voltage can be tuned to $V_{(WLS\_OPT)}$ by setting the [WLS_TH] bit HIGH.

when a fault is detected, the [WLS_FAULT_FLAG] bit is set if the [WLS_MASK] masking bit is not active. The [WLS_FAULT_FLAG] bit remains latched even if the voltage recovers. To clear the fault, issue the *RESET_STATUS* command.

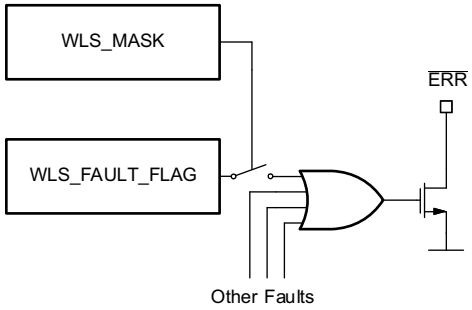

Figure 21. Weak-LED-Supply Fault-Report Topology

7.3.5.6.1 Adjacent-Pin Short Detection

On-demand adjacent-pin short detection is provided. This feature requires off-line diagnostics when the outputs are disabled. Otherwise, interruptions in normal operation and visual brightness glitches may result.

To start adjacent-pin short detection, set the [ADJ_DIAG_START] bit to HIGH. This bit automatically returns to LOW when the adjacent pin diagnostic procedure is finished.

After [ADJ_DIAG_START] has been set to HIGH and back to LOW, if any two adjacent pins are shorted, the [ADJ_FLAG_CHx] bit for the faulty channel is set HIGH. The microcontroller can read [ADJ_FLAG_CHx] to determine which two adjacent pins are shorted.

Deactivating all the channels by using the [CH_ON_MASKx] bits is suggested before starting adjacent-pin diagnostics.

when the [ADJ_FLAG_CHx] bit is set, it can only be cleared by issuing the *RESET_STATUS* command.

7.3.5.6.2 Force Error

To validate the $\overline{\text{ERR}}$ pulldown feedback without a real fault, the [FORCE_ERR] bit is provided to enable an $\overline{\text{ERR}}$ force-down to simulate a faulty scenario. When [FORCE_ERR] is HIGH, the $\overline{\text{ERR}}$ open-drain output is pulled down. To clear the fault, issue the *RESET_STATUS* command.

7.3.5.6.3 Reference Resistor Open and Short Detection

See the *Constant-Current Output* section.

7.3.5.6.4 PWM Monitor

See the *PWM Input* section.

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7.3.6 Register Protection

To avoid an unintended change of critical registers, register locking and unlocking functions are provided. when the registers are locked, they cannot be overwritten until an unlock command is issued. When the registers are locked, they are still available for reading. Critical registers include:

Dot correction register	<WRITE_CORRx>, x = 0–11
PWM mapping register	<WRITE_MAPx>, x = 0–5
Masking registers	<WRITE_CH_ON_MASK0> <WRITE_CH_ON_MASK1> <WRITE_SHORT_MASK0> <WRITE_SHORT_MASK1> <WRITE_SHORT_GND_MASK0> <WRITE_SHORT_GND_MASK1> <WRITE_OPEN_MASK0> <WRITE_OPEN_MASK1> <WRITE_PWM_FAULT_MASK> <WRITE_ERROR_MASK>
Miscellaneous register	<WRITE_MISC_CMD>

7.3.6.1 Dot Correction Register Lock and Unlock

The <WRITE_CORRx> dot correction register can be locked via the *LOCK_CORR*command. When it is locked, no data in the <WRITE_CORRx> registers can be altered. To unlock, issue the *UNLOCK_CORR* command.

7.3.6.2 PWM Mapping Register Lock and Unlock

The <WRITE_MAPx> dot correction register can be locked via the *LOCK_MAP* command. When it is locked, no data in the <WRITE_MAPx> registers can be altered. To unlock, issue the *UNLOCK_MAP* command.

7.3.6.3 Masking Register Lock and Unlock

Masking registers can be locked via *LOCK_MASK* command. When it is locked, no data in the masking registers listed in the *Register Protection* section can be altered. To unlock, issue the *UNLOCK_MASK* command.

7.3.6.4 Miscellaneous Register Lock and Unlock

Miscellaneous registers can be locked via the *LOCK_MISC* command. When it is locked, no data in the miscellaneous register listed in the *Register Protection* section can be altered. To unlock, issue the *UNLOCK_MISC* command.

7.3.6.5 Lock Flag Indication

The status of all lock registers is stored in the [LOCK_CORR_FLAG], [LOCK_MASK_FLAG], [LOCK_MAP_FLAG] and [LOCK_MISC_FLAG] bits of the <READ_STATUS1> register.

7.3.7 Serial Interface – SPI

The serial port is used to write data to, read diagnostic status from and configure settings of the TLC6C5712-Q1 device by transferring the input data to the desired address. During normal operation, an 8-bit serial address and 8-bit serial data are written into the 16-bit shift register. On an SCK rising-edge input, data is sampled. Data is shifted on a SCK falling edge and the shift registers advance, converting the 16 most-recent inputs to parallel signals on the LATCH rising edge.

At the rising edge on the LATCH input, a decoder which controls data transfer between shift and storage registers interprets the addresses. Depending on the address, valid data is conveyed from or to the appropriate latch or a command is interpreted. On latching a read address, data is read out from a storage register and shifted out of SDO to the microcontroller or daisy chained TLC6C5712-Q1 device.

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Because for each address the TLC6C5712-Q1 device shifts out a fixed amount of data at the end of a write-read cycle, it is possible to send different address codes to each IC in a daisy chain.

For a number N of daisy-chained devices, a communication cycle comprises 16 × N SCK cycles with the corresponding data, transferred from shift registers to latches or from latches to shift registers on the rising edge of LATCH. The falling edge of LATCH indicates the end of a communication cycle.

The TLC6C5712-Q1 device supports multiple devices in cascaded daisy-chain mode. Each communication sequence must only have one LATCH rising edge, and therefore cannot be split into multiple smaller sequences.

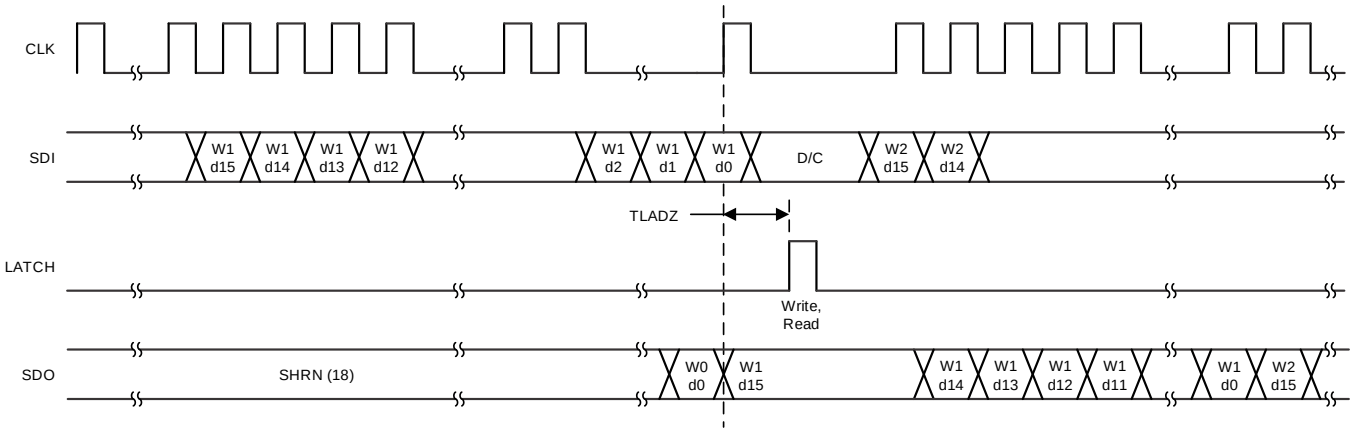

Figure 22. Write-Access Data for a Typical Use Case

7.3.8 Thermal Information

TLC6C5712-Q1 has internal thermal shutdown (TSD) protection from device overheating. For continuous operation, the junction temperature should not exceed thermal-shutdown threshold. If TSD is not disabled by register and junction temperature exceeds thermal shutdown threshold, all outputs are turned off for protection. When the junction temperature falls below the thermal threshold minus hysteresis, outputs resume.

Use Equation 4 to estimate the device power.

$$P_{D(tot)} = V_{CC} \times I_{CC} + \sum_{x=0}^{11} \left(V_{(OUTx)} \times I_{(OUTx)} \right) - \frac{V_{(IREF)}}{R_{(IREF)}^{2}} \quad (4)$$

where

- $P_{D(tot)}$ = Total power dissipation of the device
- $V_{(OUTx)}$ = Voltage drop for channel x
- $I_{(OUTx)}$ = Average LED current for channel x
- $V_{(IREF)}$ = Reference voltage
- $R_{(IREF)}$ = Reference resistor

7.4 Device Functional Modes

7.4.1 Operation With V_{CC} < 2.8 V (Power-On-Reset Threshold)

The TLC6C5712-Q1 device might not work properly with V_{CC} below 2.8 V. When POR is triggered, the device latches a POR fault and reports it through the $\overline{ERR}$ output. If V_{CC} continuous to drop, the content of the registers could be reset to their default value, with all outputs shutting down by default.

7.4.2 Operation With V_{CC} ≥ 2.8 V (Power-On-Reset Threshold)

The TLC6C5712-Q1 device is fully functional with V_{CC} at or above 2.8 V. The output current depends on the channel output voltage, $V_{(OUTx)}$. Given enough headroom for output transistors, the device should sink current as programmed. If the headroom voltage is not enough, the output current could be lower than programmed.

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7.5 Register Maps

Table 2. Register Map

Register Name	Addr	D7	D6	D5	D4	D3	D2	D1	D0	Default
WRITE_MAP0	40h	RESERVED		PWM_MAP_CH1[2:0]			PWM_MAP_CH0[2:0]			00h
WRITE_MAP1	41h	RESERVED		PWM_MAP_CH3[2:0]			PWM_MAP_CH2[2:0]			00h
WRITE_MAP2	42h	RESERVED		PWM_MAP_CH5[2:0]			PWM_MAP_CH4[2:0]			00h
WRITE_MAP3	43h	RESERVED		PWM_MAP_CH7[2:0]			PWM_MAP_CH6[2:0]			00h
WRITE_MAP4	44h	RESERVED		PWM_MAP_CH9[2:0]			PWM_MAP_CH8[2:0]			00h
WRITE_MAP5	45h	RESERVED		PWM_MAP_CH11[2:0]			PWM_MAP_CH10[2:0]			00h
WRITE_CORR0	46h	OUTPUT_DC_CH0[7:0]								00h
WRITE_CORR1	47h	OUTPUT_DC_CH1[7:0]								00h
WRITE_CORR2	48h	OUTPUT_DC_CH2[7:0]								00h
WRITE_CORR3	49h	OUTPUT_DC_CH3[7:0]								00h
WRITE_CORR4	4Ah	OUTPUT_DC_CH4[7:0]								00h
WRITE_CORR5	4Bh	OUTPUT_DC_CH5[7:0]								00h
WRITE_CORR6	4Ch	OUTPUT_DC_CH6[7:0]								00h
WRITE_CORR7	4Dh	OUTPUT_DC_CH7[7:0]								00h
WRITE_CORR8	4Eh	OUTPUT_DC_CH8[7:0]								00h
WRITE_CORR9	4Fh	OUTPUT_DC_CH9[7:0]								00h
WRITE_CORR10	50h	OUTPUT_DC_CH10[7:0]								00h
WRITE_CORR11	51h	OUTPUT_DC_CH11[7:0]								00h
WRITE_CH_ON_MASK0	52h	RESERVED		CH_ON_MASK5	CH_ON_MASK4	CH_ON_MASK3	CH_ON_MASK2	CH_ON_MASK1	CH_ON_MASK0	3Fh
WRITE_CH_ON_MASK1	53h	RESERVED		CH_ON_MASK11	CH_ON_MASK10	CH_ON_MASK9	CH_ON_MASK8	CH_ON_MASK7	CH_ON_MASK6	3Fh
WRITE_SHORT_MASK0	54h	RESERVED		SHORT_MASK_CH5	SHORT_MASK_CH4	SHORT_MASK_CH3	SHORT_MASK_CH2	SHORT_MASK_CH1	SHORT_MASK_CH0	3Fh
WRITE_SHORT_MASK1	55h	RESERVED		SHORT_MASK_CH11	SHORT_MASK_CH10	SHORT_MASK_CH9	SHORT_MASK_CH8	SHORT_MASK_CH7	SHORT_MASK_CH6	3Fh
WRITE_SHORT_GND_MASK0	56h	RESERVED		SG_MASK_CH5	SG_MASK_CH4	SG_MASK_CH3	SG_MASK_CH2	SG_MASK_CH1	SG_MASK_CH0	3Fh
WRITE_SHORT_GND_MASK1	57h	RESERVED		SG_MASK_CH11	SG_MASK_CH10	SG_MASK_CH9	SG_MASK_CH8	SG_MASK_CH7	SG_MASK_CH6	3Fh
WRITE_OPEN_MASK0	58h	RESERVED		OPEN_MASK_CH5	OPEN_MASK_CH4	OPEN_MASK_CH3	OPEN_MASK_CH2	OPEN_MASK_CH1	OPEN_MASK_CH0	3Fh
WRITE_OPEN_MASK1	59h	RESERVED		OPEN_MASK_CH11	OPEN_MASK_CH10	OPEN_MASK_CH9	OPEN_MASK_CH8	OPEN_MASK_CH7	OPEN_MASK_CH6	3Fh
—	5Ah–5Fh	RESERVED								00h
WRITE_PWM_FAULT_MASK	60h	RESERVED		PWM_FAULT_MASK5	PWM_FAULT_MASK4	PWM_FAULT_MASK3	PWM_FAULT_MASK2	PWM_FAULT_MASK1	PWM_FAULT_MASK0	3Fh
RESET_POR	61h	RESET_POR command is issued if data = 69h								00h
RESET_STATUS	62h	RESET_STATUS command is issued if data = 66h								00h
SOFTWARE_POR	63h	SOFTWARE_POR command is issued if data = 99h								00h
WRITE_DIS_PULL_UP_0	64h	RESERVED		DIS_PULL_UP_CH5	DIS_PULL_UP_CH4	DIS_PULL_UP_CH3	DIS_PULL_UP_CH2	DIS_PULL_UP_CH1	DIS_PULL_UP_CH0	00h
WRITE_DIS_PULL_UP_1	65h	RESERVED		DIS_PULL_UP_CH11	DIS_PULL_UP_CH10	DIS_PULL_UP_CH9	DIS_PULL_UP_CH8	DIS_PULL_UP_CH7	DIS_PULL_UP_CH6	00h
WRITE_ERROR_MASK	66h	REF_MASK	POR_MASK	OPEN_MASK	SHORT_MASK	PWM_MASK	WLS_MASK	PRE_TSD_MASK	TSD_MASK	00h
WRITE_MISC_CMD	67h	RESERVED			DIS_OFF_FAULT_DI AG	ADJ_DIAG_START	SLOW_SLEW_RAT E	FORCE_ERR	WLS_TH	00h
LOCK_MAP	68h	LOCK_MAP command is issued if data = A5h								00h
LOCK_CORR	69h	LOCK_CORR command is issued if data = 55h								00h

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Register Maps (continued)

Table 2. Register Map (continued)

Register Name	Addr	D7	D6	D5	D4	D3	D2	D1	D0	Default
LOCK_MASK	6Ah	LOCK_MASK command is issued if data = AAh								00h
LOCK_MISC	6Bh	UNLOCK_MISC command is issued if data = 5Ah								00h
UNLOCK_MAP	6Ch	UNLOCK_MAP command is issued if data = CCh								00h
UNLOCK_CORR	6Dh	UNLOCK_CORR command is issued if data = 33h								00h
UNLOCK_MASK	6Eh	UNLOCK_MASK command is issued if data = 3Ch								00h
UNLOCK_MISC	6Fh	UNLOCK_MISC command is issued if data = C3h								00h
—	70h–7Fh	RESERVED								00h
READ_MAP0	80h	RESERVED		PWM_MAP_CH1[2:0]			PWM_MAP_CH0[2:0]			00h
READ_MAP1	81h	RESERVED		PWM_MAP_CH3[2:0]			PWM_MAP_CH2[2:0]			00h
READ_MAP2	82h	RESERVED		PWM_MAP_CH5[2:0]			PWM_MAP_CH4[2:0]			00h
READ_MAP3	83h	RESERVED		PWM_MAP_CH7[2:0]			PWM_MAP_CH6[2:0]			00h
READ_MAP4	84h	RESERVED		PWM_MAP_CH9[2:0]			PWM_MAP_CH8[2:0]			00h
READ_MAP5	85h	RESERVED		PWM_MAP_CH11[2:0]			PWM_MAP_CH10[2:0]			00h
READ_CORR0	86h	OUTPUT_DC_CH0[7:0]								00h
READ_CORR1	87h	OUTPUT_DC_CH1[7:0]								00h
READ_CORR2	88h	OUTPUT_DC_CH2[7:0]								00h
READ_CORR3	89h	OUTPUT_DC_CH3[7:0]								00h
READ_CORR4	8Ah	OUTPUT_DC_CH4[7:0]								00h
READ_CORR5	8Bh	OUTPUT_DC_CH5[7:0]								00h
READ_CORR6	8Ch	OUTPUT_DC_CH6[7:0]								00h
READ_CORR7	8Dh	OUTPUT_DC_CH7[7:0]								00h
READ_CORR8	8Eh	OUTPUT_DC_CH8[7:0]								00h
READ_CORR9	8Fh	OUTPUT_DC_CH9[7:0]								00h
READ_CORR10	90h	OUTPUT_DC_CH10[7:0]								00h
READ_CORR11	91h	OUTPUT_DC_CH11[7:0]								00h
READ_CH_ON_MASK0	92h	RESERVED		CH_ON_MASK5	CH_ON_MASK4	CH_ON_MASK3	CH_ON_MASK2	CH_ON_MASK1	CH_ON_MASK0	3Fh
READ_CH_ON_MASK1	93h	RESERVED		CH_ON_MASK11	CH_ON_MASK10	CH_ON_MASK9	CH_ON_MASK8	CH_ON_MASK7	CH_ON_MASK6	3Fh
READ_SHORT_MASK0	94h	RESERVED		SHORT_MASK_CH5	SHORT_MASK_CH4	SHORT_MASK_CH3	SHORT_MASK_CH2	SHORT_MASK_CH1	SHORT_MASK_CH0	3Fh
READ_SHORT_MASK1	95h	RESERVED		SHORT_MASK_CH11	SHORT_MASK_CH10	SHORT_MASK_CH9	SHORT_MASK_CH8	SHORT_MASK_CH7	SHORT_MASK_CH6	3Fh
READ_SHORT_GND_MASK0	96h	RESERVED		SG_MASK_CH5	SG_MASK_CH4	SG_MASK_CH6	SG_MASK_CH5	SG_MASK_CH7	SG_MASK_CH6	3Fh
READ_SHORT_GND_MASK1	97h	RESERVED		SG_MASK_CH11	SG_MASK_CH10	SG_MASK_CH9	SG_MASK_CH8	SG_MASK_CH7	SG_MASK_CH6	3Fh
READ_OPEN_MASK0	98h	RESERVED		OPEN_MASK_CH5	OPEN_MASK_CH4	OPEN_MASK_CH3	OPEN_MASK_CH2	OPEN_MASK_CH1	OPEN_MASK_CH0	3Fh
READ_OPEN_MASK1	99h	RESERVED		OPEN_MASK_CH11	OPEN_MASK_CH10	OPEN_MASK_CH9	OPEN_MASK_CH8	OPEN_MASK_CH7	OPEN_MASK_C H6	3Fh
READ_SHORT_FAULT0	9Ah	RESERVED		SHORT_FAULT_CH5	SHORT_FAULT_CH4	SHORT_FAULT_CH3	SHORT_FAULT_CH2	SHORT_FAULT_CH1	SHORT_FAULT_CH0	00h
READ_SHORT_FAULT1	9Bh	RESERVED		SHORT_FAULT_CH11	SHORT_FAULT_CH10	SHORT_FAULT_CH9	SHORT_FAULT_CH8	SHORT_FAULT_CH7	SHORT_FAULT_CH6	00h
READ_SHORT_GND_FAULT0	9Ch	RESERVED		SG_FAULT_CH5	SG_FAULT_CH4	SG_FAULT_CH3	SG_FAULT_CH2	SG_FAULT_CH1	SG_FAULT_CH0	00h
READ_SHORT_GND_FAULT1	9Dh	RESERVED		SG_FAULT_CH11	SG_FAULT_CH10	SG_FAULT_CH9	SG_FAULT_CH8	SG_FAULT_CH7	SG_FAULT_CH6	00h
READ_OPEN_FAULT0	9Eh	RESERVED		OPEN_FAULT_CH5	OPEN_FAULT_CH4	OPEN_FAULT_CH3	OPEN_FAULT_CH2	OPEN_FAULT_CH1	OPEN_FAULT_CH0	00h

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Register Maps (continued)

Table 2. Register Map (continued)

Register Name	Addr	D7	D6	D5	D4	D3	D2	D1	D0	Default
READ_OPEN_FAULT1	9Fh	RESERVED		OPEN_FAULT_CH11	OPEN_FAULT_CH10	OPEN_FAULT_CH9	OPEN_FAULT_CH8	OPEN_FAULT_CH7	OPEN_FAULT_CH6	00h
READ_PWM_FAULT_MASK	A0h	RESERVED		PWM_FAULT_MASK5	PWM_FAULT_MASK4	PWM_FAULT_MASK3	PWM_FAULT_MASK2	PWM_FAULT_MASK1	PWM_FAULT_MASK0	3Fh
READ_PWM_FAULT	A1h	RESERVED		FAULT_PWM5	FAULT_PWM4	FAULT_PWM3	FAULT_PWM2	FAULT_PWM1	FAULT_PWM0	00h
READ_STATUS0	A2h	REF_FAULT_ FLAG	POR_ERR_ FLAG	ANY_OPEN_FLAG	ANY_SHORT_FLAG	ANY_PWM_ FAULT_FLAG	WLS_FAULT_FLAG	PRE_TSD_FLAG	TSD_FLAG	40h
READ_STATUS1	A3h	RESERVED			DIS_PULL_UP_FLAG	LOCK_MISC_FLAG	LOCK_MAP_FLAG	LOCK_MASK_FLAG	LOCK_CORR_FLAG	00h
READ_DIS_PULL_UP0	A4h	RESERVED		DIS_PULL_UP_CH5	DIS_PULL_UP_CH4	DIS_PULL_UP_CH3	DIS_PULL_UP_CH2	DIS_PULL_UP_C H1	DIS_PULL_UP_CH0	00h
READ_DIS_PULL_UP1	A5h	RESERVED		DIS_PULL_UP_CH11	DIS_PULL_UP_CH10	DIS_PULL_UP_CH9	DIS_PULL_UP_CH8	DIS_PULL_UP_C H7	DIS_PULL_UP_CH6	00h
READ_ERROR_MASK	A6h	REF_MASK	POR_MASK	OPEN_MASK	SHORT_MASK	PWM_MASK	WLS_MASK	PRE_TSD_MASK	TSD_MASK	00h
READ_MISC_CMD	A7h	RESERVED			DIS_OFF_FAULT_ DIAG	ADJ_DIAG_START	SLOW_SLEW_RATE	FORCE_ERR	WLS_TH	00h
READ_ADSHORT0	A8h	RESERVED		AD_FLAG_CH5	AD_FLAG_CH4	AD_FLAG_CH3	AD_FLAG_CH2	AD_FLAG_CH1	AD_FLAG_CH0	00h
READ_ADSHORT1	A9h	RESERVED		AD_FLAG_CH11	AD_FLAG_CH10	AD_FLAG_CH9	AD_FLAG_CH8	AD_FLAG_CH7	AD_FLAG_CH6	00h

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7.5.1 WRITE_MAP0 Register (address = 40h) [reset = 00h]

Figure 23. WRITE_MAP0 Register, Address 40h

7	6	5	4	3	2	1	0
RESERVED		PWM_MAP_CH1[2:0]			PWM_MAP_CH0[2:0]		
R		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. WRITE_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5–3	PWM_MAP_CH1	R/W	0h	Select PWM mapping for channel 1
2–0	PWM_MAP_CH0	R/W	0h	Select PWM mapping for channel 0

7.5.2 WRITE_MAP1 Register (address = 41h) [reset = 00h]

Figure 24. WRITE_MAP1 Register, Address 41h

7	6	5	4	3	2	1	0
RESERVED		PWM_MAP_CH3[2:0]			PWM_MAP_CH2[2:0]		
R		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. WRITE_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5–3	PWM_MAP_CH3	R/W	0h	Select PWM mapping for channel 3
2–0	PWM_MAP_CH2	R/W	0h	Select PWM mapping for channel 2

7.5.3 WRITE_MAP2 Register (address = 42h) [reset = 00h]

Figure 25. WRITE_MAP2 Register, Address 42h

7	6	5	4	3	2	1	0
RESERVED		PWM_MAP_CH5[2:0]			PWM_MAP_CH4[2:0]		
R		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. WRITE_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5–3	PWM_MAP_CH5	R/W	0h	Select PWM mapping for channel 5
2–0	PWM_MAP_CH4	R/W	0h	Select PWM mapping for channel 4

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7.5.4 WRITE_MAP3 Register (address = 43h) [reset = 00h]

Figure 26. WRITE_MAP3 Register, Address 43h

7	6	5	4	3	2	1	0
RESERVED		PWM_MAP_CH7[2:0]			PWM_MAP_CH6[2:0]		
R		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. WRITE_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5–3	PWM_MAP_CH7	R/W	0h	Select PWM mapping for channel 7
2–0	PWM_MAP_CH6	R/W	0h	Select PWM mapping for channel 6

7.5.5 WRITE_MAP4 Register (address = 44h) [reset = 00h]

Figure 27. WRITE_MAP4 Register, Address 44h

7	6	5	4	3	2	1	0
RESERVED		PWM_MAP_CH9[2:0]			PWM_MAP_CH8[2:0]		
R		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. WRITE_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5–3	PWM_MAP_CH9	R/W	0h	Select PWM mapping for channel 9
2–0	PWM_MAP_CH8	R/W	0h	Select PWM mapping for channel 8

7.5.6 WRITE_MAP5 Register (address = 45h) [reset = 00h]

Figure 28. WRITE_MAP5 Register, Address 45h

7	6	5	4	3	2	1	0
RESERVED		PWM_MAP_CH11[2:0]			PWM_MAP_CH10[2:0]		
R		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. WRITE_MAP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5–3	PWM_MAP_CH11	R/W	0h	Select PWM mapping for channel 11
2–0	PWM_MAP_CH10	R/W	0h	Select PWM mapping for channel 10

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7.5.7 WRITE_CORR0 Register (address = 46h) [reset = 00h]

Figure 29. WRITE_CORR0 Register, Address 46h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH0[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. WRITE_CORR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH0	R/W	00h	Dot correction register for channel 0

7.5.8 WRITE_CORR1 Register (address = 47h) [reset = 00h]

Figure 30. WRITE_CORR1 Register, Address 47h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH1[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. WRITE_CORR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH1	R/W	00h	Dot correction register for channel 1

7.5.9 WRITE_CORR2 Register (address = 48h) [reset = 00h]

Figure 31. WRITE_CORR2 Register, Address 48h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH2[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. WRITE_CORR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH2	R/W	00h	Dot correction register for channel 2

7.5.10 WRITE_CORR3 Register (address = 49h) [reset = 00h]

Figure 32. WRITE_CORR3 Register, Address 49h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH3[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. WRITE_CORR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH3	R/W	00h	Dot correction register for channel 3

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7.5.11 WRITE_CORR4 Register (address = 4Ah) [reset = 00h]

Figure 33. WRITE_CORR4 Register, Address 4Ah

7	6	5	4	3	2	1	0
OUTPUT_DC_CH4[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. WRITE_CORR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH4	R/W	00h	Dot correction register for channel 4

7.5.12 WRITE_CORR5 Register (address = 4Bh) [reset = 00h]

Figure 34. WRITE_CORR5 Register, Address 4Bh

7	6	5	4	3	2	1	0
OUTPUT_DC_CH5[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. WRITE_CORR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH5	R/W	00h	Dot correction register for channel 5

7.5.13 WRITE_CORR6 Register (address = 4Ch) [reset = 00h]

Figure 35. WRITE_CORR6 Register, Address 4Ch

7	6	5	4	3	2	1	0
OUTPUT_DC_CH6[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. WRITE_CORR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH6	R/W	00h	Dot correction register for channel 6

7.5.14 WRITE_CORR7 Register (address = 4Dh) [reset = 00h]

Figure 36. WRITE_CORR7 Register, Address 4Dh

7	6	5	4	3	2	1	0
OUTPUT_DC_CH7[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. WRITE_CORR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH7	R/W	00h	Dot correction register for channel 7

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7.5.15 WRITE_CORR8 Register (address = 4Eh) [reset = 00h]

Figure 37. WRITE_CORR8 Register, Address 4Eh

7	6	5	4	3	2	1	0
OUTPUT_DC_CH8[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. WRITE_CORR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH8	R/W	00h	Dot correction register for channel 8

7.5.16 WRITE_CORR9 Register (address = 4Fh) [reset = 00h]

Figure 38. WRITE_CORR9 Register, Address 4Fh

7	6	5	4	3	2	1	0
OUTPUT_DC_CH9[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. WRITE_CORR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH9	R/W	00h	Dot correction register for channel 9

7.5.17 WRITE_CORR10 Register (address = 50h) [reset = 00h]

Figure 39. WRITE_CORR10 Register, Address 50h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH10[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. WRITE_CORR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH10	R/W	00h	Dot correction register for channel 10

7.5.18 WRITE_CORR11 Register (address = 51h) [reset = 00h]

Figure 40. WRITE_CORR11 Register, Address 51h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH11[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. WRITE_CORR11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUTPUT_DC_CH11	R/W	00h	Dot correction register for channel 11

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7.5.19 WRITE_CH_ON_MASK0 Register (address = 52h) [reset = 3Fh]

Figure 41. WRITE_CH_ON_MASK0, Address 52h

7	6	5	4	3	2	1	0
RESERVED		CH_ON_MASK 5	CH_ON_MASK 4	CH_ON_MASK 3	CH_ON_MASK 2	CH_ON_MASK 1	CH_ON_MASK 0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. WRITE_CH_ON_MASK0 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	CH_ON_MASK5	R/W	1h	Channel-activate mask register for channel 5. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
4	CH_ON_MASK4	R/W	1h	Channel-activate mask register for channel 4. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
3	CH_ON_MASK3	R/W	1h	Channel-activate mask register for channel 3. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
2	CH_ON_MASK2	R/W	1h	Channel-activate mask register for channel 2. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
1	CH_ON_MASK1	R/W	1h	Channel-activate mask register for channel 1. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
0	CH_ON_MASK0	R/W	1h	Channel-activate mask register for channel 0. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated

7.5.20 WRITE_CH_ON_MASK1 Register (address = 53h) [reset = 3Fh]

Figure 42. WRITE_CH_ON_MASK1, Address 53h

7	6	5	4	3	2	1	0
RESERVED		CH_ON_MASK 11	CH_ON_MASK 10	CH_ON_MASK 9	CH_ON_MASK 8	CH_ON_MASK 7	CH_ON_MASK 6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. WRITE_CH_ON_MASK1 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	CH_ON_MASK11	R/W	1h	Channel-activate mask register for channel 11. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
4	CH_ON_MASK10	R/W	1h	Channel-activate mask register for channel 10. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
3	CH_ON_MASK9	R/W	1h	Channel-activate mask register for channel 9. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
2	CH_ON_MASK8	R/W	1h	Channel-activate mask register for channel 8. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
1	CH_ON_MASK7	R/W	1h	Channel-activate mask register for channel 7. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated
0	CH_ON_MASK6	R/W	1h	Channel-activate mask register for channel 6. Active-low. HIGH: Channel output deactivated. LOW: Channel output activated

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7.5.21 WRITE_SHORT_MASK0 Register (address = 54h) [reset = 3Fh]

Figure 43. SLVSCO9WRITE_SHORT_MASK0, Address 54h

7	6	5	4	3	2	1	0
RESERVED		SHORT_MASK_CH5	SHORT_MASK_CH4	SHORT_MASK_CH3	SHORT_MASK_CH2	SHORT_MASK_CH1	SHORT_MASK_CH0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. WRITE_SHORT_MASK0 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	SHORT_MASK_CH5	R/W	1h	Short-to-supply fault mask register for channel 5. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
4	SHORT_MASK_CH4	R/W	1h	Short-to-supply fault mask register for channel 4. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
3	SHORT_MASK_CH3	R/W	1h	Short-to-supply fault mask register for channel 3. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
2	SHORT_MASK_CH2	R/W	1h	Short-to-supply fault mask register for channel 2. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
1	SHORT_MASK_CH1	R/W	1h	Short-to-supply fault mask register for channel 1. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
0	SHORT_MASK_CH0	R/W	1h	Short-to-supply fault mask register for channel 0. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked

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7.5.22 WRITE_SHORT_MASK1 Register (address = 55h) [reset = 3Fh]

Figure 44. WRITE_SHORT_MASK1, Address 55h

7	6	5	4	3	2	1	0
RESERVED		SHORT_MASK_CH11	SHORT_MASK_CH10	SHORT_MASK_CH9	SHORT_MASK_CH8	SHORT_MASK_CH7	SHORT_MASK_CH6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. WRITE_SHORT_MASK1 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	SHORT_MASK_CH11	R/W	1h	Short-to-supply fault mask register for channel 11. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
4	SHORT_MASK_CH10	R/W	1h	Short-to-supply fault mask register for channel 10. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
3	SHORT_MASK_CH9	R/W	1h	Short-to-supply fault mask register for channel 9. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
2	SHORT_MASK_CH8	R/W	1h	Short-to-supply fault mask register for channel 8. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
1	SHORT_MASK_CH7	R/W	1h	Short-to-supply fault mask register for channel 7. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked
0	SHORT_MASK_CH6	R/W	1h	Short-to-supply fault mask register for channel 6. Active-high. HIGH: Short-to-supply fault masked. LOW: Short-to-supply fault not masked

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7.5.23 WRITE_SHORT_GND_MASK0 Register (address = 56h) [reset = 3Fh]

Figure 45. WRITE_SHORT_GND_MASK0, Address 56h

7	6	5	4	3	2	1	0
RESERVED		SG_MASK_CH5	SG_MASK_CH4	SG_MASK_CH3	SG_MASK_CH2	SG_MASK_CH1	SG_MASK_CH0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. WRITE_SHORT_GND_MASK0 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	SG_MASK_CH5	R/W	1h	Short-to-GND fault mask register for channel 5. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
4	SG_MASK_CH4	R/W	1h	Short-to-GND fault mask register for channel 4. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
3	SG_MASK_CH3	R/W	1h	Short-to-GND fault mask register for channel 3. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
2	SG_MASK_CH2	R/W	1h	Short-to-GND fault mask register for channel 2. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
1	SG_MASK_CH1	R/W	1h	Short-to-GND fault mask register for channel 1. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
0	SG_MASK_CH0	R/W	1h	Short-to-GND fault mask register for channel 0. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked

7.5.24 WRITE_SHORT_GND_MASK1 Register (address = 57h) [reset = 3Fh]

Figure 46. WRITE_SHORT_GND_MASK1, Address 57h

7	6	5	4	3	2	1	0
RESERVED		SG_MASK_CH11	SG_MASK_CH10	SG_MASK_CH9	SG_MASK_CH8	SG_MASK_CH7	SG_MASK_CH6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. WRITE_SHORT_GND_MASK1 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	SG_MASK_CH11	R/W	1h	Short-to-GND fault mask register for channel 11. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
4	SG_MASK_CH10	R/W	1h	Short-to-GND fault mask register for channel 10. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
3	SG_MASK_CH9	R/W	1h	Short-to-GND fault mask register for channel 9. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
2	SG_MASK_CH8	R/W	1h	Short-to-GND fault mask register for channel 8. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
1	SG_MASK_CH7	R/W	1h	Short-to-GND fault mask register for channel 7. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked
0	SG_MASK_CH6	R/W	1h	Short-to-GND fault mask register for channel 6. Active-high. HIGH: Short-to-GND fault masked. LOW: Short-to-GND fault not masked

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7.5.25 WRITE_OPEN_MASK0 Register (address = 58h) [reset = 3Fh]

Figure 47. WRITE_OPEN_MASK0, Address 58h

7	6	5	4	3	2	1	0
RESERVED		OPEN_MASK_CH5	OPEN_MASK_CH4	OPEN_MASK_CH3	OPEN_MASK_CH2	OPEN_MASK_CH1	OPEN_MASK_CH0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. WRITE_OPEN_MASK0 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	OPEN_MASK_CH5	R/W	1h	Open-fault mask register for channel 5. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
4	OPEN_MASK_CH4	R/W	1h	Open-fault mask register for channel 4. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
3	OPEN_MASK_CH3	R/W	1h	Open-fault mask register for channel 3. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
2	OPEN_MASK_CH2	R/W	1h	Open-fault mask register for channel 2. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
1	OPEN_MASK_CH1	R/W	1h	Open-fault mask register for channel 1. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
0	OPEN_MASK_CH0	R/W	1h	Open-fault mask register for channel 0. Active-high. HIGH: Open fault masked. LOW: Open fault not masked

7.5.26 WRITE_OPEN_MASK1 Register (address = 59h) [reset = 3Fh]

Figure 48. WRITE_OPEN_MASK1, Address 59h

7	6	5	4	3	2	1	0
RESERVED		OPEN_MASK_CH11	OPEN_MASK_CH10	OPEN_MASK_CH9	OPEN_MASK_CH8	OPEN_MASK_CH7	OPEN_MASK_CH6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. WRITE_OPEN_MASK1 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	OPEN_MASK_CH11	R/W	1h	Open-fault mask register for channel 11. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
4	OPEN_MASK_CH10	R/W	1h	Open-fault mask register for channel 10. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
3	OPEN_MASK_CH9	R/W	1h	Open-fault mask register for channel 9. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
2	OPEN_MASK_CH8	R/W	1h	Open-fault mask register for channel 8. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
1	OPEN_MASK_CH7	R/W	1h	Open-fault mask register for channel 7. Active-high. HIGH: Open fault masked. LOW: Open fault not masked
0	OPEN_MASK_CH6	R/W	1h	Open-fault mask register for channel 6. Active-high. HIGH: Open fault masked. LOW: Open fault not masked

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7.5.27 WRITE_PWM_FAULT_MASK Register (address = 60h) [reset = 3Fh]

Figure 49. WRITE_PWM_FAULT_MASK Register, Address 60h

7	6	5	4	3	2	1	0
RESERVED		PWM_FAULT_MASK5	PWM_FAULT_MASK4	PWM_FAULT_MASK3	PWM_FAULT_MASK2	PWM_FAULT_MASK1	PWM_FAULT_MASK0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. WRITE_PWM_FAULT_MASK Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	PWM_FAULT_MASK5	R/W	1h	PWM-fault mask register for input PWM channel 5. Active-high. HIGH: PWM fault masked. LOW: PWM fault not masked
4	PWM_FAULT_MASK4	R/W	1h	PWM-fault mask register for input PWM channel 4. Active-high. HIGH: PWM fault masked. LOW: PWM fault not masked
3	PWM_FAULT_MASK3	R/W	1h	PWM-fault mask register for input PWM channel 3. Active-high. HIGH: PWM fault masked. LOW: PWM fault not masked
2	PWM_FAULT_MASK2	R/W	1h	PWM-fault mask register for input PWM channel 2. Active-high. HIGH: PWM fault masked. LOW: PWM fault not masked
1	PWM_FAULT_MASK1	R/W	1h	PWM-fault mask register for input PWM channel 1. Active-high. HIGH: PWM fault masked. LOW: PWM fault not masked
0	PWM_FAULT_MASK0	R/W	1h	PWM-fault mask register for input PWM channel 0. Active-high. HIGH: PWM fault masked. LOW: PWM fault not masked

7.5.28 RESET_POR Register (address = 61h) [reset = 00h]

Figure 50. RESET_POR Register, Address 61h

7	6	5	4	3	2	1	0
RESET_POR							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 30. RESET_POR Field Descriptions

Bit	Field	Type	Reset	Description
7–0	RESET_POR	W	00h	A *RESET_POR* command is issued if the register content = 69h. The register content is automatically cleared.

7.5.29 RESET_STATUS Register (address = 62h) [reset = 00h]

Figure 51. RESET_STATUS Register, Address 62h

7	6	5	4	3	2	1	0
RESET_STATUS							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 31. RESET_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7–0	RESET_STATUS	W	00h	A *RESET_STATUS* command is issued if the register content = 66h. The register content is automatically cleared.

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7.5.30 SOFTWARE_POR Register (address = 63h) [reset = 00h]

Figure 52. SOFTWARE_POR Register, Address 63h

7	6	5	4	3	2	1	0
SOFTWARE_POR							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 32. SOFTWARE_POR Field Descriptions

Bit	Field	Type	Reset	Description
7–0	SOFTWARE_POR	W	00h	A *SOFTWARE_POR* command is issued if the register content = 99h. The register content is automatically cleared.

7.5.31 WRITE_DIS_PULL_UP_0 Register (address = 64h) [reset = 00h]

Figure 53. WRITE_DIS_PULL_UP_0 Register, Address 64h

7	6	5	4	3	2	1	0
RESERVED		DIS_PULL_UP_CH5	DIS_PULL_UP_CH4	DIS_PULL_UP_CH3	DIS_PULL_UP_CH2	DIS_PULL_UP_CH1	DIS_PULL_UP_CH0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. WRITE_DIS_PULL_UP_0 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	DIS_PULL_UP_CH5	R/W	0h	Disable deactivated-channel internal pullup register for channel 5. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
4	DIS_PULL_UP_CH4	R/W	0h	Disable deactivated-channel internal pullup register for channel 4. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
3	DIS_PULL_UP_CH3	R/W	0h	Disable deactivated-channel internal pullup register for channel 3. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
2	DIS_PULL_UP_CH2	R/W	0h	Disable deactivated-channel internal pullup register for channel 2. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
1	DIS_PULL_UP_CH1	R/W	0h	Disable deactivated-channel internal pullup register for channel 1. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
0	DIS_PULL_UP_CH0	R/W	0h	Disable deactivated-channel internal pullup register for channel 0. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.

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7.5.32 WRITE_DIS_PULL_UP_1 Register (address = 65h) [reset = 00h]

Figure 54. WRITE_DIS_PULL_UP_1 Register, Address 65h

7	6	5	4	3	2	1	0
RESERVED		DIS_PULL_UP_CH11	DIS_PULL_UP_CH10	DIS_PULL_UP_CH9	DIS_PULL_UP_CH8	DIS_PULL_UP_CH7	DIS_PULL_UP_CH6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. WRITE_DIS_PULL_UP_1 Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	DIS_PULL_UP_CH11	R/W	0h	Disable deactivated-channel internal pullup register for channel 11. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
4	DIS_PULL_UP_CH10	R/W	0h	Disable deactivated-channel internal pullup register for channel 10. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
3	DIS_PULL_UP_CH9	R/W	0h	Disable deactivated-channel internal pullup register for channel 9. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
2	DIS_PULL_UP_CH8	R/W	0h	Disable deactivated-channel internal pullup register for channel 8. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
1	DIS_PULL_UP_CH7	R/W	0h	Disable deactivated-channel internal pullup register for channel 7. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.
0	DIS_PULL_UP_CH6	R/W	0h	Disable deactivated-channel internal pullup register for channel 6. Active-high. HIGH: internal pullup disabled; LOW: internal pullup enabled.

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7.5.33 WRITE_ERROR_MASK Register (address = 66h) [reset = 00h]

Figure 55. WRITE_ERROR_MASK Register, Address 66h

7	6	5	4	3	2	1	0
REF_MASK	POR_MASK	OPEN_MASK	SHORT_MASK	PWM_MASK	WLS_MASK	PRE_TSD_MASK	TSD_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. WRITE_ERROR_MASK Field Descriptions

Bit	Field	Type	Reset	Description
7	REF_MASK	R/W	0h	Reference fault mask bit. Active-high. HIGH: Reference fault is masked; LOW: Reference fault is not masked.
6	POR_MASK	R/W	0h	Power-on-reset fault mask bit Active-high. HIGH: POR fault is masked; LOW: POR fault is not masked.
5	OPEN_MASK	R/W	0h	Open fault mask bit. Active-high. HIGH: Open fault is masked; LOW: Open fault is not masked.
4	SHORT_MASK	R/W	0h	Short fault mask bit. Active-high. HIGH: Short fault is masked; LOW: Short fault is not masked.
3	PWM_MASK	R/W	0h	PWM fault mask bit. Active-high. HIGH: PWM fault is masked; LOW: PWM fault is not masked.
2	WLS_MASK	R/W	0h	Weak-LED-supply (WLS) fault mask bit. Active-high. HIGH: WLS fault is masked; LOW: WLS fault is not masked.
1	PRE_TSD_MASK	R/W	0h	Pre-thermal-warning fault mask bit. Active-high. HIGH: PRE_TSD fault is masked; LOW: PRE_TSD fault is not masked.
0	TSD_MASK	R/W	0h	Thermal-shutdown fault mask bit. Active-high. HIGH: TSD fault is masked; LOW: TSD fault is not masked.

7.5.34 WRITE_MISC_CMD Register (address = 67h) [reset = 00h]

Figure 56. WRITE_MISC_CMD Register, Address 67h

7	6	5	4	3	2	1	0
RESERVED			DIS_OFF_FAULT_DIAG	ADJ_DIAG_START	SLOW_SLEW_RATE	FORCE_ERR	WLS_TH
R			R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. WRITE_MISC_CMD Field Descriptions

Bit	Field	Type	Reset	Description
7–5	RESERVED	R	0h	
4	DIS_OFF_FAULT_DIAG	R/W	0h	Off-state output fault diagnostics control bit. Active-high. HIGH: Off-state fault diagnostics disabled; LOW: Off-state fault diagnostics enabled
3	ADJ_DIAG_START	R/W	0h	Adjacent-pin diagnostics start control bit. Active-high, returns low when adjacent-pin diagnostic procedure is concluded. HIGH: Start adjacent-pin diagnostics or adjacent-pin diagnostics are ongoing; LOW: Adjacent-pin diagnostics are not running.
2	SLOW_SLEW_RATE	R/W	0h	Slow slew rate control bit. Active-high. HIGH: Output-current slew rate is in slow mode. LOW: Output-current slew rate is in normal mode.
1	FORCE_ERR	R/W	0h	Force error control bit. Active-high. HIGH: ERR output is forced low. LOW: ERR output is not forced low.
0	WLS_TH	R/W	0h	Weak-LED-supply threshold-control bit. Active-high. HIGH: WLS threshold is set to 3.3-V mode. LOW: WLS threshold is set to 5-V mode.

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7.5.35 LOCK_MAP Register (address = 68h) [reset = 00h]

Figure 57. LOCK_MAP Register, Address 68h

7	6	5	4	3	2	1	0
LOCK_MAP							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 37. LOCK_MAP Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LOCK_MAP	W	00h	A *LOCK_MAP* command is issued if the register content = A5h. The register content is automatically cleared.

7.5.36 LOCK_CORR Register (address = 69h) [reset = 00h]

Figure 58. LOCK_CORR Register, Address 69h

7	6	5	4	3	2	1	0
LOCK_CORR							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 38. LOCK_CORR Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LOCK_CORR	W	00h	A *LOCK_CORR* command is issued if the register content = 55h. The register content is automatically cleared.

7.5.37 LOCK_MASK Register (address = 6Ah) [reset = 00h]

Figure 59. LOCK_MASK Register, Address 6Ah

7	6	5	4	3	2	1	0
LOCK_MASK							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 39. LOCK_MASK Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LOCK_MASK	W	00h	A *LOCK_MASK* command is issued if the register content = AAh. The register content is automatically cleared.

7.5.38 LOCK_MISC Register (address = 6Bh) [reset = 00h]

Figure 60. LOCK_MISC Register, Address 6Bh

7	6	5	4	3	2	1	0
LOCK_MISC							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 40. LOCK_MISC Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LOCK_MISC	W	00h	A *LOCK_MISC* command is issued if the register content = 5Ah. The register content is automatically cleared.

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7.5.39 UNLOCK_MAP Register (address = 6Ch) [reset = 00h]

Figure 61. UNLOCK_MAP Register, Address 6Ch

7	6	5	4	3	2	1	0
UNLOCK_MAP							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 41. UNLOCK_MAP Field Descriptions

Bit	Field	Type	Reset	Description
7–0	UNLOCK_MAP	W	00h	An *UNLOCK_MAP* command is issued if the register content = CCh. The register content is automatically cleared.

7.5.40 UNLOCK_CORR Register (address = 6Dh) [reset = 00h]

Figure 62. UNLOCK_CORR Register, Address 6Dh

7	6	5	4	3	2	1	0
UNLOCK_CORR							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 42. UNLOCK_CORR Field Descriptions

Bit	Field	Type	Reset	Description
7–0	UNLOCK_CORR	W	00h	An *UNLOCK_CORR* command is issued if the register content = 33h. The register content is automatically cleared.

7.5.41 UNLOCK_MASK Register (address = 6Eh) [reset = 00h]

Figure 63. UNLOCK_MASK Register, Address 6Eh

7	6	5	4	3	2	1	0
UNLOCK_MASK							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 43. UNLOCK_MASK Field Descriptions

Bit	Field	Type	Reset	Description
7–0	UNLOCK_MASK	W	00h	An *UNLOCK_MASK* command is issued if the register content = 3Ch. The register content is automatically cleared.

7.5.42 UNLOCK_MISC Register (address = 6Fh) [reset = 00h]

Figure 64. UNLOCK_MISC Register, Address 6Fh

7	6	5	4	3	2	1	0
UNLOCK_MISC							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 44. UNLOCK_MISC Field Descriptions

Bit	Field	Type	Reset	Description
7–0	UNLOCK_MISC	W	00h	An *UNLOCK_MISC* command is issued if the register content = C3h. The register content is automatically cleared.

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7.5.43 READ_MAP0 Register (address = 80h) [reset = 00h]

Address 40h is used for writing the MAP0 data using the register pseudonym WRITE_MAP0, and address 80h is used for reading the MAP0 data using the register pseudonym READ_MAP0. See the *WRITE_MAP0 Register (address = 40h) [reset = 00h]* section for a description of the register contents.

Figure 65. READ_MAP0 Register, Address 80h

7	6	5	4	3	2	1	0
RESERVED			PWM_MAP_CH1[2:0]			PWM_MAP_CH0[2:0]	
R			R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.44 READ_MAP1 Register (address = 81h) [reset = 00h]

Address 41h is used for writing the MAP1 data using the register pseudonym WRITE_MAP1, and address 81h is used for reading the MAP1 data using the register pseudonym READ_MAP1. See the *WRITE_MAP1 Register (address = 41h) [reset = 00h]* section for a description of the register contents.

Figure 66. READ_MAP1 Register, Address 81h

7	6	5	4	3	2	1	0
RESERVED			PWM_MAP_CH3[2:0]			PWM_MAP_CH2[2:0]	
R			R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.45 READ_MAP2 Register (address = 82h) [reset = 00h]

Address 42h is used for writing the MAP2 data using the register pseudonym WRITE_MAP2, and address 82h is used for reading the MAP2 data using the register pseudonym READ_MAP2. See the *WRITE_MAP2 Register (address = 42h) [reset = 00h]* section for a description of the register contents.

Figure 67. READ_MAP2 Register, Address 82h

7	6	5	4	3	2	1	0
RESERVED			PWM_MAP_CH5[2:0]			PWM_MAP_CH4[2:0]	
R			R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.46 READ_MAP3 Register (address = 83h) [reset = 00h]

Address 43h is used for writing the MAP3 data using the register pseudonym WRITE_MAP3, and address 83h is used for reading the MAP3 data using the register pseudonym READ_MAP3. See the *WRITE_MAP3 Register (address = 43h) [reset = 00h]* section for a description of the register contents.

Figure 68. READ_MAP3 Register, Address 83h

7	6	5	4	3	2	1	0
RESERVED			PWM_MAP_CH7[2:0]			PWM_MAP_CH6[2:0]	
R			R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.5.47 READ_MAP4 Register (address = 84h) [reset = 00h]

Address 44h is used for writing the MAP4 data using the register pseudonym WRITE_MAP4, and address 84h is used for reading the MAP4 data using the register pseudonym READ_MAP4. See the *WRITE_MAP4 Register (address = 44h) [reset = 00h]* section for a description of the register contents.

Figure 69. READ_MAP4 Register, Address 84h

7	6	5	4	3	2	1	0
RESERVED		PWM_MAP_CH9[2:0]			PWM_MAP_CH8[2:0]		
R		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.48 READ_MAP5 Register (address = 85h) [reset = 00h]

Address 45h is used for writing the MAP5 data using the register pseudonym WRITE_MAP5, and address 85h is used for reading the MAP5 data using the register pseudonym READ_MAP5. See the *WRITE_MAP5 Register (address = 45h) [reset = 00h]* section for a description of the register contents.

Figure 70. READ_MAP5 Register, Address 85h

7	6	5	4	3	2	1	0
RESERVED		PWM_MAP_CH11[2:0]			PWM_MAP_CH10[2:0]		
R		R/W			R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.49 READ_CORR0 Register (address = 86h) [reset = 00h]

Address 46h is used for writing the CORR0 data using the register pseudonym WRITE_CORR0, and address 86h is used for reading the CORR0 data using the register pseudonym READ_CORR0. See the *WRITE_CORR0 Register (address = 46h) [reset = 00h]* section for a description of the register contents.

Figure 71. READ_CORR0 Register, Address 86h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH0[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.50 READ_CORR1 Register (address = 87h) [reset = 00h]

Address 47h is used for writing the CORR1 data using the register pseudonym WRITE_CORR1, and address 86h is used for reading the CORR1 data using the register pseudonym READ_CORR1. See the *WRITE_CORR1 Register (address = 47h) [reset = 00h]* section for a description of the register contents.

Figure 72. READ_CORR1 Register, Address 87h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH1[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.5.51 READ_CORR2 Register (address = 88h) [reset = 00h]

Address 48h is used for writing the CORR2 data using the register pseudonym WRITE_CORR2, and address 88h is used for reading the CORR2 data using the register pseudonym READ_CORR2. See the *WRITE_CORR2 Register (address = 48h) [reset = 00h]* section for a description of the register contents.

Figure 73. READ_CORR2 Register, Address 88h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH2[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.52 READ_CORR3 Register (address = 89h) [reset = 00h]

Address 49h is used for writing the CORR3 data using the register pseudonym WRITE_CORR3, and address 89h is used for reading the CORR3 data using the register pseudonym READ_CORR3. See the *WRITE_CORR3 Register (address = 49h) [reset = 00h]* section for a description of the register contents.

Figure 74. READ_CORR3 Register, Address 89h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH3[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.53 READ_CORR4 Register (address = 8Ah) [reset = 00h]

Address 4Ah is used for writing the CORR4 data using the register pseudonym WRITE_CORR4, and address 8Ah is used for reading the CORR4 data using the register pseudonym READ_CORR4. See the *WRITE_CORR4 Register (address = 4Ah) [reset = 00h]* section for a description of the register contents.

Figure 75. READ_CORR4 Register, Address 8Ah

7	6	5	4	3	2	1	0
OUTPUT_DC_CH4[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.54 READ_CORR5 Register (address = 8Bh) [reset = 00h]

Address 4Bh is used for writing the CORR5 data using the register pseudonym WRITE_CORR5, and address 8Bh is used for reading the CORR5 data using the register pseudonym READ_CORR5. See the *WRITE_CORR5 Register (address = 4Bh) [reset = 00h]* section for a description of the register contents.

Figure 76. READ_CORR5 Register, Address 8Bh

7	6	5	4	3	2	1	0
OUTPUT_DC_CH5[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.5.55 READ_CORR6 Register (address = 8Ch) [reset = 00h]

Address 4Ch is used for writing the CORR6 data using the register pseudonym WRITE_CORR6, and address 8Ch is used for reading the CORR6 data using the register pseudonym READ_CORR6. See the *WRITE_CORR6 Register (address = 4Ch) [reset = 00h]* section for a description of the register contents.

Figure 77. READ_CORR6 Register, Address 8Ch

7	6	5	4	3	2	1	0
OUTPUT_DC_CH6[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.56 READ_CORR7 Register (address = 8Dh) [reset = 00h]

Address 4Dh is used for writing the CORR7 data using the register pseudonym WRITE_CORR7, and address 8Dh is used for reading the CORR7 data using the register pseudonym READ_CORR7. See the *WRITE_CORR7 Register (address = 4Dh) [reset = 00h]* section for a description of the register contents.

Figure 78. READ_CORR7 Register, Address 8Dh

7	6	5	4	3	2	1	0
OUTPUT_DC_CH7[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.57 READ_CORR8 Register (address = 8Eh) [reset = 00h]

Address 4Eh is used for writing the CORR8 data using the register pseudonym WRITE_CORR8, and address 8Eh is used for reading the CORR8 data using the register pseudonym READ_CORR8. See the *WRITE_CORR8 Register (address = 4Eh) [reset = 00h]* section for a description of the register contents.

Figure 79. READ_CORR8 Register, Address 8Eh

7	6	5	4	3	2	1	0
OUTPUT_DC_CH8[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.58 READ_CORR9 Register (address = 8Fh) [reset = 00h]

Address 4Fh is used for writing the CORR9 data using the register pseudonym WRITE_CORR9, and address 8Fh is used for reading the CORR9 data using the register pseudonym READ_CORR9. See the *WRITE_CORR9 Register (address = 4Fh) [reset = 00h]* section for a description of the register contents.

Figure 80. READ_CORR9 Register, Address 8Fh

7	6	5	4	3	2	1	0
OUTPUT_DC_CH9[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.5.59 READ_CORR10 Register (address = 90h) [reset = 00h]

Address 50h is used for writing the CORR10 data using the register pseudonym WRITE_CORR10, and address 90h is used for reading the CORR10 data using the register pseudonym READ_CORR10. See the *WRITE_CORR10 Register (address = 50h) [reset = 00h]* section for a description of the register contents.

Figure 81. READ_CORR10 Register, Address 90h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH10[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.60 READ_CORR11 Register (address = 91h) [reset = 00h]

Address 51h is used for writing the CORR11 data using the register pseudonym WRITE_CORR11, and address 91h is used for reading the CORR11 data using the register pseudonym READ_CORR11. See the *WRITE_CORR11 Register (address = 51h) [reset = 00h]* section for a description of the register contents.

Figure 82. READ_CORR11 Register, Address 91h

7	6	5	4	3	2	1	0
OUTPUT_DC_CH11[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.61 READ_CH_ON_MASK0 Register (address = 92h) [reset = 3Fh]

Address 52h is used for writing the CH_ON_MASK0 data using the register pseudonym WRITE_CH_ON_MASK0, and address 92h is used for reading the CH_ON_MASK0 data using the register pseudonym READ_CH_ON_MASK0. See the *WRITE_CH_ON_MASK0 Register (address = 52h) [reset = 3Fh]* section for a description of the register contents.

Figure 83. READ_CH_ON_MASK0, Address 92h

7	6	5	4	3	2	1	0
RESERVED		CH_ON_MASK 5	CH_ON_MASK 4	CH_ON_MASK 3	CH_ON_MASK 2	CH_ON_MASK 1	CH_ON_MASK 0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.62 READ_CH_ON_MASK1 Register (address = 93h) [reset = 3Fh]

Address 53h is used for writing the CH_ON_MASK1 data using the register pseudonym WRITE_CH_ON_MASK1, and address 93h is used for reading the CH_ON_MASK1 data using the register pseudonym READ_CH_ON_MASK1. See the *WRITE_CH_ON_MASK1 Register (address = 53h) [reset = 3Fh]* section for a description of the register contents.

Figure 84. READ_CH_ON_MASK1, Address 93h

7	6	5	4	3	2	1	0
RESERVED		CH_ON_MASK 11	CH_ON_MASK 10	CH_ON_MASK 9	CH_ON_MASK 8	CH_ON_MASK 7	CH_ON_MASK 6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.5.63 READ_SHORT_MASK0 Register (address = 94h) [reset = 3Fh]

Address 54h is used for writing the SHORT_MASK0 data using the register pseudonym WRITE_SHORT_MASK0, and address 94h is used for reading the SHORT_MASK0 data using the register pseudonym READ_SHORT_MASK0. See the *WRITE_SHORT_MASK0 Register (address = 54h) [reset = 3Fh]* section for a description of the register contents.

Figure 85. READ_SHORT_MASK0, Address 94h

7	6	5	4	3	2	1	0
RESERVED		SHORT_MASK_CH5	SHORT_MASK_CH4	SHORT_MASK_CH3	SHORT_MASK_CH2	SHORT_MASK_CH1	SHORT_MASK_CH0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.64 READ_SHORT_MASK1 Register (address = 95h) [reset = 3Fh]

Address 55h is used for writing the SHORT_MASK1 data using the register pseudonym WRITE_SHORT_MASK1, and address 95h is used for reading the SHORT_MASK1 data using the register pseudonym READ_SHORT_MASK1. See the *WRITE_SHORT_MASK1 Register (address = 55h) [reset = 3Fh]* section for a description of the register contents.

Figure 86. READ_SHORT_MASK1, Address 95h

7	6	5	4	3	2	1	0
RESERVED		SHORT_MASK_CH11	SHORT_MASK_CH10	SHORT_MASK_CH9	SHORT_MASK_CH8	SHORT_MASK_CH7	SHORT_MASK_CH6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.65 READ_SHORT_GND_MASK0 Register (address = 96h) [reset = 3Fh]

Address 56h is used for writing the SHORT_GND_MASK0 data using the register pseudonym WRITE_SHORT_GND_MASK0, and address 96h is used for reading the SHORT_GND_MASK0 data using the register pseudonym READ_SHORT_GND_MASK0. See the *WRITE_SHORT_GND_MASK0 Register (address = 56h) [reset = 3Fh]* section for a description of the register contents.

Figure 87. READ_SHORT_GND_MASK0, Address 96h

7	6	5	4	3	2	1	0
RESERVED		SG_MASK_CH5	SG_MASK_CH4	SG_MASK_CH3	SG_MASK_CH2	SG_MASK_CH1	SG_MASK_CH0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.66 READ_SHORT_GND_MASK1 Register (address = 97h) [reset = 3Fh]

Address 57h is used for writing the SHORT_GND_MASK1 data using the register pseudonym WRITE_SHORT_GND_MASK1, and address 97h is used for reading the SHORT_GND_MASK1 data using the register pseudonym READ_SHORT_GND_MASK1. See the *WRITE_SHORT_GND_MASK1 Register (address = 57h) [reset = 3Fh]* section for a description of the register contents.

Figure 88. READ_SHORT_GND_MASK1, Address 97h

7	6	5	4	3	2	1	0
RESERVED		SG_MASK_CH11	SG_MASK_CH10	SG_MASK_CH9	SG_MASK_CH8	SG_MASK_CH7	SG_MASK_CH6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.5.67 READ_OPEN_MASK0 Register (address = 98h) [reset = 3Fh]

Address 58h is used for writing the OPEN_MASK0 data using the register pseudonym WRITE_OPEN_MASK0, and address 98h is used for reading the OPEN_MASK0 data using the register pseudonym READ_OPEN_MASK0. See the *WRITE_OPEN_MASK0 Register (address = 58h) [reset = 3Fh]* section for a description of the register contents.

Figure 89. READ_OPEN_MASK0, Address 98h

7	6	5	4	3	2	1	0
RESERVED		OPEN_MASK_CH5	OPEN_MASK_CH4	OPEN_MASK_CH3	OPEN_MASK_CH2	OPEN_MASK_CH1	OPEN_MASK_CH0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.68 READ_OPEN_MASK1 Register (address = 99h) [reset = 3Fh]

Address 59h is used for writing the OPEN_MASK1 data using the register pseudonym WRITE_OPEN_MASK1, and address 99h is used for reading the OPEN_MASK1 data using the register pseudonym READ_OPEN_MASK1. See the *WRITE_OPEN_MASK1 Register (address = 59h) [reset = 3Fh]* section for a description of the register contents.

Figure 90. READ_OPEN_MASK1, Address 99h

7	6	5	4	3	2	1	0
RESERVED		OPEN_MASK_CH11	OPEN_MASK_CH10	OPEN_MASK_CH9	OPEN_MASK_CH8	OPEN_MASK_CH7	OPEN_MASK_CH6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.69 READ_SHORT_FAULT0 (address = 9Ah) [reset = 00h]

Figure 91. READ_SHORT_FAULT0, Address 9Ah

7	6	5	4	3	2	1	0
RESERVED		SHORT_FAULT5	SHORT_FAULT4	SHORT_FAULT3	SHORT_FAULT2	SHORT_FAULT1	SHORT_FAULT0
R		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 45. READ_SHORT_FAULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	SHORT_FAULT5	R	0h	Channel 5 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
4	SHORT_FAULT4	R	0h	Channel 4 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
3	SHORT_FAULT3	R	0h	Channel 3 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
2	SHORT_FAULT2	R	0h	Channel 2 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
1	SHORT_FAULT1	R	0h	Channel 1 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
0	SHORT_FAULT0	R	0h	Channel 0 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.

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7.5.70 READ_SHORT_FAULT1 (address = 9Bh) [reset = 00h]

Figure 92. READ_SHORT_FAULT1, Address 9Bh

7	6	5	4	3	2	1	0
RESERVED		SHORT_ FAULT11	SHORT_ FAULT10	SHORT_ FAULT9	SHORT_ FAULT8	SHORT_ FAULT7	SHORT_ FAULT6
R		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 46. READ_SHORT_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	SHORT_FAULT11	R	0h	Channel 11 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
4	SHORT_FAULT10	R	0h	Channel 10 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
3	SHORT_FAULT9	R	0h	Channel 9 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
2	SHORT_FAULT8	R	0h	Channel 8 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
1	SHORT_FAULT7	R	0h	Channel 7 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.
0	SHORT_FAULT6	R	0h	Channel 6 LED short-to-supply fault flag. Active-high. HIGH: LED short-to-supply detected; LOW: LED short-to-supply not detected.

7.5.71 READ_SHORT_GND_FAULT0 (address = 9Ch) [reset = 00h]

Figure 93. READ_SHORT_GND_FAULT0, Address 9Ch

7	6	5	4	3	2	1	0
RESERVED		SG_FAULT5	SG_FAULT4	SG_FAULT3	SG_FAULT2	SG_FAULT1	SG_FAULT0
R		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 47. READ_SHORT_GND_FAULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	SG_FAULT5	R	0h	Channel 5 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
4	SG_FAULT4	R	0h	Channel 4 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
3	SG_FAULT3	R	0h	Channel 3 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
2	SG_FAULT2	R	0h	Channel 2 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
1	SG_FAULT1	R	0h	Channel 1 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
0	SG_FAULT0	R	0h	Channel 0 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.

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7.5.72 READ_SHORT_GND_FAULT1 (address = 9Dh) [reset = 00h]

Figure 94. READ_SHORT_GND_FAULT1, Address 9Dh

7	6	5	4	3	2	1	0
RESERVED		SG_FAULT11	SG_FAULT10	SG_FAULT9	SG_FAULT8	SG_FAULT7	SG_FAULT6
R		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 48. READ_SHORT_GND_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	SG_FAULT11	R	0h	Channel 11 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
4	SG_FAULT10	R	0h	Channel 10 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
3	SG_FAULT9	R	0h	Channel 9 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
2	SG_FAULT8	R	0h	Channel 8 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
1	SG_FAULT7	R	0h	Channel 7 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.
0	SG_FAULT6	R	0h	Channel 6 LED short-to-GND fault flag. Active-high. HIGH: LED short-to-GND detected; LOW: LED short-to-GND not detected.

7.5.73 READ_OPEN_FAULT0 (address = 9Eh) [reset = 00h]

Figure 95. READ_OPEN_FAULT0, Address 9Eh

7	6	5	4	3	2	1	0
RESERVED		OPEN_FAULT_CH5	OPEN_FAULT_CH4	OPEN_FAULT_CH3	OPEN_FAULT_CH2	OPEN_FAULT_CH1	OPEN_FAULT_CH0
R		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 49. READ_OPEN_FAULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	OPEN_FAULT_CH5	R	0h	Channel 5 LED-open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
4	OPEN_FAULT_CH4	R	0h	Channel 4 LEDopen fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
3	OPEN_FAULT_CH3	R	0h	Channel 3 LED-open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
2	OPEN_FAULT_CH2	R	0h	Channel 2 LED-open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
1	OPEN_FAULT_CH1	R	0h	Channel 1 LED-open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
0	OPEN_FAULT_CH0	R	0h	Channel 0 LED-open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.

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7.5.74 READ_OPEN_FAULT1 (address = 9Fh) [reset = 00h]

Figure 96. READ_OPEN_FAULT1, Address 9Fh

7	6	5	4	3	2	1	0
RESERVED		OPEN_FAULT_CH11	OPEN_FAULT_CH10	OPEN_FAULT_CH9	OPEN_FAULT_CH8	OPEN_FAULT_CH7	OPEN_FAULT_CH6
R		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 50. READ_OPEN_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	OPEN_FAULT_CH11	R	0h	Channel 11 LED open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
4	OPEN_FAULT_CH10	R	0h	Channel 10 LED open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
3	OPEN_FAULT_CH9	R	0h	Channel 9 LED open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
2	OPEN_FAULT_CH8	R	0h	Channel 8 LED open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
1	OPEN_FAULT_CH7	R	0h	Channel 7 LED open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.
0	OPEN_FAULT_CH6	R	0h	Channel 6 LED open fault flag. Active-high. HIGH: LED open detected; LOW: LED open not detected.

7.5.75 READ_PWM_FAULT_MASK Register (address = A1h) [reset = 3Fh]

Address 60h is used for writing the PWM_FAULT_MASK data using the register pseudonym WRITE_PWM_FAULT_MASK, and address A0h is used for reading the PWM_FAULT_MASK data using the register pseudonym READ_PWM_FAULT_MASK. See the *WRITE_PWM_FAULT_MASK Register (address = 60h) [reset = 3Fh]* section for a description of the register contents.

Figure 97. READ_PWM_FAULT_MASK, Address A1h

7	6	5	4	3	2	1	0
RESERVED		PWM_FAULT_MASK5	PWM_FAULT_MASK4	PWM_FAULT_MASK3	PWM_FAULT_MASK2	PWM_FAULT_MASK1	SG_MASK_CH0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.5.76 READ_STATUS0 (address = A2h) [reset = 40h]

Figure 98. READ_STATUS0, Address A2h

7	6	5	4	3	2	1	0
REF_FAULT_FLAG	POR_ERR_FLAG	ANY_OPEN_FLAG	ANY_SHORT_FLAG	ANY_PWM_FAULT_FLAG	WLS_FAULT_FLAG	PRE_TSD_FLAG	TSD_FLAG
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 51. READ_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	REF_FAULT_FLAG	R	0h	Reference-resistor fault flag. Active-high. HIGH: Reference fault detected; LOW: Reference fault not detected.
6	POR_ERR_FLAG	R	1h	Power-on-reset error flag. Active-high. HIGH: POR error detected; LOW: POR error not detected.
5	ANY_OPEN_FLAG	R	0h	Any-channel-open fault flag. Active-high. HIGH: One or more channels has an open fault; LOW: an open fault is not detected or an open fault is masked.
4	ANY_SHORT_FLAG	R	0h	Any channel short-to-supply fault flag. Active-high. HIGH: One or more channels has a short-to-supply fault; LOW: a short-to-supply fault is not detected or a short-to-supply fault is masked.
3	ANY_PWM_FAULT_FLAG	R	0h	Any-input PWM-fault flag. Active-high. HIGH: One or more PWM channels has a fault; LOW: a PWM fault is not detected or a PWM fault is masked.
2	WLS_FAULT_FLAG	R	0h	Weak-LED-supply fault flag. Active-high. HIGH: WLS fault detected; LOW: a WLS fault is not detected or a WLS fault is masked.
1	PRE_TSD_FLAG	R	0h	PRE-TSD warning flag. Active-high. HIGH: a PRE TSD warning is detected; LOW: a PRE-TSD warning is not detected or a PRE_TSD warning is masked.
0	TSD_FLAG	R	0h	Thermal shutdown flag. Active-high. HIGH: a thermal shutdown has been triggered; LOW: a thermal shutdown is not triggered or it is masked.

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7.5.77 READ_STATUS1 (address = A3h) [reset = 00h]

See the *PWM MAP Register Lock* section for a list of miscellaneous (MISC), mapping (MAP), masking (MASK), and correction (CORR) registers.

Figure 99. READ_STATUS1, Address A3h

7	6	5	4	3	2	1	0
RESERVED			DIS_PULL_UP_FLAG	LOCK_MISC_FLAG	LOCK_MAP_FLAG	LOCK_MASK_FLAG	LOCK_CORR_FLAG
R			R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 52. READ_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–5	RESERVED	R	0h	
4	DIS_PULL_UP_FLAG	R	0h	Off-state pullup disabled flag. Active-high. HIGH: One or more channels have off-state pullup disabled. LOW: No channel has off-state pullup disabled.
3	LOCK_MISC_FLAG	R	0h	LOCK_MISC status flag. Active-high. HIGH: MISC registers are locked. LOW: MISC registers are not locked.
2	LOCK_MAP_FLAG	R	0h	LOCK_MAP status flag. Active-high. HIGH: MAP registers are locked. LOW: MAP registers are not locked.
1	LOCK_MASK_FLAG	R	0h	LOCK_MASK status flag. Active-high. HIGH: MASK registers are locked. LOW: MASK registers are not locked.
0	LOCK_CORR_FLAG	R	0h	LOCK_CORR status flag. Active-high. HIGH: CORR registers are locked. LOW: CORR registers are not locked.

7.5.78 READ_DIS_PULL_UP_0 Register (address = A4h) [reset = 00h]

Address 64h is used for writing the DIS_PULL_UP_0 data using the register pseudonym WRITE_DIS_PULL_UP_0, and address A4h is used for reading the DIS_PULL_UP_0 data using the register pseudonym READ_DIS_PULL_UP_0. See the *WRITE_DIS_PULL_UP_0 Register (address = 64h) [reset = 00h]* section for a description of the register contents.

Figure 100. READ_DIS_PULL_UP_0 Register, Address A4h

7	6	5	4	3	2	1	0
RESERVED		DIS_PULL_UP_CH5	DIS_PULL_UP_CH4	DIS_PULL_UP_CH3	DIS_PULL_UP_CH2	DIS_PULL_UP_CH1	DIS_PULL_UP_CH0
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.79 READ_DIS_PULL_UP_1 Register (address = A5h) [reset = 00h]

Address 65h is used for writing the DIS_PULL_UP_1 data using the register pseudonym WRITE_DIS_PULL_UP_1, and address A5h is used for reading the DIS_PULL_UP_1 data using the register pseudonym READ_DIS_PULL_UP_1. See the *WRITE_DIS_PULL_UP_1 Register (address = 65h) [reset = 00h]* section for a description of the register contents.

Figure 101. READ_DIS_PULL_UP_1 Register, Address A5h

7	6	5	4	3	2	1	0
RESERVED		DIS_PULL_UP_CH11	DIS_PULL_UP_CH10	DIS_PULL_UP_CH9	DIS_PULL_UP_CH8	DIS_PULL_UP_CH7	DIS_PULL_UP_CH6
R		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.5.80 READ_ERROR_MASK (address = A6h) [reset = 00h]

Address 66h is used for writing the ERROR_MASK data using the register pseudonym WRITE_ERROR_MASK, and address A6h is used for reading the ERROR_MASK data using the register pseudonym READ_ERROR_MASK. See the *WRITE_ERROR_MASK Register (address = 66h) [reset = 00h]* section for a description of the register contents.

Figure 102. READ_ERROR_MASK, Address A6h

7	6	5	4	3	2	1	0
REF_MASK	POR_MASK	OPEN_MASK	SHORT_MASK	PWM_MASK	WLS_MASK	PRE_TSD_ MASK	TSD_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.5.81 READ_MISC_CMD Register (address = A7h) [reset = 00h]

Address 67h is used for writing the MISC_CMD data using the register pseudonym WRITE_MISC_CMD, and address A7h is used for reading the MISC_CMD data using the register pseudonym READ_MISC_CMD. See the *WRITE_MISC_CMD Register (address = 67h) [reset = 00h]* section for a description of the register contents.

Figure 103. READ_MISC_CMD Register, Address A7h

7	6	5	4	3	2	1	0
RESERVED		RESERVED	DIS_OFF_ FAULT_DIAG	ADJ_DIAG_ START	SLOW_SLEW_ RATE	FORCE_ERR	WLS_TH
R		R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.5.82 READ_ADSHORT0 (address = A8h) [reset = 00h]

Figure 104. READ_ADSHORT0, Address A8h

7	6	5	4	3	2	1	0
RESERVED		AD_FLAG_CH11	AD_FLAG_CH10	AD_FLAG_CH9	AD_FLAG_CH8	AD_FLAG_CH7	AD_FLAG_CH6
R		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 53. READ_ADSHORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	AD_FLAG_CH11	R	0h	Adjacent-pin short fault flag for channel 11. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
4	AD_FLAG_CH10	R	0h	Adjacent-pin short fault flag for channel 10. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
3	AD_FLAG_CH9	R	0h	Adjacent-pin short fault flag for channel 9. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
2	AD_FLAG_CH8	R	0h	Adjacent-pin short fault flag for channel 8. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
1	AD_FLAG_CH7	R	0h	Adjacent-pin short fault flag for channel 7. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
0	AD_FLAG_CH6	R	0h	Adjacent-pin short fault flag for channel 6. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.

7.5.83 READ_ADSHORT1 (address = A9h) [reset = 00h]

Figure 105. READ_ADSHORT1, Address A9h

7	6	5	4	3	2	1	0
RESERVED		AD_FLAG_CH5	AD_FLAG_CH4	AD_FLAG_CH3	AD_FLAG_CH2	AD_FLAG_CH1	AD_FLAG_CH0
R		R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 54. READ_ADSHORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R	0h	
5	AD_FLAG_CH5	R	0h	Adjacent-pin short fault flag for channel 5. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
4	AD_FLAG_CH4	R	0h	Adjacent-pin short fault flag for channel 4. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
3	AD_FLAG_CH3	R	0h	Adjacent-pin short fault flag for channel 3. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
2	AD_FLAG_CH2	R	0h	Adjacent-pin short fault flag for channel 2. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
1	AD_FLAG_CH1	R	0h	Adjacent-pin short fault flag for channel 1. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.
0	AD_FLAG_CH0	R	0h	Adjacent-pin short fault flag for channel 0. Active-high. HIGH: Adjacent-pin short detected; LOW: adjacent-pin short not detected.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLC6C5712-Q1 device is capable of driving different numbers of LEDs with accurate current driving and the most-advanced diagnostics. The device is suitable for automotive cluster tell-tale lighting, gear-shifter PRNDL indicators, and other safety-critical LED applications.

8.2 Typical Applications

8.2.1 Multiple Devices Connected in Cascade

The TLC6C5712-Q1 design supports multiple devices in cascaded daisy-chain mode. Each communication sequence must only have one LATCH rising edge and, therefore, cannot be split into multiple smaller sequences.

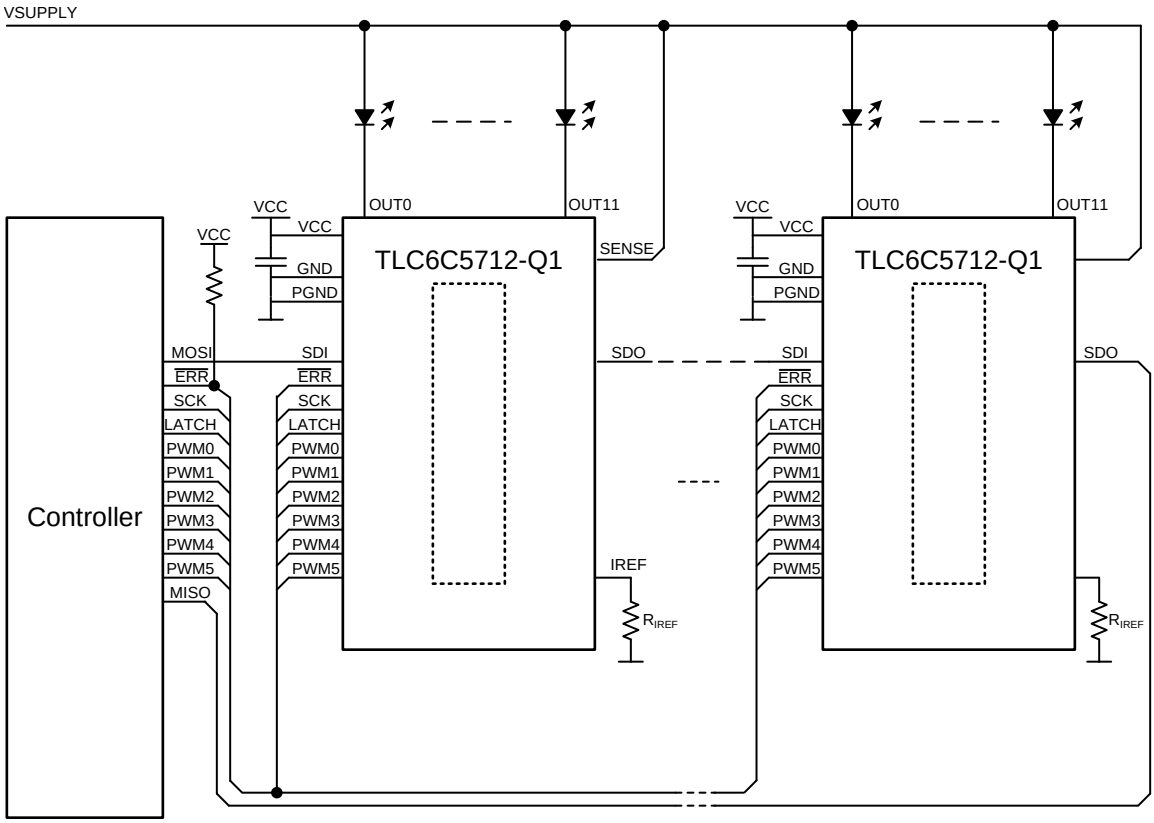

Figure 106. Application Schematic for TLC6C5712-Q1 Devices Connected in Cascade

Typical Applications (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 55.

Table 55. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$I_{(LED\_FULLRANGE)}$ (1)	20 mA
$I_{(LED)}$ (2)	16 mA

(1) $I_{(LED\_FULLRANGE)}$ is the maximum LED current allowed.
(2) $I_{(LED)}$ is the required output driving current for this application.

8.2.1.2 Detailed Design Procedure

This design has multiple TLC6C5712-Q1 devices connected by a SPI daisy chain. Use Equation 5 to calculate the reference resistor value.

$$R_{(IREF)} = \frac{V_{(IREF)}}{I_{(LED\_FULLRANGE)}} \times K_{(OUT)} = \frac{1.229\ V}{0.02\ A} \times 500 = 30.725\ k\Omega \quad (5)$$

Use Equation 6 to calculate the dot correction for each channel.

$$\text{Dot correction} = \frac{16}{20} \times 256 - 1 = 204, \quad (0xCC) \quad (6)$$

8.2.1.3 Application Curves

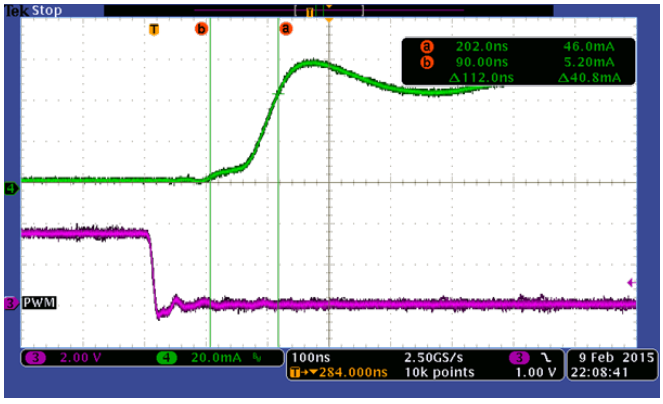

Figure 107. PWM Delay and Output Rise Time
CH3: PWM0, CH4: OUT0

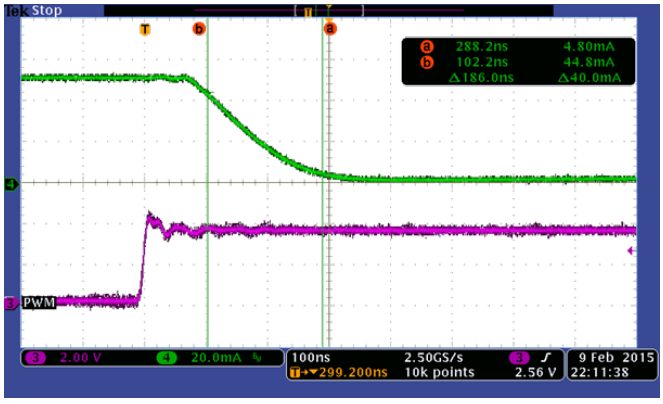

Figure 108. PWM Delay and Output Fall Time
CH3: PWM0, CH4: OUT0

8.2.2 Parallel Channels for Driving Higher Current

In some applications, capability to drive higher current is needed. To deliver higher current while maintaining adjacent-short detection capability, channels with odd numbers can be shorted together; similarly, channels with even numbers can be shorted together. If odd and even numbers are shorted together, the device reports a false error during adjacent-pin short detection.

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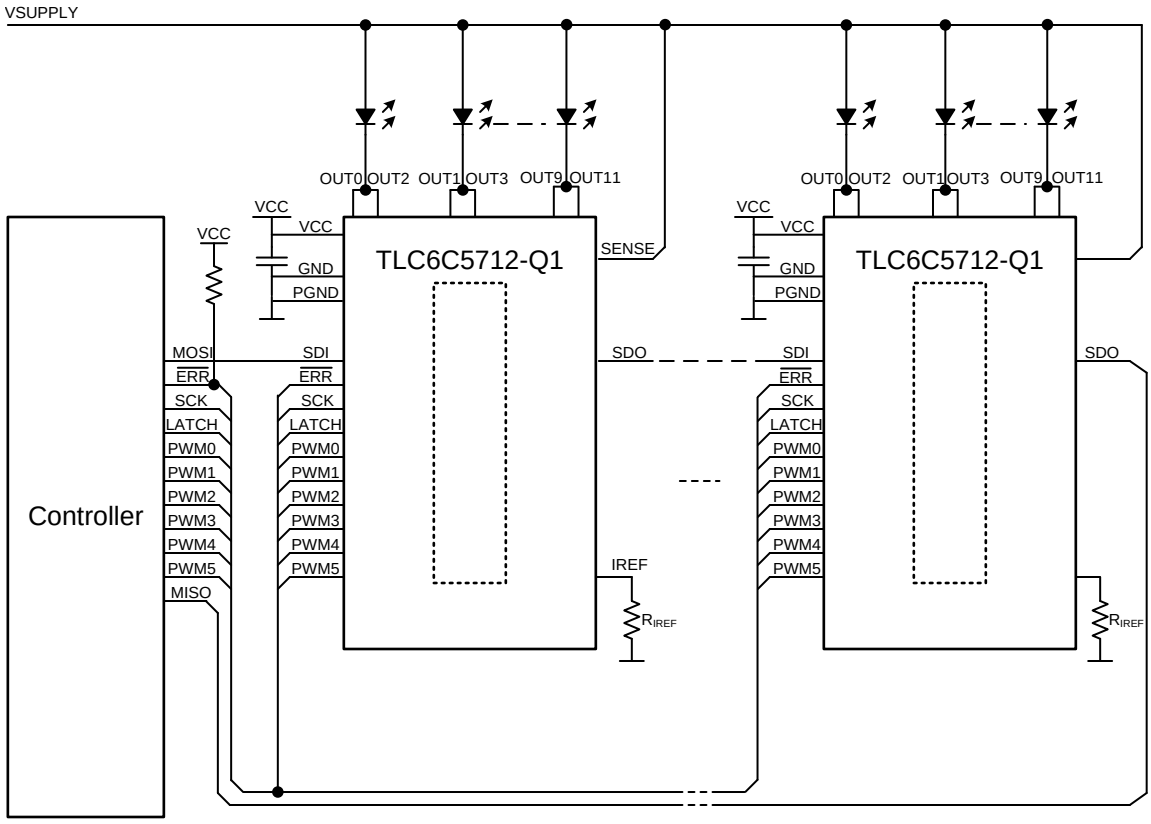

Figure 109. Application Schematic for TLC6C5712-Q1 Devices With Parallel Outputs

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 56.

Table 56. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$I_{(LED\_FULLRANGE)}$ (1)	20 mA
$I_{(LED)}$ (2)	16 mA
Channels in parallel	2

(1) $I_{(LED\_FULLRANGE)}$ is the maximum LED current allowed.
(2) $I_{(LED)}$ is the required output driving current for this application.

8.2.2.2 Detailed Design Procedure

This design has multiple TLC6C5712-Q1 devices connected by a SPI daisy chain. Use Equation 7 to calculate the reference resistor value.

$$R_{(IREF)} = \frac{V_{(IREF)}}{\frac{I_{(LED\_FULLRANGE)}}{\text{No. of parallel channels}}} \times K_{(OUT)} = \frac{1.229\ V}{0.14\ A / 2} \times 500 = 878\ \Omega \quad (7)$$

Use Equation 8 to calculate the dot correction for each channel.

$$\text{Dot correction} = \frac{140}{140} \times 256 - 1 = 255, \quad (0xFF) \quad (8)$$

9 Power Supply Recommendations

The TLC6C5712-Q1 device is qualified for automotive applications. Because of voltage-level limitations, the device requires a first-stage power supply to provide LED and device power. V_{CC} and $V_{(SENSE)}$ voltages can be provided by the same voltage supply or independent voltage supplies. The supply voltage range is specified in *Recommended Operating Conditions*.

10 Layout

10.1 Layout Guidelines

To prevent thermal shutdown, the junction temperature, T_J, must be less than 150°C. If the voltage drop across the output channels is high, the device power dissipation can be large. The TLC6C5712-Q1 device has very good thermal performance because of the thermal pad design; however, the PCB layout is also very important to ensure that the device has good thermal performance. Good PCB design can optimize heat transfer, which is essential for the long-term reliability of the device.

Use the following guidelines when designing the device layout:

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through copper on the PCB. Maximum copper density is extremely important when no heat sinks are attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- Use either plated shut or plugged and capped vias for all the thermal vias on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

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10.2 Layout Example

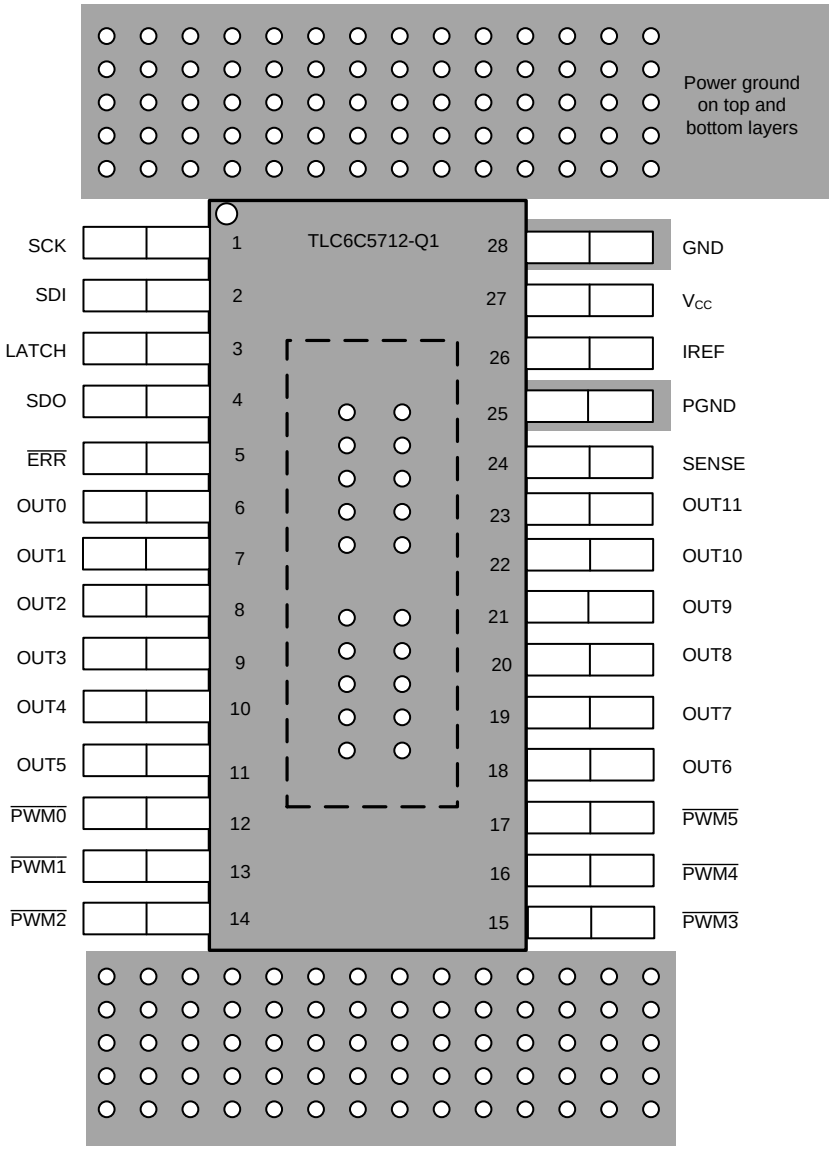

Figure 110. TLC6C7512-Q1 Layout Diagram

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

TLC6C5712-Q1 Evaluation Module, SLVUAE6

11.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC6C5712QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	6C5712	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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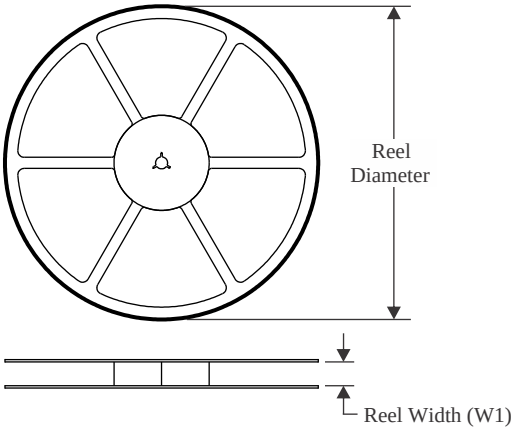
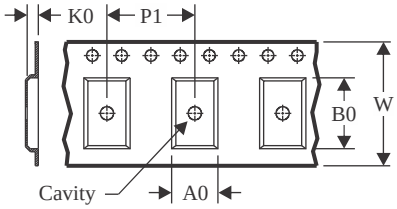
TAPE AND REEL INFORMATION

REEL DIMENSIONS

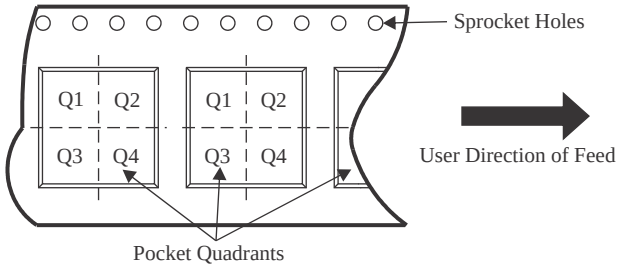


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

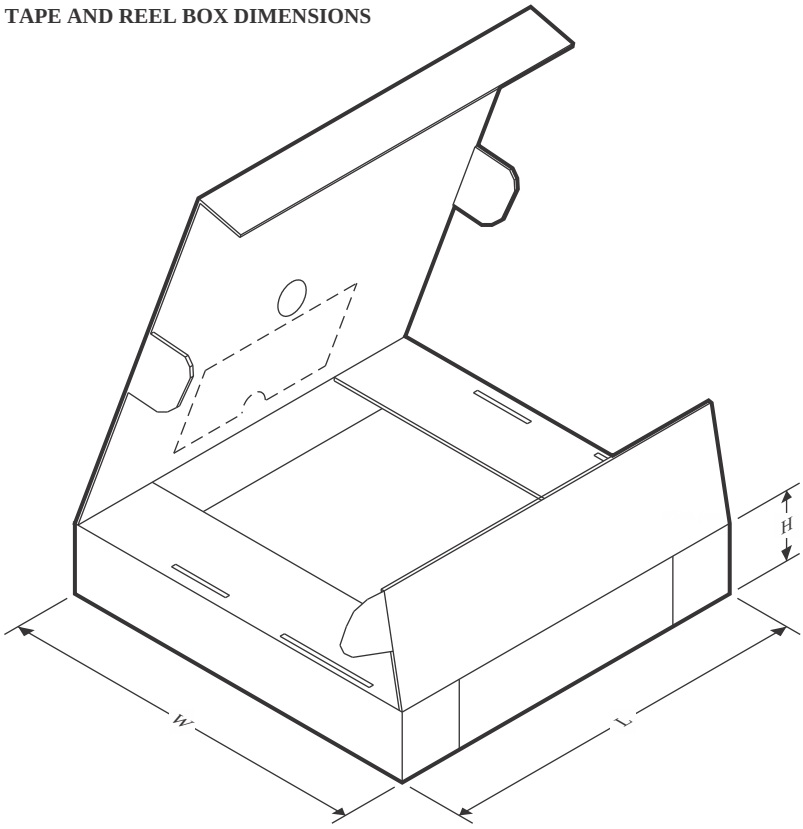
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6C5712QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6C5712QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

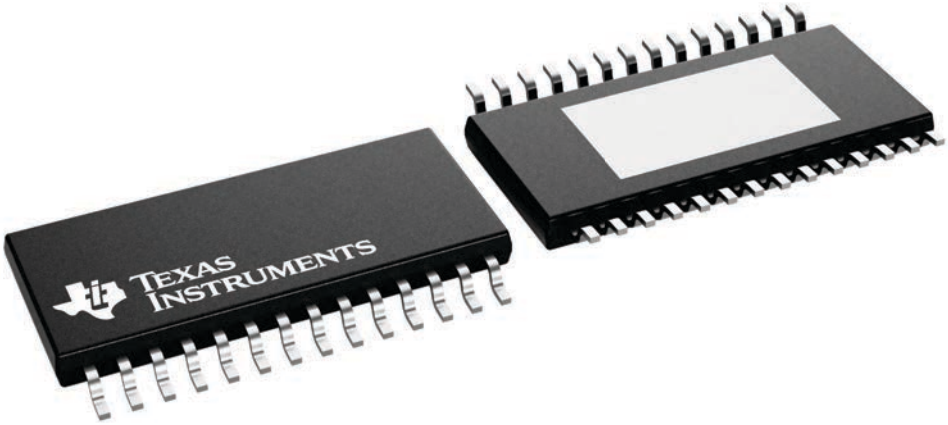
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

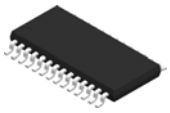
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

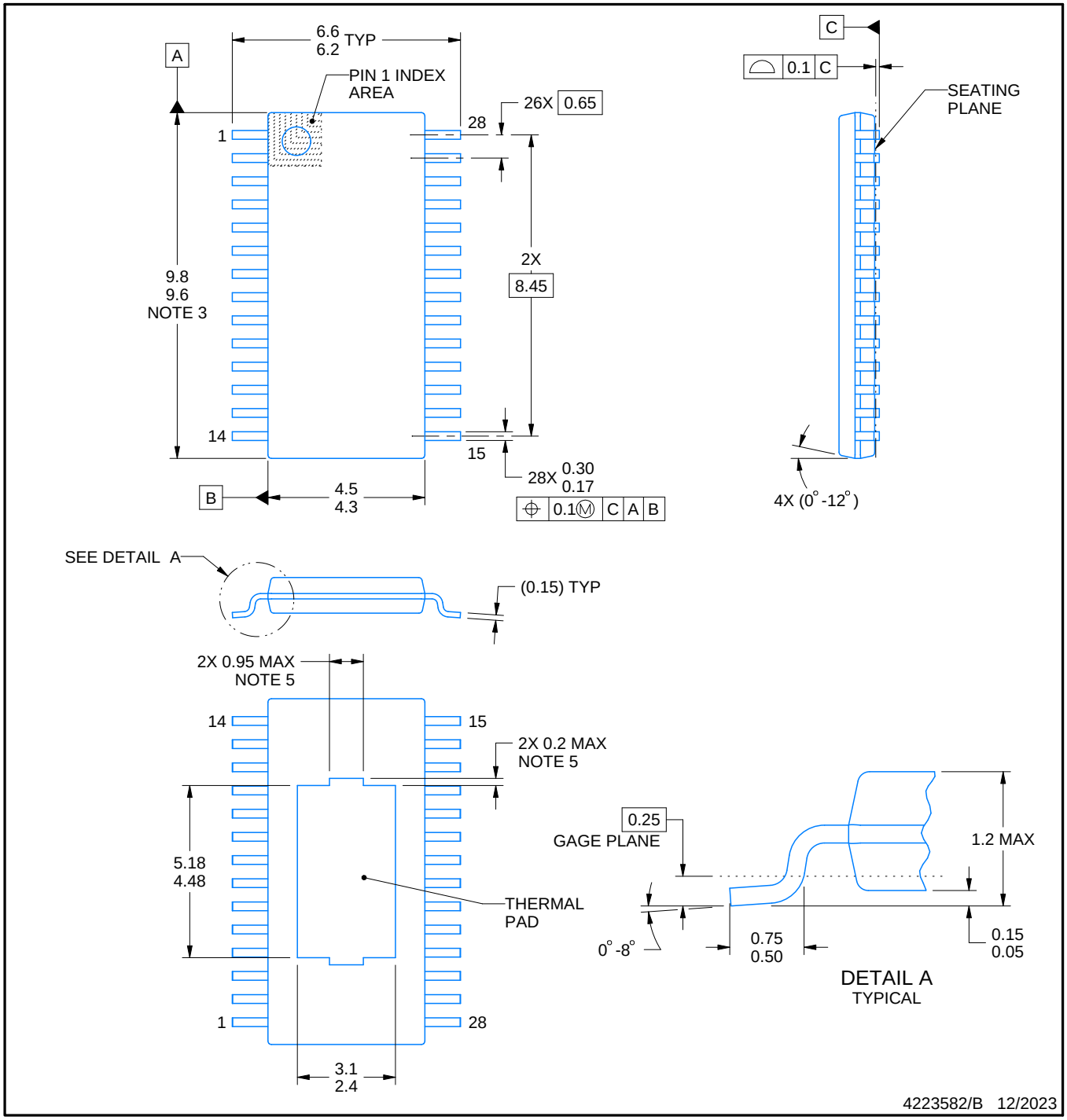
PACKAGE OUTLINE

PWP0028C



PowerPAD™ TSSOP - 1.2 mm max height

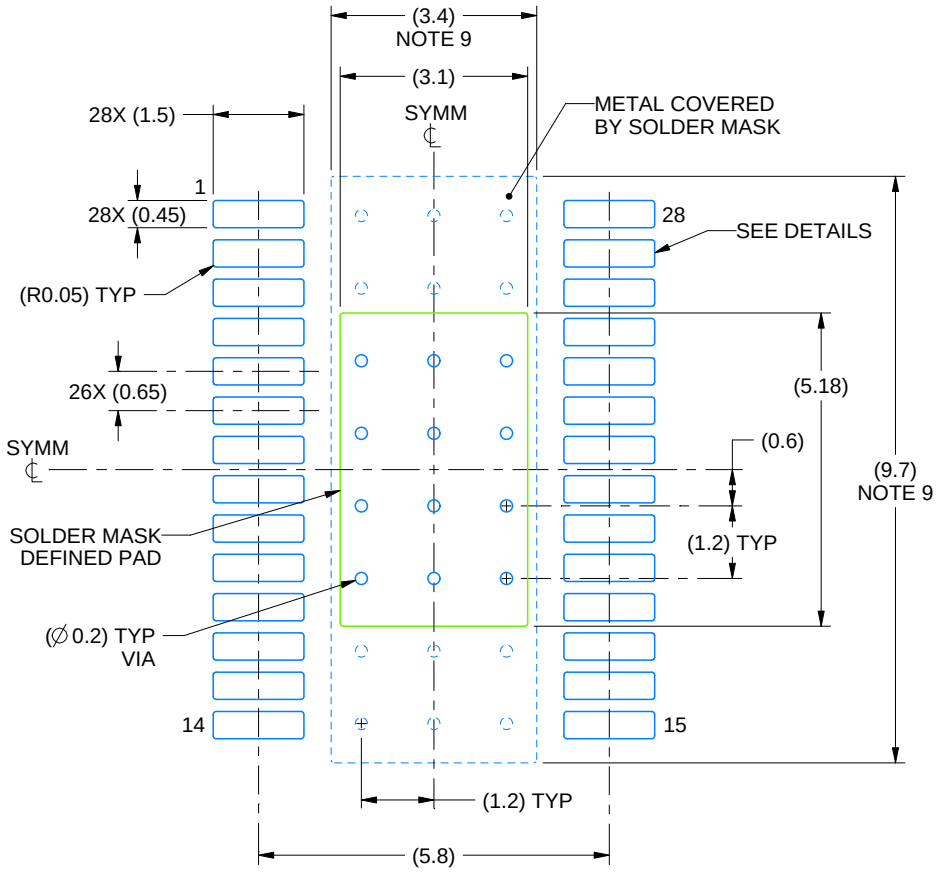
SMALL OUTLINE PACKAGE



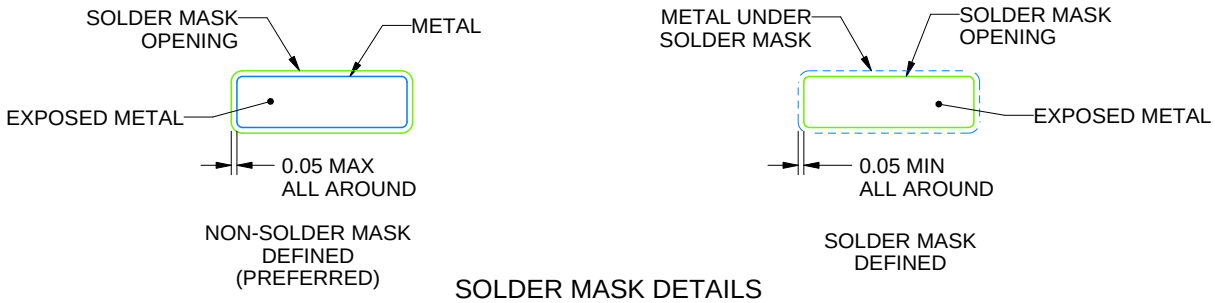
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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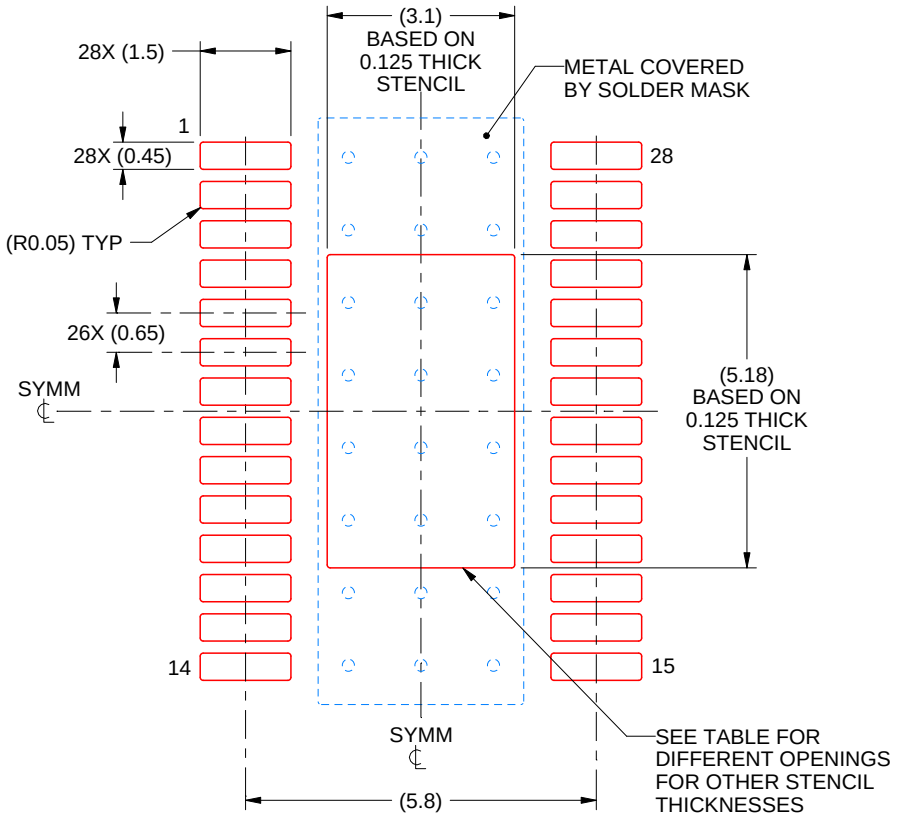
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC6C5712QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	6C5712	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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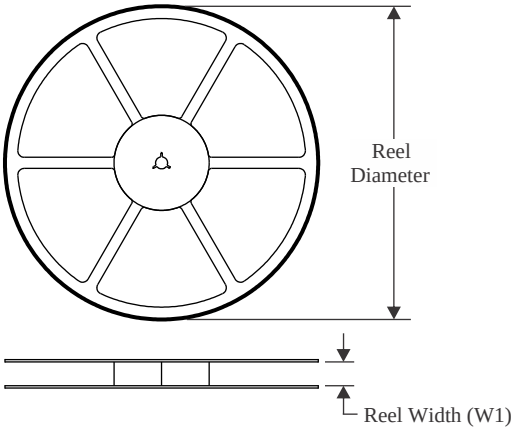
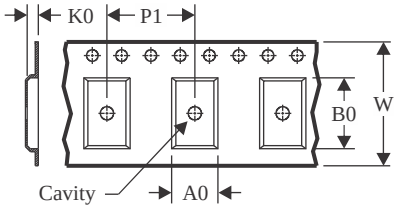
TAPE AND REEL INFORMATION

REEL DIMENSIONS

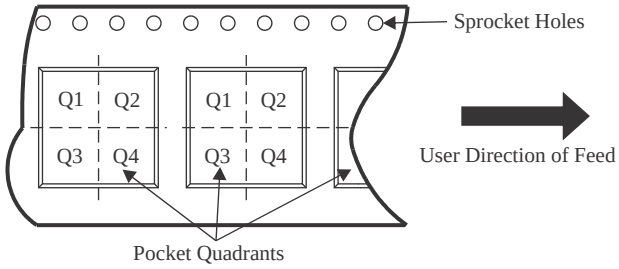


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

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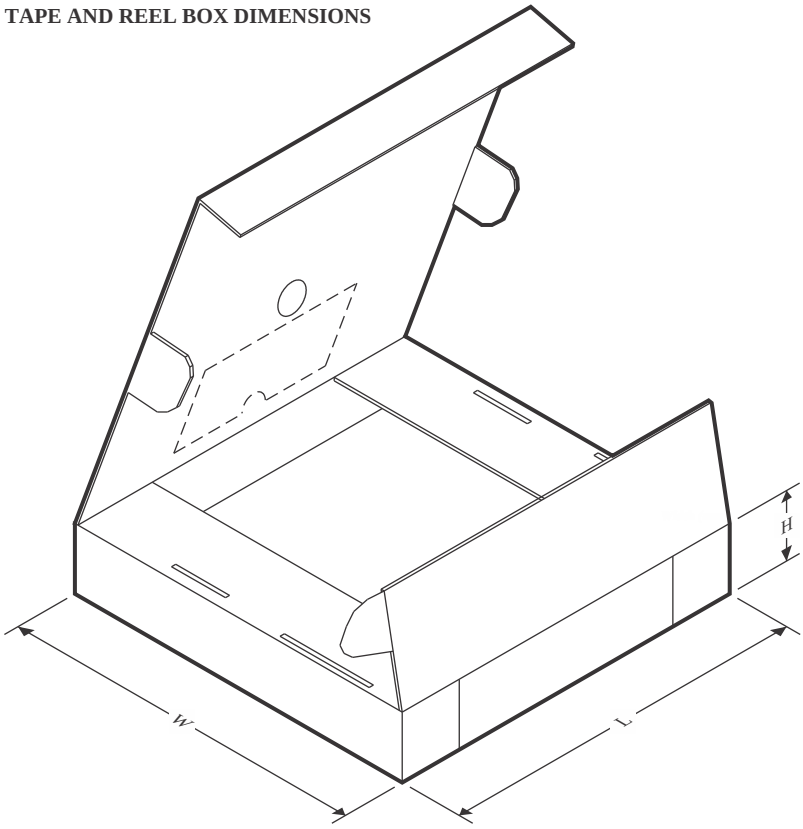
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6C5712QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

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