

ADC08060 8-Bit, 20 MSPS to 60 MSPS, 1.3 m W/MSPS A/D Converter with Internal Sample-and-Hold

Check for Samples: [ADC08060](#)

FEATURES

- Single-Ended Input
- Internal Sample-and-Hold Function
- Low Voltage (Single +3V) Operation
- Small Package
- Power-Down Feature

KEY SPECIFICATION

- Resolution: 8 bits
- Maximum Sampling Frequency: 60 MSPS (min)
- DNL: 0.4 LSB(typ)
- ENOB 7.5bits (typ) at $f_{IN} = 25$ MHz
- THD: -60 dB (typ)
- Power Consumption
 - Operating: 1.3 mW/MSPS (typ)
 - Power Down Mode: 1 mW (typ)

APPLICATIONS

- Digital Imaging Systems
- Communication Systems
- Portable Instrumentation
- Viterbi Decoders
- Set-Top Boxes

DESCRIPTION

The ADC08060 is a low-power, 8-bit, monolithic analog-to-digital converter with an on-chip track-and-hold circuit. Optimized for low cost, low power, small size and ease of use, this product operates at conversion rates of 20 MSPS to 70 MSPS with outstanding dynamic performance over its full operating range while consuming just 1.3 mW per MHz of clock frequency. That's just 78 mW of power at 60 MSPS. Raising the PD pin puts the ADC08060 into a Power Down mode where it consumes just 1 mW.

The unique architecture achieves 7.5 Effective Bits with 25 MHz input frequency. The excellent DC and AC characteristics of this device, together with its low power consumption and single +3V supply operation, make it ideally suited for many imaging and communications applications, including use in portable equipment. Furthermore, the ADC08060 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08060's reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 3V or 2.5V logic. The output coding is straight binary and the digital inputs (CLK and PD) are TTL/CMOS compatible.

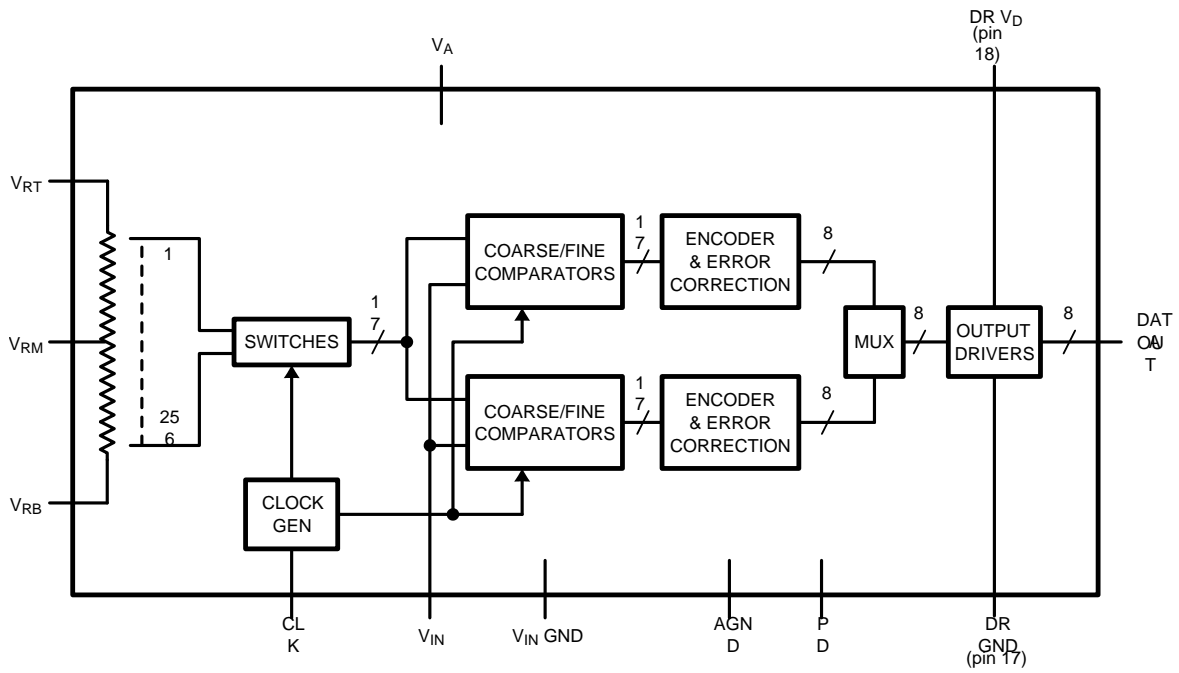
The ADC08060 is offered in a 24-lead TSSOP package and is specified over the industrial temperature range of -40°C to $+85^{\circ}\text{C}$.



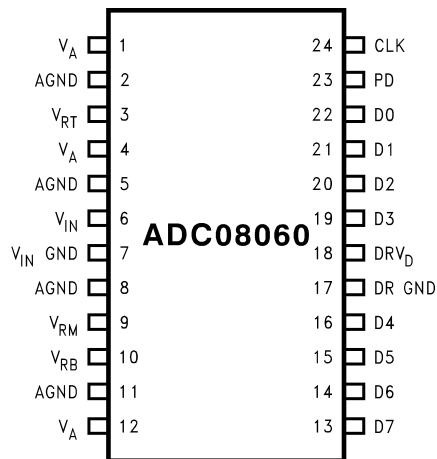
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Block Diagram



Pin Configuration



**Figure 1. 24-Lead TSSOP
See PW Package**

PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS

Pin No.	Symbol	Equivalent Circuit	Description
6	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT} .
3	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 1.0V to V_A . Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See THE ANALOG INPUT for more information.
9	V_{RM}		Mid-point of the reference ladder. This pin should be bypassed to a clean, quiet point in the analog ground plane with a 0.1 μ F capacitor.
10	V_{RB}		Analog Input that is the low side (bottom) of the reference ladder of the ADC. Nominal range is 0.0V to ($V_{RT} - 1.0$ V). Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See THE ANALOG INPUT for more information.
23	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins hold the last conversion result.
24	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the falling edge of CLK input.
13 thru 16 and 19 thru 22	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input.
7	V_{IN} GND		Reference ground for the single-ended analog input, V_{IN} .
1, 4, 12	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +3V. V_A should be bypassed with a 0.1 μ F ceramic chip capacitor for each pin, plus one 10 μ F capacitor. See POWER SUPPLY CONSIDERATIONS for more information.
18	DR V_D		Power supply for the output drivers. If connected to V_A , decouple well from V_A .
17	DR GND		The ground return for the output driver supply.
2, 5, 8, 11	AGND		The ground return for the analog supply.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

Supply Voltage (V_A)	3.8V	
Driver Supply Voltage (DR V_D)	$V_A + 0.3V$	
Voltage on Any Input or Output Pin	-0.3V to V_A	
Reference Voltage (V_{RT} , V_{RB})	V_A to AGND	
CLK, \overline{OE} Voltage Range	-0.3V to ($V_A + 0.3V$)	
Digital Output Voltage (V_{OH} , V_{OL})	DR GND to DR V_D	
Input Current at Any Pin (4)	± 25 mA	
Package Input Current (4)	± 50 mA	
Power Dissipation at $T_A = 25^\circ\text{C}$	See (5)	
ESD Susceptibility (6)	Human Body Model	2500V
	Machine Model	250V
Soldering Temperature, Infrared, 10 seconds (7)	235°C	
Storage Temperature	-65°C to +150°C	

- (1) All voltages are measured with respect to GND = AGND = DR GND = 0V, unless otherwise specified.
- (2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) When the input voltage at any pin exceeds the power supplies (that is, less than AGND or DR GND, or greater than V_A or DR V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
- (5) The absolute maximum junction temperature (T_{Jmax}) for this device is 150°C. The maximum allowable power dissipation is dictated by T_{Jmax} , the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_{DMAX} = (T_{Jmax} - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when this device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
- (6) Human body model is 100 pF capacitor discharged through a 1.5 k Ω resistor. Machine model is 220 pF discharged through ZERO Ohms.
- (7) See AN-450, "Surface Mounting Methods and Their Effect on Product Reliability" ().

Operating Ratings (1)(2)

Operating Temperature Range	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
Supply Voltage (V_A)	+2.7V to +3.6V
Driver Supply Voltage (DR V_D)	+2.4V to V_A
Ground Difference GND - DR GND	0V to 300 mV
Upper Reference Voltage (V_{RT})	1.0V to ($V_A + 0.1V$)
Lower Reference Voltage (V_{RB})	0V to ($V_{RT} - 1.0V$)
V_{IN} Voltage Range	V_{RB} to V_{RT}

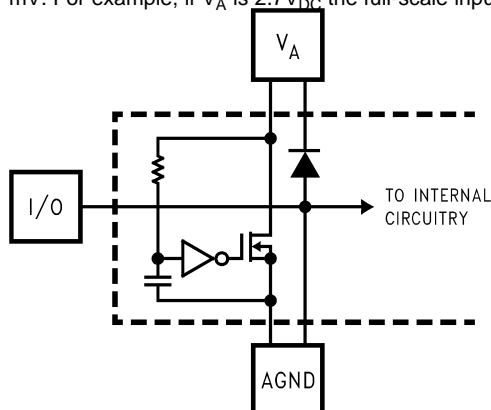
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- (2) All voltages are measured with respect to GND = AGND = DR GND = 0V, unless otherwise specified.

Converter Electrical Characteristics

The following specifications apply for $V_A = DR V_D = +3.0V_{DC}$, $V_{RT} = +1.9V$, $V_{RB} = 0.3V$, $C_L = 10\text{ pF}$, $f_{CLK} = 60\text{ MHz}$ at 50% duty cycle. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ\text{C}$ ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Typical ⁽⁴⁾	Limits ⁽⁴⁾	Units (Limits)
DC ACCURACY					
INL	Integral Non-Linearity		±0.5	±1.3	LSB (max)
DNL	Differential Non-Linearity		±0.4	+1.0 -0.9	LSB (max) LSB (min)
	Missing Codes			0	(max)
FSE	Full Scale Error		18	±28	mV (max)
ZSE	Zero Scale Offset Error		26	±35	mV (max)
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
V_{IN}	Input Voltage		1.6	V_{RB} V_{RT}	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance	$V_{IN} = 0.75V + 0.5\text{ Vrms}$	(CLK LOW)	3	pF
			(CLK HIGH)	4	pF
R_{IN}	R_{IN} Input Resistance		>1		MΩ
BW	Full Power Bandwidth		200		MHz
V_{RT}	Top Reference Voltage		1.9	V_A	V (max)
				1.0	V (min)
V_{RB}	Bottom Reference Voltage		0.3	$V_{RT} - 1.0$	V (max)
				0	V (min)
$V_{RT} - V_{RB}$	Reference Delta		1.6	1.0	V (min)
				2.3	V (max)
R_{REF}	Reference Ladder Resistance	V_{RT} to V_{RB}	220	150	Ω (min)
				300	Ω (max)
I_{REF}	Reference Ladder Current		7.3	5.3	mA (min)
				10.6	mA (max)

- (1) The Electrical characteristics tables list ensured specifications under the listed Recommended Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations for room temperature only and are not ensured.
- (2) The analog inputs are protected as shown below. Input voltage magnitudes up to $V_A + 300\text{ mV}$ or to 300 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above $DR V_D$ or below GND by more than 100 mV. For example, if V_A is $2.7V_{DC}$ the full-scale input voltage must be $\leq 2.6V_{DC}$ to ensure accurate conversions.



- (3) To ensure accuracy, it is required that V_A and $DR V_D$ be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.
- (4) Typical figures are at $T_J = 25^\circ\text{C}$, and represent most likely parametric norms at specific conditions at the time of product characterization and are not ensured. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).

Converter Electrical Characteristics (continued)

The following specifications apply for $V_A = DR$, $V_D = +3.0V_{DC}$, $V_{RT} = +1.9V$, $V_{RB} = 0.3V$, $C_L = 10$ pF, $f_{CLK} = 60$ MHz at 50% duty cycle. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$ ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Typical ⁽⁴⁾	Limits ⁽⁴⁾	Units (Limits)
CLK, PD DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Logical High Input Voltage	DR $V_D = V_A = 3.3V$		2.0	V (min)
V_{IL}	Logical Low Input Voltage	DR $V_D = V_A = 2.7V$		0.8	V (max)
I_{IH}	Logical High Input Current	$V_{IH} = DR$, $V_D = V_A = 3.3V$	10		nA
I_{IL}	Logical Low Input Current	$V_{IL} = 0V$, DR $V_D = V_A = 2.7V$	-50		nA
C_{IN}	Logic Input Capacitance		3		pF
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	High Level Output Voltage	$V_A = DR$, $V_D = 2.7V$, $I_{OH} = -400$ μA	2.6	2.4	V (min)
V_{OL}	Low Level Output Voltage	$V_A = DR$, $V_D = 2.7V$, $I_{OL} = 1.0$ mA	0.4	0.5	V (max)
DYNAMIC PERFORMANCE					
ENOB	Effective Number of Bits	$f_{IN} = 4.4$ MHz, $V_{IN} = -0.25$ dBFS	7.6		Bits
		$f_{IN} = 10$ MHz, $V_{IN} = -0.25$ dBFS	7.6	7.1	Bits (min)
		$f_{IN} = 25$ MHz, $V_{IN} = -0.25$ dBFS	7.5		Bits
		$f_{IN} = 29$ MHz, $V_{IN} = -0.25$ dBFS	7.4		Bits
SINAD	Signal-to-Noise & Distortion	$f_{IN} = 4.4$ MHz, $V_{IN} = -0.25$ dBFS	47		dB
		$f_{IN} = 10$ MHz, $V_{IN} = -0.25$ dBFS	47	44.5	dB (min)
		$f_{IN} = 25$ MHz, $V_{IN} = -0.25$ dBFS	47		dB
		$f_{IN} = 29$ MHz, $V_{IN} = -0.25$ dBFS	46		dB
SNR	Signal-to-Noise Ratio	$f_{IN} = 4.4$ MHz, $V_{IN} = -0.25$ dBFS	47		dB
		$f_{IN} = 10$ MHz, $V_{IN} = -0.25$ dBFS	47	44.6	dB (min)
		$f_{IN} = 25$ MHz, $V_{IN} = -0.25$ dBFS	47		dB
		$f_{IN} = 29$ MHz, $V_{IN} = -0.25$ dBFS	46		dB
SFDR	Spurious Free Dynamic Range	$f_{IN} = 4.4$ MHz, $V_{IN} = -0.25$ dBFS	64		dBc
		$f_{IN} = 10$ MHz, $V_{IN} = -0.25$ dBFS	63		dBc
		$f_{IN} = 25$ MHz, $V_{IN} = -0.25$ dBFS	60		dBc
		$f_{IN} = 29$ MHz, $V_{IN} = -0.25$ dBFS	54		dBc
THD	Total Harmonic Distortion	$f_{IN} = 4.4$ MHz, $V_{IN} = -0.25$ dBFS	-64		dBc
		$f_{IN} = 10$ MHz, $V_{IN} = -0.25$ dBFS	-63		dBc
		$f_{IN} = 25$ MHz, $V_{IN} = -0.25$ dBFS	-57		dBc
		$f_{IN} = 29$ MHz, $V_{IN} = -0.25$ dBFS	-54		dBc
HD2	2nd Harmonic Distortion	$f_{IN} = 4.4$ MHz, $V_{IN} = -0.25$ dBFS	-70		dBc
		$f_{IN} = 10$ MHz, $V_{IN} = -0.25$ dBFS	-65		dBc
		$f_{IN} = 25$ MHz, $V_{IN} = -0.25$ dBFS	-64		dBc
		$f_{IN} = 29$ MHz, $V_{IN} = -0.25$ dBFS	-54		dBc
HD3	3rd Harmonic Distortion	$f_{IN} = 4.4$ MHz, $V_{IN} = -0.25$ dBFS	-72		dBc
		$f_{IN} = 10$ MHz, $V_{IN} = -0.25$ dBFS	-70		dBc
		$f_{IN} = 25$ MHz, $V_{IN} = -0.25$ dBFS	-68		dBc
		$f_{IN} = 29$ MHz, $V_{IN} = -0.25$ dBFS	-65		dBc
IMD	Intermodulation Distortion	$f_1 = 11$ MHz, $V_{IN} = -6.25$ dBFS $f_2 = 12$ MHz, $V_{IN} = -6.25$ dBFS	-55		dBc

Converter Electrical Characteristics (continued)

The following specifications apply for $V_A = DR$, $V_D = +3.0V_{DC}$, $V_{RT} = +1.9V$, $V_{RB} = 0.3V$, $C_L = 10$ pF, $f_{CLK} = 60$ MHz at 50% duty cycle. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$ ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Typical ⁽⁴⁾	Limits ⁽⁴⁾	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	DC Input	25	31	mA (max)
		$f_{IN} = 10$ MHz, $V_{IN} = -3$ dBFS	25		mA
$DR I_D$	Output Driver Supply Current	DC Input	0.3	1	mA (max)
		$f_{IN} = 10$ MHz, $V_{IN} = 3$ dBFS ⁽⁵⁾	4.4		mA
$I_A + DR I_D$	Total Operating Current	DC Input	25.3	32	mA (max)
		$f_{IN} = 10$ MHz, $V_{IN} = -3$ dBFS, PD = Low	29.4		mA (max)
		CLK Low, PD = Hi	0.2		
PC	Power Consumption	DC Input	76	96	mW (max)
		$f_{IN} = 10$ MHz, $V_{IN} = -3$ dBFS, PD = Low	88		mW
		CLK Low, PD = Hi	0.6		mW
$PSRR_1$	Power Supply Rejection Ratio	FSE change with 2.7V to 3.3V change in V_A	54		dB
$PSRR_2$	Power Supply Rejection Ratio	SNR change with 200 mV at 200 kHz on supply	45		dB
AC ELECTRICAL CHARACTERISTICS					
f_{C1}	Maximum Conversion Rate		70	60	MHz (min)
f_{C2}	Minimum Conversion Rate		20		MHz
t_{CL}	Minimum Clock Low Time			6.7	ns (min)
t_{CH}	Minimum Clock High Time			6.7	ns (min)
t_{OH}	Output Hold Time	CLK Rise to Data Invalid	4.4		ns
t_{OD}	Output Delay	CLK Rise to Data Valid	8.2	12	ns (max)
	Pipeline Delay (Latency)		2.5		Clock Cycles
t_{AD}	Sampling (Aperture) Delay	CLK Fall to Acquisition of Data	1.5		ns
t_{AJ}	Aperture Jitter		2		ps rms

- (5) I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by the load capacitance on the output pins, the supply voltage, V_{DR} , and the rate at which the outputs are switching (which is signal dependent), $I_{DR} = V_{DR} (C_O \times f_O + C_1 \times f_1 + \dots + C_{71} \times f_7)$ where V_{DR} is the output driver power supply voltage, C_n is the total capacitance on any given output pin, and f_n is the average frequency at which that pin is toggling.

Typical Performance Characteristics

$V_A = DR$ $V_D = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated

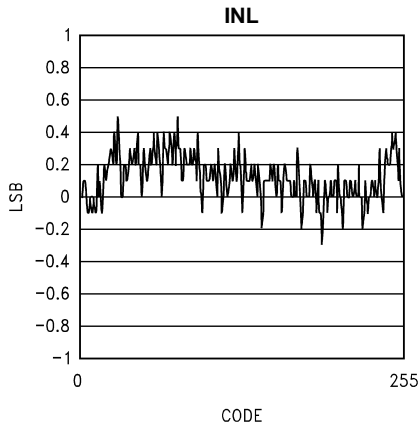


Figure 2.

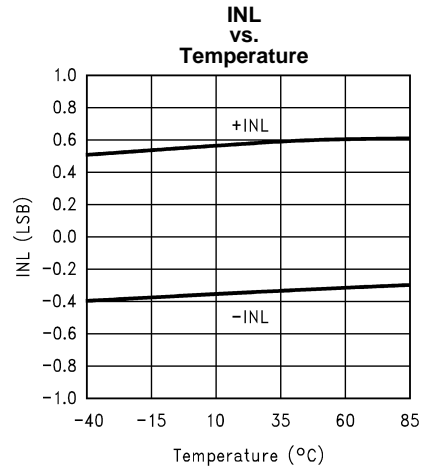


Figure 3.

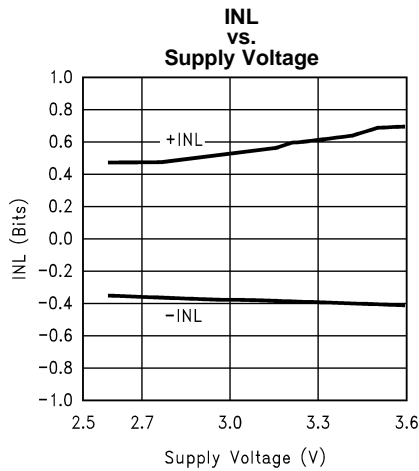


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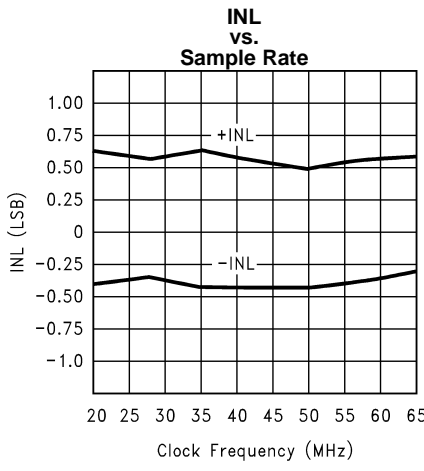


Figure 5.

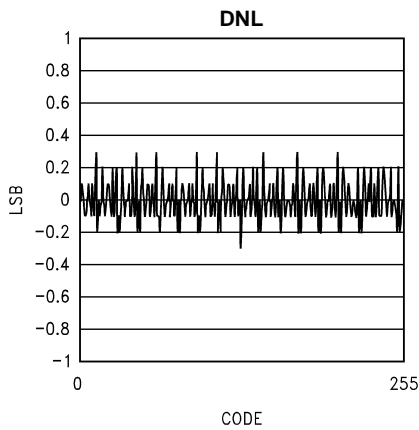


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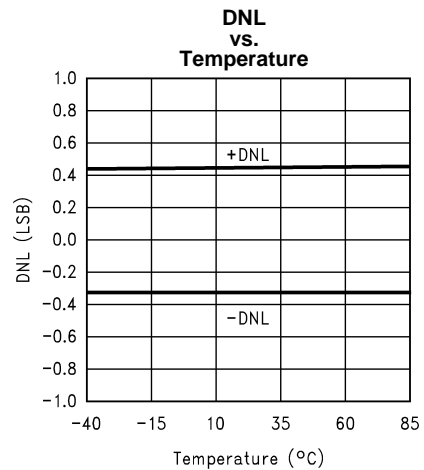


Figure 7.

Typical Performance Characteristics (continued)

$V_A = DR V_D = 3V$, $f_{CLK} = 60\text{ MHz}$, $f_{IN} = 10\text{ MHz}$, unless otherwise stated

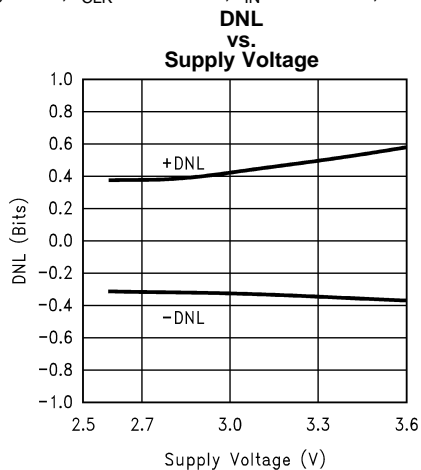


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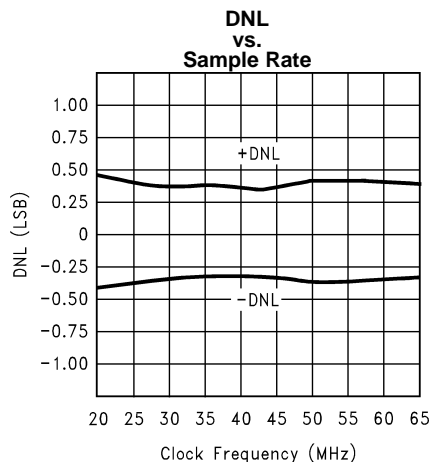


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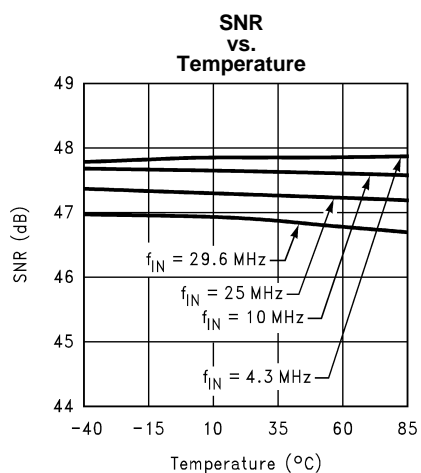


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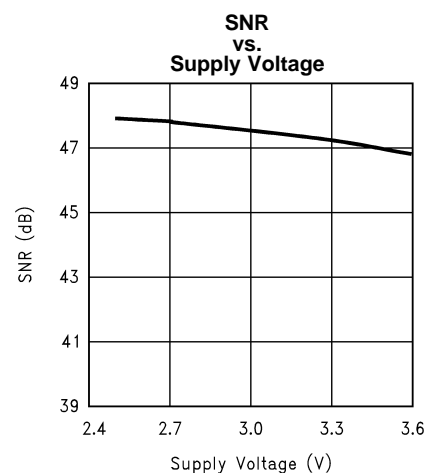


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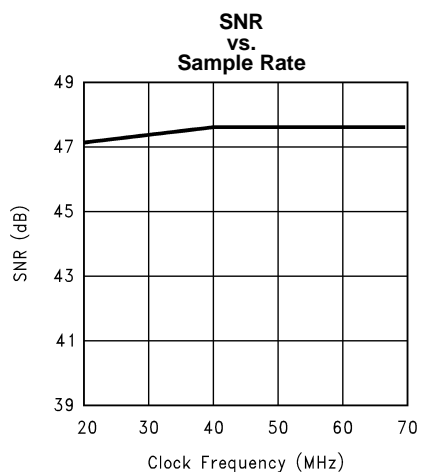


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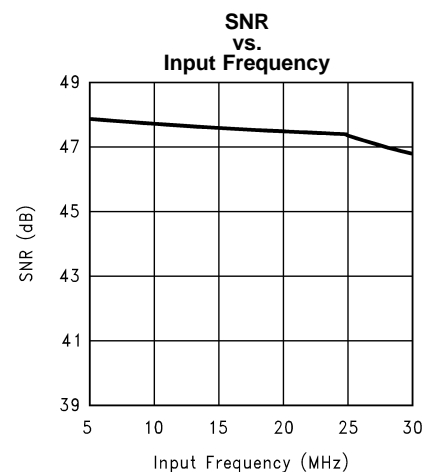


Figure 13.

Typical Performance Characteristics (continued)

$V_A = DR$ $V_D = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated

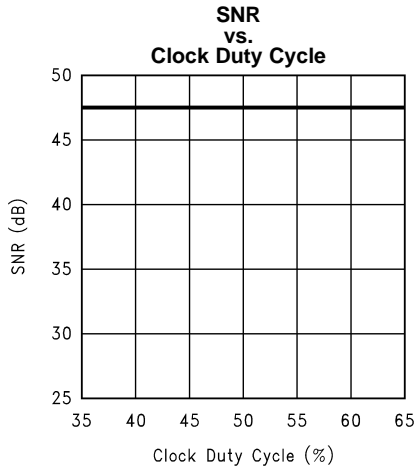


Figure 14.

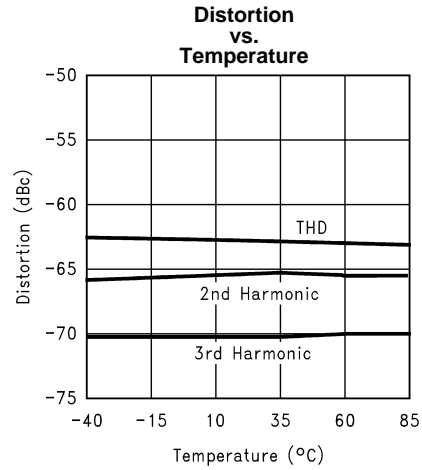


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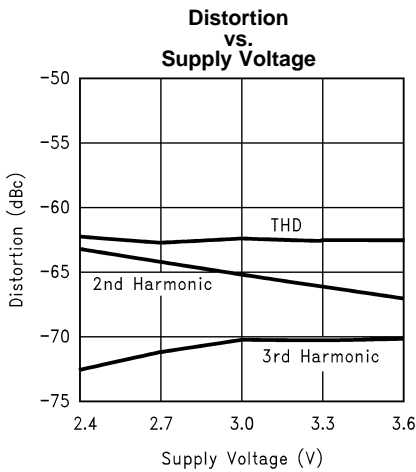


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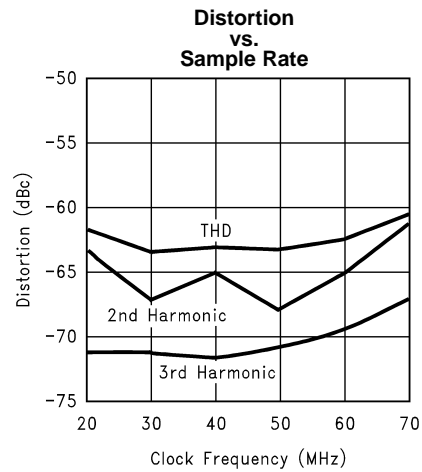


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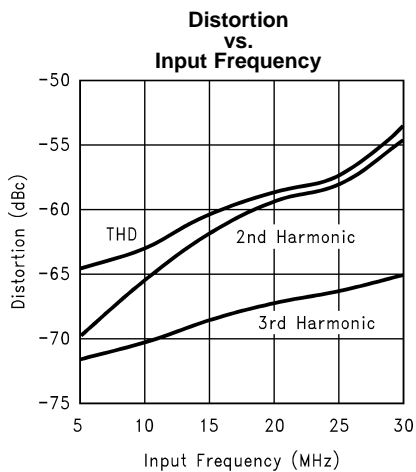


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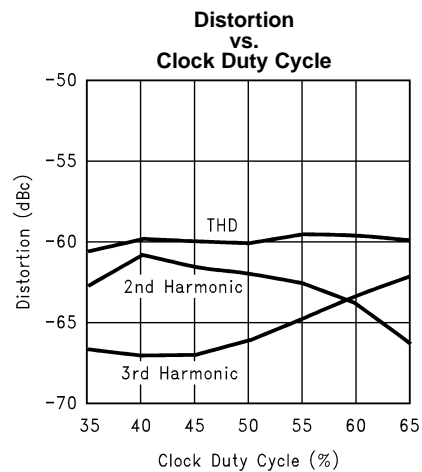


Figure 19.

Typical Performance Characteristics (continued)

$V_A = DR$ $V_D = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated

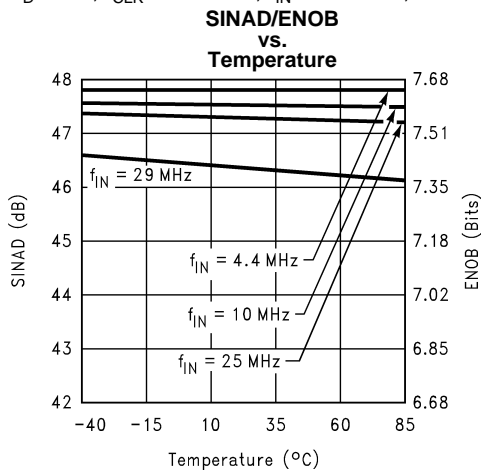


Figure 20.

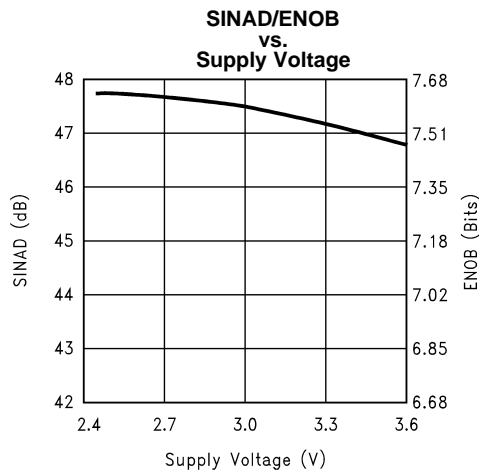


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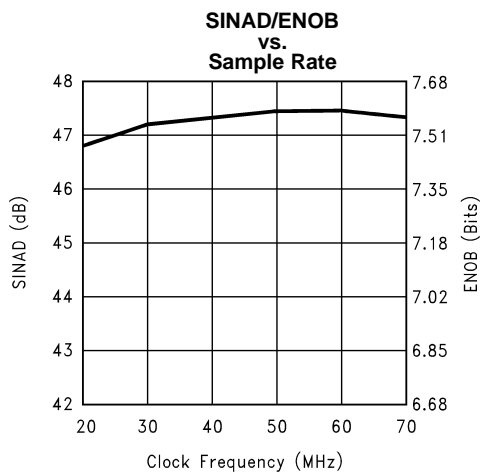


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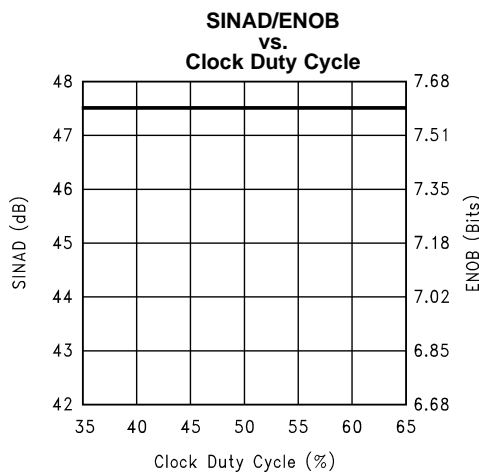


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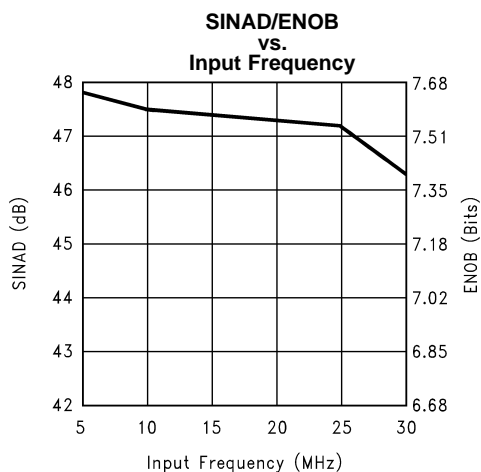


Figure 24.

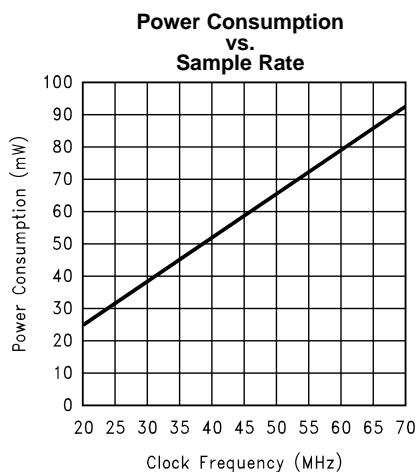
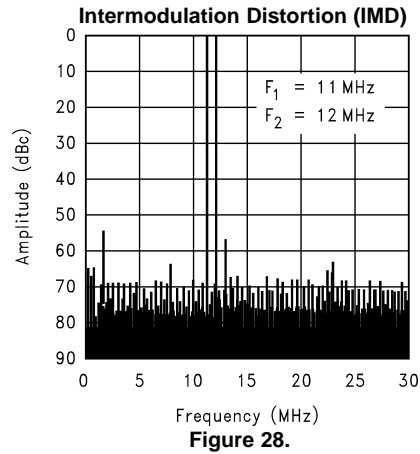
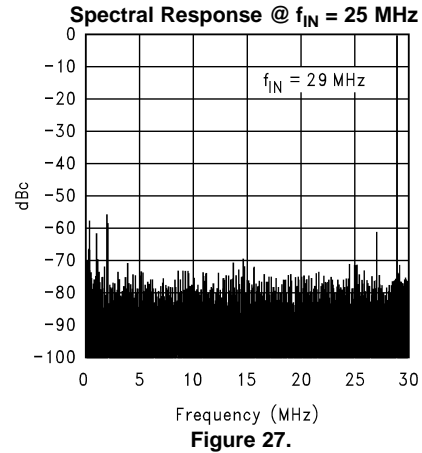
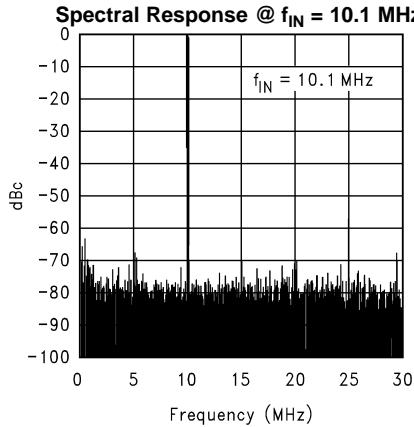


Figure 25.

Typical Performance Characteristics (continued)

$V_A = DR$ $V_D = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated



Specification Definitions

APERTURE (SAMPLING) DELAY is that time required after the fall of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the “hold” mode t_{AD} after the clock goes low.

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as noise at the output.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 60 MSPS with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as $(\text{SINAD} - 1.76) / 6.02$ and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL-POWER BANDWIDTH is the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL-SCALE ERROR is a measure of how far the last code transition is from the ideal $1\frac{1}{2}$ LSB below V_{RT} and is defined as:

$$V_{\max} + 1.5 \text{ LSB} - V_{RT}$$

where

- V_{\max} is the voltage at which the transition to the maximum (full scale) code occurs (1)

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from zero scale ($\frac{1}{2}$ LSB below the first code transition) through positive full scale ($\frac{1}{2}$ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. Measured at 60 MSPS with a ramp input.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of the interaction between two sinusoidal frequencies that are applied to the ADC input at the same time. IMD is the ratio of the power in the second and third order intermodulation products to the total power in the original frequencies.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC08060, PSRR1 is the ratio of the change in d.c. power supply voltage to the resulting change in Full-Scale Error, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected and is here defined as:

$$\text{PSRR2} = 20\text{Log} \left(4 \sqrt{10^{\frac{-\text{SNR1}}{10}} - 10^{\frac{-\text{SNR0}}{10}}} \right)$$

where

- SNR0 is the SNR measured with no noise or signal on the supply lines and SNR1 is the SNR measured with a 200 kHz, 200 mV_{P-P} signal riding upon the supply lines (2)

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data changes at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the Output Delay.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal frequency at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal frequency at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal frequency at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + f_3^2 + f_4^2 + f_5^2 + f_6^2 + f_7^2 + f_8^2 + f_9^2 + f_{10}^2}{f_1^2}}$$

where

- f_1 is the RMS power of the fundamental (input) frequency
 - f_2 through f_{10} is the power in the first 9 harmonics in the output spectrum
- (3)

ZERO SCALE OFFSET ERROR is the error in the input voltage required to cause the first code transition. It is defined as

$$V_{OFF} = V_{ZT} - V_{RB}$$

where

- V_{ZT} is the first code transition input voltage
- (4)

Timing Diagram

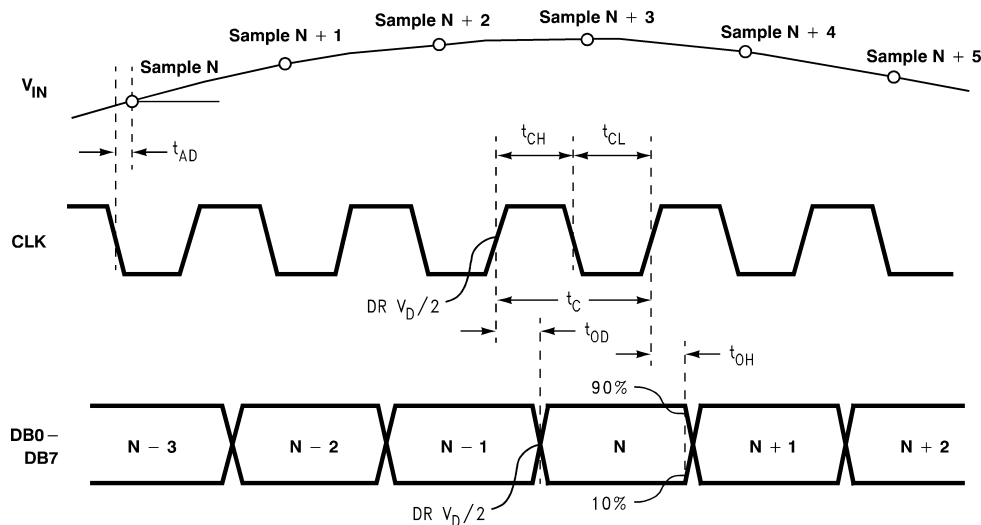


Figure 29. ADC08060 Timing Diagram

FUNCTIONAL DESCRIPTION

The ADC08060 uses a new, unique architecture that achieves over 7.4 effective bits at input frequencies up to 30 MHz.

The analog input signal that is within the voltage range set by V_{RT} and V_{RB} is digitized to eight bits. Output format is straight binary. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RB} will cause the output word to consist of all ones.

Incorporating a switched capacitor bandgap, the ADC08060 exhibits a power consumption that is proportional to frequency, limiting power consumption to what is needed at the clock rate that is used. This and its excellent performance over a wide range of clock frequencies makes it an ideal choice as a single ADC for many 8-bit needs.

Data is acquired at the falling edge of the clock and the digital equivalent of that data is available at the digital outputs 2.5 clock cycles plus t_{OD} later. The ADC08060 will convert as long as the clock signal is present. The output coding is straight binary.

The device is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode, where the output pins hold the last conversion before the PD pin went high and the device consumes just 1 mW.

APPLICATIONS INFORMATION

REFERENCE INPUTS

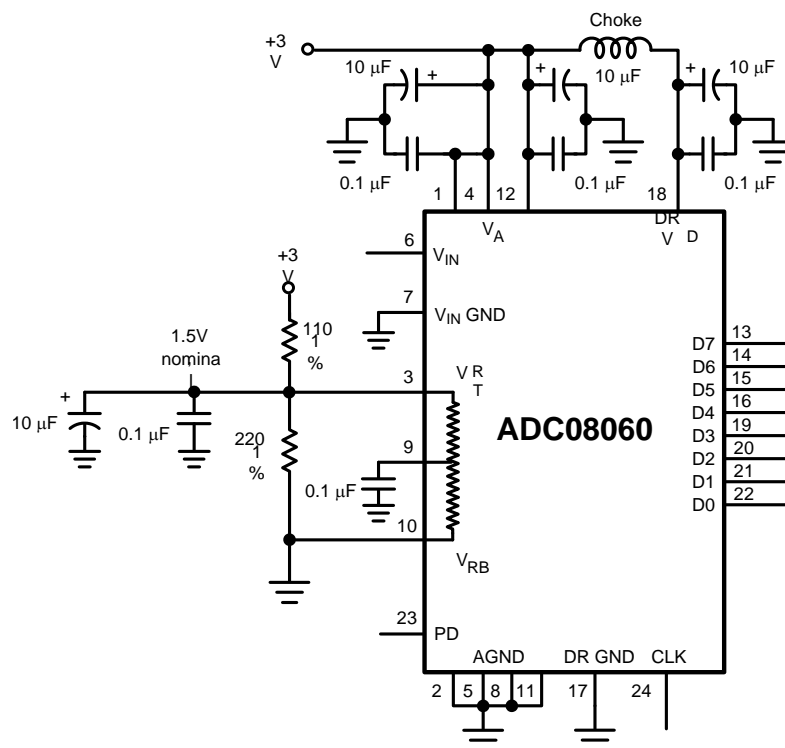
The reference inputs V_{RT} and V_{RB} are the top and bottom of the reference ladder, respectively. Input signals between these two voltages will be digitized to 8 bits. External voltages applied to the reference input pins should be within the range specified in the [Operating Ratings](#) (1.0V to $(V_A + 0.1V)$ for V_{RT} and 0V to $(V_{RT} - 1.0V)$ for V_{RB}). Any device used to drive the reference pins should be able to source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin.

The reference bias circuit of [Figure 30](#) is very simple and the performance is adequate for many applications. However, circuit tolerances will lead to a wide reference voltage range. Superior performance can generally be achieved by driving the reference pins with a low impedance source.

The circuit of [Figure 31](#) will allow a more accurate setting of the reference voltages. The upper amplifier must be able to source the reference current as determined by the value of the reference resistor and the value of $(V_{RT} - V_{RB})$. The lower amplifier must be able to sink this reference current. Both should be stable with a capacitive load. The LM8272 was chosen because of its rail-to-rail input and output capability, its high current output and its ability to drive large capacitance loads. Of course, the divider resistors at the amplifier input could be changed to suit your reference voltage needs, or the divider can be replaced with potentiometers or DACs for precise settings. The bottom of the ladder (V_{RB}) may simply be returned to ground if the minimum input signal excursion is 0V. Be sure that the driving sources can source sufficient current into the V_{RT} pin and sink enough current from the V_{RB} pin to keep these pins stable.

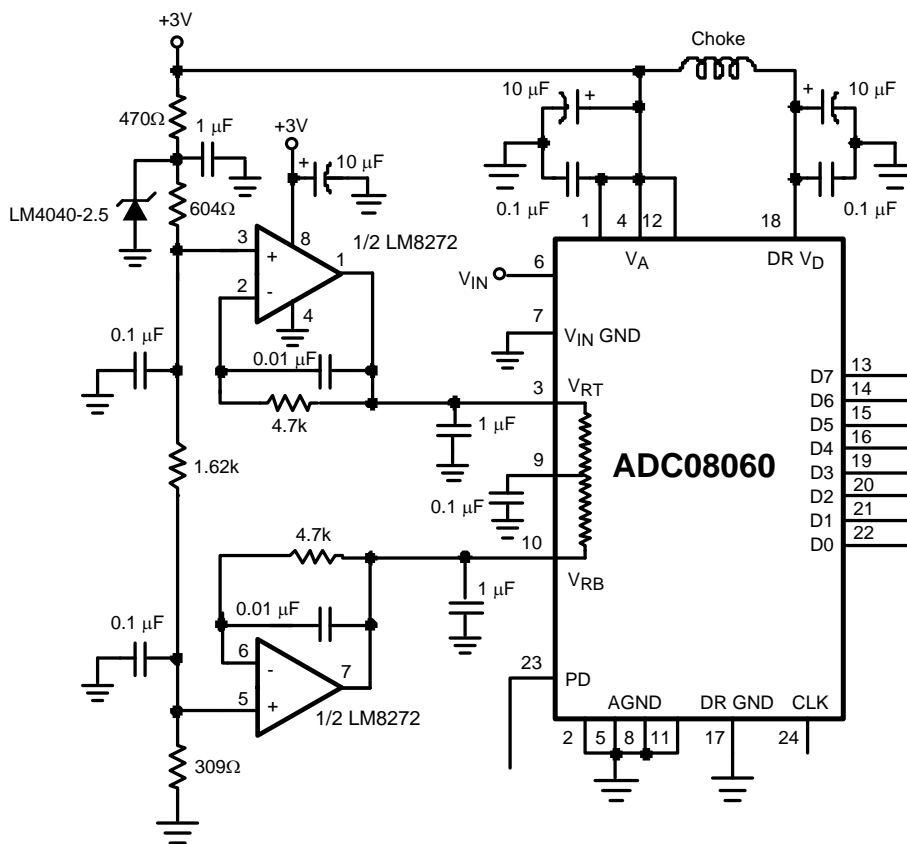
V_{RT} should always be more positive than V_{RB} at least by the minimum $V_{RT} - V_{RB}$ difference in [Electrical Characteristics](#) to minimize noise. Furthermore, the difference between V_{RT} and V_{RB} should not exceed the maximum value specified in [Electrical Characteristics](#) to avoid signal distortion.

V_{RM} (pin 9) is the center of the reference ladder and should be bypassed to a clean, quiet point in the analog ground plane with a 0.1 μF capacitor. DO NOT allow this pin to float.



Because of the ladder and external resistor tolerances, the reference voltage can vary too much for some applications.

Figure 30. Simple, low component count reference biasing.



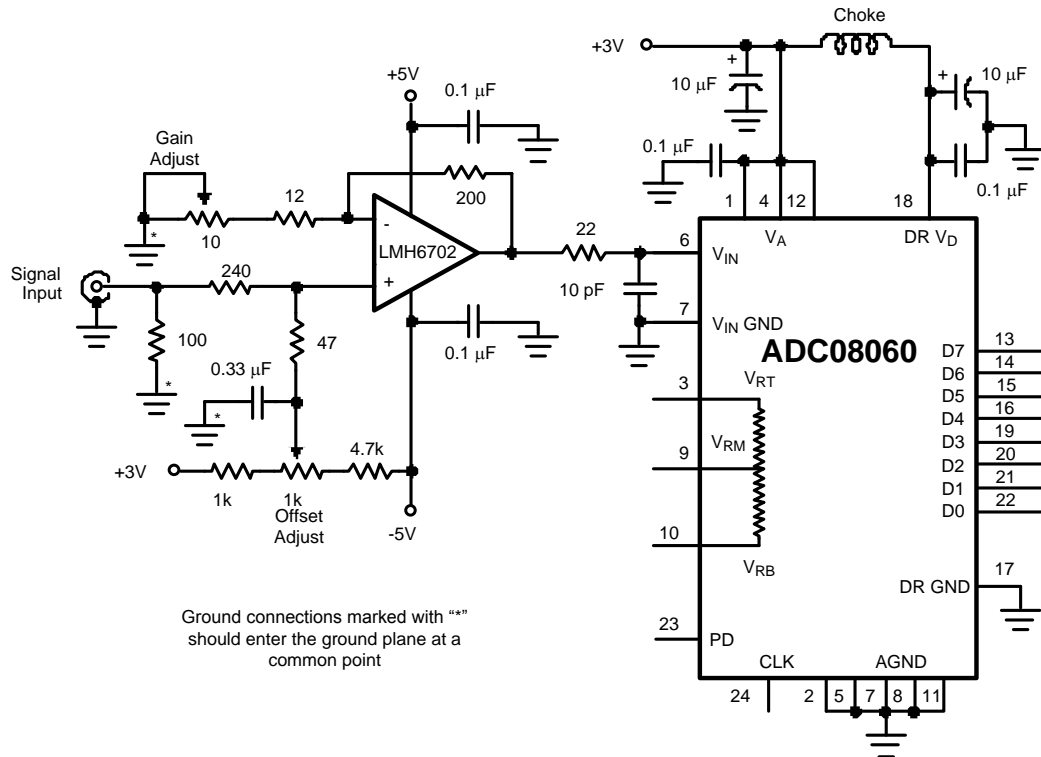
Driving the reference to force desired values requires driving with a low impedance source.

Figure 31.

THE ANALOG INPUT

The analog input of the ADC08060 is a switch followed by an integrator. The input capacitance changes with the clock level, appearing as 3 pF when the clock is low, and 4 pF when the clock is high. The sampling nature of the analog input causes current spikes that result in voltage spikes at the analog input pin. Any circuit used to drive the analog input must be able to drive that input and to settle within the clock high time. The LMH6702 has been found to be a good amplifier to drive the ADC08060.

Figure 32 shows an example of an input circuit using the LMH6702. Any input amplifier should incorporate some gain as operational amplifiers exhibit better phase margin and transient response with gains above 2 or 3 than with unity gain. If an overall gain of less than 3 is required, attenuate the input and operate the amplifier at a higher gain, as shown in Figure 32.



The input amplifier should incorporate some gain for best performance (see text).

Figure 32.

The RC at the amplifier output filters the clock rate energy that comes out of the analog input due to the input sampling circuit. The optimum time constant for this circuit depends not only upon the amplifier and ADC, but also on the circuit layout and board material. A resistor value should be chosen between 18Ω and 47Ω and the capacitor value chose according to the formula

$$C = \frac{1}{2 \cdot \pi \cdot R \cdot f_{CLK}} \quad (5)$$

This will provide optimum SNR performance. Best THD performance is realized when the capacitor and resistor values are both zero. To optimize SINAD, reduce the capacitor or resistor value until SINAD performance is optimized. That is, until $SNR = -THD$. This value will usually be in the range of 40% to 65% of the value calculated with the above formula. An accurate calculation is not possible because of the board material and layout dependence.

The above is intended for oversampling or Nyquist applications. There should be no resistor or capacitor between the ADC input and any amplifier for undersampling applications.

The circuit of [Figure 32](#) has both gain and offset adjustments. If you eliminate these adjustments normal circuit tolerances may cause signal clipping unless care is exercised in the worst case analysis of component tolerances and the input signal excursion is appropriately limited to account for the worst case conditions. Of course, this means that the designer will not be able to depend upon getting a full scale output with maximum signal input.

POWER SUPPLY CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10 μF tantalum or aluminum electrolytic capacitor should be placed within an inch (2.5 cm) of the A/D power pins, with a 0.1 μF ceramic chip capacitor placed within one centimeter of the converter's power supply pins. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source is recommended for the V_A and DR V_D supplies of the ADC08060, these supply pins should be well isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A choke or 27Ω resistor is recommended between these supply lines with adequate bypass capacitors close to the supply pins.

As is the case with all high speed converters, the ADC08060 should be assumed to have little power supply rejection. None of the supplies for the converter should be the supply that is used for other digital circuitry in any system with a lot of digital power being consumed. The ADC supplies should be the same supply used for other analog circuitry.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 300 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08060 power pins.

THE DIGITAL INPUT PINS

The ADC08060 has two digital input pins: The PD pin and the Clock pin.

The PD Pin

The Power Down (PD) pin, when high, puts the ADC08060 into a low power mode where power consumption is reduced to 1 mW. Output data is valid and accurate about 1 microsecond after the PD pin is brought low.

The digital output pins retain the last conversion output code when either the clock is stopped or the PD pin is high.

The ADC08060 Clock

Although the ADC08060 is tested and its performance is ensured with a 60 MHz clock, it typically will function well with clock frequencies from 20 MHz to 70 MHz.

Halting the clock will provide nearly as much power saving as raising the PD pin high. Typical power consumption with a stopped clock is 3 mW, compared to 1 mW when PD is high. The digital outputs will remain in the same state as they were before the clock was halted.

Once the clock is restored (or the PD pin is brought low), there is a time of about 1 μ s before the output data is valid. However, because of the linear relationship between total power consumption and clock frequency, the part requires about 1 μ s after the clock is restarted or substantially changed in frequency before the part returns to its specified accuracy.

The low and high times of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC08060 is designed to maintain performance over a range of duty cycles. While it is specified and performance is ensured with a 50% clock duty cycle and 60 Msps, ADC08060 performance is typically maintained with clock high and low times of 3.3 ns, corresponding to a clock duty cycle range of 40% to 50% with a 60 MHz clock. Note that the clock minimum high and low times may not be used simultaneously.

The **CLOCK** line should be series terminated at the clock source in the characteristic impedance of that line. If the clock line is longer than

$$\frac{t_r}{6 \times t_{PD}}$$

where

- t_r is the clock rise time
- t_{PD} is the propagation rate of the signal along the trace

(6)

If the clock source is used to drive more than just the ADD08060, the **CLOCK** pin should be a.c. terminated with a series RC to ground such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o}$$

where

- t_{PD} is the signal propagation rate down the clock line, "L" is the line length
- Z_0 is the characteristic impedance of the clock line

(7)

This termination should be located as close as possible to, but within one centimeter of, the ADC08060 clock pin. Further, the termination should be beyond the ADC08060 clock pin as seen from the clock source. Typical t_{PD} is about 150 ps/inch on FR-4 board material. For FR-4 board material, the value of C becomes

$$C \geq \frac{6 \times 10^{-10} \times L}{Z_0}$$

where

- L is the length of the clock line in inches

(8)

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A combined analog and digital ground plane should be used.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise because of the skin effect. Total surface area is more important than is total ground plane volume. Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

The DR GND connection to the ground plane should not use the same feedthrough used by other ground connections.

High power digital components should not be located on or near a straight line between the ADC (or any linear component) and the power supply area as the resulting common return current path could cause fluctuation in the analog "ground" return of the ADC.

Generally, analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog AND digital. Even the generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane.

Figure 33 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed together away from any digital components.

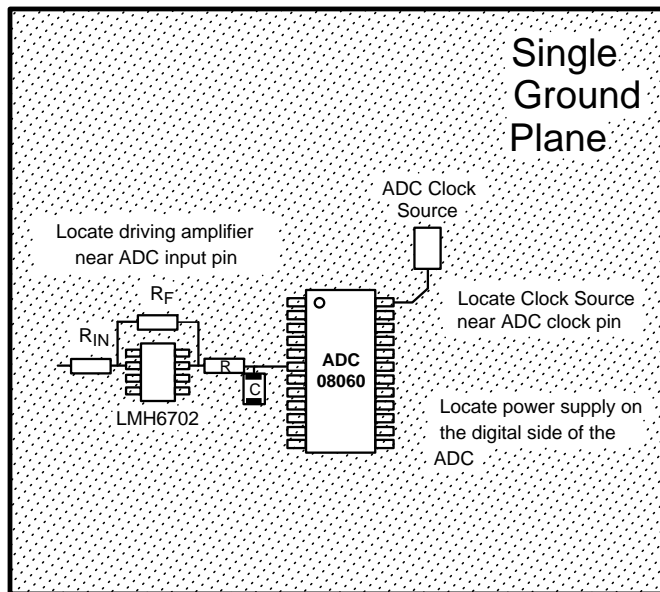


Figure 33. Layout Example

DYNAMIC PERFORMANCE

The ADC08060 is a.c. tested and its dynamic performance is ensured. To meet the published specifications, the clock source driving the CLK input must exhibit less than 10 ps (rms) of jitter. For best a.c. performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See [Figure 34](#).

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal. The clock signal can also introduce noise into the analog path.

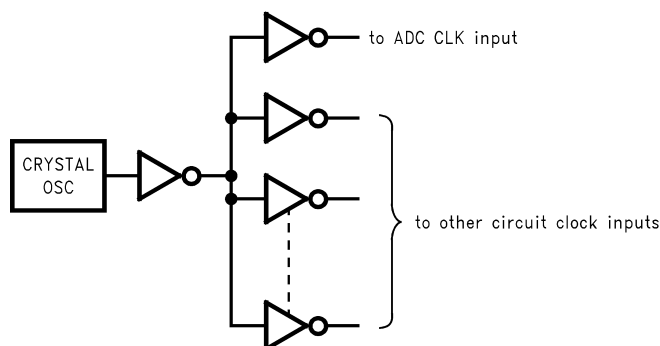


Figure 34. Isolating the ADC Clock from Digital Circuitry

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300 mV below the ground pins or 300 mV above the supply pins. Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground. A 51Ω resistor in series with the offending digital input will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC08060. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current is required from DR V_D and DR GND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs (with a 74F541, for example) may be necessary if the data bus capacitance exceeds 10 pF. Dynamic performance can also be improved by adding 100 Ω series resistors at each digital output, reducing the energy coupled back into the converter input pins.

Using an inadequate amplifier to drive the analog input. As explained in [THE ANALOG INPUT](#), the capacitance seen at the input alternates between 3 pF and 4 pF with the clock. This dynamic capacitance is more difficult to drive than is a fixed capacitance, and should be considered when choosing a driving device. The LMH6702 has been found to be a good device for driving the ADC08060.



Driving the V_{RT} pin or the V_{RB} pin with devices that can not source or sink the current required by the ladder. As mentioned in [REFERENCE INPUTS](#), care should be taken to see that any driving devices can source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin. If these pins are not driven with devices than can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. The use of simple gates with RC timing is generally inadequate as a clock source.

REVISION HISTORY

Changes from Revision G (March 2013) to Revision H	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC08060CIMT/NOPB	ACTIVE	TSSOP	PW	24	61	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	ADC08060 CIMT	
ADC08060CIMTX/NOPB	ACTIVE	TSSOP	PW	24	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	ADC08060 CIMT	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC08060CIMTX/NOPB	TSSOP	PW	24	2500	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC08060CIMTX/NOPB	TSSOP	PW	24	2500	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
ADC08060CIMT/NOPB	PW	TSSOP	24	61	495	8	2514.6	4.06

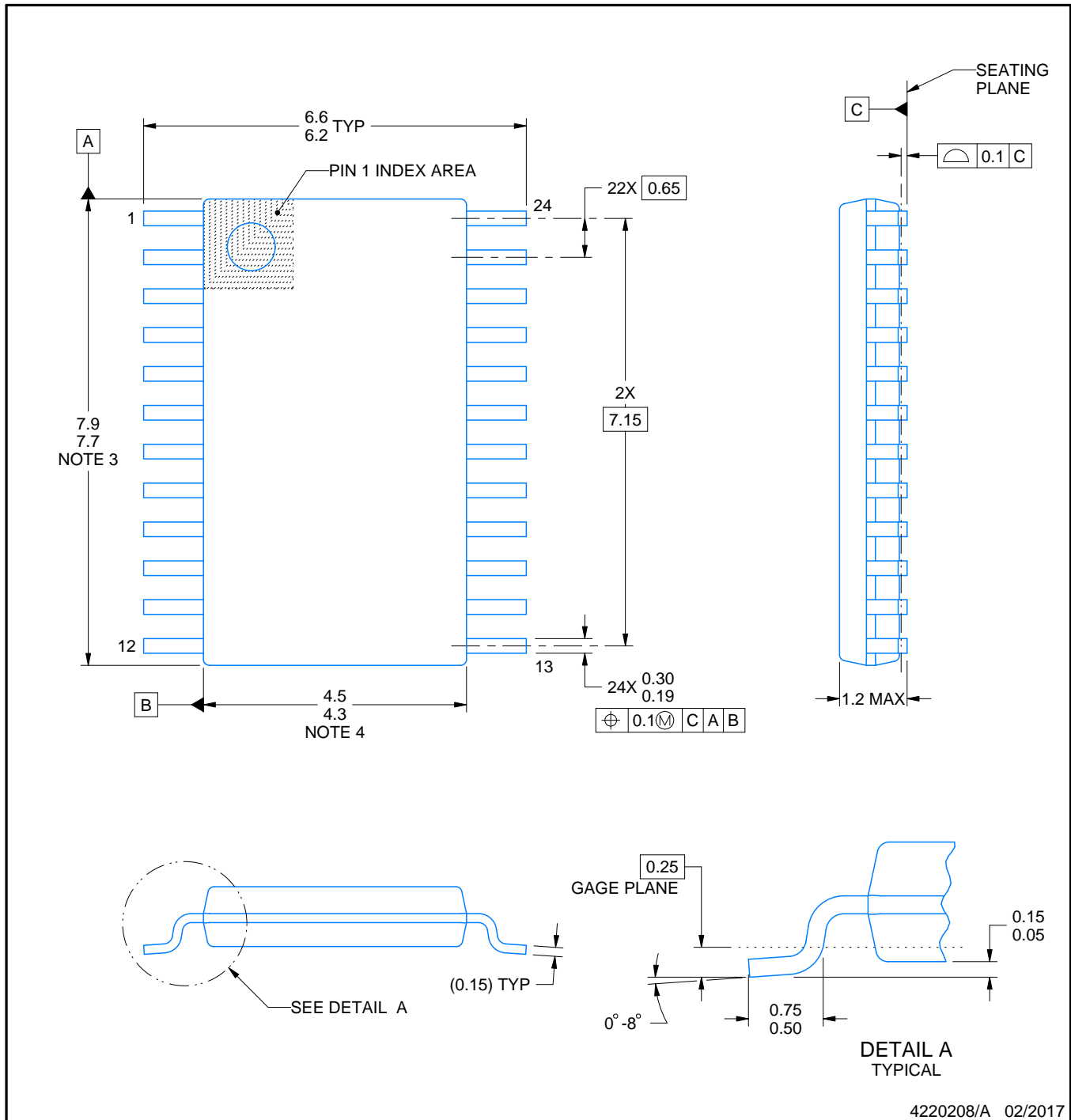
PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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