CLASS V, 14-BIT, 105-MSPS ANALOG-TO-DIGITAL CONVERTER

1 FEATURES

- 14-Bit Resolution
- 105-MSPS Maximum Sample Rate
- SNR = 70 dBc at 105 MSPS and 50 MHz IF
- SFDR = 78 dBc at 105 MSPS and 50 MHz IF
- 2.2-V_{PP} Differential Input Range
- 5-V Supply Operation
- 3.3-V CMOS Compatible Outputs
- 2.3-W Total Power Dissipation
- 2s Complement Output Format
- On-Chip Input Analog Buffer, Track and Hold, and Reference Circuit
- 52-Pin Ceramic Nonconductive Tie-Bar Package (HFG)
- Military Temperature Range (–55°C to 125°C T_{case})
- QML-V Qualified, SMD 5962-07206

2 APPLICATIONS

- Single and Multichannel Digital Receivers
- Base Station Infrastructure
- Instrumentation
- Video and Imaging
- Engineering Evaluation (/EM) Samples are Available (1)

3 RELATED DEVICES

- Clocking: CDC7005
- Amplifiers: OPA695, THS4509

(1) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. No Burn-In, etc.) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of - 55°C to 125°C or operating life.

4 DESCRIPTION

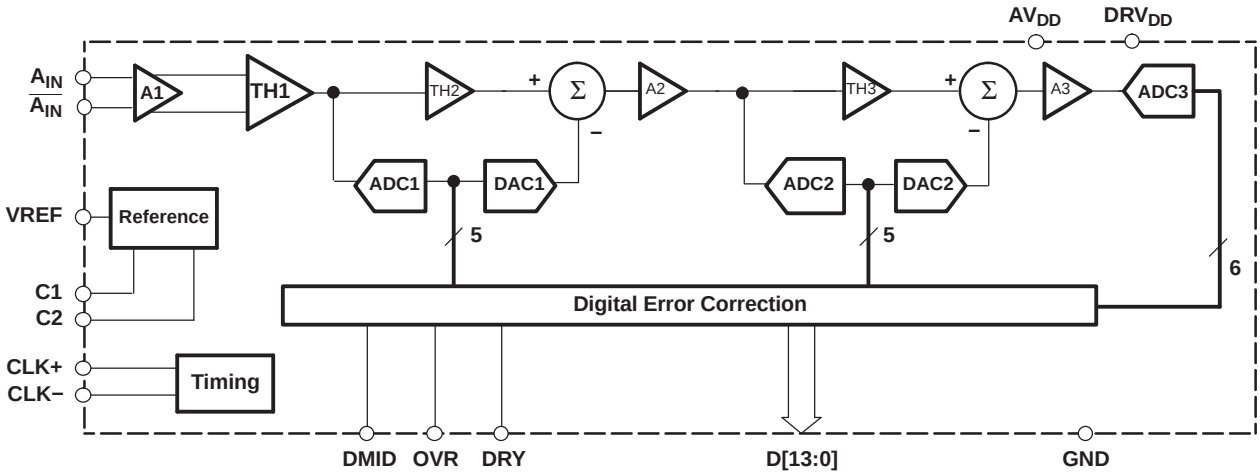
The ADS5424 is a 14-bit, 105-MSPS analog-to-digital converter (ADC) that operates from a 5-V supply, while providing 3.3-V CMOS compatible digital outputs. The ADS5424 input buffer isolates the internal switching of the on-chip track and hold (T&H) from disturbing the signal source. An internal reference generator is also provided to further simplify the system design. The ADS5424 has outstanding low noise and linearity, over input frequency. With only a 2.2-V_{PP} input range, ADS5424 simplifies the design of multicarrier applications, where the carriers are selected on the digital domain.

The ADS5424 is available in a 52-pin ceramic nonconductive tie-bar package (HFG). The ADS5424 is built on state of the art Texas Instruments complementary bipolar process (BiCom3) and is specified over full military temperature range (–55°C to 125°C T_{case}).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



4.1 ABSOLUTE MAXIMUM RATINGS

over operating temperature range (unless otherwise noted)(1)

		ADS5424	UNIT
Supply voltage	AV_{DD} to GND	6	V
	DRV_{DD} to GND	5	
Analog input to GND		–0.3 V to AV_{DD} + 0.3	V
Clock input to GND		–0.3 V to AV_{DD} + 0.3	V
CLK to $\overline{CLK}$		±2.5	V
Digital data output to GND		–0.3 V to DRV_{DD} + 0.3	V
T_C	Characterized case operating temperature range	–55°C to 125	°C
T_J	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	–65°C to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.

4.2 RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
SUPPLIES					
AV_{DD}	Analog supply voltage	4.75	5	5.25	V
DRV_{DD}	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input range		2.2		V_{PP}
V_{CM}	Input common mode voltage		2.4		V
DIGITAL OUTPUT					
	Maximum output load		10		pF
CLOCK INPUT					
	ADCLK input sample rate (sine wave)	30		105	MSPS
	Clock amplitude, differential sine wave		3		V_{PP}
	Clock duty cycle		50%		
T_C	Open case temperature range	–55		125	°C

4.3 ELECTRICAL CHARACTERISTICS (Unchanged after 100 kRad)

Typical values at T_C = 25°C, Over full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 105 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3-V_{PP} sinusoidal clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution				14		Bits
ANALOG INPUTS							
	Differential input range				2.2		V_{pp}
	Differential input resistance	See Figure 11			1		kΩ
	Differential input capacitance	See Figure 11			1.5		pF
	Analog input bandwidth				570		MHz
INTERNAL REFERENCE VOLTAGES							
V_{REF}	Reference voltage			2.38	2.4	2.41	V
DYNAMIC ACCURACY							
	No missing codes				Tested		
DNL	Differential linearity error	f_{IN} = 10 MHz		–0.98	±0.5	1.5	LSB
INL	Integral linearity error	f_{IN} = 10 MHz	T_C= 25°C and $T_{C,MAX}$	–5.0	±3.0	+5.0	LSB
		f_{IN} = 10 MHz	T_C= $T_{C,MIN}$	–-6.9		+6.9	LSB
	Offset error			–1.5	0	1.5	%FS
	Offset temperature coefficient				0.0007		%FS/°C
	Gain error			–5	0.9	5	%FS
	Gain temperature coefficient				0.006		%FS/°C
POWER SUPPLY							
I_{AVDD}	Analog supply current	V_{IN} = full scale, f_{IN} = 70 MHz	F_S = 105 MSPS		355	410	mA
I_{DRVDD}	Output buffer supply current	V_{IN} = full scale, f_{IN} = 70 MHz	F_S = 105 MSPS		47	55	mA
	Power dissipation	Total power with 10-pF load on each digital output to ground, f_{IN} = 70 MHz	F_S = 105 MSPS		1.9	2.3	W
	Power-up time		F_S = 105 MSPS		20		ms

ELECTRICAL CHARACTERISTICS (Unchanged after 100 kRad) (continued)

Typical values at T_C = 25°C, Over full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 105 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3-V_{PP} sinusoidal clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC AC CHARACTERISTICS							
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz	T_C= 25°C	70.5	72.4		dBc
			T_C = $T_{C,MAX}$	71.0			
			T_C= $T_{C,MIN}$	70.5			
		f_{IN} = 30 MHz	Full Temp Range	70.0	71.5		
		f_{IN} = 50 MHz			70.9		
		f_{IN} = 70 MHz	T_C= 25°C	68.2	70.1		
			T_C = $T_{C,MAX}$	67.0			
			T_C= $T_{C,MIN}$	68.0			
		f_{IN} = 100 MHz			68.9		
		f_{IN} = 170 MHz			66.3		
		f_{IN} = 230 MHz			64.0		
SFDR	Spurious free dynamic range	f_{IN} = 10 MHz	T_C = 25°C	72.0	81.6		dBc
			Full Temp Range	71.0			
		f_{IN} = 30 MHz	T_C= 25°C	77.0	80.6		
			T_C = $T_{C,MAX}$	69.0			
			T_C= $T_{C,MIN}$	75.0			
		f_{IN} = 50 MHz			78.1		
		f_{IN} = 70 MHz	T_C= 25°C	68.0	82.6		
			T_C = $T_{C,MAX}$	69.0			
			T_C= $T_{C,MIN}$	67.0			
		f_{IN} = 100 MHz			82.5		
		f_{IN} = 170 MHz			68.0		
		f_{IN} = 230 MHz			65.4		
SINAD	Signal-to-noise + distortion	f_{IN} = 10 MHz	T_C= 25°C	68.6	71.3		dBc
			T_C = $T_{C,MAX}$	68.3			
			T_C= $T_{C,MIN}$	68.2			
		f_{IN} = 30 MHz	T_C= 25°C	69.4	70.2		
			T_C = $T_{C,MAX}$	67.0			
			T_C= $T_{C,MIN}$	69.4			
		f_{IN} = 50 MHz			69.9		
		f_{IN} = 70 MHz	T_C= 25°C	65.8	69.7		
			T_C = $T_{C,MAX}$	64.6			
			T_C= $T_{C,MIN}$	65.0			
		f_{IN} = 100 MHz			68.6		
		f_{IN} = 170 MHz			64.0		
		f_{IN} = 230 MHz			61.1		

ELECTRICAL CHARACTERISTICS (Unchanged after 100 kRad) (continued)

Typical values at T_C = 25°C, Over full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 105 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3-V_{PP} sinusoidal clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD2	Second harmonic	f_{IN} = 10 MHz	T_C = 25°C	72.0	81.8		dBc
			Full Temp Range	71.0			
		f_{IN} = 30 MHz	T_C= 25°C	77.0	80.6		
			T_C = $T_{C,MAX}$	69.0			
			T_C= $T_{C,MIN}$	75.0			
		f_{IN} = 50 MHz			86.5		
		f_{IN} = 70 MHz	T_C= 25°C	68.0	85.0		
			T_C = $T_{C,MAX}$	69.0			
			T_C= $T_{C,MIN}$	67.0			
		f_{IN} = 100 MHz			86.1		
		f_{IN} = 170 MHz			93.0		
		f_{IN} = 230 MHz			71.0		
HD3	Third harmonic	f_{IN} = 10 MHz	T_C = 25°C	72.0	81.6		dBc
			Full Temp Range	71.0			
		f_{IN} = 30 MHz	T_C= 25°C	77.0	81.3		
			T_C = $T_{C,MAX}$	69.0			
			T_C= $T_{C,MIN}$	75.0			
		f_{IN} = 50 MHz			78.1		
		f_{IN} = 70 MHz	T_C= 25°C	68.0	82.6		
			T_C = $T_{C,MAX}$	69.0			
			T_C= $T_{C,MIN}$	67.0			
		f_{IN} = 100 MHz			83.3		
		f_{IN} = 170 MHz			68.0		
		f_{IN} = 230 MHz			65.4		
	Worst other harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz	Full Temp Range	75.0	85.5		dBc
		f_{IN} = 30 MHz	T_C= 25°C	80.0	83.8		
			T_C = $T_{C,MAX}$	74.0			
			T_C= $T_{C,MIN}$	80.0			
		f_{IN} = 50 MHz			87.0		
		f_{IN} = 70 MHz	T_C= 25°C	74.0	83.0		
			T_C = $T_{C,MAX}$	72.0			
			T_C= $T_{C,MIN}$	74.0			
		f_{IN} = 100 MHz			82.5		
		f_{IN} = 170 MHz			79.8		
		f_{IN} = 230 MHz			78.0		

ELECTRICAL CHARACTERISTICS (Unchanged after 100 kRad) (continued)

Typical values at T_C = 25°C, Over full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 105 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3-V_{PP} sinusoidal clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f_{IN} = 10 MHz	T_C = 25°C	71.0	77.8		dBC
			Full Temp Range	70.0			
		f_{IN} = 30 MHz	T_C= 25°C	75.0	77.4		
			T_C = $T_{C,MAX}$	68.0			
			T_C= $T_{C,MIN}$	73.8			
		f_{IN} = 50 MHz			76.7		
		f_{IN} = 70 MHz	T_C= 25°C	67.4	79.6		
			T_C = $T_{C,MAX}$	67.2			
			T_C= $T_{C,MIN}$	66.4			
		f_{IN} = 100 MHz			79.9		
		f_{IN} = 170 MHz			67.6		
		f_{IN} = 230 MHz			64.1		
ENOB	Effective number of bits	f_{IN} = 10 MHz	T_C= 25°C	11.1	11.7		Bits
			T_C = $T_{C,MAX}$	11.0			
			T_C= $T_{C,MIN}$	11.0			
		f_{IN} = 30 MHz	T_C= 25°C	11.2	11.5		
			T_C = $T_{C,MAX}$	10.8			
			T_C= $T_{C,MIN}$	11.2			
		f_{IN} = 70 MHz	T_C= 25°C	10.6	11.4		
			T_C = $T_{C,MAX}$	10.4			
			T_C= $T_{C,MIN}$	10.5			
	RMS idle channel noise	Input pins tied together			0.9		LSB

4.4 DIGITAL CHARACTERISTICS (Unchanged after 100 kRad)

Typical values at T_C = 25 °C, Over full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, AV_{DD} = 5 V, DRV_{DD} = 3.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Outputs					
Low-level output voltage	C_{LOAD} = 10 pF(1)		0.1	0.6	V
High-level output voltage	C_{LOAD} = 10 pF(1)	2.6	3.2		V
Output capacitance			3		pF
DMID		1.65		1.8	V

(1) Equivalent capacitance to ground of (load + parasitics of transmission lines)

4.5 TIMING CHARACTERISTICS(1)(Unchanged after 100 kRad)

Typical values at T_C = 25°C, Over full temperature range, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, sampling rate = 105 MSPS

PARAMETER		MIN	TYP	MAX	UNIT
Aperture Time					
t_A	Aperture delay		500		ps
t_J	Clock slope independent aperture uncertainty (jitter)		150		fs
k_J	Clock slope dependent jitter factor		50		µV
Clock Input					
t_{CLK}	Clock period		9.5		ns
t_{CLKH}	Clock pulse width high		4.75		ns
t_{CLKL}	Clock pulse width low		4.75		ns
Clock to DataReady (DRY)					
t_{DR}	Clock rising 50% to DRY falling 50%	2.2	3.0	4.7	ns
t_{C_DR}	Clock rising 50% to DRY rising 50%		t_{DR} + t_{CLKH}		ns
$t_{C\_DR\_50\%}$	Clock rising 50% to DRY rising 50% with 50% duty cycle clock	7.0	7.8	9.5	ns
Clock to DATA, OVR(2)					
t_r	Data V_{OL} to data V_{OH} (rise time)		0.6		ns
t_f	Data V_{OH} to data V_{OL} (fall time)		0.6		ns
L	Latency		3		Cycles
t_{su_c}	Valid DATA(3) to clock 50% with 50% duty cycle clock (setup time)	1.8	3.6		ns
t_{h_c}	Clock 50% to invalid DATA(3) (hold time)	2.6	4.1		ns
DataReady (DRY)/DATA, OVR(2)					
$t_{su(DR)\_50\%}$	Valid DATA(3) to DRY 50% with 50% duty cycle clock (setup time)	0.9	1.40		ns
$t_{h(DR)\_50\%}$	DRY 50% to invalid DATA(3) with 50% duty cycle clock (hold time)	3.9	6.3		ns

(1) All values obtained from design and characterization.
(2) Data is updated with clock rising edge or DRY falling edge.
(3) See V_{OH} and V_{OL} levels.

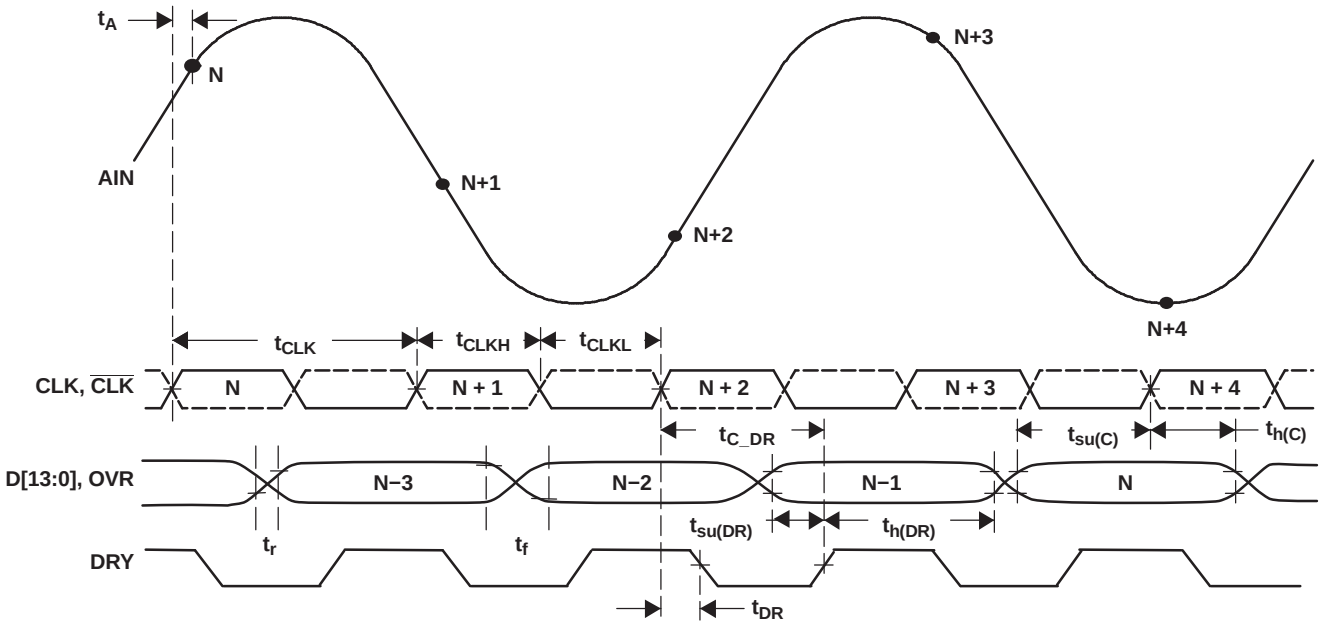
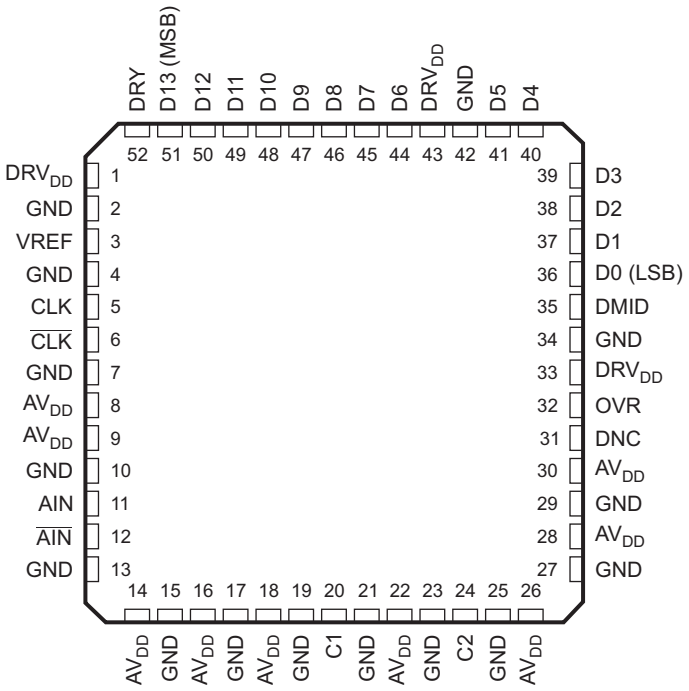


Figure 1. Timing Diagram

5 DEVICE INFORMATION

HFG PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
DRV_{DD}	1, 33, 43	3.3 V power supply, digital output stage only
GND	2, 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, 29, 34, 42	Ground
VREF	3	2.4 V reference. Bypass to ground with a 0.1 µF microwave chip capacitor.
CLK	5	Clock input. Conversion initiated on rising edge
$\overline{CLK}$	6	Complement of CLK, differential input
AV_{DD}	8, 9, 14, 16, 18, 22, 26, 28, 30	5 V analog power supply
AIN	11	Analog input
$\overline{AIN}$	12	Complement of AIN, differential analog input
C1	20	Internal voltage reference. Bypass to ground with a 0.1 µF chip capacitor.
C2	24	Internal voltage reference. Bypass to ground with a 0.1 µF chip capacitor.
DNC	31	Do not connect
OVR	32	Overrange bit. A logic level high indicates the analog input exceeds full scale.
DMID	35	Output data voltage midpoint. Approximately equal to $(DV_{CC})/2$
D0 (LSB)	36	Digital output bit (least significant bit); two's complement
D1–D5, D6–D12	37–41, 44–50	Digital output bits in two's complement
D13 (MSB)	51	Digital output bit (most significant bit); two's complement
DRY	52	Data ready output

5.1 THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board Mounted, Per JESD 51-5 methodology	21.81	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	MIL-STD-883 Test Method 1012	0.849	°C/W

6 Thermal Notes

This CQFP package has built-in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. To efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. TI typically recommends a 16-mm^2 board-mount thermal pad. This allows maximum area for thermal dissipation, while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically at ground potential.

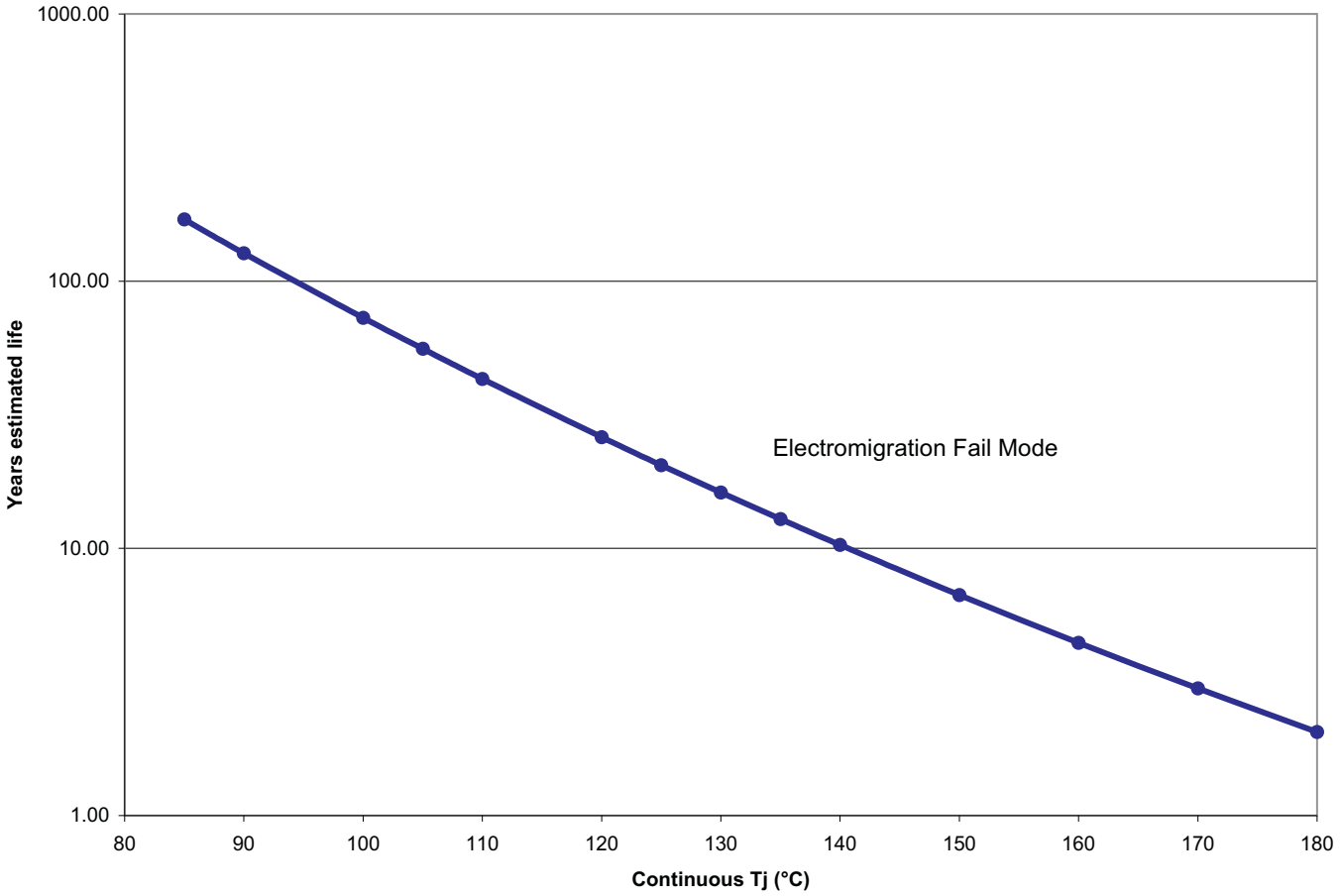


Figure 2. ADS5424 Estimated Device Life at Elevated Temperatures Electromigration Fail Mode

7 DEFINITION OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value

Aperture Delay
The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay

Clock Pulse Width/Duty Cycle
The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate
The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate
The minimum sampling rate at which the ADC functions

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Integral Nonlinearity (INL)
INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function, measured in units of LSB.

Gain Error
Gain error is the deviation of the ADC actual input full-scale range from its ideal value. Gain error is given as a percentage of the ideal input full-scale range.

Offset Error
The offset error is the difference, given in number of LSBs, between the ADC's actual value average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift
The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree celsius of the parameter from T_{MIN} or T_{MAX}. It is computed as the maximum variation of that parameter over the whole temperature range divided by $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

$$SNR = 10Log_{10}\frac{P_S}{P_N}$$

SNR is given either in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)
SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log_{10}\frac{P_S}{P_N + P_D}$$

SINAD is given either in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to Full Scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Total Harmonic Distortion (THD)
THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10Log_{10}\frac{P_S}{P_D}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)
The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion
IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is given either in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when it is referred to the full-scale range

8 TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 105 MSPS, 3 V_{PP} sinusoidal clock, 50% duty cycle, 16k FFT points (unless otherwise noted)

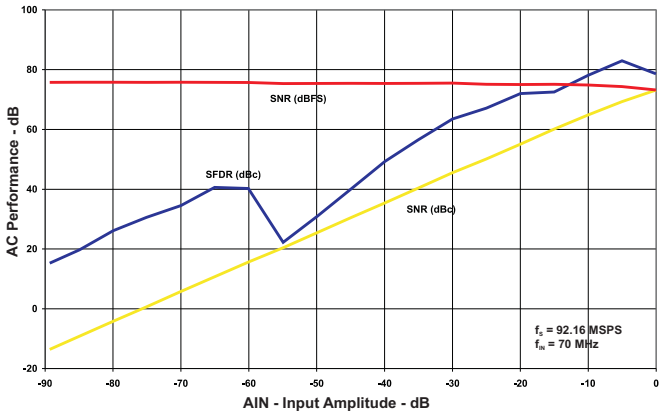


Figure 3.

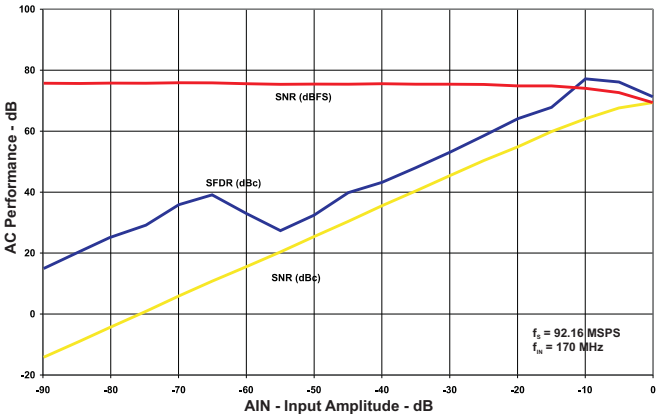


Figure 4.

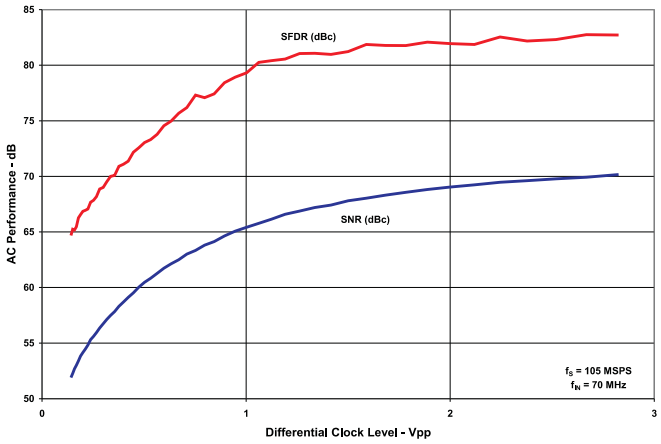


Figure 5.

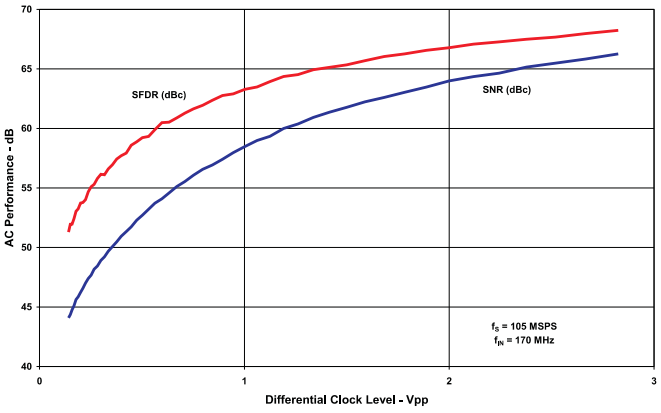


Figure 6.

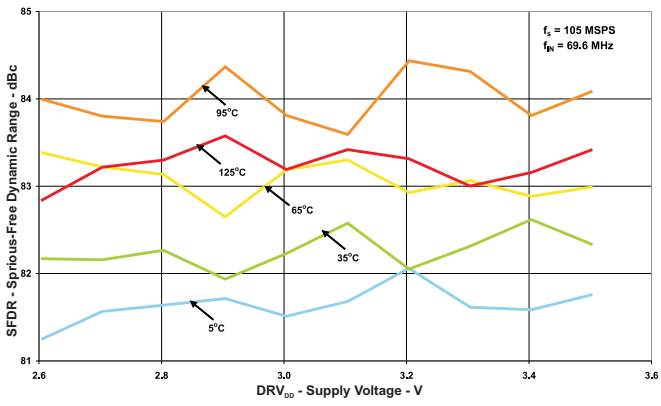


Figure 7.

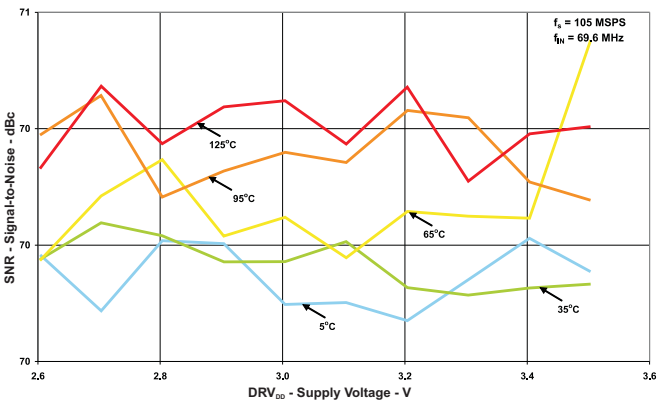


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 105 MSPS, 3 V_{PP} sinusoidal clock, 50% duty cycle, 16k FFT points (unless otherwise noted)

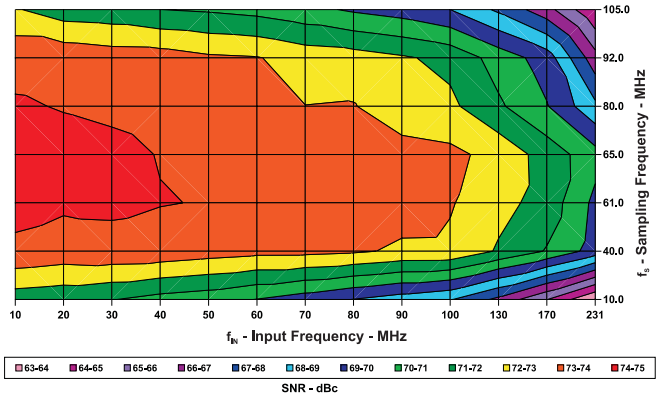


Figure 9.

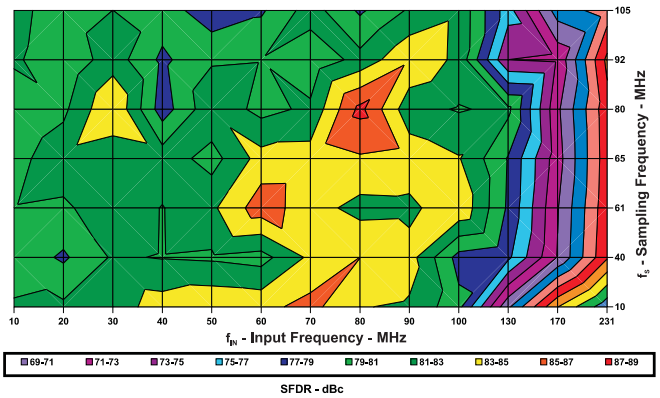


Figure 10.

9 EQUIVALENT CIRCUITS

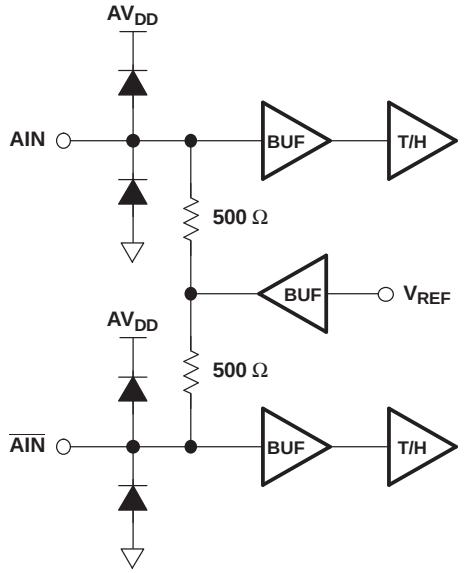


Figure 11. Analog Input

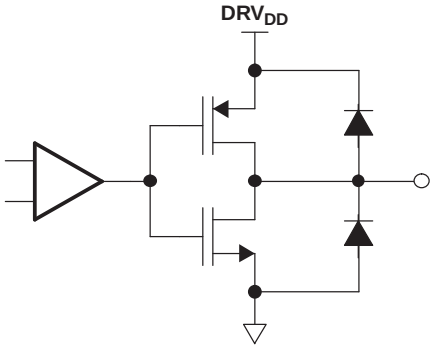


Figure 12. Digital Output

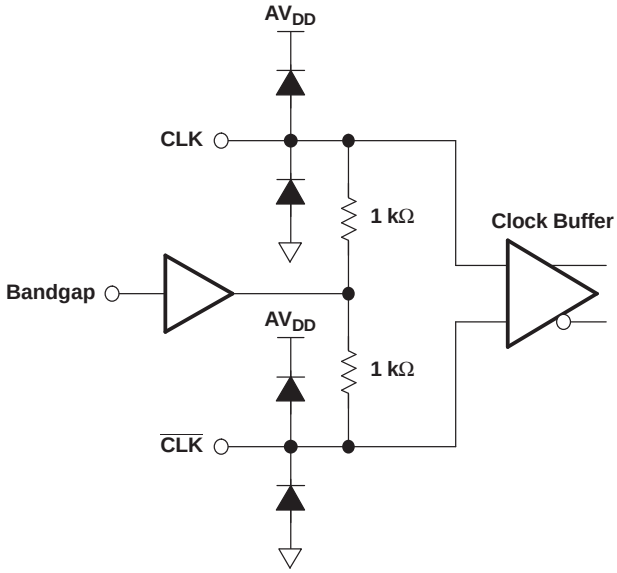


Figure 13. Clock Input

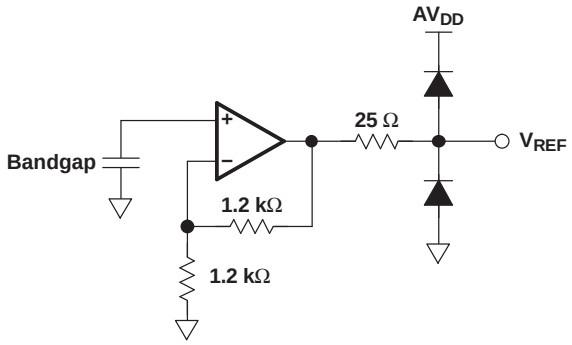


Figure 14. Reference

EQUIVALENT CIRCUITS (continued)

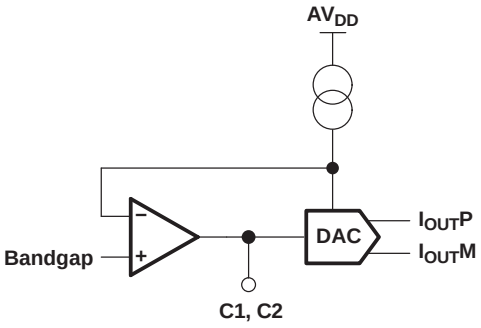


Figure 15. Decoupling Pin

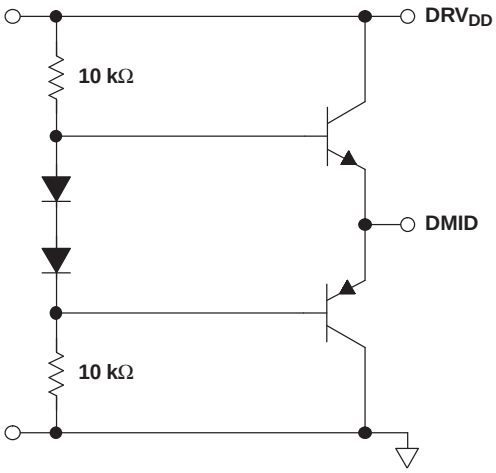


Figure 16. DMID Generation

10 APPLICATION INFORMATION

10.1 THEORY OF OPERATION

The ADS5424 is a 14-bit, 105-MSPS, monolithic pipeline analog to digital converter. Its bipolar analog core operates from a 5-V supply, while the output uses 3.3-V supply for compatibility with the CMOS family. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track and hold (T&H) and the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of three clock cycles, after which the output data is available as a 14 bit parallel word, coded in binary 2's complement format.

10.2 INPUT CONFIGURATION

The analog input for the ADS5424 (see Figure 11) consists of an analog differential buffer followed by a bipolar track-and-hold. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a 500-Ω resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ.

For a full-scale differential input, each of the differential lines of the input signal (pins 11 and 12) swings symmetrically between 2.4 ±0.55 V and 2.4 –0.55 V. This means that each input is driven with a signal of up to 2.4 ±0.55 V, so that each input has a maximum signal swing of 1.1 V_{PP} for a total differential input signal swing of 2.2 V_{PP}. The maximum swing is determined by the internal reference voltage generator eliminating any external circuitry for this purpose.

The ADS5424 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 17 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. If voltage gain is required, a step-up transformer can be used. For higher gains that would require impractical higher turn ratios on the transformer, a single-ended amplifier driving the transformer can be used (see Figure 18). Another circuit optimized for performance would be the one on Figure 19, using the THS4304 or the OPA695. Texas Instruments has shown excellent performance on this configuration up to 10-dB gain with the THS4304 and at 14-dB gain with the OPA695. For the best performance, they need to be configured differentially after the transformer (as shown) or in inverting mode for the OPA695 (see SBAA113); otherwise, HD2 from the op amps limits the useful frequency.

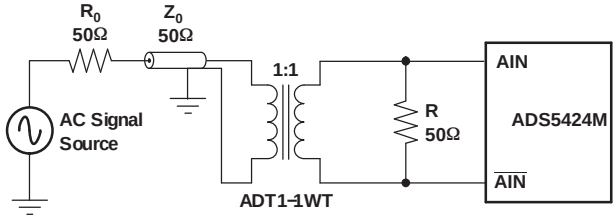


Figure 17. Converting a Single-Ended Input to a Differential Signal Using RF Transformers

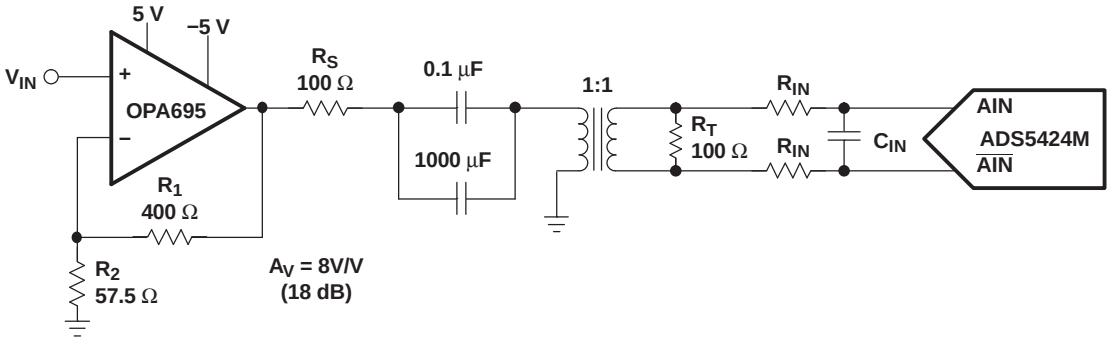


Figure 18. Using the OPA695 With the ADS5424

INPUT CONFIGURATION (continued)

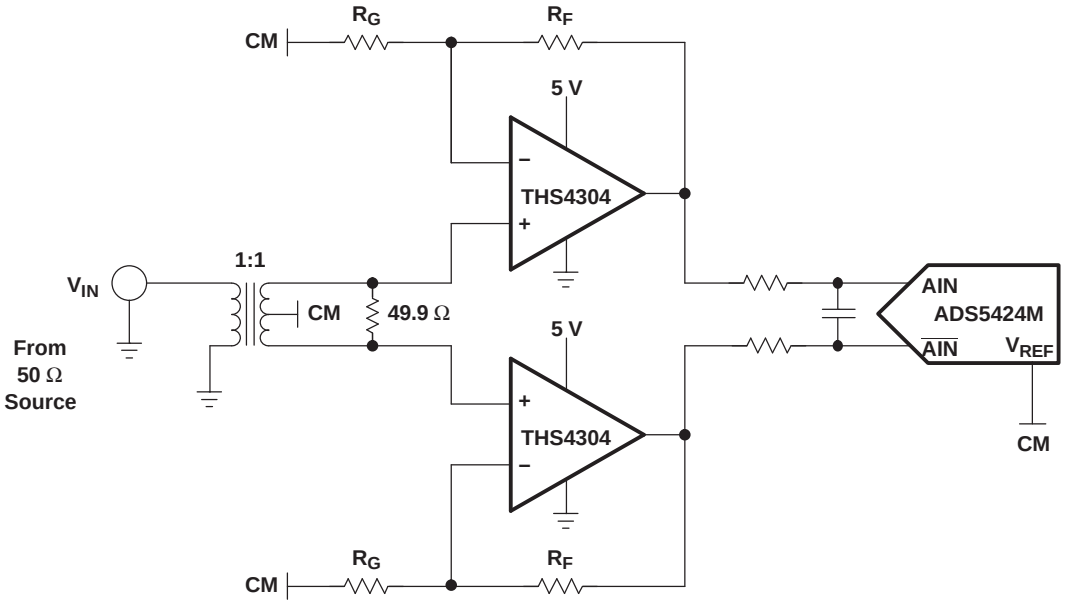


Figure 19. Using the THS4304 With the ADS5424

Texas Instruments offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202 and OPA847) that can be selected depending on the application. An RF gain block amplifier, such as Texas Instrument's THS9001, also can be used with an RF transformer for high input frequency applications. For applications requiring dc-coupling with the signal source, instead of using a topology with three single-ended amplifiers, a differential input/differential output amplifier like the THS4509 (see Figure 20) can be used, which minimizes board space and reduces the number of components.

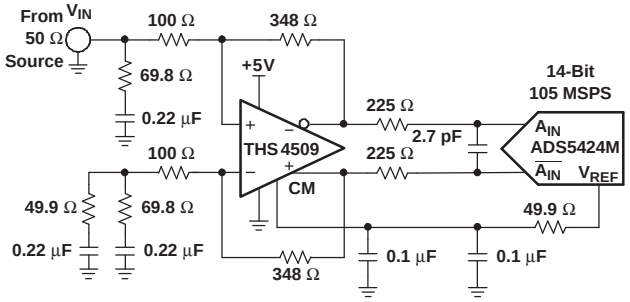


Figure 20. Using the THS4509 With the ADS5424

On this configuration, the THS4509 amplifier circuit provides 10-dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424.

The 225-Ω resistors and 2.7-pF capacitor between the THS4509 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100 MHz (–3 dB).

For this test, an Agilent signal generator is used for the signal source. The generator is an ac-coupled 50-Ω source. A bandpass filter is inserted in series with the input to reduce harmonics and noise from the signal source.

Input termination is accomplished via the 69.8-Ω resistor and 0.22-µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor is inserted to ground across the 69.8-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit.

INPUT CONFIGURATION (continued)

Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50-Ω termination for other common gains.

Because the ADS5424 recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power supply input with V_{S+} = 5 V and V_{S-} = 0 V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

10.3 CLOCK INPUTS

The ADS5424 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. In low-input-frequency applications, where jitter may not be a big concern, the use of single-ended clock (see Figure 21) could save cost and board space without any trade-off in performance. When driven on this configuration, it is best to connect CLKM (pin 11) to ground with a 0.01-µF capacitor, while CLKP is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 22.

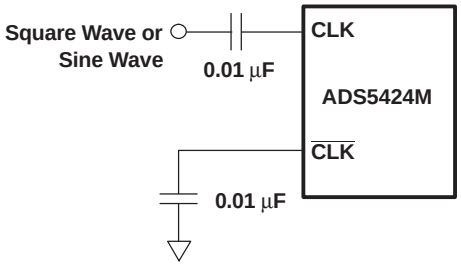


Figure 21. Single-Ended Clock

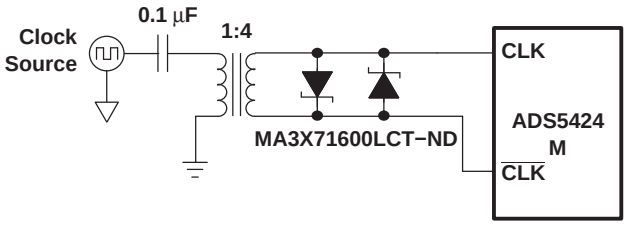


Figure 22. Differential Clock

For jitter sensitive applications, the use of a differential clock has advantages (as with any other ADCs) at the system level. The first advantage is that it allows for common-mode noise rejection at the PCB level. A further analysis (see *Clocking High Speed Data Converters*, SLYT075) reveals one more advantage. The following formula describes the different contributions to clock jitter:

$(\text{Jittertotal})^2 = (\text{EXT\_jitter})^2 + (\text{ADC\_jitter})^2 = (\text{EXT\_jitter})^2 + (\text{ADC\_int})^2 + (\text{K/clock\_slope})^2$

The first term represents the external jitter, coming from the clock source, plus noise added by the system on the clock distribution, up to the ADC. The second term is the ADC contribution, which can be divided in two portions. The first does not depend directly on any external factor. The second contribution is a term inversely proportional to the clock slope. The faster the slope, the smaller this term will be. As an example, the ADC jitter contribution could be computed from a sinusoidal input clock of 3-V_{pp} amplitude and Fs = 80 MSPS:

$\text{ADC\_jitter} = \text{sqrt}\left((150\text{ fs})^2 + (5 \times 10^{-5}/(1.5 \times 2 \times \text{PI} \times 80 \times 10^6))^2\right) = 164\text{ fs}$

The use of differential clock allows for the use of bigger clock amplitudes without exceeding the absolute maximum ratings. This, on the case of sinusoidal clock, results on higher slew rates, which minimize the impact of the jitter factor inversely proportional to the clock slope.

Figure 23 shows this approach. The back-to-back Schottky can be added to limit the clock amplitude in cases where this would exceed the absolute maximum ratings, even when using a differential clock.

CLOCK INPUTS (continued)

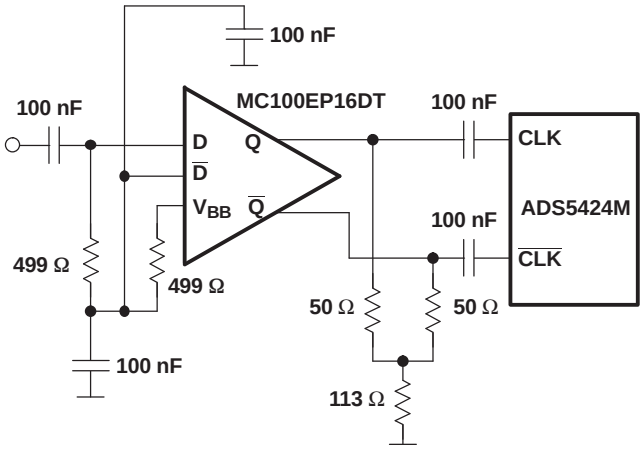


Figure 23. Differential Clock Using PECL Logic

Another possibility is the use of a logic based clock, as PECL. In this case, the slew rate of the edges will most likely be much higher than the one obtained for the same clock amplitude based on a sinusoidal clock. This solution would minimize the effect of the slope dependent ADC jitter. Nevertheless, observe that for the ADS5424, this term is small and has been optimized. Using logic gates to square a sinusoidal clock may not produce the best results as logic gates, which may not have been optimized to act as comparators, adding too much jitter while squaring the inputs.

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1-kΩ resistors. It is recommended to use an ac coupling, but if for any reason, this scheme is not possible, due to, for instance, asynchronous clocking, the ADS5424 presents a good tolerance to clock common-mode variation.

Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided.

10.4 DIGITAL OUTPUTS

The ADC provides 14 data outputs (D13 to D0, with D13 being the MSB and D0 the LSB), a data-ready signal (DRY, pin 52), and an out-of-range indicator (OVR, pin 32) that equals 1 when the output reaches the full-scale limits.

The output format is two's complement. When the input voltage is at negative full scale (around –1.1-V differential), the output will be, from MSB to LSB, 10 0000 0000 0000. Then, as the input voltage is increased, the output switches to 10 0000 0000 0001, 10 0000 0000 0010 and so on until 11 1111 1111 1111 right before mid-scale (when both inputs are tight together if we neglect offset errors). Further increases on input voltage, outputs the word 00 0000 0000 0000, to be followed by 00 0000 0000 0001, 00 0000 0000 0010 and so on until reaching 01 1111 1111 1111 at full-scale input (1.1-V differential).

Although the output circuitry of the ADS5424 has been designed to minimize the noise produced by the transients of the data switching, care must be taken when designing the circuitry reading the ADS5424 outputs. Output load capacitance should be minimized by minimizing the load on the output traces, reducing their length and the number of gates connected to them, and by the use of a series resistor with each pin. Typical numbers on the data sheet tables and graphs are obtained with 100-Ω series resistor on each digital output pin, followed by a 74AVC16244 digital buffer as the one used in the evaluation board.

10.5 POWER SUPPLIES

The use of low noise power supplies with adequate decoupling is recommended, being the linear supplies the first choice versus switched ones, which tend to generate more noise components that can be coupled to the ADS5424.

POWER SUPPLIES (continued)

The ADS5424 uses two power supplies. For the analog portion of the design, a 5-V AV_{DD} is used, while for the digital outputs supply (DRV_{DD}), we recommend the use of 3.3 V. All the ground pins are marked as GND, although AGND pins and DRGND pins are not tied together inside the package. Customers willing to experiment with different grounding schemes should know that AGND pins are 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, and 29, while DRGND pins are 2, 34, and 42. We recommend that both grounds are tied together externally, using a common ground plane. That is the case on the production test boards and modules provided to customer for evaluation. To obtain the best performance, user should lay out the board to assure that the digital return currents do not flow under the analog portion of the board. This can be achieved without splitting the board and with careful component placement and increasing the number of vias and ground planes.

Finally, notice that the metallic heat sink under the package is also connected to analog ground.

10.6 LAYOUT INFORMATION

The evaluation board represents a good guideline of how to lay out the board to obtain the maximum performance out of the ADS5424. General design rules for use of multilayer boards, single ground plane for both, analog and digital ADC ground connections, and local decoupling ceramic chip capacitors should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. Clock also should be isolated from other signals, especially on applications where low jitter is required, as high IF sampling.

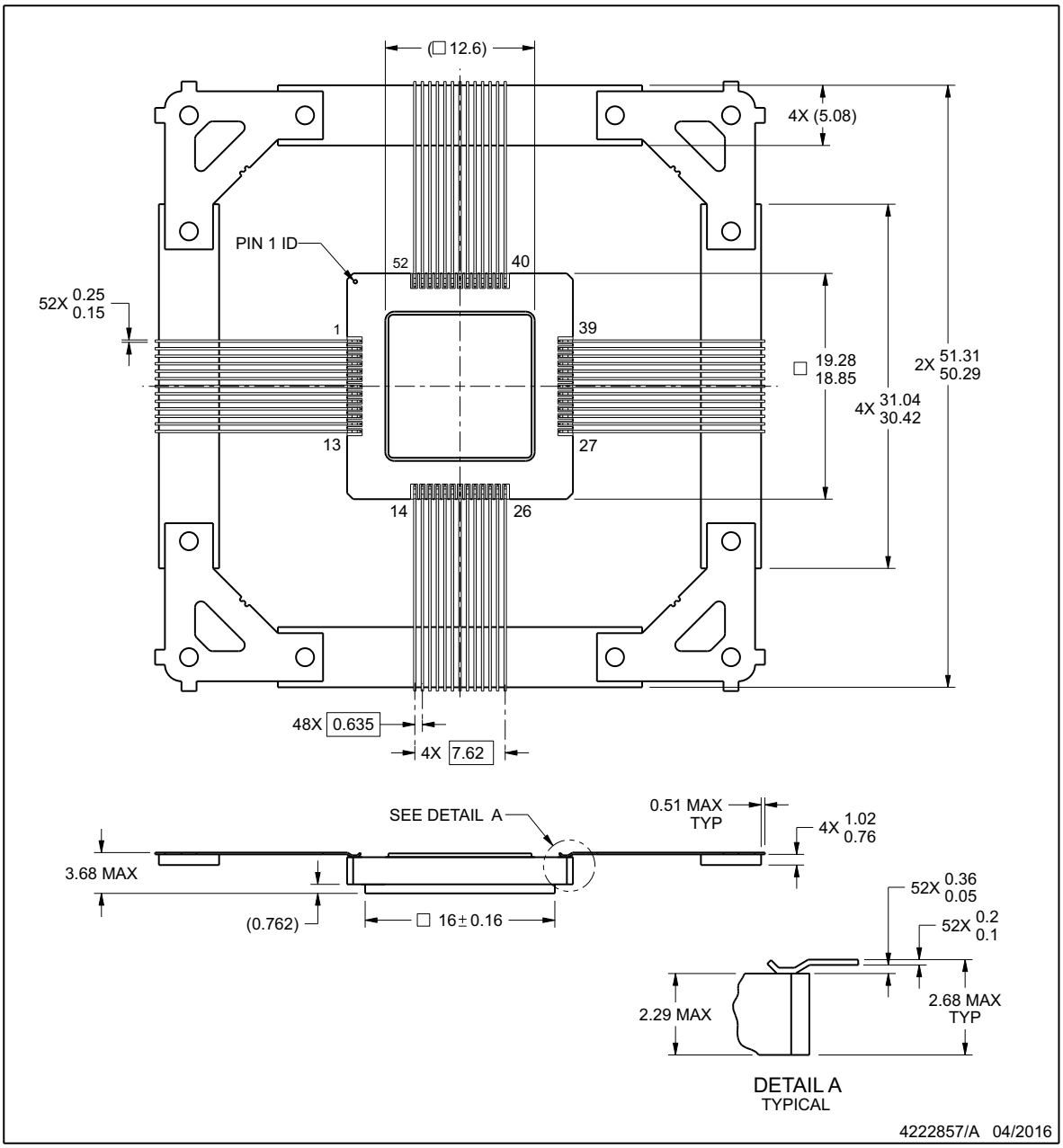
Besides performance oriented rules, special care has to be taken when considering the heat dissipation out of the device. The thermal package information describes the T_{JA} values obtained on the different configurations.

PACKAGE OUTLINE

HFG0052B

CFP - 3.68 mm max height

CFP



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The lid and the heat sink are connected to ground leads.
5. The leads are gold plated and can be solder dipped.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0720601VXC	ACTIVE	CFP	HFG	52	10	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	5962-0720601VXC ADS5424MHFG-V	Samples
ADS5424HFG/EM	ACTIVE	CFP	HFG	52	10	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25	ADS5424HFG/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ADS5424-SP :

- Catalog : ADS5424

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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