CDx4HC365-Q1, CD74HC366-Q1 High-Speed CMOS Logic HEX Buffer/Line Driver, Three-State Non-Inverting and Inverting

1 Features

- Qualified for automotive applications
- Buffered inputs
- High current bus driver outputs
- Typical propagation delay t_{PLH}, t_{PHL} = 8 ns at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C
- Fanout (over temperature range)
  - Standard outputs – 10 LSTTL loads
  - Bus driver outputs – 15 LSTTL loads
- Wide operating temperature range: –40°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL}= 0.8 V (maximum), V_{IH} = 2 V (minimum)
  - CMOS input compatibility, Il ≤ 1 μA at V_{OL}, V_{OH}

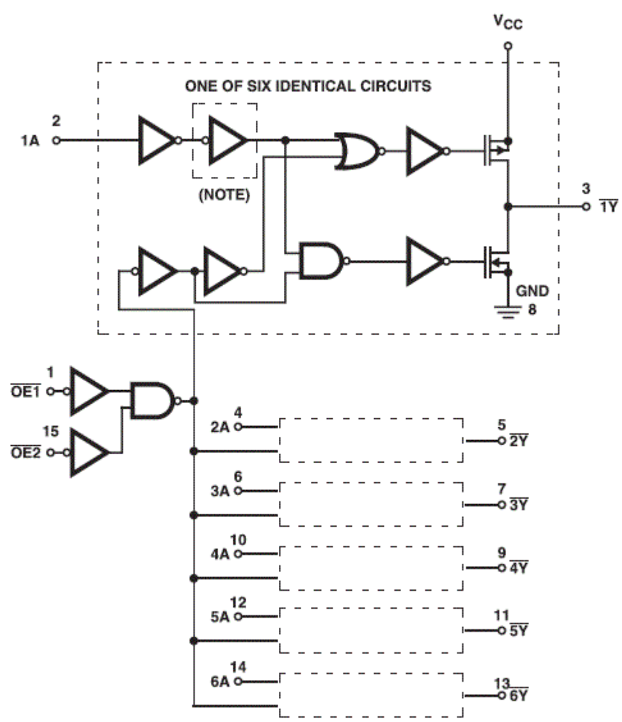
2 Description

The CD74HC365-Q1, CD74HC366-Q1, and CD74HCT365-Q1 silicon gate CMOS three state buffers are general purpose high-speed non-inverting and inverting buffers. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

Device Information

PART NUMBER	PACKAGE[(1)]	BODY SIZE (NOM)
CD74HC366QDRQ1	D (SOIC, 16)	9.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



NOTE: Inverter not included in CD74HC365-Q1, CD74HCT365-Q1

Functional Block Diagram

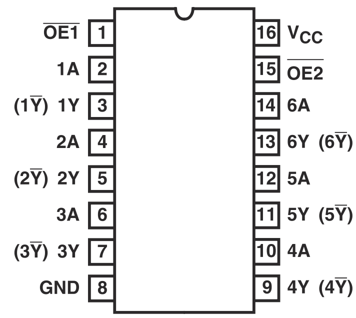
Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2010) to Revision A (August 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1

4 Pin Configuration and Functions



D Package
16-Pin SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input clamp current	$V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$		±20	mA
I_{OK}	Output clamp current	$V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$		±20	mA
I_O	Drain current	$V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$		±35	mA
	Continuous output current			±25	
I_{CC}	Continuous current through V_{CC} or GND			±50	mA
Latch up					Class I
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C
	Lead temperature (soldering 10s)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	250	
		Machine model	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		–40	125	°C
Δt/Δv	Input Rise and Fall Time	2 V		1000	ns
		4.5 V		500	
		6 V		400	

5.4 Thermal Information

THERMAL METRIC		D (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	73	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS[2]	V_{CC} (V)	25°C			-40°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	
HC Types										
V_{IH}	High-level input voltage			2	1.5			1.5		V
				4.5	3.15			3.15		
				6	4.2			4.2		
V_{IL}	Low-level input voltage			2			0.5		0.5	V
				4.5			1.35		1.35	
				6			1.8		1.8	
V_{OH}	High-level output voltage loads	CMOS	I_{OH} = –20 µA	2	1.9			1.9		V
				4.5	4.4			4.4		
				6	5.9			5.9		
		TTL	I_{OH} = –6 mA	4.5	3.98			3.7		
			I_{OH} = –7.8 mA	6	5.48			5.2		
V_{OL}	Low-level output voltage loads	CMOS	I_{OL} = 20 µA	2			0.1		0.1	V
				4.5			0.1		0.1	
				6			0.1		0.1	
		TTL	I_{OL} = 6 mA	4.5			0.26		0.4	
			I_{OL} = 7.8 mA	6			0.26		0.4	
I_I	Input leakage current		$V_I = V_{CC}$ or GND	6			±0.1		±1	µA
I_{CC}	Supply current		$V_I = V_{CC}$ or GND; I_o = 0 A	6			8		160	µA
I_{OZ}	Three-state leakage current		$V_O = V_{CC}$ or GND	6			±0.5		±10	µA
HCT Types										
V_{IH}	High-level input voltage			4.5 to 5.5	2			2		V
V_{IL}	Low-level input voltage			4.5 to 5.5			0.8		0.8	V
V_{OH}	High-level output voltage loads		I_{OH} = – 20 µA	4.5	4.4			4.4		V
			I_{OH} = – 4 mA	4.5	3.98			3.7		
V_{OL}	Low-level output voltage loads		I_{OL} = 20 µA	4.5			0.1		0.1	V
			I_{OL} = 4 mA	4.5			0.26		0.4	
I_I	Input leakage current		$V_I = V_{CC}$ or GND	5.5			±0.1		±1	µA
I_{CC}	Supply current		$V_I = V_{CC}$ or GND	5.5			8		160	µA
ΔI_{CC}	Additional supply current per input pin: 1 unit load[1]		V_{CC} - 2.1	4.5 to 5.5		100	360		490	µA
I_{OZ}	Three-state leakage current		$V_O = V_{CC}$ or GND	5.5			±0.5		±10	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.
(2) $V_I = V_{IH}$ or V_{IL}, unless otherwise specified.

5.6 Switching Characteristics

C_L = 50pF. Input t_r, t_f = 6ns

PARAMETER			V_{CC} (V)	25°C TYP	25°C MAX	-40°C TO 125°C MAX	UNITS
HC Types							
t_{PLH}, t_{PHL}	Propagation delay, data to outputs	HC365	2		110	165	ns
			4.5		22	33	
			6		19	28	
		HC366	2		150	225	
			4.5		31	45	
			6		26	38	
t_{TLH}, t_{THL}	Output transition time		2		60	90	ns
			4.5		12	18	
			6		10	15	
C_I	Input capacitance				10	10	pF
C_O	Three-state output capacitance				20	20	pF
C_{PD}	Power dissipation capacitance(1) (2)		5	40			pF
HCT Types							
t_{PLH}, t_{PHL}	Propagation delay, data to outputs	HCT365	4.5		25	38	ns
		HCT366	4.5		27	41	
t_{PLH}, t_{PHL}	Propagation delay, output enable and disable to outputs		4.5		35	53	ns
t_{TLH}, t_{THL}	Output transition time		4.5		12	18	ns
C_I	Input capacitance				10	10	pF
C_O	Three-state output capacitance				20	20	pF
C_{PD}	Power dissipation capacitance(1) (2)		5	42			pF

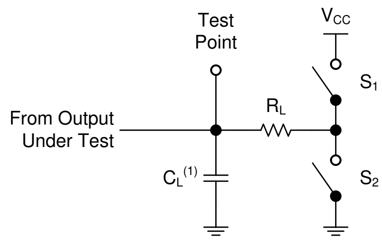
(1) C_{PD} is used to determine the dynamic power consumption, per inverter.
(2) $P_D = V_{CC}{}^2 \times f_i (C_{PD} + C_L)$, where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

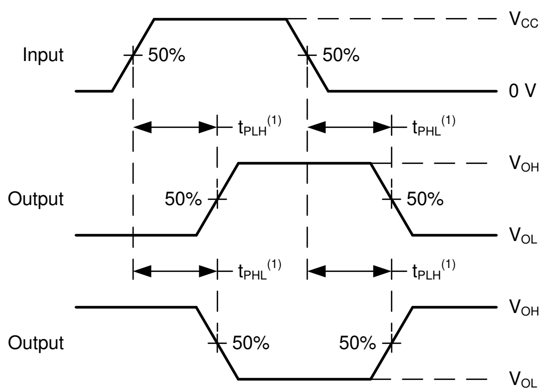
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



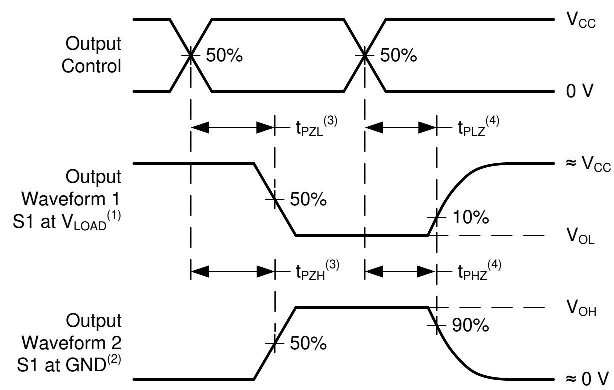
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

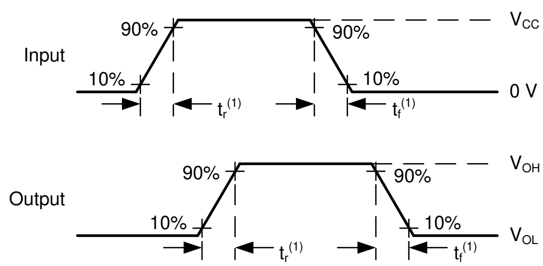
Figure 6-2. Voltage Waveforms, Standard CMOS Inputs Setup Propagation Delays



(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

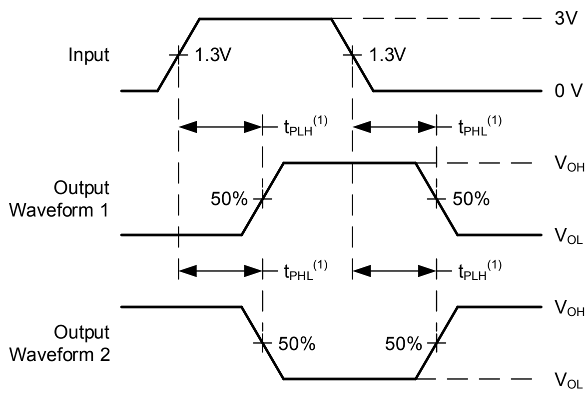
(2) t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-3. Voltage Waveforms, Standard CMOS Inputs Propagation Delays



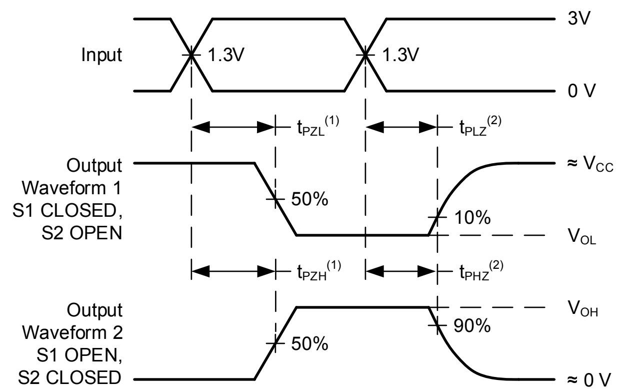
(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Input Devices



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-5. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays



(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays

7 Detailed Description

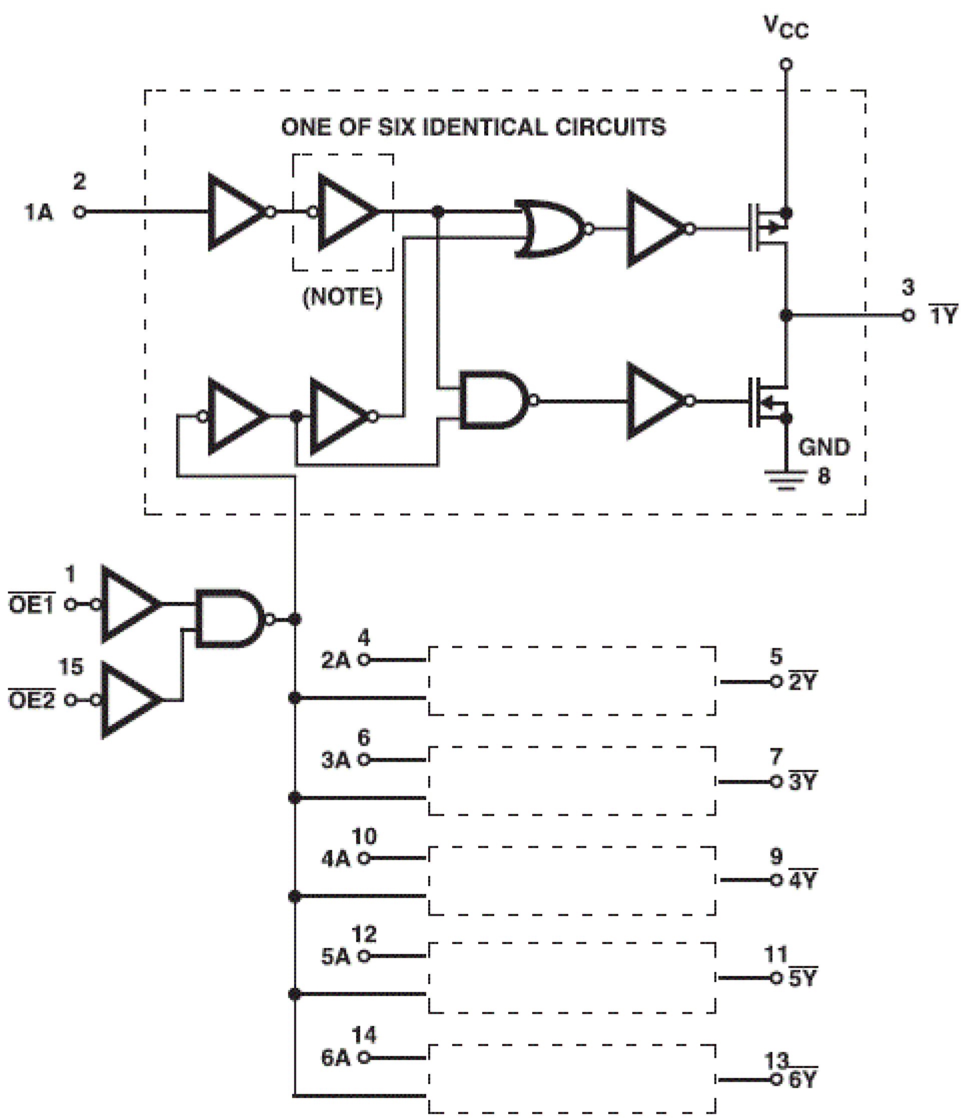
7.1 Overview

The CD74HC365-Q1, CD74HC366-Q1, and CD74HCT365-Q1 silicon gate CMOS three state buffers are general purpose high-speed non-inverting and inverting buffers. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The CD74HC365-Q1 and CD74HCT365-Q1 are non-inverting buffers, whereas the CD74HC366-Q1 is an inverting buffer. These devices have two three-state control inputs ($\overline{OE1}$ and $\overline{OE2}$) which are NORed together to control all six gates.

The ’HCT365-Q1 logic families are speed, function and pin compatible with the standard LS logic family.

7.2 Functional Block Diagram



NOTE: Inverter not included in CD74HC365-Q1, CD74HCT365-Q1

7.3 Device Functional Modes

Table 7-1. Function Table

INPUTS(1)			OUTPUTS (Y)(2)	
OE1	**OE2**	**A**	**HC/HCT365**	**HC366**
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC366QDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC366Q	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

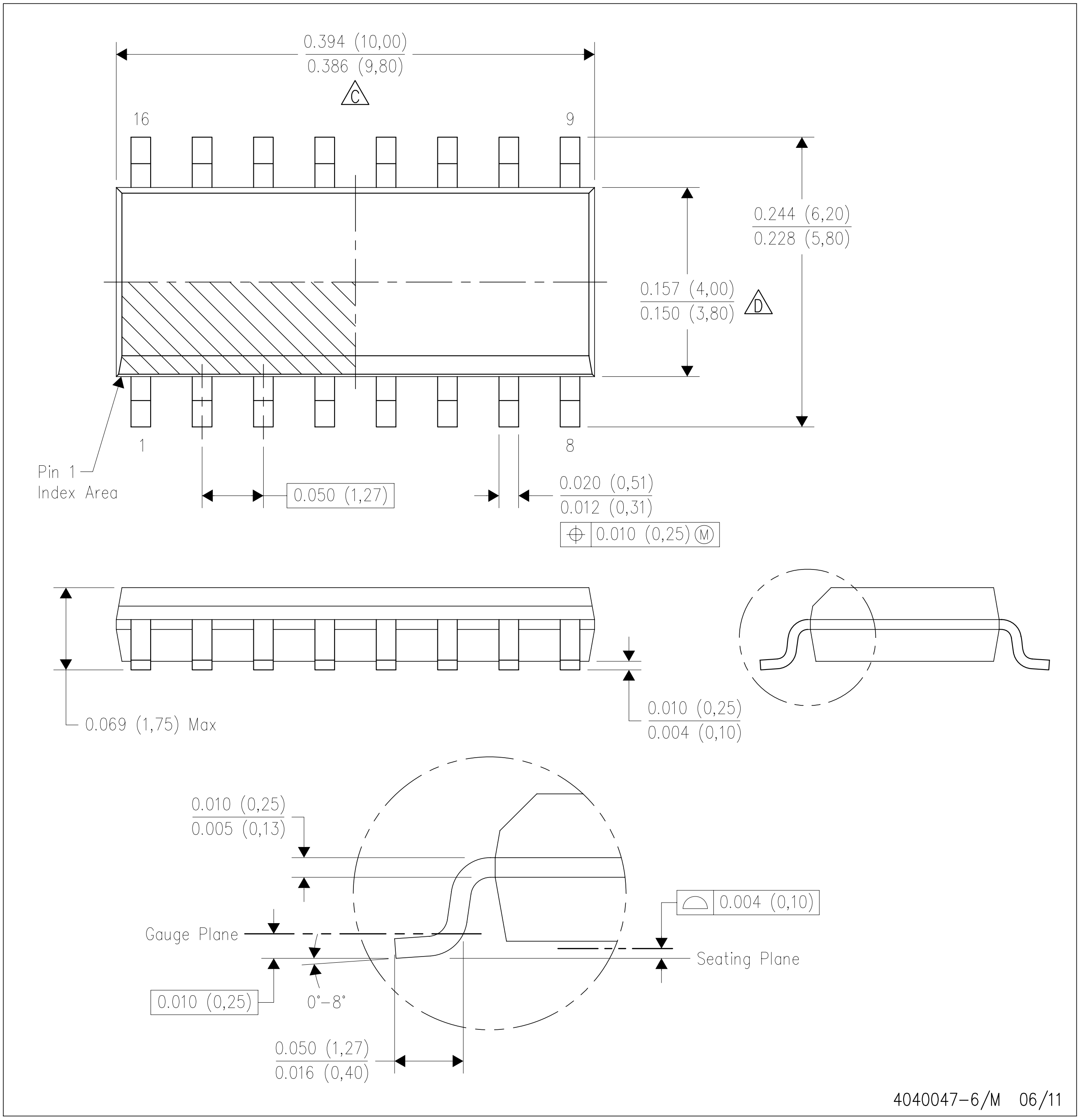
OTHER QUALIFIED VERSIONS OF CD74HC366-Q1 :

- Catalog : CD74HC366
- Military : CD54HC366

NOTE: Qualified Version Definitions:

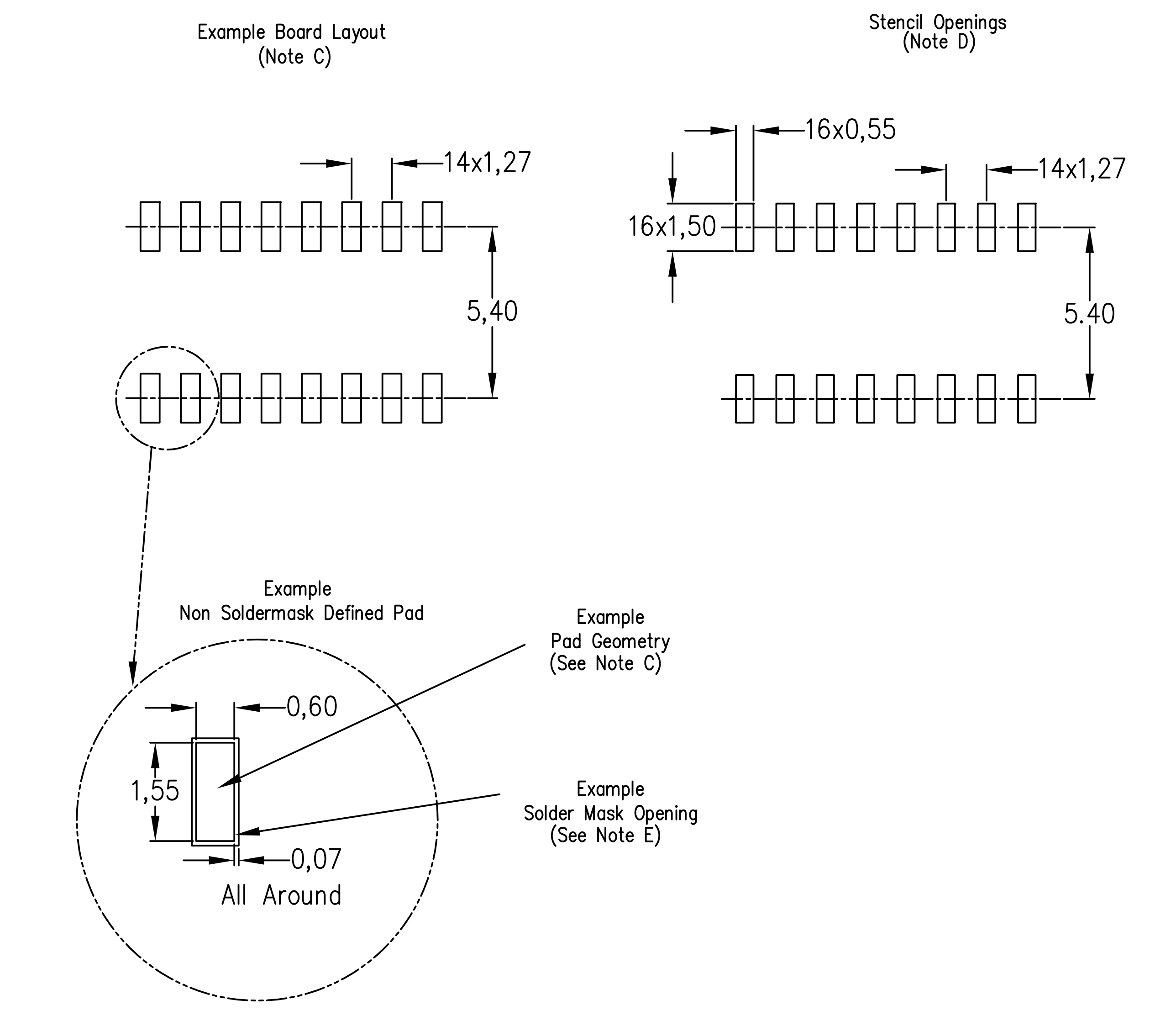
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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