CDCBT1001 1.2-V to 1.8-V Clock Buffer and Level Translator

1 Features

- Clock frequency range: DC to 24 MHz
- 1.2-V to 1.8-V LVCMOS clock level translation:
  - VDD_IN = 1.2 V ± 10%
  - VDD_OUT = 1.8 V ± 10%
- Low additive jitter and phase noise:
  - 0.8-ps maximum 12-kHz to 5-MHz additive RMS jitter (f_{out} = 24 MHz)
  - –120-dBc/Hz maximum phase noise at 1-kHz offset (f_{out} = 24 MHz)
  - –148-dBc/Hz maximum phase noise floor (f_{out} = 24 MHz, $f_{offset} \geq$ 1 MHz)
- 5-ns 20% to 80% rise/fall time
- 10-ns propagation delay
- Low current consumption
- –40°C to 85°C operating temperature range

2 Applications

- FPGA/processor clock buffering/level translation in personal electronics
- 1.2-V clock buffer and level translator in servers and add-in cards

3 Description

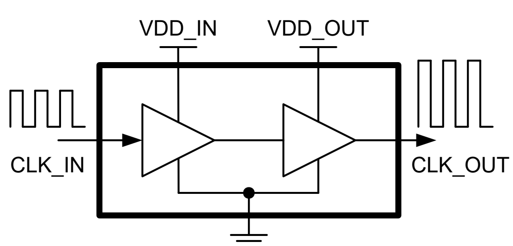
The CDCBT1001 is a 1.2-V to 1.8-V clock buffer and level translator. The VDD_IN pin supply voltage defines the input LVCMOS clock level. The VDD_OUT pin supply voltage defines the output LVCMOS clock level. VDD_IN = 1.2 V ± 10%. VDD_OUT = 1.8 V ± 10%

The 12-kHz to 5-MHz additive RMS jitter at 24 MHz is less than 0.8 ps.

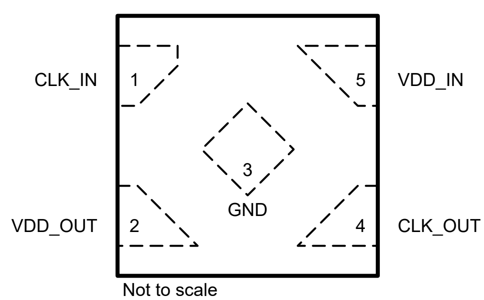
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CDCBT1001	X2SON (5)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Block Diagram



Pin Configuration

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2022	*	Initial Release

5 Pin Configuration and Functions

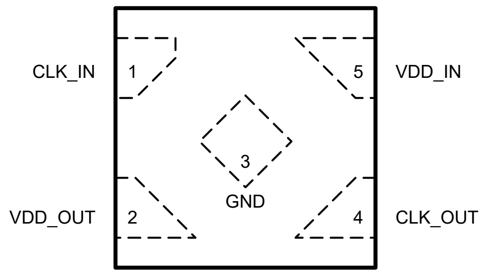


Figure 5-1. DPW Package 5-Pin X2SON Transparent Top View

Table 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
CLK_IN	1	I	Clock input. LVCMOS input clock is injected into this pin. The acceptable LVCMOS voltage level is defined by VDD_IN.
CLK_OUT	4	O	Clock output. This pin outputs LVCMOS clock. The output LVCMOS voltage level is defined by VDD_OUT
VDD_IN	5	P	Input supply voltage. 1.08 V ≤ VDD_IN ≤ 1.32 V.
VDD_OUT	2	P	Output supply voltage. 1.62 V ≤ VDD_OUT ≤ 1.98 V.
GND	3	G	Ground

(1) I = Input, O = Output, P = Power, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
VDD_IN	VDD_IN supply voltage	–0.5	1.5	V
VDD_OUT	VDD_OUT supply voltage	–0.5	2.25	V
V_I	Input voltage[(2)]	–0.5	1.5	V
V_O	Voltage applied to the output in the high-impedance or power-off state[(2)]	–0.5	2.25	V
	Voltage applied to the output in the high or low state[(2)] [(3)]	–0.5	VDD_OUT + 0.2	V
I_{IK}	Input clamp current, $V_I < 0$		–50	mA
I_{OK}	Output clamp current, $V_O < 0$		–50	mA
I_O	Continuous output current	–50	50	mA
	Continuous current through VDD_OUT or GND	–50	50	mA
I_O	Continuous current through VDD_IN	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 2.25 V maximum if the output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT	OWNER
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V	
		Charged device model (CDM), per JEDEC specification JS-002, all pins[(2)]	±1000	V	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD_IN	Input supply voltage	1.08		1.32	V
VDD_OUT	Output supply voltage	1.62		1.98	V
T_A	Ambient temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		CDCBT1001 DPW (X2SON) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	462.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	227.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	326.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.8	°C/W

THERMAL METRIC[(1)]		CDCBT1001 DPW (X2SON) 5 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	325.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

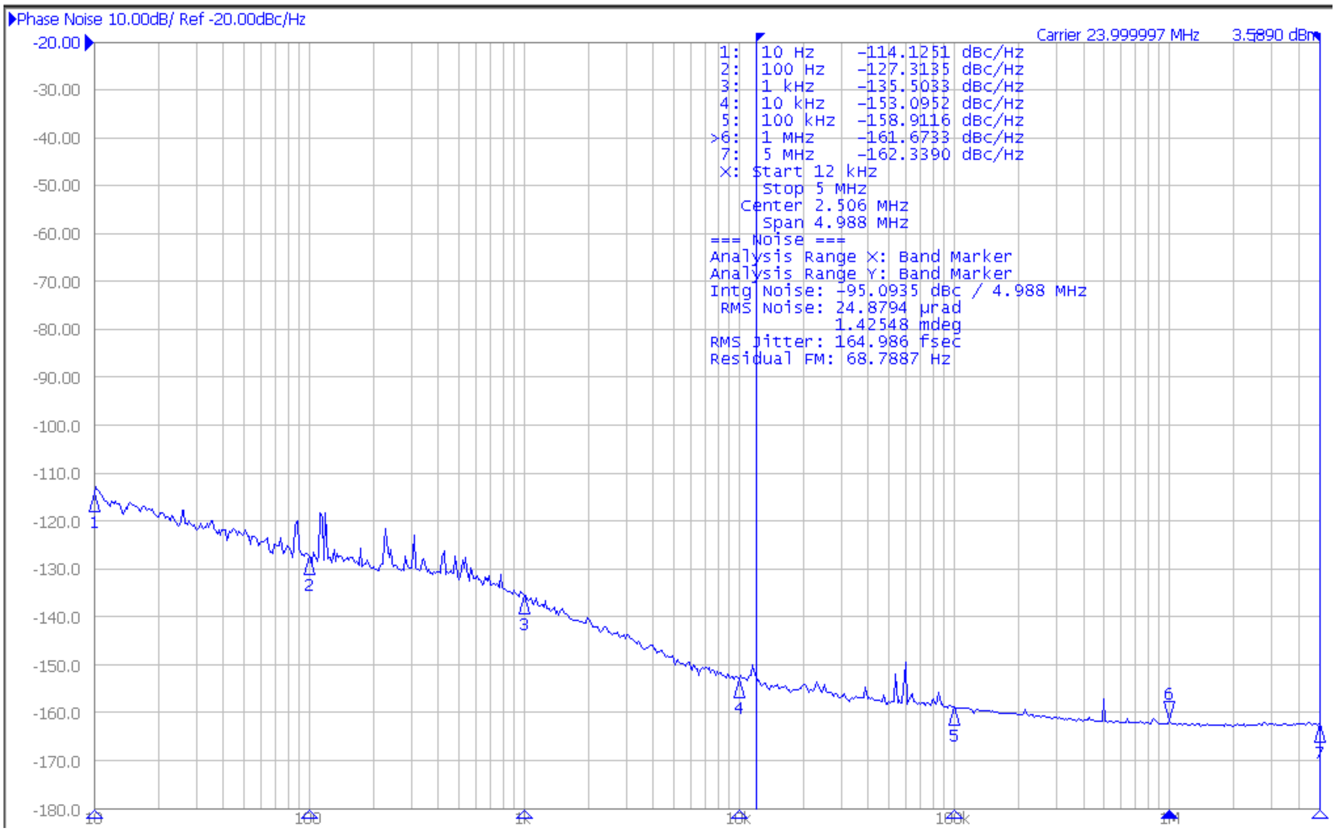
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS						
IDD_IN	Current consumption on VDD_IN	Both input and output clocks are toggling. 2 pF load termination. f_0 = 12 MHz.			35	µA
		Both input and output clocks are toggling. 2 pF load termination. f_0 = 24 MHz.			60	µA
IDD_OUT	Current consumption on VDD_OUT	Both input and output clocks are toggling. 2 pF load termination. f_0 = 12 MHz.			500	µA
		Both input and output clocks are toggling. 2 pF load termination. f_0 = 24 MHz.			1000	µA
CLOCK INPUT CHARACTERISTICS						
f_0	Operating frequency		DC		24	MHz
I_{IN_LEAK}	Input leakage current		–8		8	µA
V_{IH}	Input voltage high		VDD_IN x 0.8			V
V_{IL}	Input voltage low				VDD_IN x 0.2	V
$\Delta v/\Delta t$	Input edge rate		0.01			V/ns
C_I	Input capacitance				2	pF
$t_{startup}$	Time after power supply exceeds 0.5 V before applying input clock, to ensure glitchless output				225	us
CLOCK OUTPUT CHARACTERISTICS						
V_{OH}	Output voltage high	$V_I = V_{IH}$, I_{OH} = -100 µA, VDD_OUT = 1.62-1.98 V	VDD_OUT – 0.1			V
V_{OH}	Output voltage high	$V_I = V_{IH}$, I_{OH} = -8 mA, VDD_OUT = 1.62 V	1.2			V
V_{OL}	Output voltage low	$V_I = V_{IL}$, I_{OL} = 100 µA, VDD_OUT = 1.62-1.98 V			0.1	V
V_{OL}	Output voltage low	$V_I = V_{IL}$, I_{OL} = 8 mA, VDD_OUT = 1.62 V			0.45	V
ODC	Output duty cycle	Input duty cycle = 45% - 55%, input slew rate ≥ 0.2 V/ns, V_{IL} ≤ 0.15 * VDD_IN, V_{IH} ≥ 0.85 * VDD_IN, V_{IH} - V_{IL} ≥ 850 mVpp	40		60	%
		Input duty cycle = 45% - 55%, input slew rate ≥ 0.2 V/ns, V_{IL} ≤ 0.2 * VDD_IN, V_{IH} ≥ 0.8 * VDD_IN, V_{IH} - V_{IL} ≥ 850 mVpp	37		63	%
t_R, t_F	Clock output rise/fall time	20% to 80%, 2 pF load capacitance			3	ns
t_{PD}	Input-to-output propagation delay	Input slew rate ≥ 0.2 V/ns, V_{IL} ≤ 0.2 * VDD_IN, V_{IH} ≥ 0.8 * VDD_IN, V_{IH} - V_{IL} ≥ 850 mVpp			10	ns
R_{out}	Output impedance			34		Ω
CLOCK OUTPUT PERFORMANCE						
$RJ_{RMS\text{-}ADD}$	12 kHz to 5 MHz additive RMS random jitter	f_0 =24 MHz, input slew rate ≥ 0.2 V/ns, V_{IH} - V_{IL} ≥ 850 mVpp			0.8	ps

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN_{10}	Output phase noise @10 Hz	f_0 =24 MHz, input phase noise = -104 dBc/Hz, input slew rate ≥ 0.2 V/ns, V_{IH} - V_{IL} ≥ 850 mVpp			–100	dBc/Hz
PN_{100}	Output phase noise @100 Hz	f_0 =24 MHz, input phase noise = -127 dBc/Hz, input slew rate ≥ 0.2 V/ns, V_{IH} - V_{IL} ≥ 850 mVpp			–110	dBc/Hz
PN_{1k}	Output phase noise @1 kHz	f_0 =24 MHz, input phase noise = -137 dBc/Hz, input slew rate ≥ 0.2 V/ns, V_{IH} - V_{IL} ≥ 850 mVpp			–120	dBc/Hz
PN_{10k}	Output phase noise @10 kHz	f_0 =24 MHz, input phase noise = -159 dBc/Hz, input slew rate ≥ 0.2 V/ns, V_{IH} - V_{IL} ≥ 850 mVpp			–130	dBc/Hz
PN_{100k}	Output phase noise @100 kHz	f_0 =24 MHz, input phase noise = -164 dBc/Hz, input slew rate ≥ 0.2 V/ns, V_{IH} - V_{IL} ≥ 850 mVpp			–140	dBc/Hz
PN_{1M}	Output phase noise @1 MHz	f_0 =24 MHz, input phase noise = -166 dBc/Hz, input slew rate ≥ 0.2 V/ns, V_{IH} - V_{IL} ≥ 850 mVpp			–148	dBc/Hz
PN_{5M}	Output phase noise @5 MHz	f_0 =24 MHz, input phase noise = -165 dBc/Hz, input slew rate ≥ 0.2 V/ns, V_{IH} - V_{IL} ≥ 850 mVpp			–148	dBc/Hz

6.6 Typical Characteristics



VDD_IN = 1.2 V, VDD_OUT = 1.8 V, T_A = 25 °C,

Input phase noise as specified in *Electrical Characteristics* table

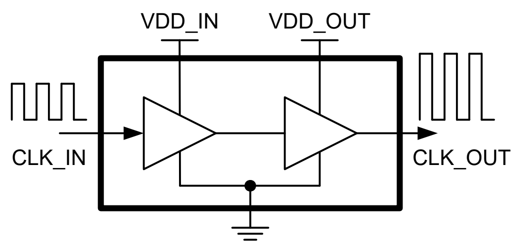
Figure 6-1. 24-MHz Phase Noise

7 Detailed Description

7.1 Overview

The CDCBT1001 is a single-channel, 1.2-V to 1.8-V clock buffer and level translator. VDD_IN defines input LVCMOS clock level and VDD_OUT defines output LVCMOS clock level.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Down Tolerant Input

The device can have a clock signal on the input pin when the chip is powered down.

7.3.2 Up Conversion

The device supports 1.2-V to 1.8-V up conversion.

7.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The CDCBT1001 device can be used in level-translation applications for interfacing between devices or systems that are operating at different interface voltages.

8.2 Typical Applications

8.2.1 Processor Clock Up Translation

Figure 8-1 shows an example of CDCBT1001 being used in a clock level shifting application.

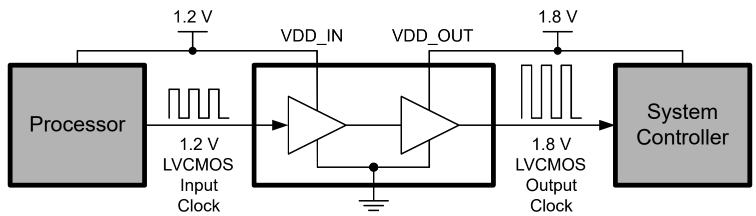


Figure 8-1. Processor Clock Up Translation Application

8.2.1.1 Design Requirements

For this design example, use the parameters shown in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage supply	1.2 V
Output voltage supply	1.8 V

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input clock
  - The supply voltage on VDD_IN will determine the input clock voltage range.
  - For a valid logic-high, the high level clock input must exceed V_{IH} spec. For a valid logic-low, the low level clock input must be below V_{IL}.
  - Some specifications such as duty cycle and phase noise have additional requirements for V_{IH}, V_{IL}, input swing and input slew rate. Refer to the test conditions column in the *Electrical Characteristics* table.
- Output clock
  - The supply voltage on VDD_OUT will determine the output clock voltage range.

8.2.1.3 Application Curve

Figure 6-1 listed in the *Typical Characteristics* section can also be used as an application curve for the *Processor Clock Up Translation* application example.

Table 8-2. Table of Graphs

TITLE	FIGURE
24-MHz Phase Noise	Figure 6-1

9 Power Supply Recommendations

TI recommends to place a 0.1-μF bypass capacitor on each VDD pin.

10 Layout

10.1 Layout Guidelines

To ensure reliability of the device, follow the common printed-circuit board layout guidelines listed below:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.

Figure 10-1 shows an example layout for the DPW (X2SON-5) package. This example layout includes two 0402 (metric) capacitors, and uses the measurements listed in the package outline drawing appended to the end of this data sheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or the via can be left out of the layout.

10.2 Layout Example

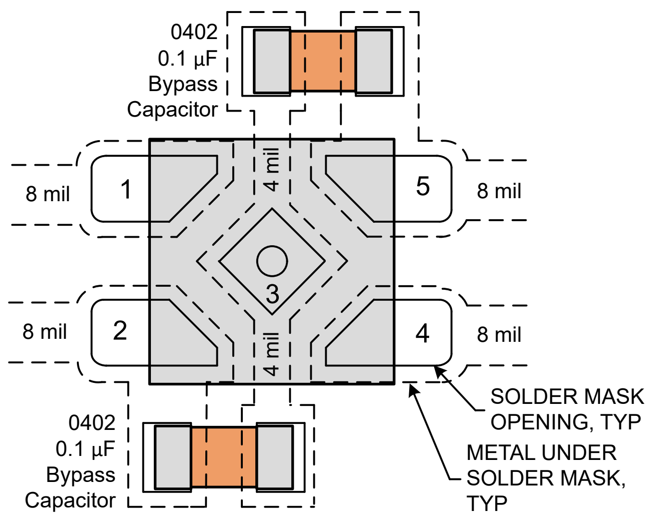


Figure 10-1. Example Layout for the DPW (X2SON-5) Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Designing and Manufacturing with TI's X2SON Packages* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCBT1001DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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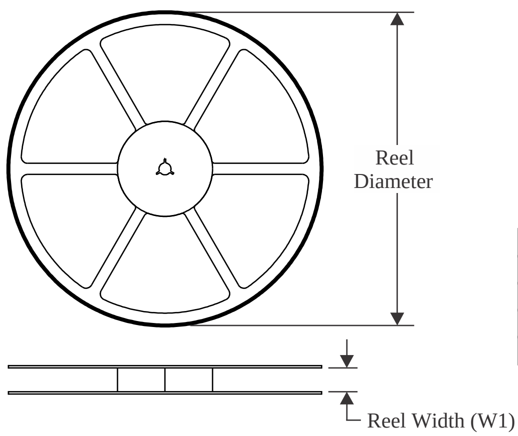
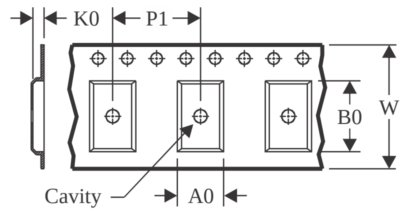
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

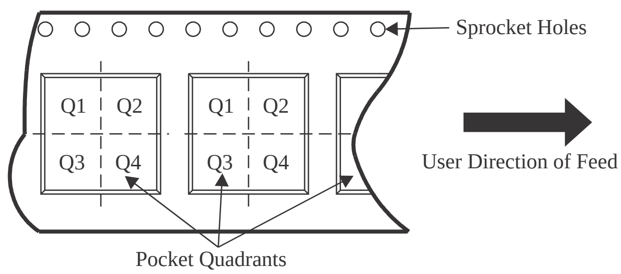


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

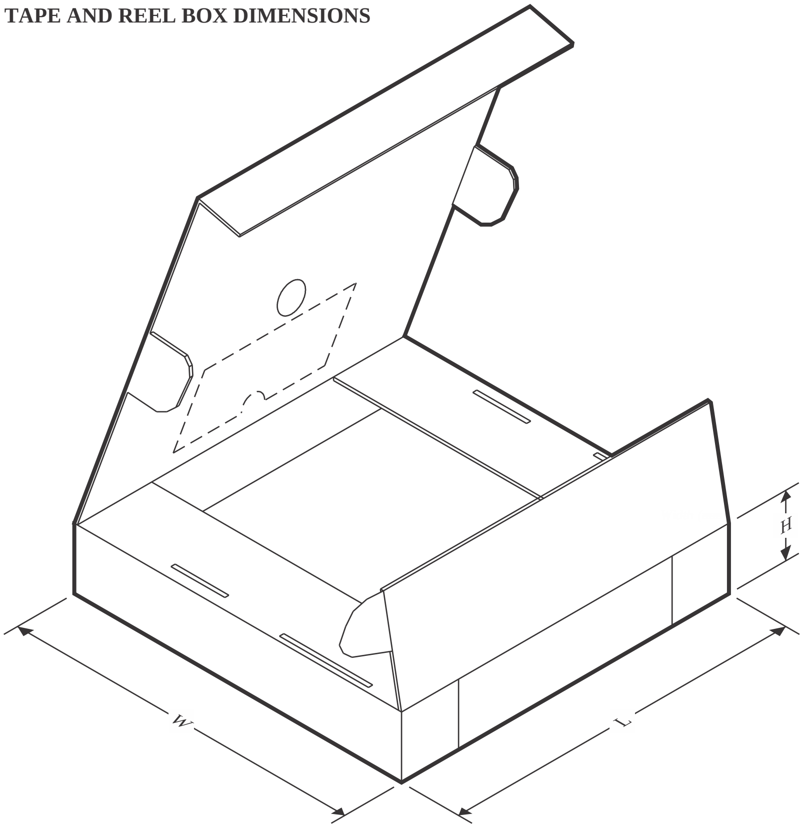
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCBT1001DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3

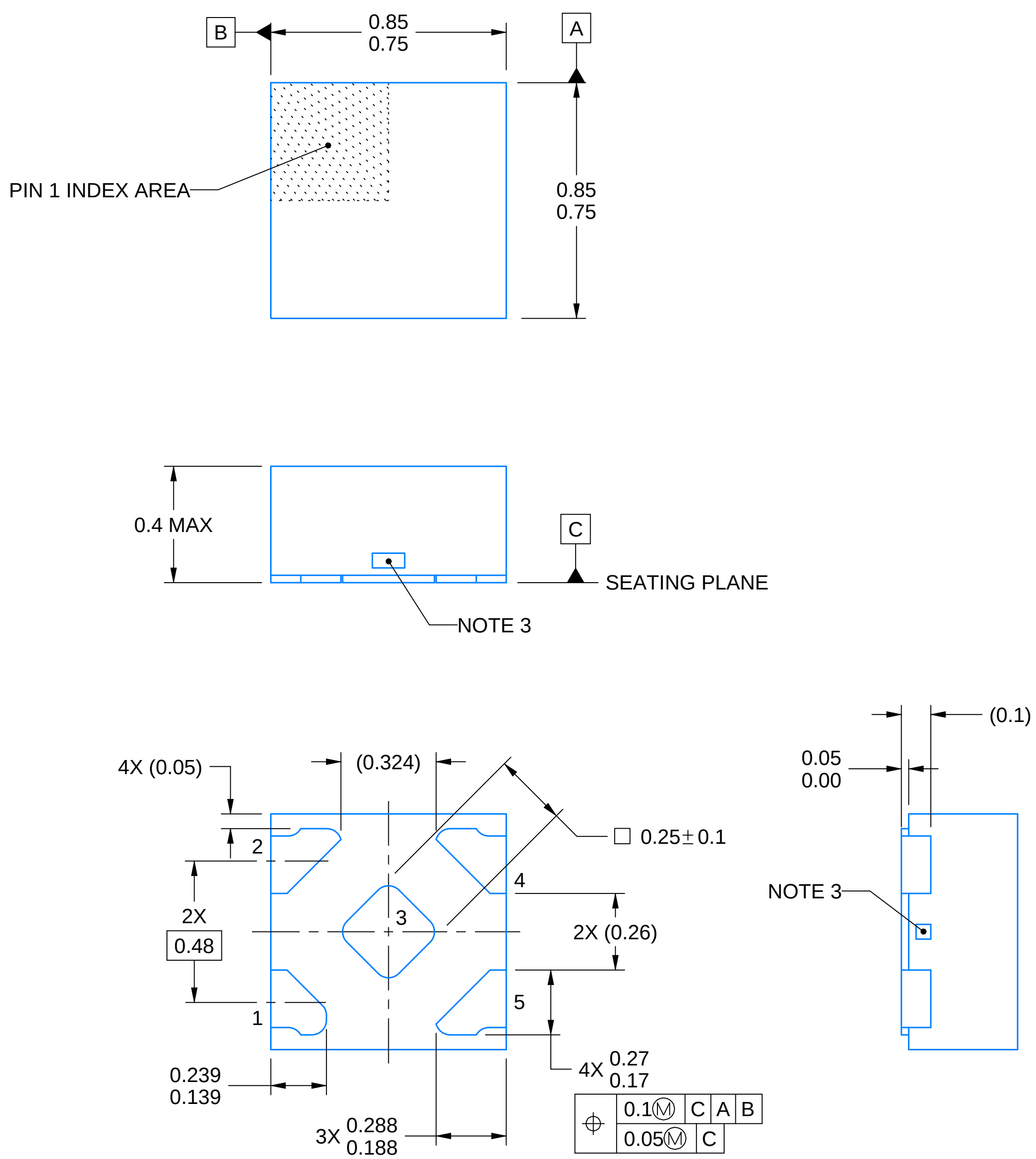
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCBT1001DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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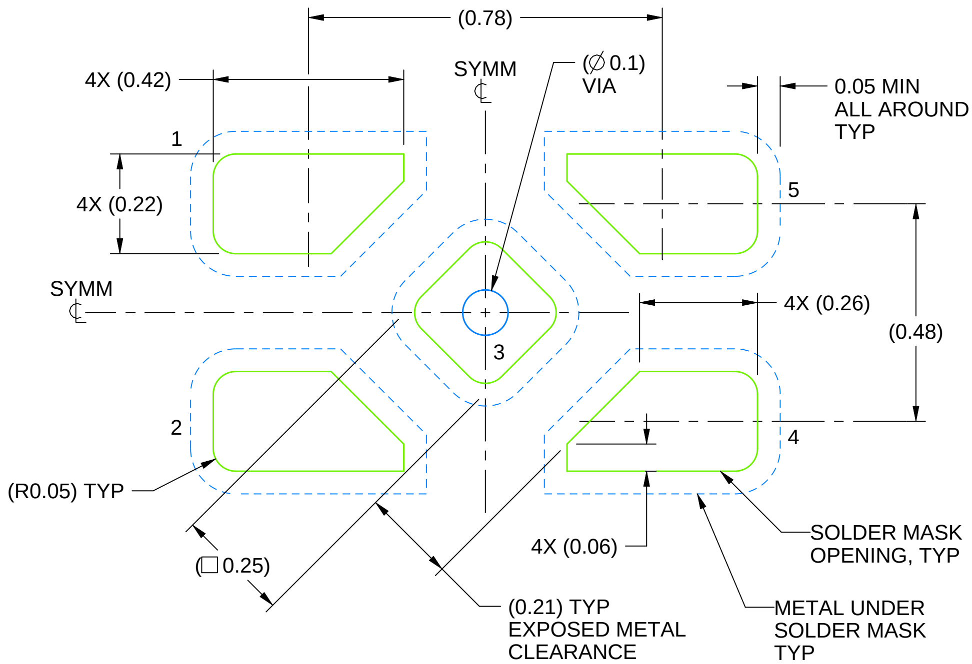
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

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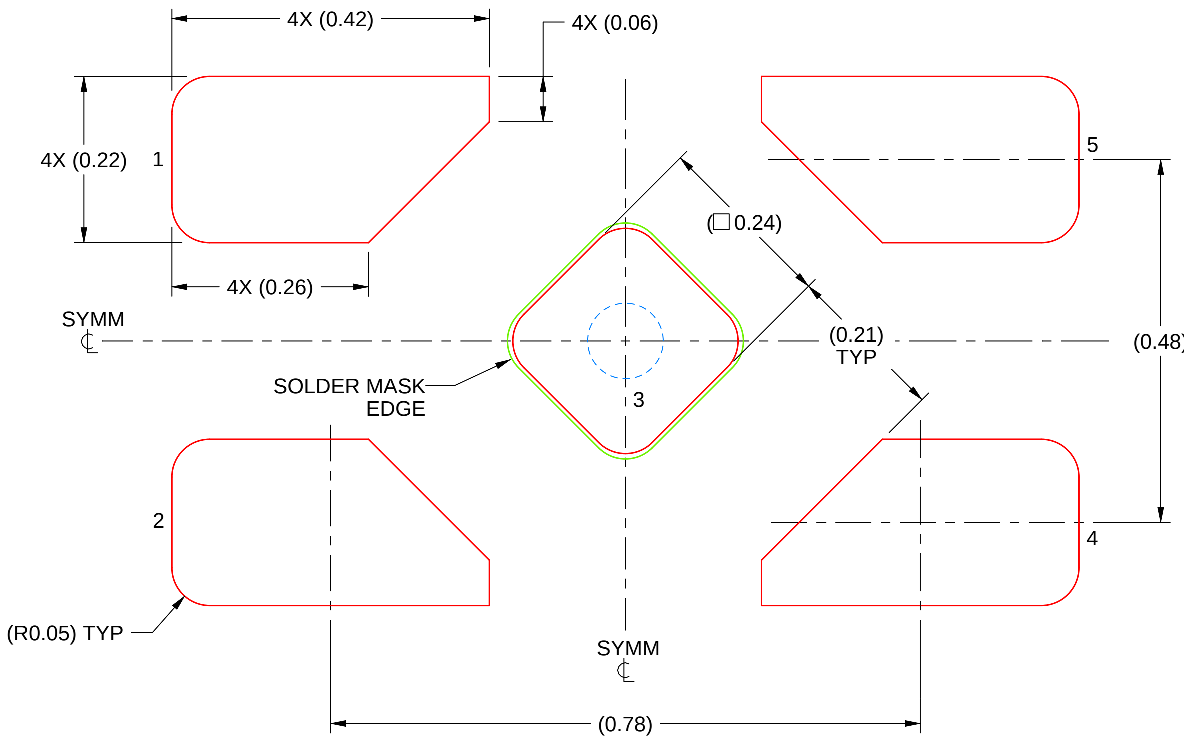
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.