DS10BR254 1.5 Gbps 1:4 LVDS Repeater

Check for Samples: DS10BR254

FEATURES

- **DC - 1.5 Gbps Low Jitter, Low Skew, Low Power Operation**
- **Wide Input Common Mode Voltage Range Allows for DC-Coupled Interface to LVDS, CML and LVPECL Drivers**
- **Redundant Inputs**
- **$\overline{\text{LOS}}$ Circuitry Detects Open Inputs Fault Condition**
- **Integrated 100Ω Input and Output Terminations**
- **8 kV ESD on LVDS I/O Pins Protects Adjoining Components**
- **Small 6 mm x 6 mm WQFN-40 Space Saving Package**

APPLICATIONS

- **Clock Distribution**
- **Clock and Data Buffering and Muxing**
- **OC-12 / STM-4**
- **SD/HD SDI Routers**

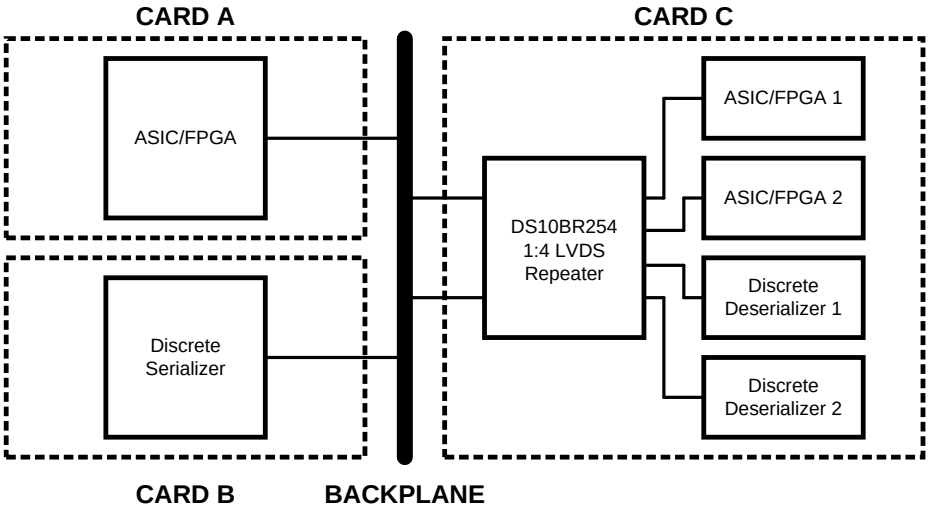
DESCRIPTION

The DS10BR254 is a 1.5 Gbps 1:4 LVDS repeater optimized for high-speed signal routing and distribution over FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

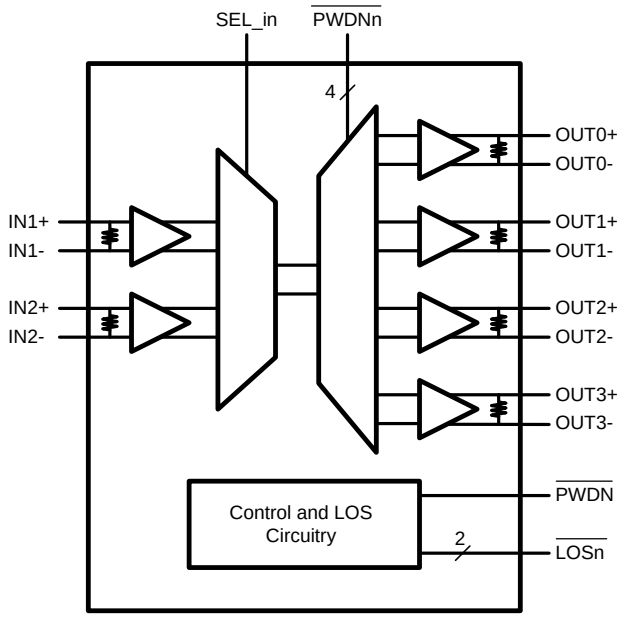
The device has two different LVDS input channels and a select pin determines which input is active. A loss-of-signal ($\overline{\text{LOS}}$) circuit monitors both input channels and a unique $\overline{\text{LOS}}$ pin is asserted when no signal is detected at that input.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower device return losses, reduce component count and further minimize board space.

Typical Application



Block Diagram



Connection Diagram

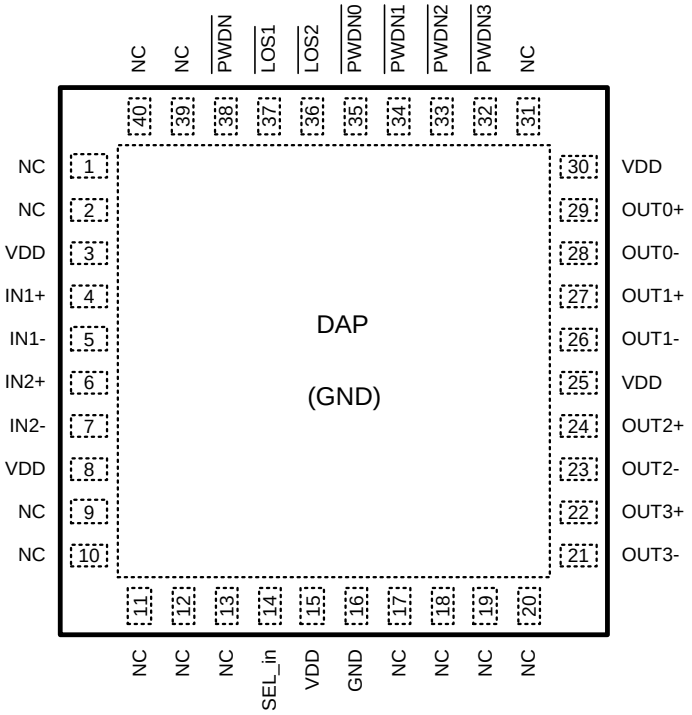


Figure 1. DS10BR254 Pin Diagram
See Package Number RTA0040A

PIN DESCRIPTIONS

Pin Name	Pin Number	I/O, Type	Pin Description
IN1+, IN1-, IN2+, IN2-,	4, 5, 6, 7,	I, LVDS	Inverting and non-inverting high speed LVDS input pins.
OUT0+, OUT0-, OUT1+, OUT1-, OUT2+, OUT2-, OUT3+, OUT3-	29, 28, 27, 26, 24, 23, 22, 21	O, LVDS	Inverting and non-inverting high speed LVDS output pins.
SEL_in	14	I, LVCMOS	This pin selects which LVDS input is active.
$\overline{\text{LOS1}}$, $\overline{\text{LOS2}}$	37, 36	O, LVCMOS	Loss Of Signal output pins, $\overline{\text{LOSn}}$ report when an open input fault condition is detected at the input, INn. These are open drain outputs. External pull up resistors are required.
$\overline{\text{PWDN0}}$, $\overline{\text{PWDN1}}$, $\overline{\text{PWDN2}}$, $\overline{\text{PWDN3}}$	35, 34 33, 32	I, LVCMOS	Channel output power down pin. When the $\overline{\text{PWDNn}}$ is set to L, the channel output OUTn is in the power down mode.
$\overline{\text{PWDN}}$	38	I, LVCMOS	Device power down pin. When the $\overline{\text{PWDN}}$ is set to L, the device is in the power down mode.
VDD	3, 8, 15,25, 30	Power	Power supply pins.
GND	16, DAP	Power	Ground pin and a pad (DAP - die attach pad).
NC	1, 2 9, 10, 11, 12, 13, 17, 18, 19, 20, 31, 39, 40	NC	NO CONNECT pins. May be left floating.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage		−0.3V to +4V
LVCMOS Input Voltage		−0.3V to (V_{CC} + 0.3V)
LVCMOS Output Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Input Voltage		−0.3V to +4V
Differential Input Voltage |VID|		1V
LVDS Output Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Differential Output Voltage		0.0V to +1V
LVDS Output Short Circuit Current Duration		5 ms
Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range	Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	SQA Package	4.65W
	Derate SQA Package	37.2 mW/°C above +25°C
Package Thermal Resistance	θ_{JA}	+26.9°C/W
	θ_{JC}	+3.8°C/W
ESD Susceptibility	HBM[3]	≥8 kV
	MM[4]	≥250V
	CDM[5]	≥1250V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V V_{CC} = 3.6V		0	±10	µA
I_{IL}	Low Level Input Current	V_{IN} = GND V_{CC} = 3.6V		0	±10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA, V_{CC} = 0V		−0.9	−1.5	V
V_{OL}	Low Level Output Voltage	I_{OL}= 4 mA		0.26	0.4	V
LVDS INPUT DC SPECIFICATIONS						
V_{ID}	Input Differential Voltage		0		1	V
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V or V_{CC}-0.05V		0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input Current	V_{IN} = +3.6V or 0V V_{CC} = 3.6V or 0V		±1	±10	µA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
LVDS OUTPUT DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current(4)	OUT to GND		-35	-55	mA
		OUT to V_{CC}		7	55	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
SUPPLY CURRENT						
I_{CC}	Supply Current	$\overline{PWDN}$ = H		113	135	mA
I_{CCZ}	Power Down Supply Current	$\overline{PWDN}$ = L		50	60	mA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics

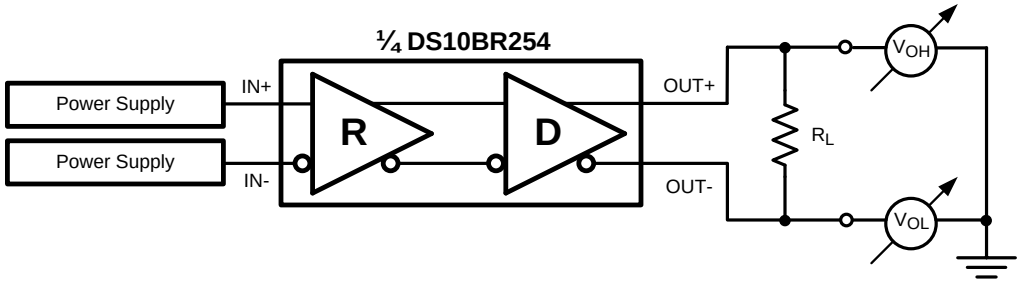
Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS							
t_{PLHD}	Differential Propagation Delay Low to High(1)	R_L = 100Ω			440	650	ps
t_{PHLD}	Differential Propagation Delay High to Low(1)				400	650	ps
t_{SKD1}	Pulse Skew $\|t_{PLHD} - t_{PHLD}\|$(1)(2)				40	100	ps
t_{SKD2}	Channel to Channel Skew(1)(3)				40	125	ps
t_{SKD3}	Part to Part Skew(1)(4)				50	200	ps
t_{LHT}	Rise Time(1)	R_L = 100Ω			150	300	ps
t_{HLT}	Fall Time(1)				150	300	ps
t_{ON}	Any $\overline{PWDN}$ to Output Active Time				8	20	µs
t_{OFF}	Any $\overline{PWDN}$ to Output Inactive Time				5	12	ns
t_{SEL}	Select Time				5	12	ns
JITTER PERFORMANCE(1)							
t_{RJ1}	Random Jitter (RMS Value)(5)	V_{ID} = 350 mV, V_{CM} = 1.2V, Clock (RZ)	135 MHz		0.5	1	ps
t_{RJ2}			311 MHz		0.5	1	ps
t_{RJ3}			503 MHz		0.5	1	ps
t_{RJ4}			750 MHz		0.5	1	ps
t_{DJ1}	Deterministic Jitter (Peak to Peak Value)(6)	V_{ID} = 350 mV, V_{CM} = 1.2V, K28.5 (NRZ)	270 Mbps		6	22	ps
t_{DJ2}			622 Mbps		6	21	ps
t_{DJ3}			1.0625 Gbps		9	18	ps
t_{DJ4}			1.5 Gbps		9	17	ps
t_{TJ1}	Total Jitter(7)	V_{ID} = 350 mV, V_{CM} = 1.2V, PRBS-23 (NRZ)	270 Mbps		0.01	0.03	UI_{P-P}
t_{TJ2}			622 Mbps		0.01	0.03	UI_{P-P}
t_{TJ3}			1.0625 Gbps		0.01	0.04	UI_{P-P}
t_{TJ4}			1.5 Gbps		0.01	0.06	UI_{P-P}

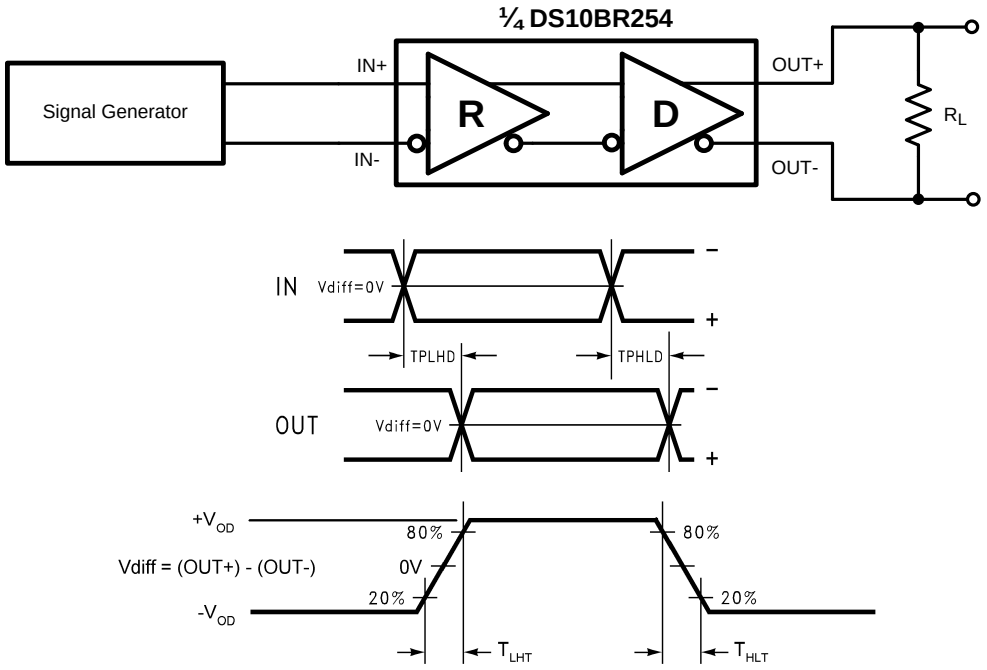
(1) Specification is specified by characterization and is not tested in production.
(2) t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(3) t_{SKD2}, Channel to Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).
(4) t_{SKD3}, Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(5) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
(6) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(7) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

APPLICATION INFORMATION

DC TEST CIRCUITS



AC TEST CIRCUITS AND TIMING DIAGRAMS



FUNCTIONAL DESCRIPTION

The DS10BR254 is a 1.5 Gbps 1:4 LVDS repeater optimized for high-speed signal routing and distribution over lossy FR-4 printed circuit board backplanes and balanced cables.

Table 1. Input Select Truth Table

CONTROL Pin (SEL_in) State	Input Selected
0	IN1
1	IN2

Input Interfacing

The DS10BR254 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS10BR254 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS10BR254 inputs are internally terminated with a 100Ω resistor.

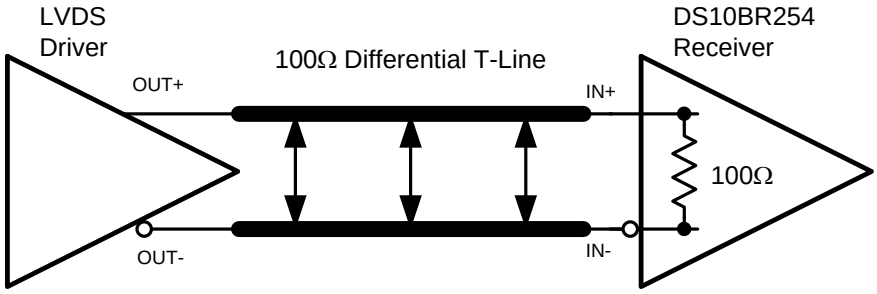


Figure 2. Typical LVDS Driver DC-Coupled Interface to an DS10BR254 Input

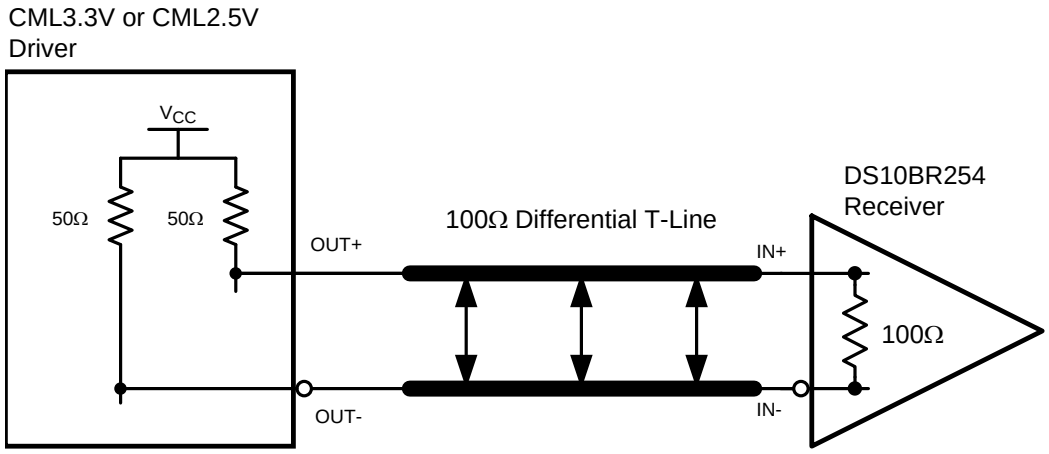


Figure 3. Typical CML Driver DC-Coupled Interface to an DS10BR254 Input

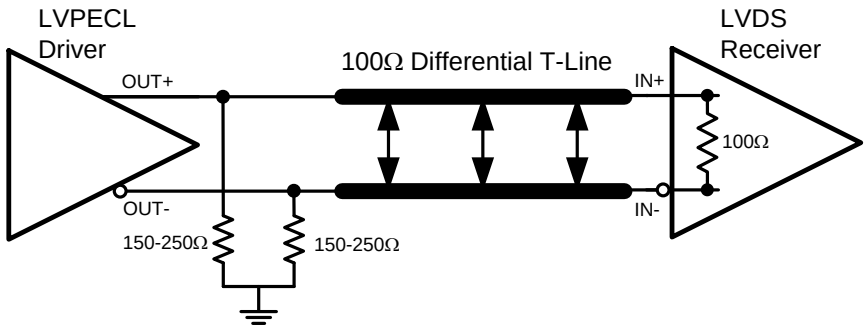


Figure 4. Typical LVPECL Driver DC-Coupled Interface to an DS10BR254 Input

Output Interfacing

The DS10BR254 outputs signals compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accomodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

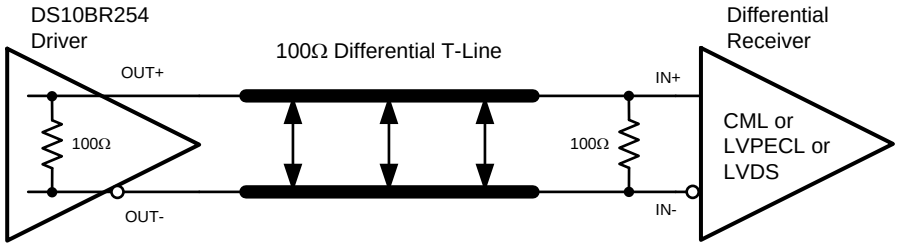


Figure 5. Typical DS10BR254 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance

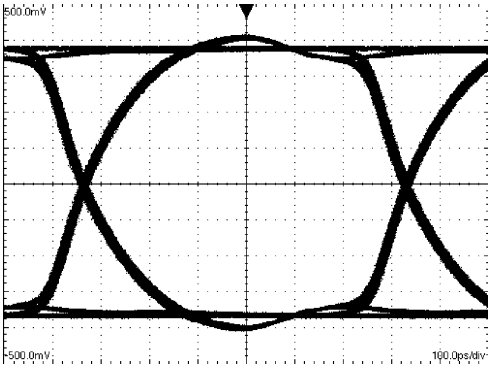


Figure 6. A 1.5 Gbps NRZ PRBS-7 After 2" Differential FR-4 Stripline V:100 mV / DIV, H:100 ps / DIV

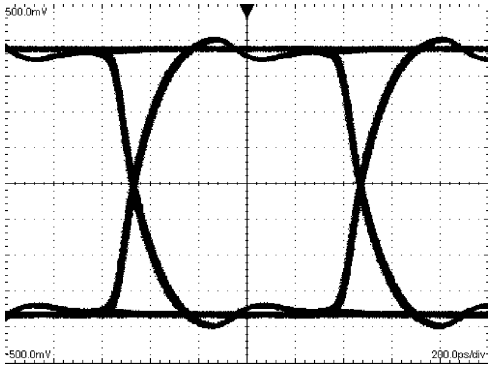


Figure 7. A 1.06 Gbps NRZ PRBS-7 After 2" Differential FR-4 Stripline V:100 mV / DIV, H:200 ps / DIV

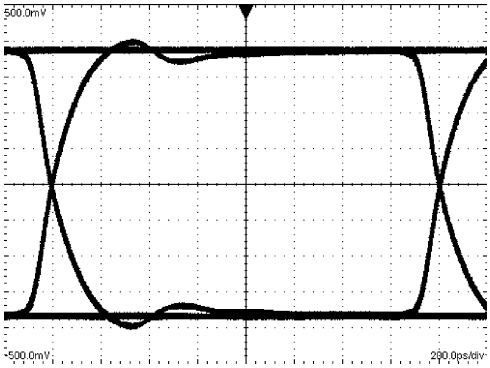


Figure 8. A 622 Mbps NRZ PRBS-7 After 2" Differential FR-4 Stripline V:100 mV / DIV, H:200 ps / DIV

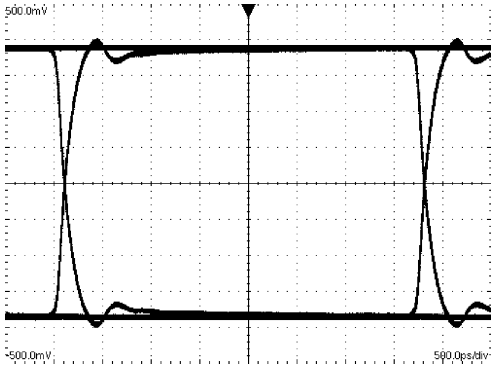


Figure 9. A 270 Mbps NRZ PRBS-7 After 2" Differential FR-4 Stripline V:100 mV / DIV, H:500 ps / DIV

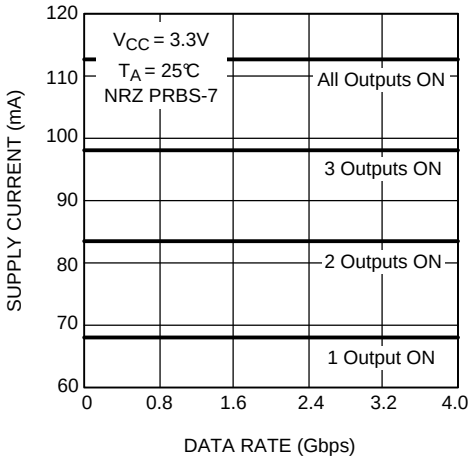


Figure 10. Supply Current as a Function of a Number of Outputs Used

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D **Page**

- Changed layout of National Data Sheet to TI format 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS10BR254TSQ/NOPB	ACTIVE	WQFN	RTA	40	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	1BR254SQ	Samples
DS10BR254TSQX/NOPB	ACTIVE	WQFN	RTA	40	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	1BR254SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

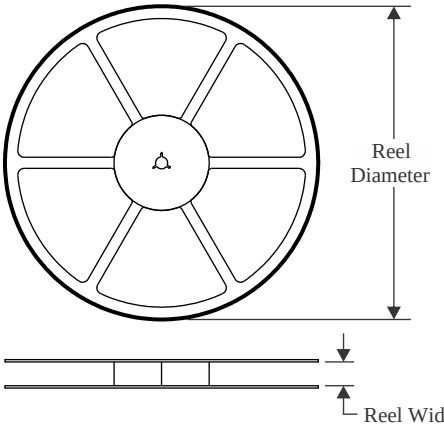
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

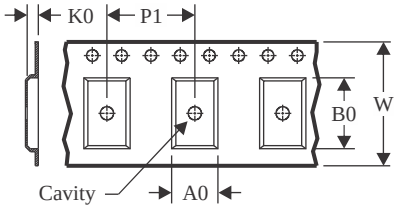
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

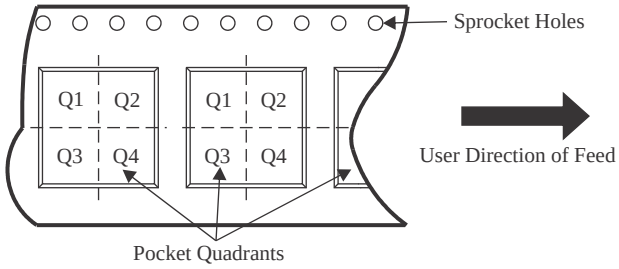


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

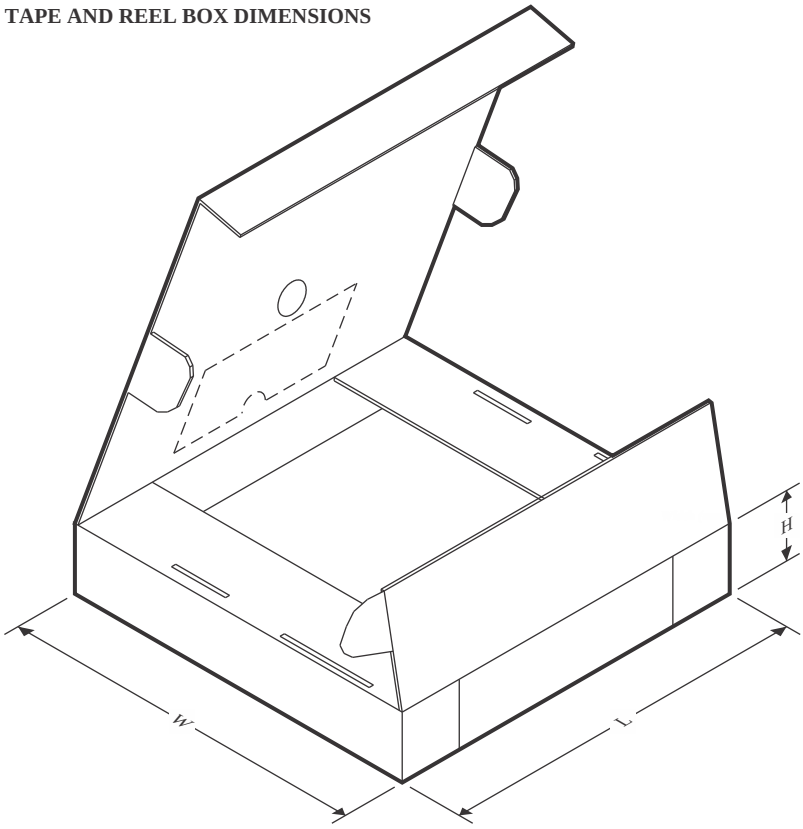
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS10BR254TSQ/NOPB	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS10BR254TSQX/NOPB	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

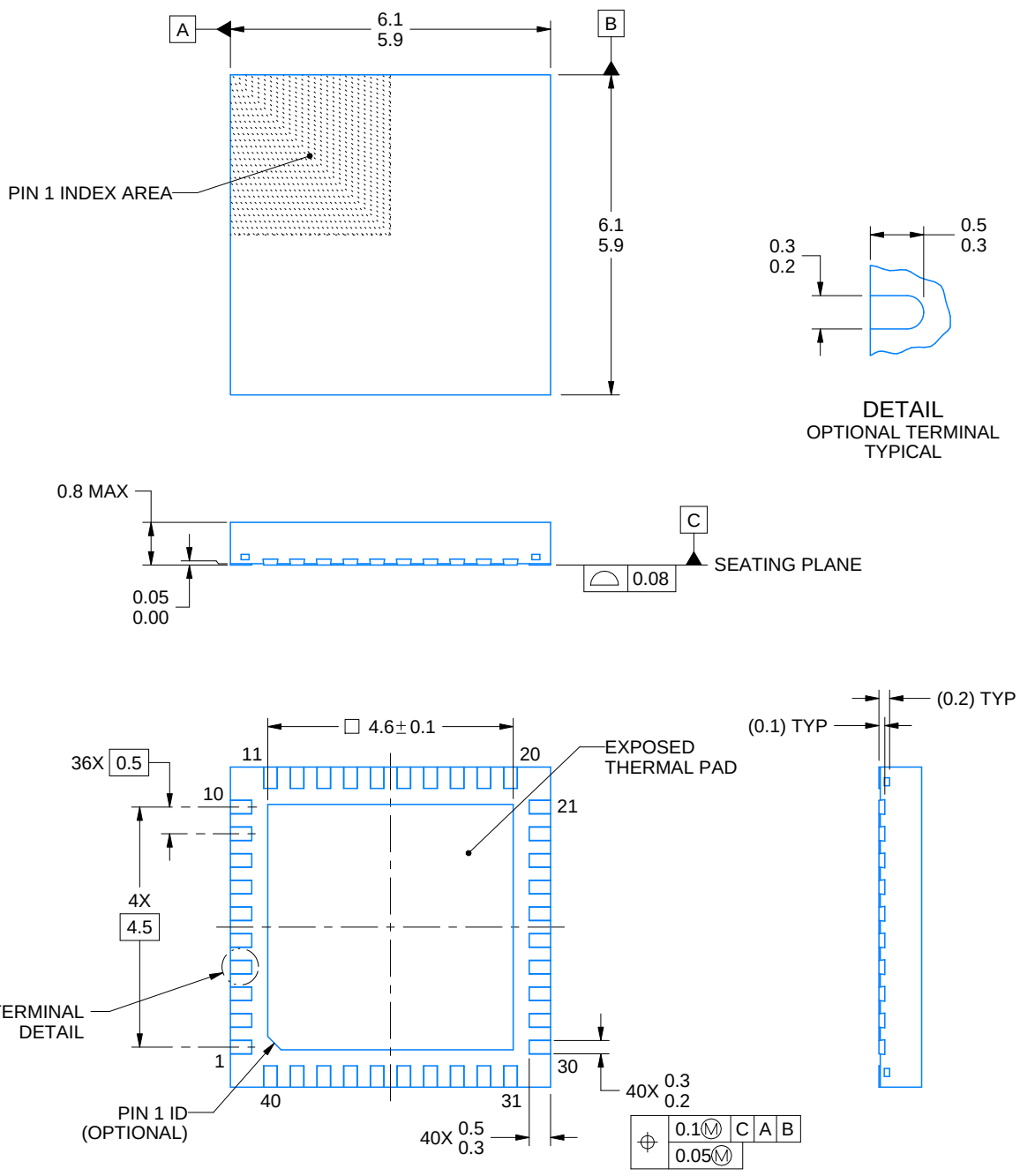
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS10BR254TSQ/NOPB	WQFN	RTA	40	250	208.0	191.0	35.0
DS10BR254TSQX/NOPB	WQFN	RTA	40	2500	356.0	356.0	36.0

PACKAGE OUTLINE

RTA0040A

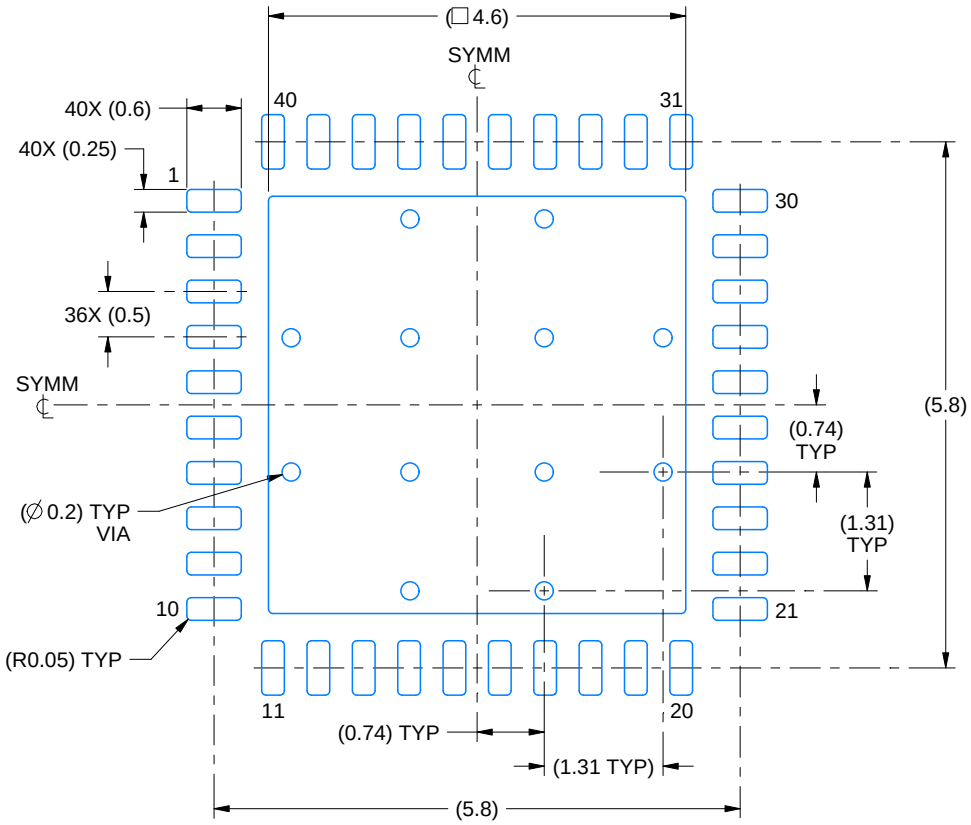
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

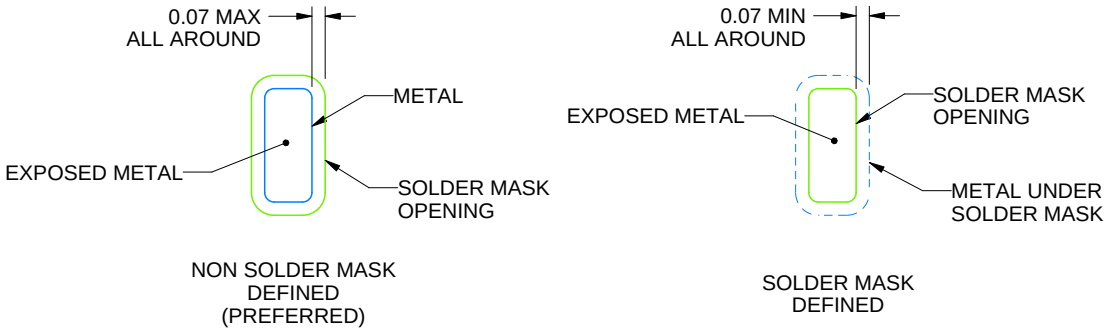


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

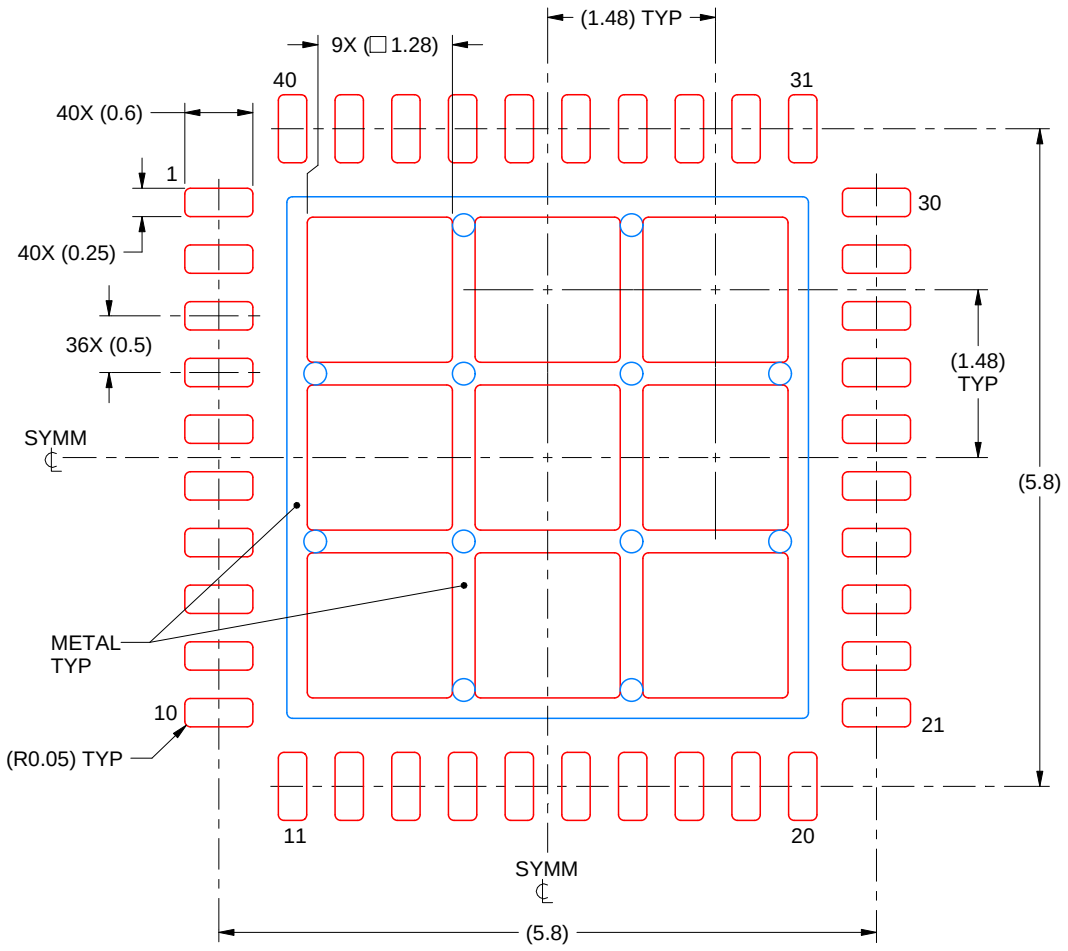


SOLDER MASK DETAILS

4214989/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4214989/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265