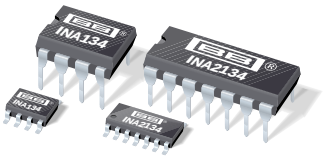
BURR-BROWN®



INA134
INA2134

AUDIO DIFFERENTIAL LINE RECEIVERS
0dB (G = 1)

FEATURES

- SINGLE AND DUAL VERSIONS
- LOW DISTORTION: 0.0005% at f = 1kHz
- HIGH SLEW RATE: 14V/µs
- FAST SETTLING TIME: 3µs to 0.01%
- WIDE SUPPLY RANGE: ±4V to ±18V
- LOW QUIESCENT CURRENT: 2.9mA max
- HIGH CMRR: 90dB
- FIXED GAIN = 0dB (1V/V)
- PACKAGES—SINGLE: 8-PIN DIP, SO-8
  DUAL: 14-PIN DIP, SO-14

APPLICATIONS

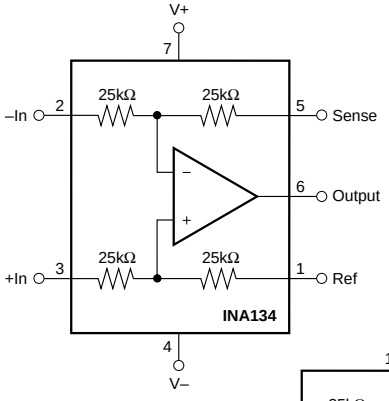
- AUDIO DIFFERENTIAL LINE RECEIVER
- SUMMING AMPLIFIER
- UNITY-GAIN INVERTING AMPLIFIER
- PSUEDOGROUND GENERATOR
- INSTRUMENTATION BUILDING BLOCK
- CURRENT SHUNT MONITOR
- VOLTAGE-CONTROLLED CURRENT SOURCE
- GROUND LOOP ELIMINATOR

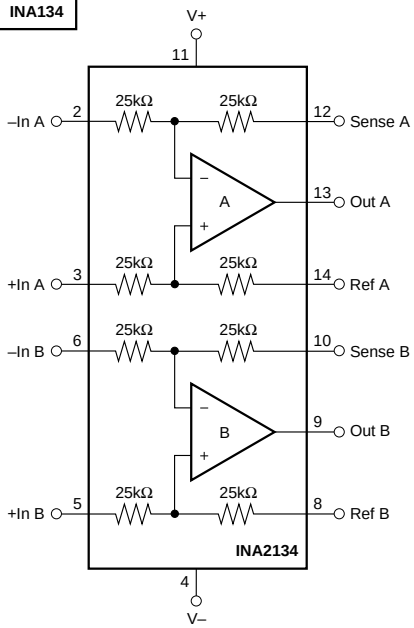
DESCRIPTION

The INA134 and INA2134 are differential line receivers consisting of high performance op amps with on-chip precision resistors. They are fully specified for high performance audio applications and have excellent ac specifications, including low distortion (0.0005% at 1kHz) and high slew rate (14V/µs), assuring good dynamic response. In addition, wide output voltage swing and high output drive capability allow use in a wide variety of demanding applications. The dual version features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The INA134 and INA2134 on-chip resistors are laser trimmed for accurate gain and optimum common-mode rejection. Furthermore, excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. Operation is guaranteed from ±4V to ±18V (8V to 36V total supply).

The INA134 is available in 8-pin DIP and SO-8 surface-mount packages. The INA2134 comes in 14-pin DIP and SO-14 surface-mount packages. Both are specified for operation over the extended industrial temperature range, –40°C to +85°C.





International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1390A
Printed in U.S.A. July, 1997
SBOS071

SPECIFICATIONS: $V_S = \pm 18V$

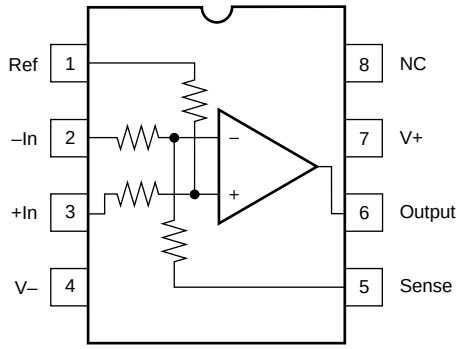
At T_A = +25°C, V_S = ±18V, R_L = 2kΩ, and Ref Pin connected to Ground, unless otherwise noted.

PARAMETER	CONDITIONS	INA134PA, UA INA2134PA, UA MIN	TYP	MAX	UNITS
AUDIO PERFORMANCE					
Total Harmonic Distortion + Noise, f = 1kHz	V_{IN} = 10Vrms		0.0005		%
Noise Floor(1)	20kHz BW		–100		dBu
Headroom(1)	THD+N < 1%		+23		dBu
FREQUENCY RESPONSE					
Small-Signal Bandwidth			3.1		MHz
Slew Rate			14		V/µs
Settling Time: 0.1%	10V Step, C_L = 100pF		2		µs
0.01%	10V Step, C_L = 100pF		3		µs
Overload Recovery Time	50% Overdrive		3		µs
Channel Separation (dual), f = 1kHz			117		dB
OUTPUT NOISE VOLTAGE(2)					
f = 20Hz to 20kHz			7		µVrms
f = 1kHz			52		$nV/\sqrt{HZ}$
OFFSET VOLTAGE(3)					
Input Offset Voltage	V_{CM} = 0V		±100	±1000	µV
vs Temperature	Specified Temperature Range		±2		µV/°C
vs Power Supply	V_S = ±4V to ±18V		±5	±60	µV/V
INPUT					
Common-Mode Voltage Range: Positive	V_O = 0V	2(V+)–5	2(V+)–4		V
Negative	V_O = 0V	2(V–)+5	2(V–)+2		V
Differential Voltage Range			See Typical Curve		
Common-Mode Rejection	V_{CM} = ±31V, R_S = 0Ω	74	90		dB
Impedance(4)					
Differential			50		kΩ
Common-Mode			50		kΩ
GAIN					
Initial			1		V/V
Error	V_O = –16V to 16V		±0.02	±0.1	%
vs Temperature			±1	±10	ppm/°C
Nonlinearity	V_O = –16V to 16V		0.0001		%
OUTPUT					
Voltage Output, Positive		(V+)–2	(V+)–1.8		V
Negative		(V–)+2	(V–)+1.6		V
Current Limit, Continuous to Common			±60		mA
Capacitive Load (Stable Operation)			500		pF
POWER SUPPLY					
Rated Voltage			±18		V
Voltage Range		±4		±18	V
Quiescent Current (per Amplifier)	I_O = 0		±2.4	±2.9	mA
TEMPERATURE RANGE					
Specification Range		–40		85	°C
Operation Range		–55		125	°C
Storage Range		–55		125	°C
Thermal Resistance, θ_{JA}					
8-Pin DIP			100		°C/W
SO-8 Surface-Mount			150		°C/W
14-Pin DIP			80		°C/W
SO-14 Surface-Mount			100		°C/W

NOTES: (1) dBu = 20log (Vrms/0.7746). (2) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network. (3) Includes effects of amplifier's input bias and offset currents. (4) 25kΩ resistors are ratio matched but have ±25% absolute value.

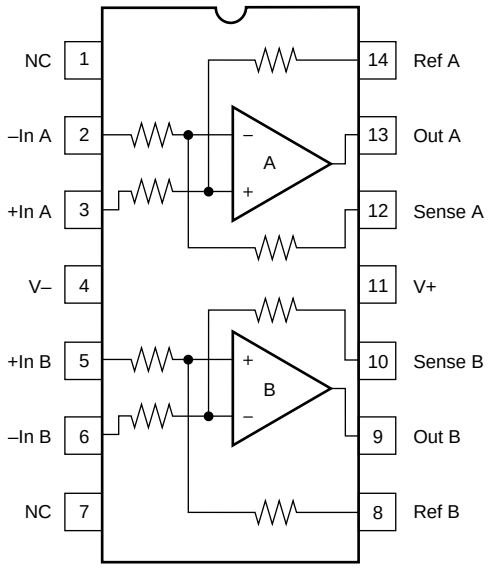
PIN CONFIGURATIONS

Top View **8-Pin DIP/SO-8**



NC = No Connection

Top View **14-Pin DIP/SO-14**



NC = No Connection

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V–	40V
Input Voltage Range	±80V
Output Short-Circuit (to ground)(2)	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. (2) One channel per package.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFICATION TEMPERATURE RANGE
Single			
INA134PA	8-Pin DIP	006	–40°C to +85°C
INA134UA	SO-8 Surface-Mount	182	–40°C to +85°C
Dual			
INA2134PA	14-Pin DIP	010	–40°C to +85°C
INA2134UA	SO-14 Surface-Mount	235	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

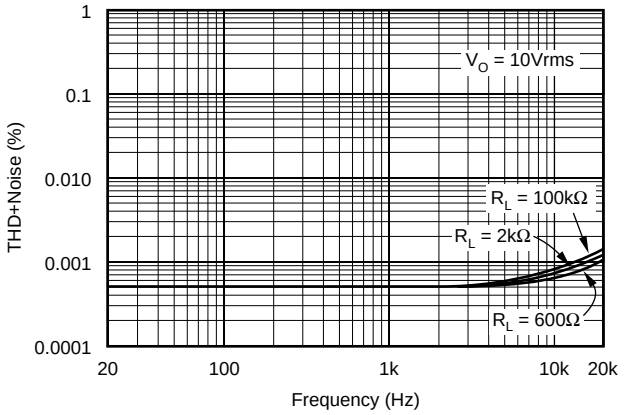
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

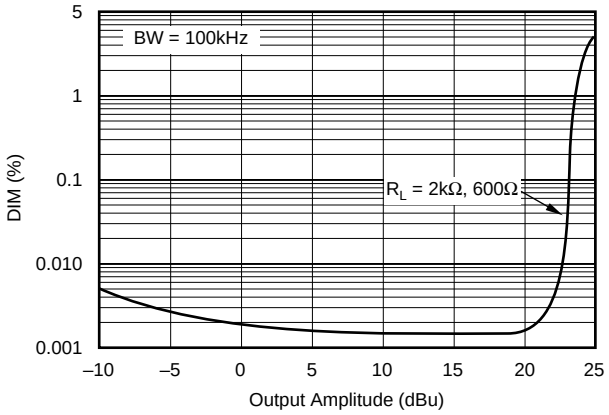
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±18V, unless otherwise noted.

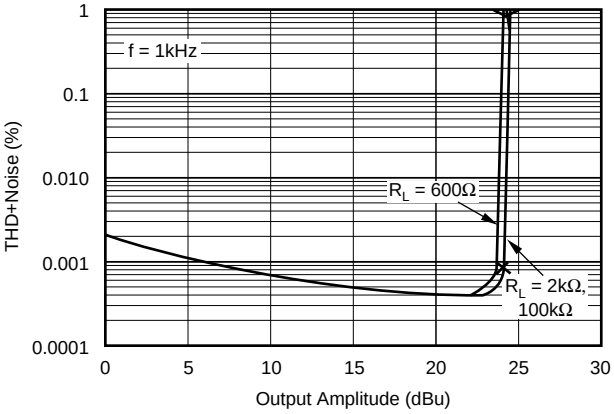
TOTAL HARMONIC DISTORTION+NOISE
vs FREQUENCY



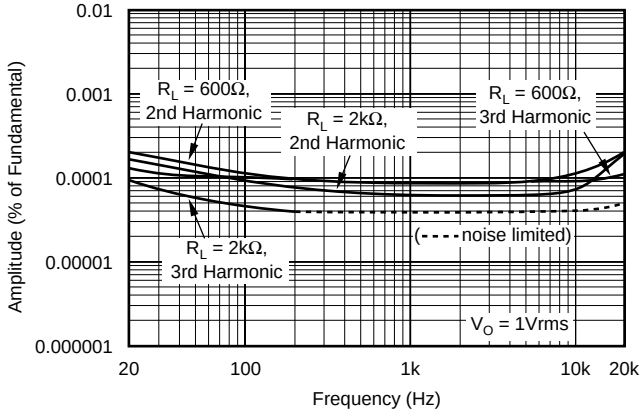
DIM INTERMODULATION DISTORTION
vs OUTPUT AMPLITUDE



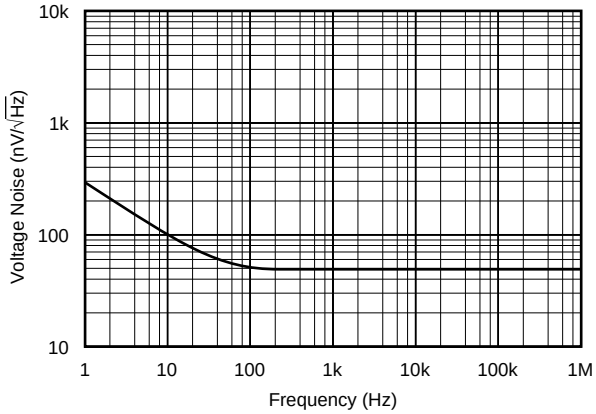
HEADROOM - TOTAL HARMONIC DISTORTION+NOISE
vs OUTPUT AMPLITUDE



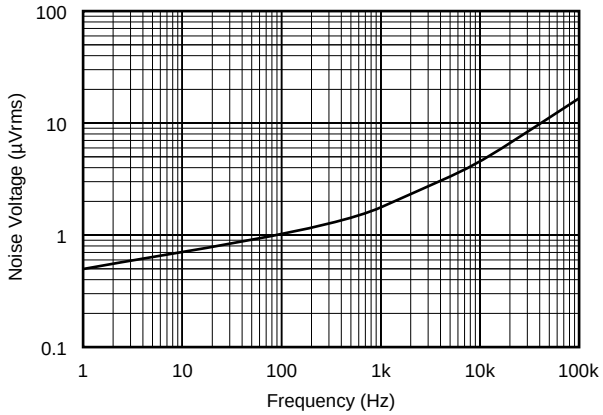
HARMONIC DISTORTION PRODUCTS
vs FREQUENCY



OUTPUT VOLTAGE NOISE SPECTRAL DENSITY
vs FREQUENCY



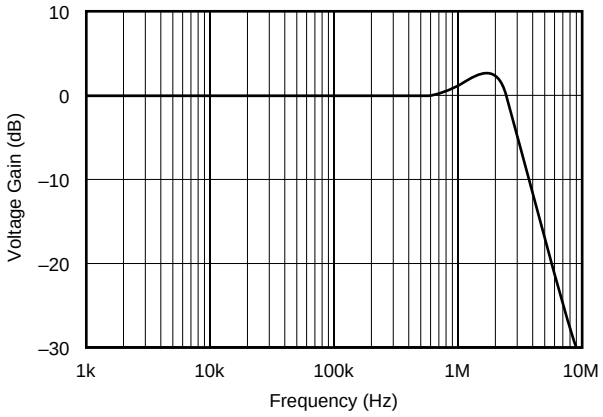
OUTPUT NOISE VOLTAGE
vs NOISE BANDWIDTH



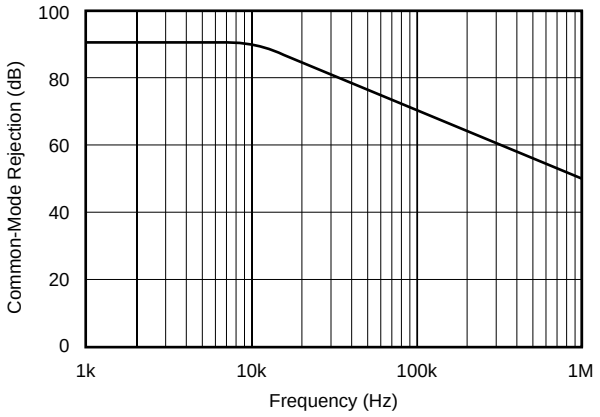
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±18V, unless otherwise noted.

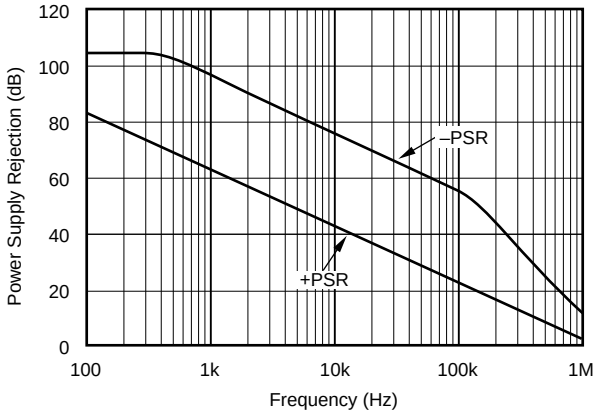
GAIN vs FREQUENCY



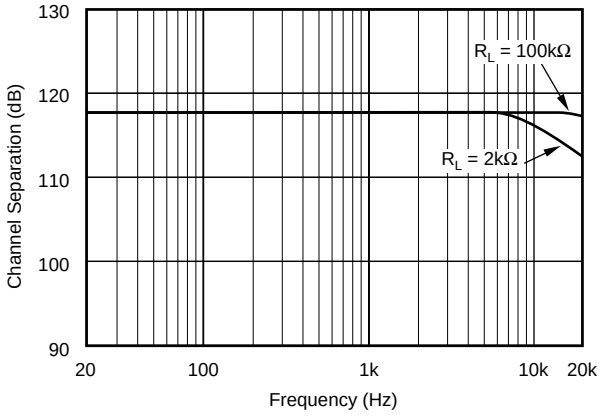
COMMON-MODE REJECTION vs FREQUENCY



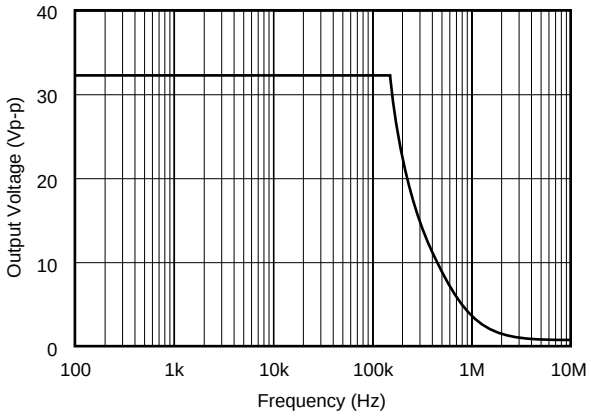
POWER SUPPLY REJECTION vs FREQUENCY



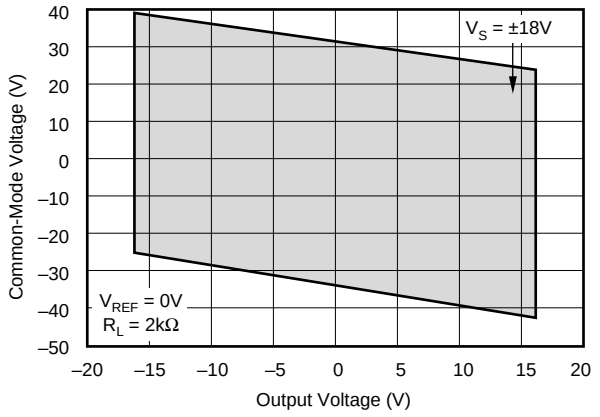
CHANNEL SEPARATION vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



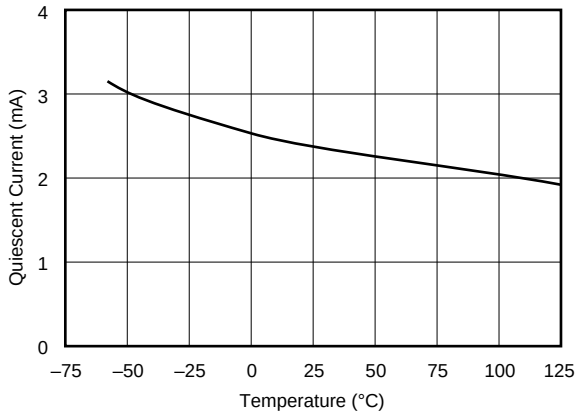
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



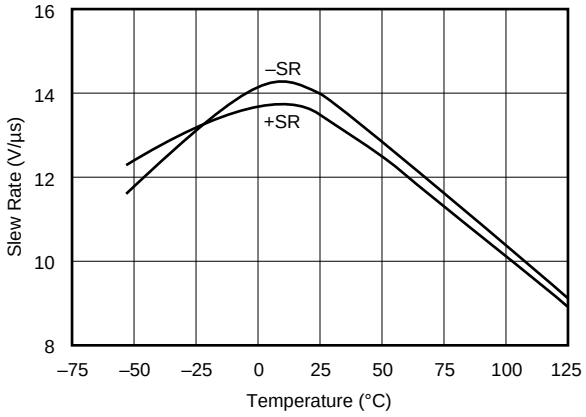
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±18V, unless otherwise noted.

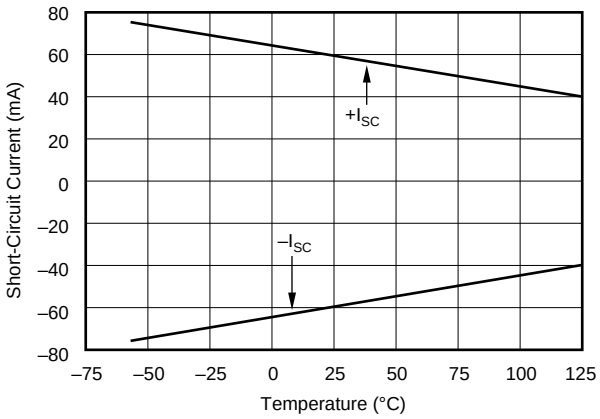
QUIESCENT CURRENT vs TEMPERATURE



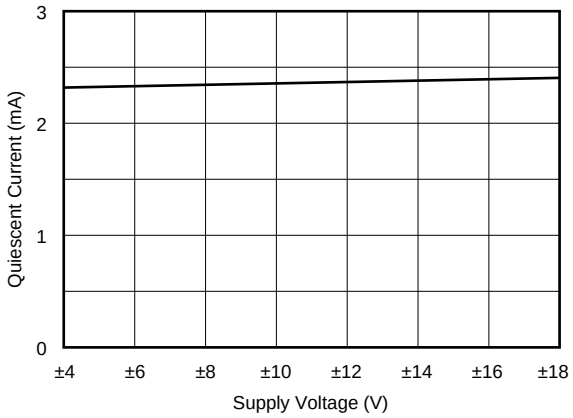
SLEW RATE vs TEMPERATURE



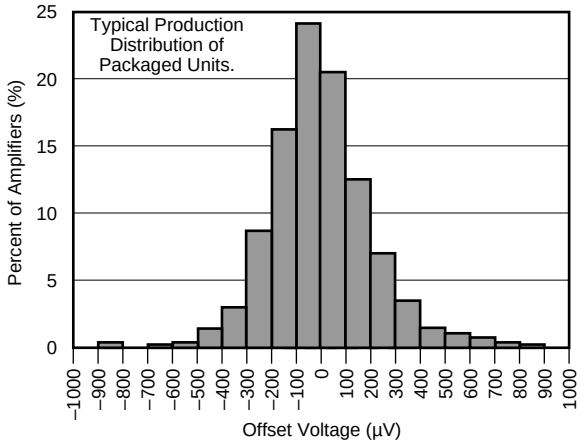
SHORT-CIRCUIT CURRENT vs TEMPERATURE



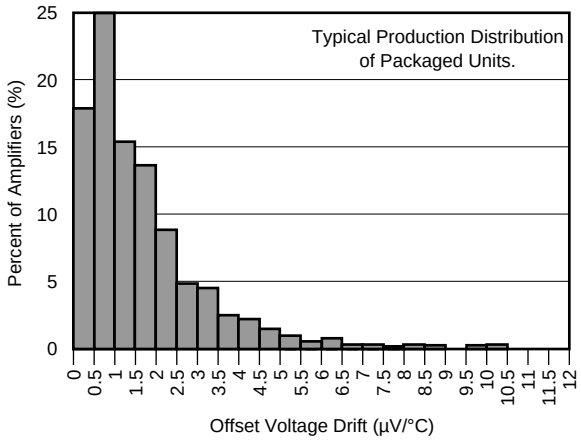
QUIESCENT CURRENT vs SUPPLY VOLTAGE



OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



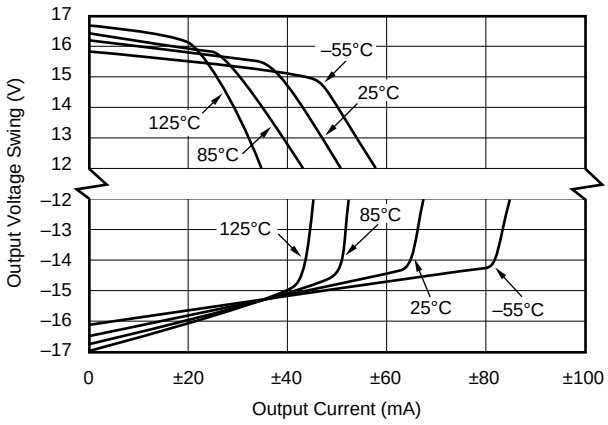
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



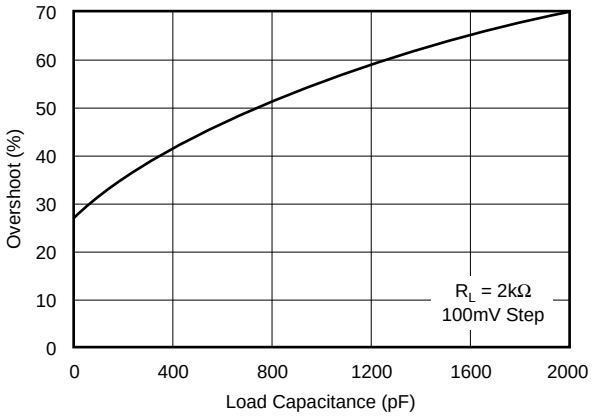
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±18V, unless otherwise noted.

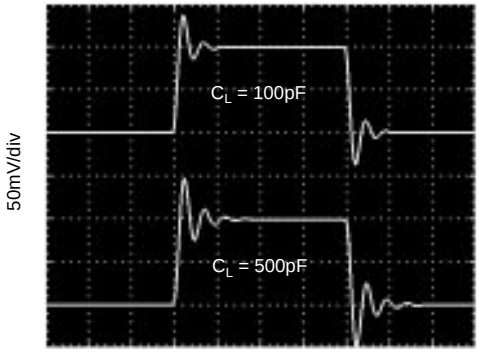
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



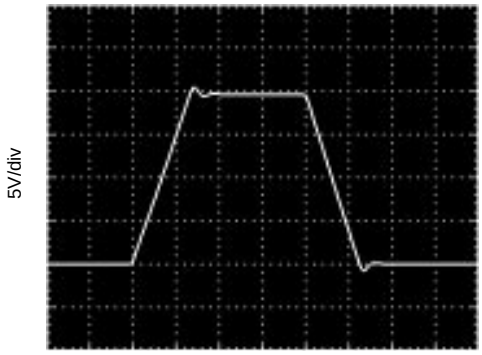
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



SMALL-SIGNAL STEP RESPONSE



LARGE-SIGNAL STEP RESPONSE
C_L = 500pF



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA134. Decoupling capacitors are strongly recommended in applications with noisy or high impedance power supplies. The capacitors should be placed close to the device pins as shown in Figure 1. All circuitry is completely independent in the dual version assuring lowest crosstalk and normal behavior when one amplifier is overdriven or short-circuited.

As shown in Figure 1, the differential input signal is connected to pins 2 and 3. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. A 10Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 74dB. If the source has a known impedance mismatch, an additional resistor in series with the opposite input can be used to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance.

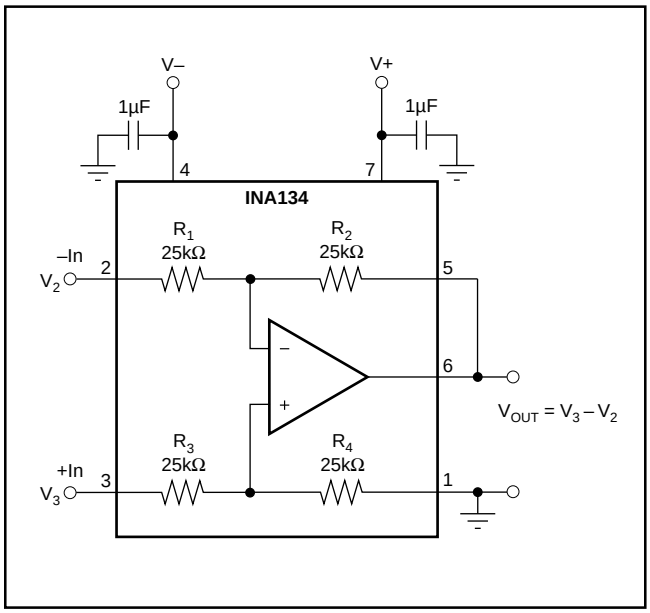


FIGURE 1. Precision Difference Amplifier (Basic Power Supply and Signal Connections).

AUDIO PERFORMANCE

The INA134 and INA2134 were designed for enhanced ac performance. Very low distortion, low noise, and wide bandwidth provide superior performance in high quality audio applications. Laser-trimmed matched resistors provide optimum common-mode rejection (typically 90dB), especially when compared to circuits implemented with an op amp and discrete precision resistors. In addition, high slew rate (14V/µs) and fast settling time (3µs to 0.01%) ensure good dynamic performance.

The INA134 and INA2134 have excellent distortion characteristics. THD+Noise is below 0.002% throughout the audio frequency range. Up to approximately 10kHz distortion is below the measurement limit of commonly used test equipment. Furthermore, distortion remains relatively flat over its wide output voltage swing range (approximately 1.7V from either supply).

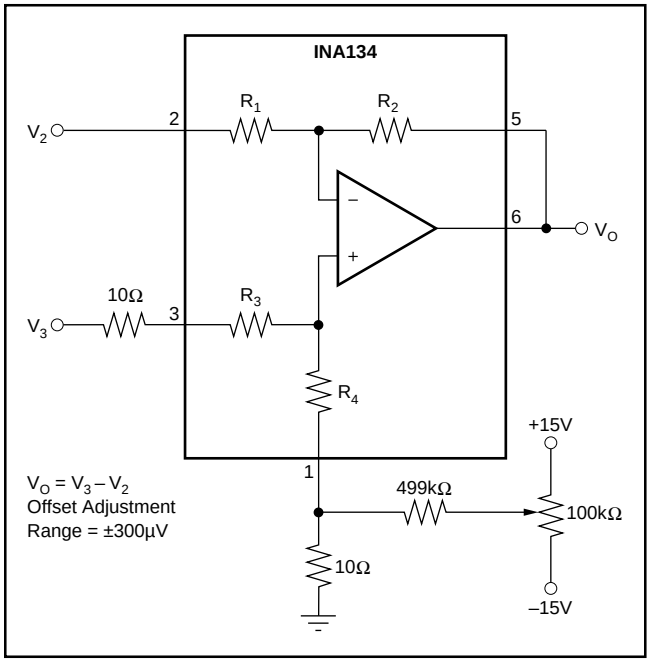


FIGURE 2. Offset Adjustment.

OFFSET VOLTAGE TRIM

The INA134 and INA2134 are laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 2. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

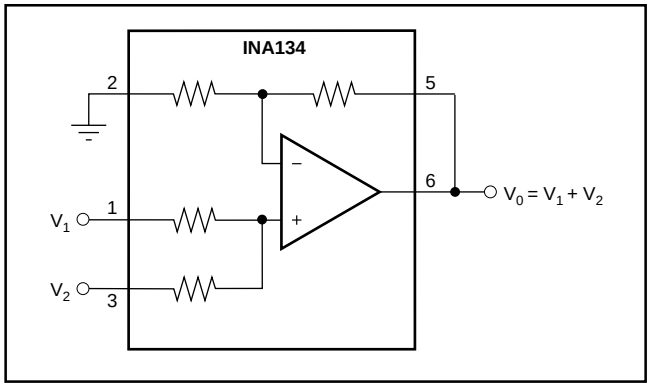


FIGURE 3. Precision Summing Amplifier.

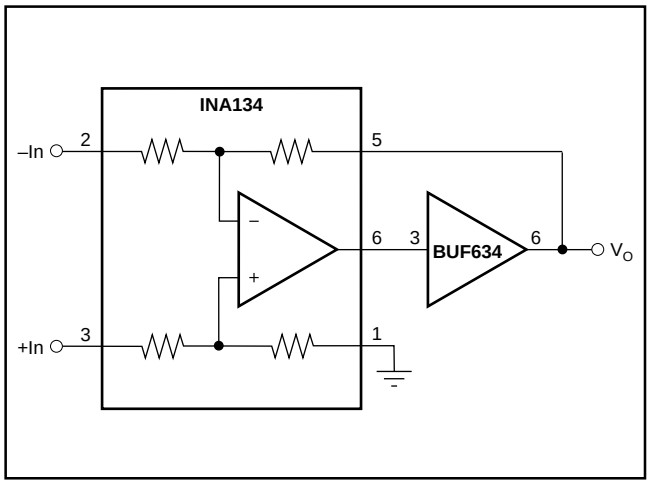


FIGURE 4. Boosting Output Current.

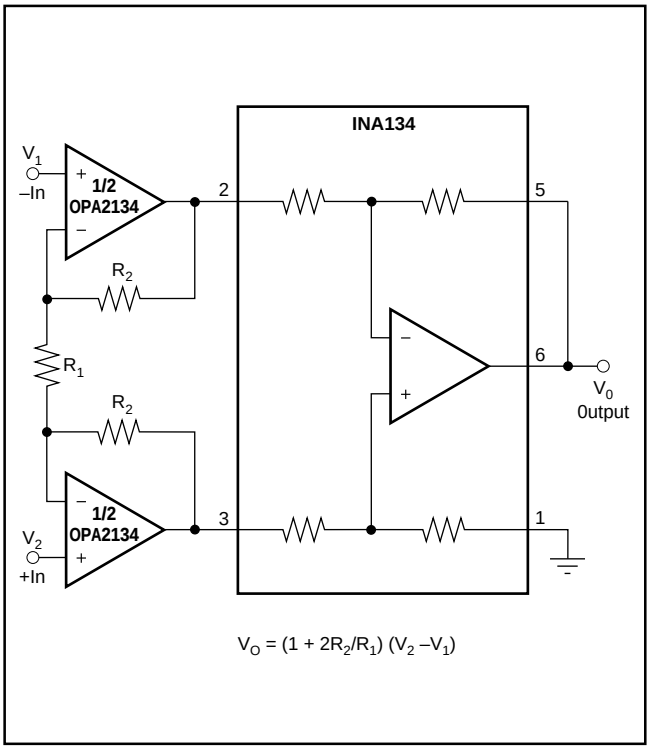


FIGURE 5. High Input Impedance Instrumentation Amplifier.

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet for additional applications ideas, including:

- Current Receiver with Compliance to Rails
- Precision Unity-Gain Inverting Amplifier
- ±10V Precision Voltage Reference
- ±5V Precision Voltage Reference
- Precision Unity-Gain Buffer
- Precision Average Value Amplifier
- Precision G = 2 Amplifier
- Precision Summing Amplifier
- Precision G = 1/2 Amplifier
- Precision Bipolar Offsetting
- Precision Summing Amplifier with Gain
- Instrumentation Amplifier Guard Drive Generator
- Precision Summing Instrumentation Amplifier
- Precision Absolute Value Buffer
- Precision Voltage-to-Current Converter with Differential Inputs
- Differential Input Voltage-to-Current Converter for Low I_{OUT}
- Isolating Current Source
- Differential Output Difference Amplifier
- Isolating Current Source with Buffering Amplifier for Greater Accuracy
- Window Comparator with Window Span and Window Center Inputs
- Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain
- Digitally Controlled Gain of ±1 Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA134PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI		INA134PA	
INA134UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 134UA	Samples
INA134UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 134UA	Samples
INA2134PA	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		INA2134PA	Samples
INA2134UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2134UA	Samples
INA2134UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2134UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA2134 :

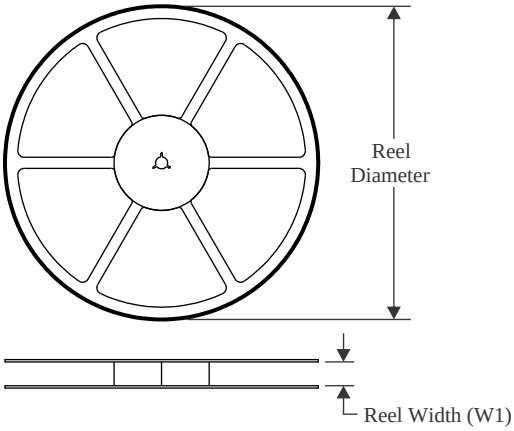
- Enhanced Product : INA2134-EP

NOTE: Qualified Version Definitions:

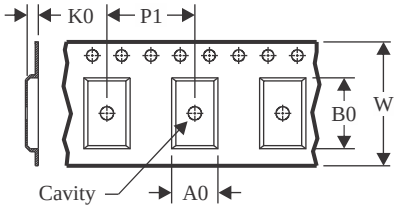
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

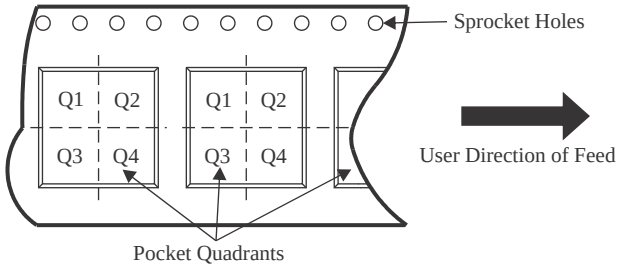


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

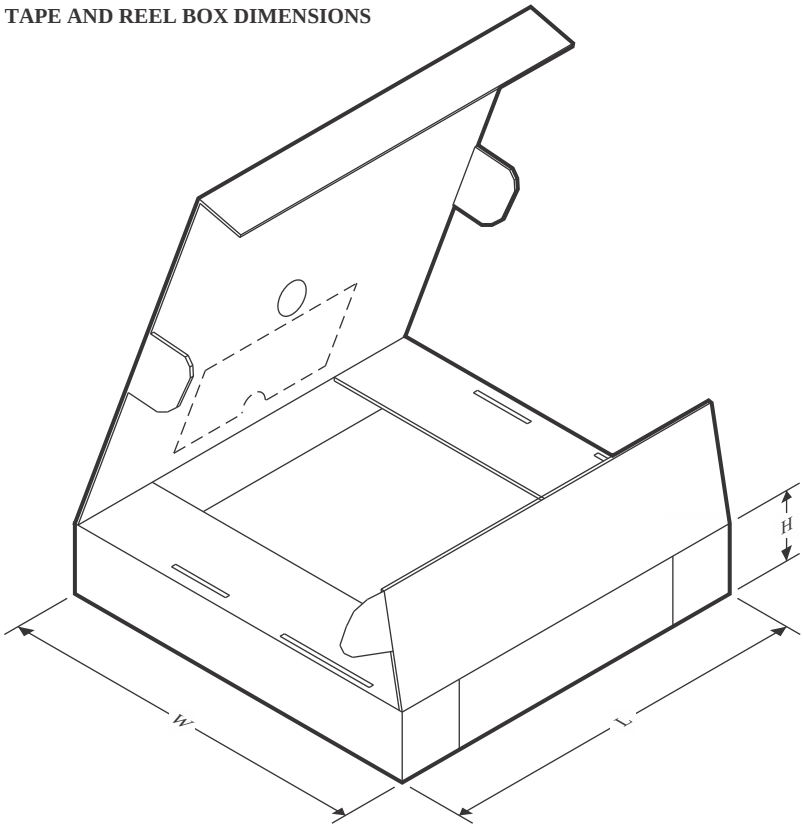
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA134UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA2134UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

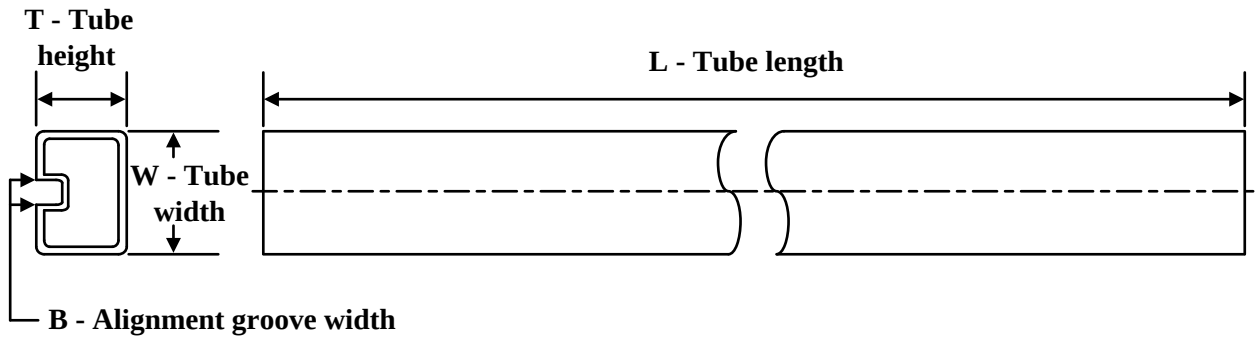
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA134UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA2134UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

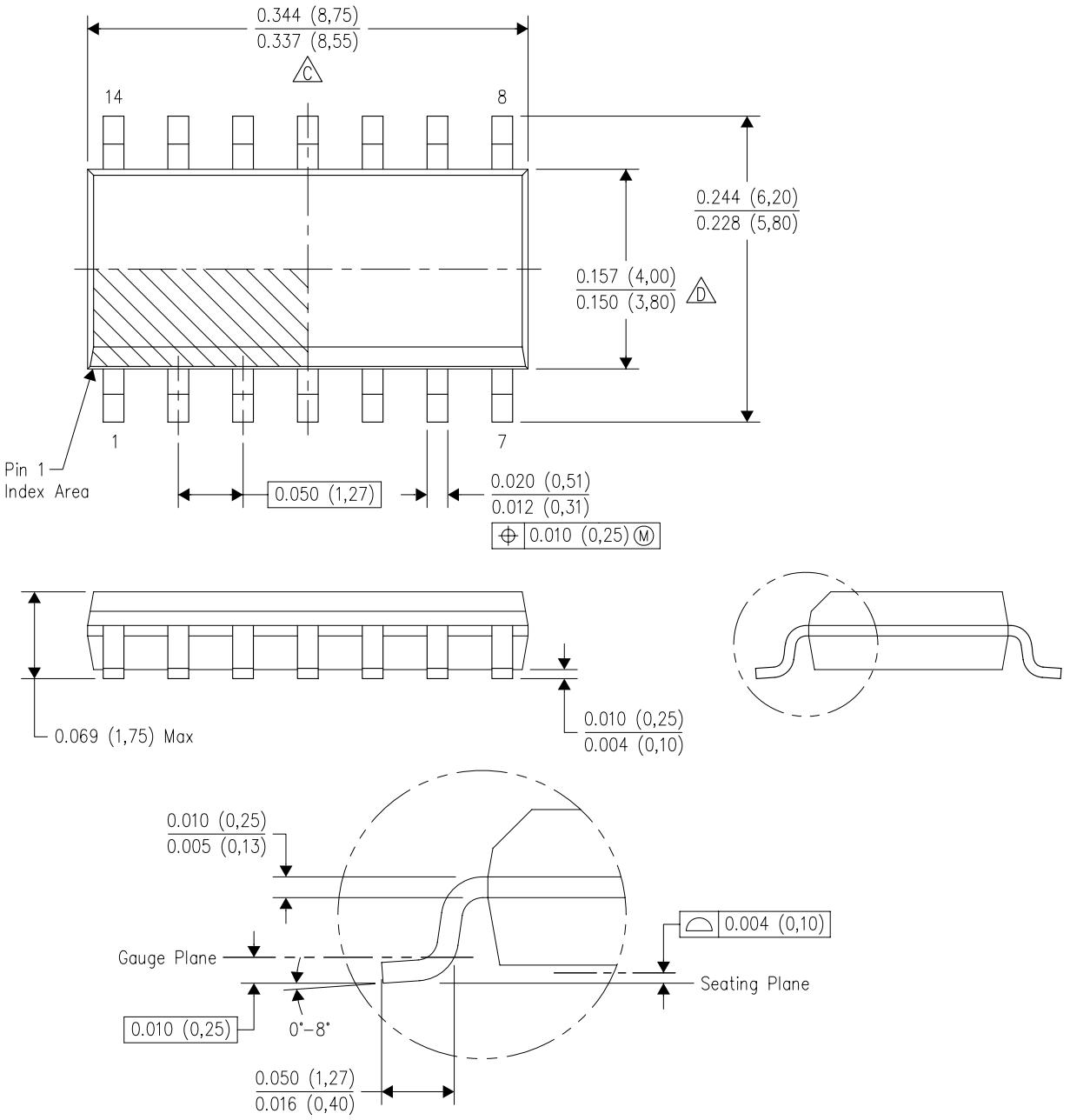
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA134PA	P	PDIP	8	50	506	13.97	11230	4.32
INA134UA	D	SOIC	8	75	506.6	8	3940	4.32
INA134UAE4	D	SOIC	8	75	506.6	8	3940	4.32
INA2134PA	N	PDIP	14	25	506	13.97	11230	4.32
INA2134UA	D	SOIC	14	50	506.6	8	3940	4.32

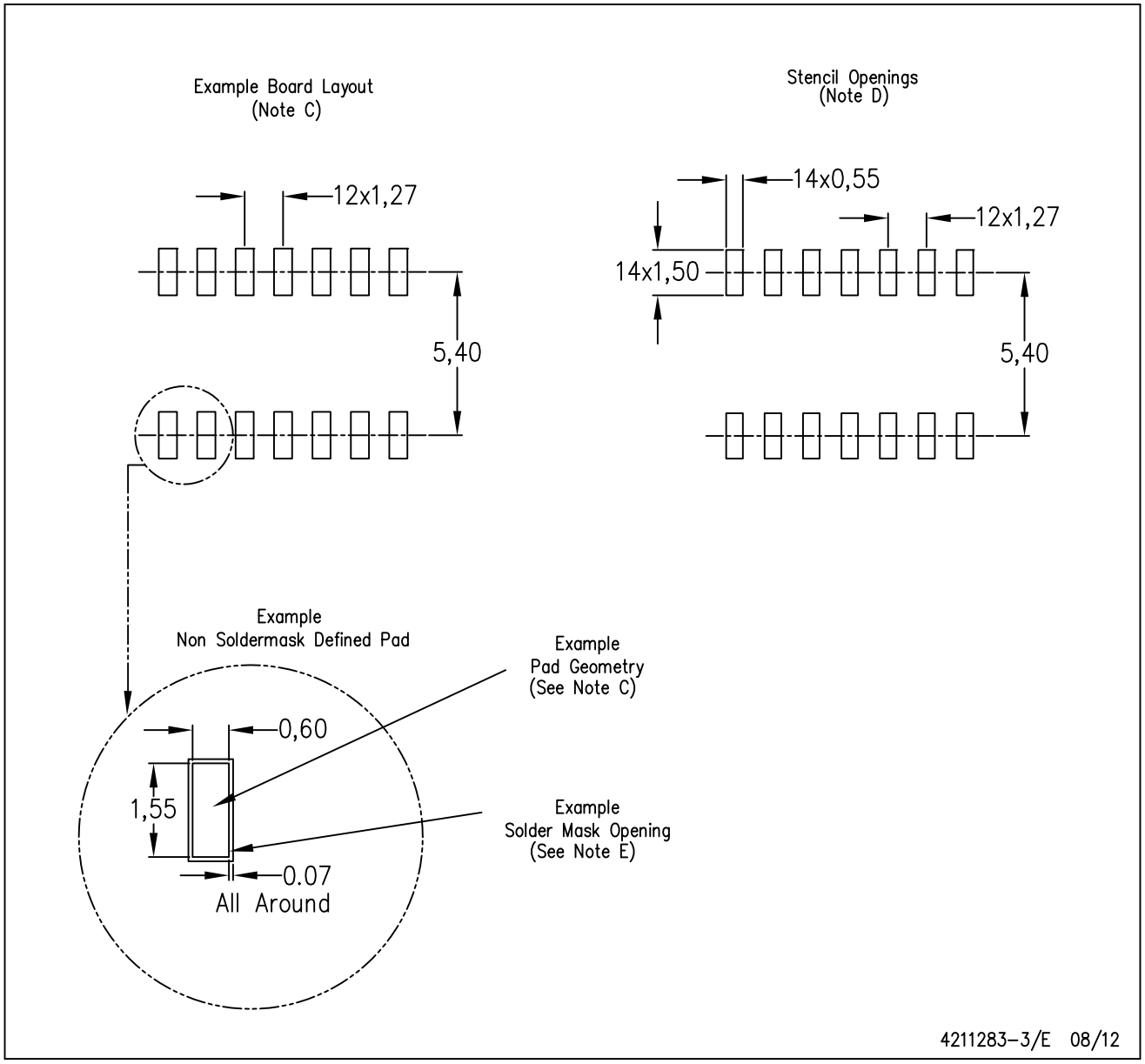
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



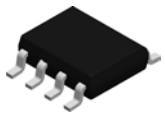
4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

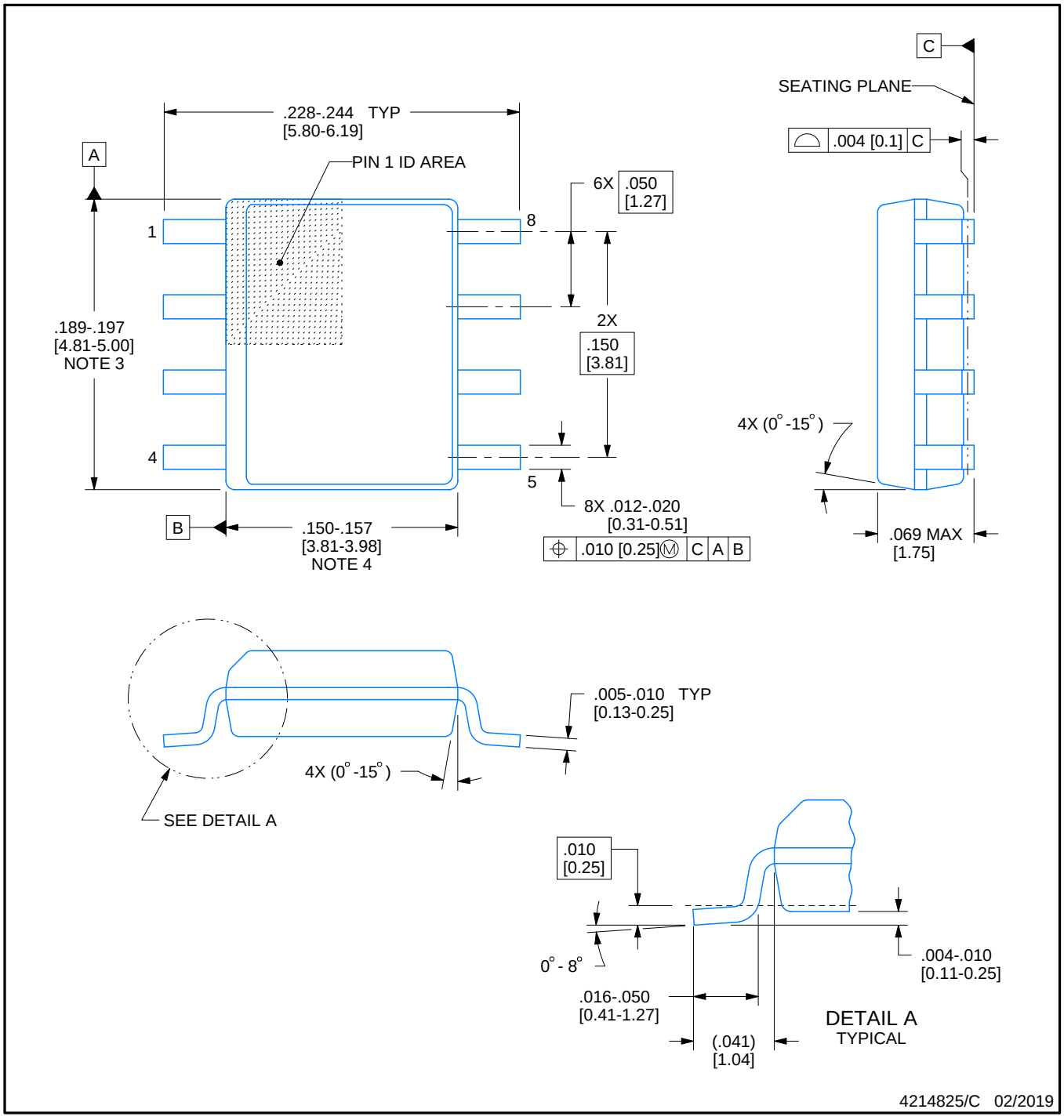


PACKAGE OUTLINE

D0008A

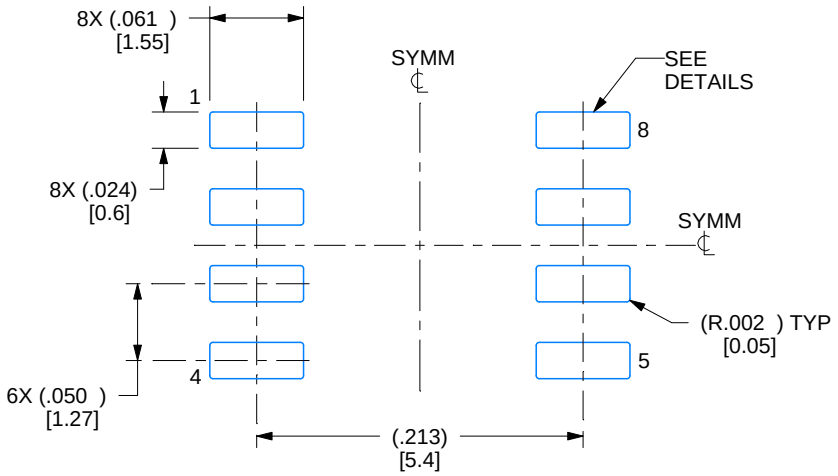
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

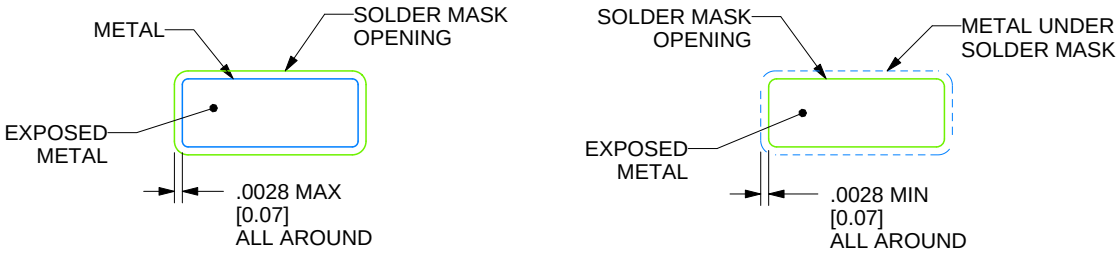


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

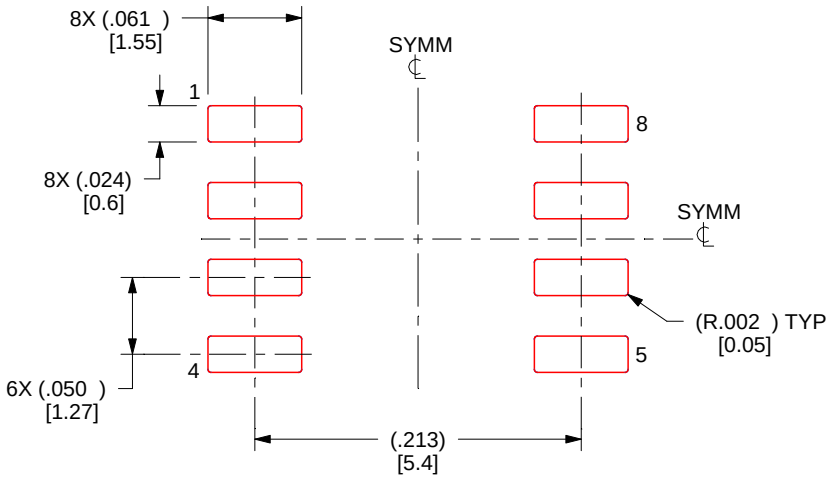
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



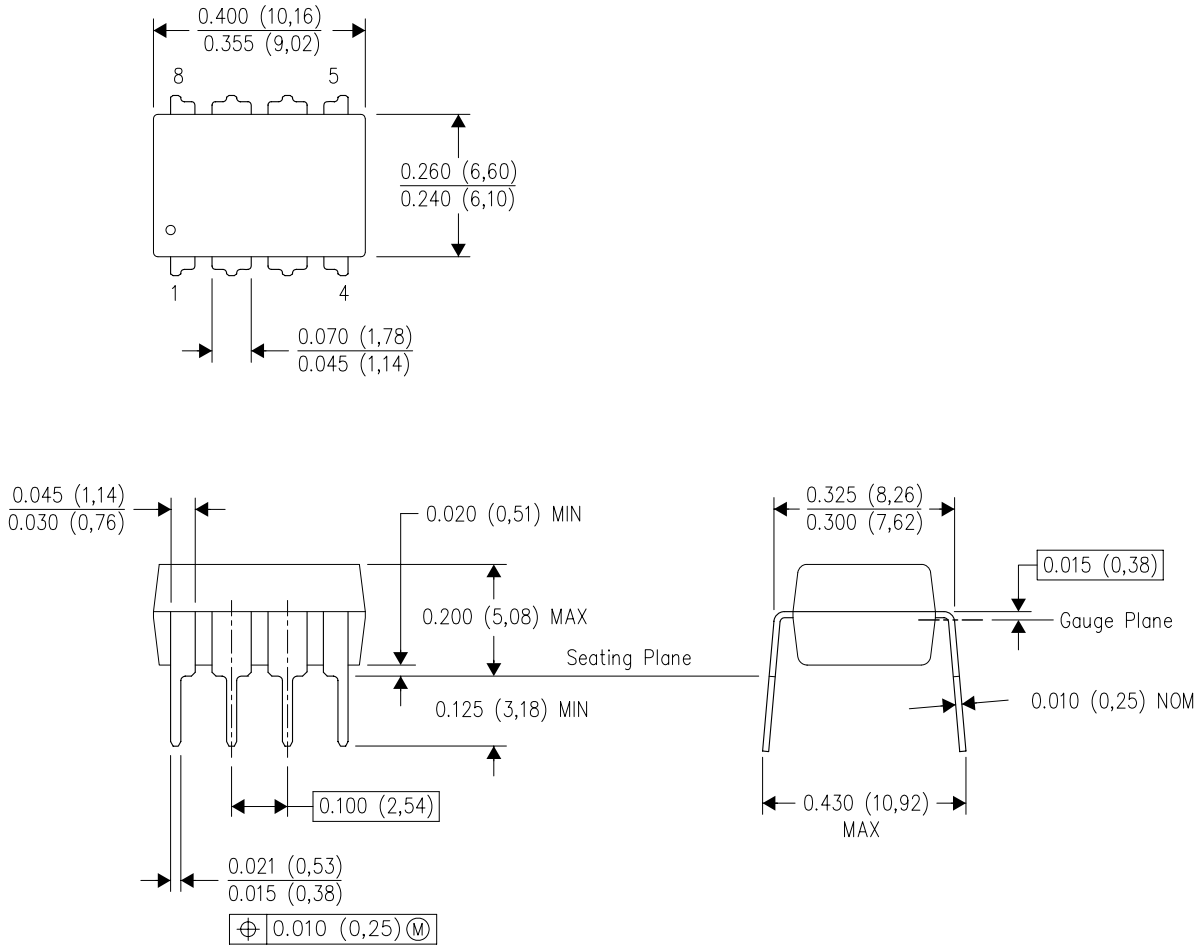
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

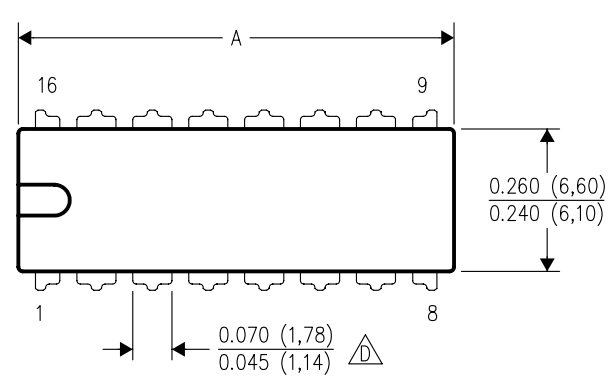


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

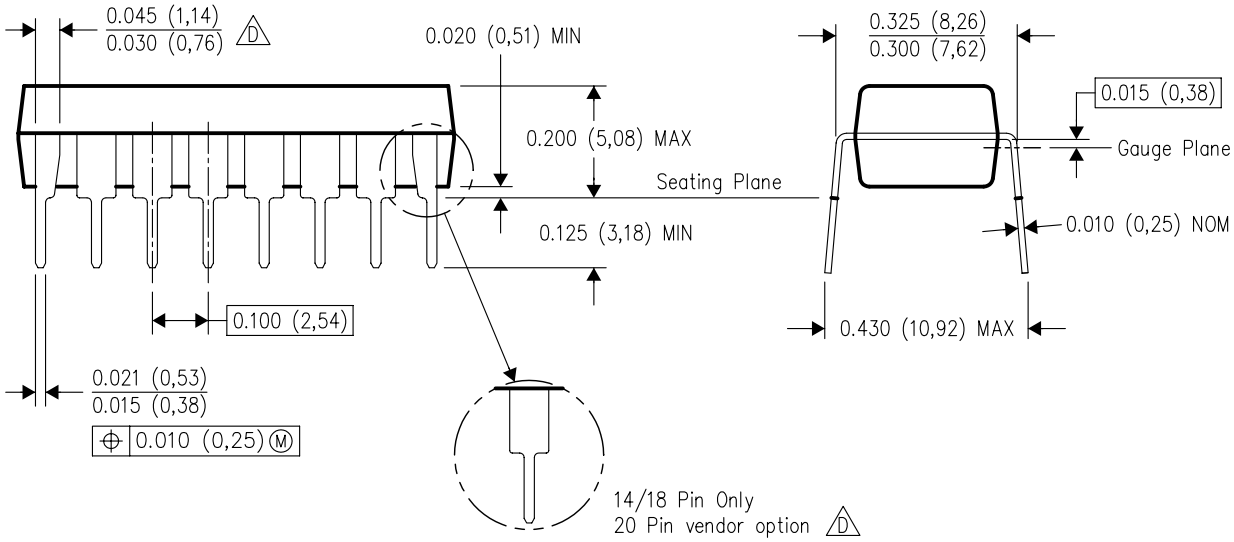
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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