LMC7215/LMC7215-Q1/LMC7225 Micro-Power, Rail-to-Rail CMOS Comparators with Push-Pull/Open-Drain Outputs

Check for Samples: LMC7215, LMC7225

FEATURES

(Typical Unless Otherwise Noted)

- **Ultra Low Power Consumption 0.7 µA**
- **Wide Range of Supply Voltages 2V to 8V**
- **Input Common-Mode Range Beyond V^+ and V^-**
- **Open Collector and Push-Pull Output**
- **High Output Current Drive: (@ V_S = 5V) 45 mA**
- **Propagation Delay (@ V_S = 5V, 10 mV Overdrive) 25 µs**
- **Tiny 5-Pin SOT-23 Package**
- **Latch-up Resistance >300 mA**
- **LMC7215-Q1 is an Automotive Grade Product that is AEC-Q100 Grade 3 Qualified.**

APPLICATIONS

- **Laptop Computers**
- **Mobile Phones**
- **Metering Systems**
- **Hand-held Electronics**
- **RC Timers**
- **Alarm and Monitoring Circuits**
- **Window Comparators, Multivibrators**
- **Automotive**

DESCRIPTION

The LMC7215/LMC7215-Q1/LMC7225 are ultra low power comparators with a maximum of 1 µA power supply current. They are designed to operate over a wide range of supply voltages, from 2V to 8V.

The LMC7215/LMC7215-Q1/LMC7225 have a greater than rail-to-rail common mode voltage range. This is a real advantage in single supply applications.

The LMC7215 features a push-pull output stage. This feature allows operation with absolute minimum amount of power consumption when driving any load.

The LMC7225 features an open drain output. By connecting an external resistor, the output of the comparator can be used as a level shifter to any desired voltage to as high as 15V.

The LMC7215/LMC7215-Q1/LMC7225 are designed for systems where low power consumption is the critical parameter.

Ensured operation over the full supply voltage range of 2.7V to 5V and rail-to-rail performance makes this comparator ideal for battery-powered applications.

Connection Diagrams

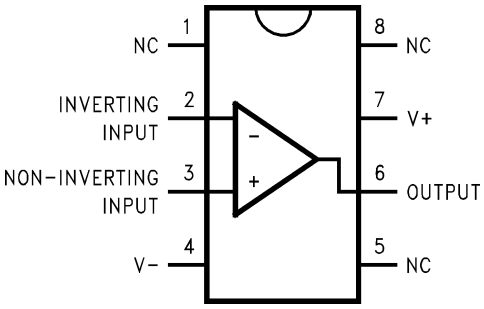


Figure 1. 8-Pin SOIC (Top View)

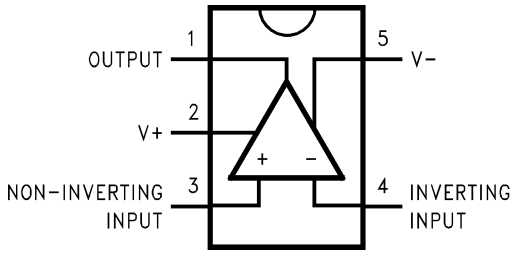


Figure 2. 5-Pin SOT-23 (Top View)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)		2 kV
Differential Input Voltage		V^+ +0.3V, V^- −0.3V
Voltage at Input/Output Pin		V^+ +0.3V, V^- −0.3V
Supply Voltage (V^+–V^-)		10V
Current at Input Pin		±5 mA
Current at Output Pin (4)		±30 mA
Current at Power Supply Pin		40 mA
Lead Temperature	(soldering, 10 sec)	260°C
Storage Temperature Range		−65°C to +150°C
Junction Temperature (5)		150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is$P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings (1)

Supply Voltage		$2V \le V_{CC} \le 8V$
Temperature Range (2)		−40°C to +85°C
Package Thermal Resistance (θ_{JA})	8-Pin SOIC	165°C/W
	5-Pin SOT-23	325°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is$P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

2.7V to 5V Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V to 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7215 Limit (2)	LMC7225 Limit (2)	Units
V_{OS}	Input Offset Voltage		1	6 **8**	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2			µV/°C
I_B	Input Current		5			fA
I_{OS}	Input Offset Current		1			fA
CMRR	Common Mode Rejection Ratio	See (3)	80	60	60	dB min

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(2) All limits are specified by testing or statistical analysis.
(3) CMRR measured at V_{CM} = 0V to 2.5V and 2.5V to 5V when V_S = 5V, V_{CM} = 0.2V to 1.35V and 1.35V to 2.7V when V_S = 2.7V. This eliminates units that have large V_{OS} at the V_{CM} extremes and low or opposite V_{OS} at $V_{CM} = V_S/2$.

2.7V to 5V Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V to 5V, V^- = 0V, V_{CM} = V_O = V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7215 Limit (2)	LMC7225 Limit (2)	Units
PSRR	Power Supply Rejection Ratio	V^+ = 2.2V to 8V	90	60	60	dB min
A_V	Voltage Gain		140			dB
CMVR	Input Common-Mode Voltage Range	V^+ = 2.7V	3.0	2.9	2.9	V
		CMRR > 50 dB		**2.7**	**2.7**	min
		V^+ = 2.7V	−0.2	0.0	0.0	V
		CMRR > 50 dB		**0.2**	**0.2**	max
		V^+ = 5.0V	5.3	5.2	5.2	V
		CMRR > 50 dB		**5.0**	**5.0**	min
		V^+ = 5.0V	−0.3	−0.2	−0.2	V
		CMRR > 50 dB		**0.0**	**0.0**	max
V_{OH}	Output Voltage High	V^+ = 2.2V	2.05	1.8	NA	V
		I_{OH} = 1.5 mA		**1.7**		min
		V^+ = 2.7V	2.05	2.3	NA	V
		I_{OH} = 2.0 mA		**2.2**		min
		V^+ = 5.0V	4.8	4.6	NA	V
		I_{OH} = 4.0 mA		**4.5**		min
V_{OL}	Output Voltage Low	V^+ = 2.2V	0.17	0.4	0.4	V
		I_{OH} = 1.5 mA		**0.5**	**0.5**	max
		V^+ = 2.7V	0.17	0.4	0.4	V
		I_{OH} = 2.0 mA		**0.5**	**0.5**	max
		V^+ = 5.0V	0.2	0.4	0.4	V
		I_{OH} = 4.0 mA		**0.5**	**0.5**	max
I_{SC+}	Output Short Circuit Current (4)	V^+ = 2.7V, Sourcing	15		NA	mA
		V^+ = 5.0V, Sourcing	50		NA	mA
I_{SC-}	Output Short Circuit Current (4)	V^+ = 2.7V, Sinking	12			mA
		V^+ = 5.0V, Sinking	30			mA
$I_{Leakage}$	Output Leakage Current	V^+ = 2.2V				nA
		V_{IN}+ = 0.1V, V_{IN}− = 0V,	0.01	NA	500	max
		V_{OUT} = 15V				
I_S	Supply Current	V^+ = 5.0V	0.7	1	1	µA
		V_{IN}+ = 5V, V_{IN}− = 0V		**1.2**	**1.2**	max

(4) Do not short the output of the LMC7225 to voltages greater than 10V or damage may occur.

AC Electrical Characteristics

Unless otherwise specified, T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2

Symbol	Parameter	Conditions	LMC7215 Typ (1)	LMC7225 Typ (1) (2)	Units
t_{rise}	Rise Time	Overdrive = 10 mV (2)	1	12.2	µs
t_{fall}	Fall Time	Overdrive = 10 mV (2)	0.4	0.35	µs

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

(2) All measurements made at 10 kHz. A 100 kΩ pull-up resistor was used when measuring the LMC7225. C_{LOAD} = 50 pF including the test jig and scope probe. The rise times of the LMC7225 are a function of the R-C time constant.

AC Electrical Characteristics (continued)

Unless otherwise specified, T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2

Symbol	Parameter	Conditions		LMC7215 Typ(1)	LMC7225 Typ(1) (2)	Units
t_{PHL}	Propagation Delay (High to Low)	See(2) (3)	Overdrive = 10 mV	24	24	µs
			Overdrive = 100 mV	12	12	
		V^+ = 2.7V(2) (3)	Overdrive = 10 mV	17	17	µs
			Overdrive = 100 mV	11	11	
t_{PLH}	Propagation Delay (Low to High)	See(2) (3)	Overdrive = 10 mV	24	29	µs
			Overdrive = 100 mV	12	17	
		V^+ = 2.7V(2) (3)	Overdrive = 10 mV	17	22	µs
			Overdrive = 100 mV	11	16	

(3) Input step voltage for the propagation measurements is 100 mV.

Typical Performance Characteristics

T_A= 25°C unless otherwise specified

Supply Current vs. Supply Voltage

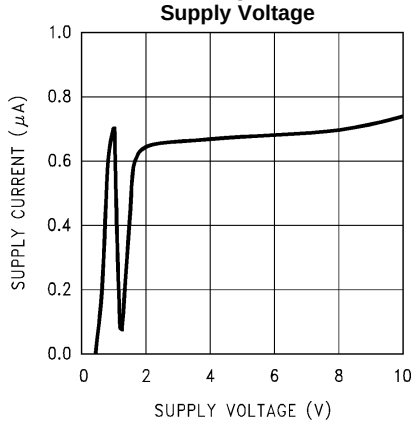


Figure 3.

Prop Delay vs. V_{SUPPLY}

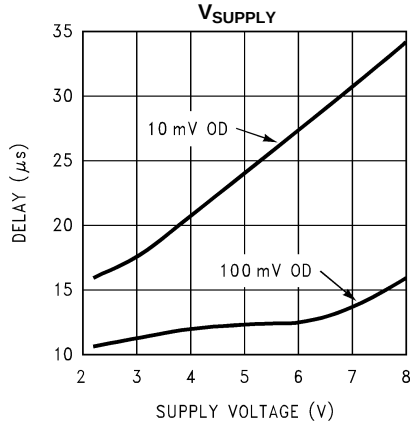


Figure 4.

Prop Delay vs. Overdrive

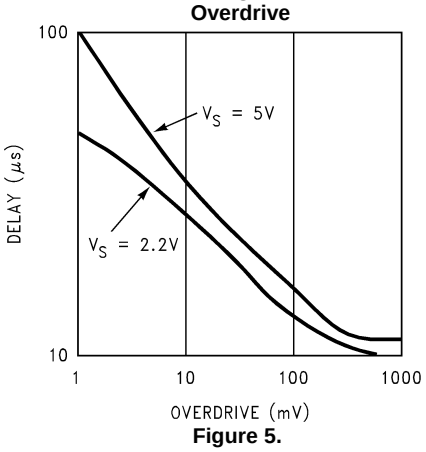


Figure 5.

Short Circuit Current vs. V_{SUPPLY}

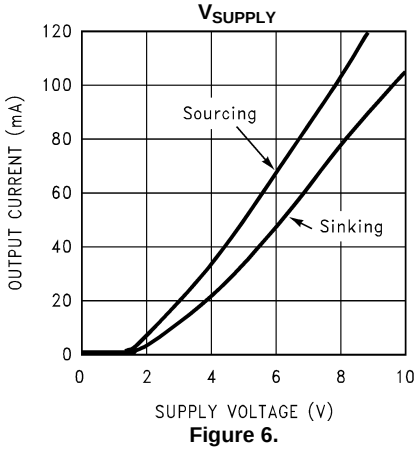


Figure 6.

Output Voltage vs. Output Current LMC7215

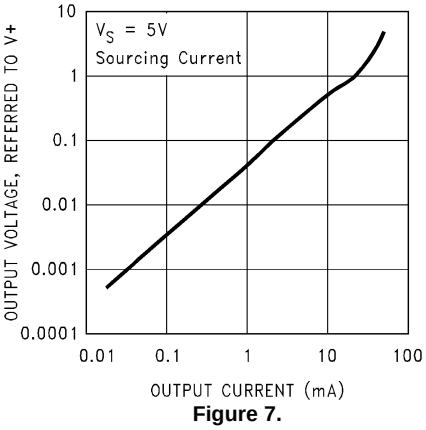


Figure 7.

Output Voltage vs. Output Current

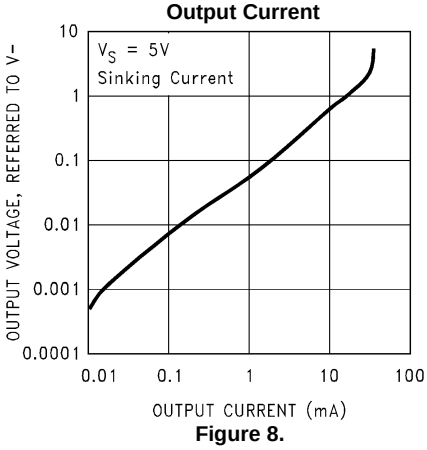


Figure 8.

Typical Performance Characteristics (continued)

T_A= 25°C unless otherwise specified

Output Voltage vs. Output Current LMC7215

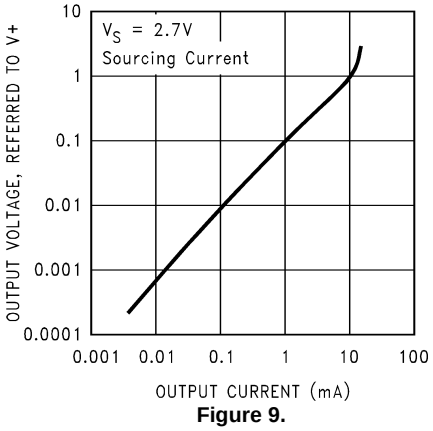


Figure 9.

Output Voltage vs. Output Current

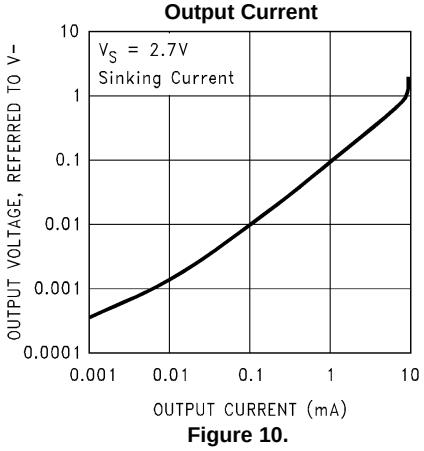


Figure 10.

Output Leakage Current vs. Output Voltage LMC7225

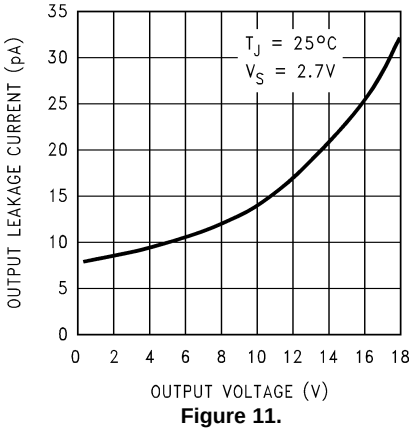


Figure 11.

Output Leakage Current vs. Output Voltage LMC7225

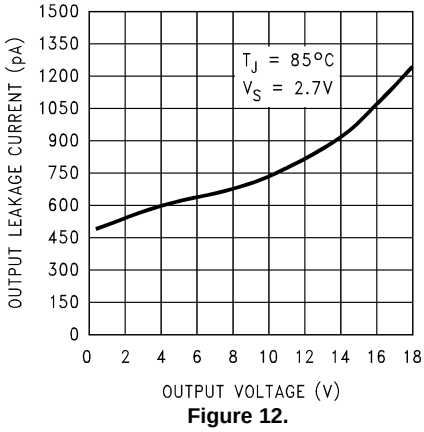


Figure 12.

APPLICATION INFORMATION

RESPONSE TIME

Depending upon the amount of overdrive, the delay will typically be between 10 µs to 200 µs. The curve showing delay vs. overdrive in the " Typical Characteristics" section shows the delay time when the input is preset with 100 mV across the inputs and then is driven the other way by 1 mV to 500 mV.

The transition from high to low or low to high is fast. Typically 1 µs rise and 400 ns fall.

With a small signal input, the comparators will provide a square wave output from sine wave inputs at frequencies as high as 25 kHz. Figure 13 shows a worst case example where a ±5 mV sine wave is applied to the input. Note that the output is delayed by almost 180°.

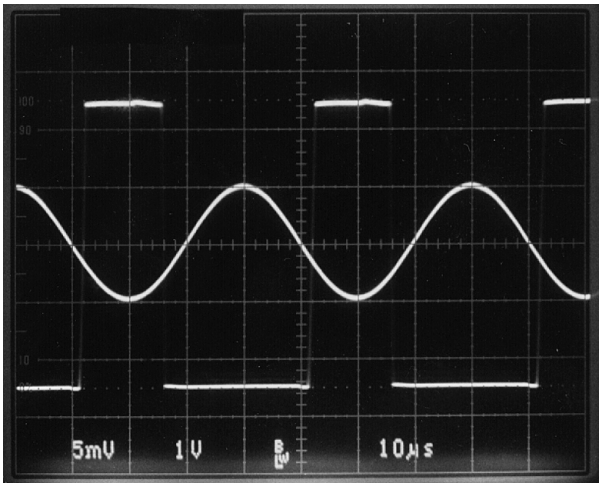


Figure 13.

NOISE

Most comparators have rather low gain. This allows the output to spend time between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero.

The exceptionally high gain of these comparators, 10,000 V/mV, eliminates this problem. Less then 1 µV of change on the input will drive the output from one rail to the other rail.

If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback.

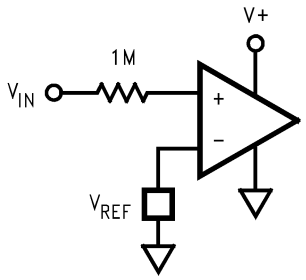


Figure 14.

INPUT VOLTAGE RANGE

The LMC7215/25 have input voltage ranges that are larger than the supply voltage ensures that signals from other parts of the system cannot overdrive the inputs. This allows sensing supply current by connecting one input directly to the V^+ line and the other to the other side of a current sense resistor. The same is true if the sense resistor is in the ground return line.

Sensing supply voltage is also easy by connecting one input directly to the supply.

The inputs of these comparators are protected by diodes to both supplies. This protects the inputs from both ESD as well as signals that greatly exceed the supply voltages. As a result, current will flow through these forward biased diodes whenever the input voltage is more than a few hundred millivolts larger than the supplies. Until this occurs, there is essentially no input current. As a result, placing a large resistor in series with any input that may be exposed to large voltages, will limit the input current but have no other noticeable effect.

If the input current is limited to less than 5 mA by a series resistor, (see Figure 14), a threshold or zero crossing detector, that works with inputs from as low as a few millivolts to as high as 5,000V, is made with only one resistor and the comparator.

INPUTS

As mentioned above, these comparators have near zero input current. This allows very high resistance circuits to be used without any concern for matching input resistances. This also allows the use of very small capacitors in R-C type timing circuits. This reduces the cost of the capacitors and amount of board space used.

CAPACITIVE LOADS

The high output current drive allows large capacitive loads with little effect. Capacitive loads as large as 10,000 pF have no effect upon delay and only slow the transition by about 3 µs.

OUTPUT CURRENT

Even though these comparators use less than 1 µA supply current, the outputs are able to drive very large currents.

The LMC7215 can source up to 50 mA when operated on a 5V supply. Both the LMC7215 and LMC7225 can sink over 20 mA. (See the graph of Max I_O vs. V_{SUPPLY} in the " Typical Characteristics" section.)

This large current handling ability allows driving heavy loads directly. LEDs, beepers and other loads can be driven easily.

The push-pull output stage of the LMC7215 is a very important feature. This keeps the total system power consumption to the absolute minimum. The only current consumed is the less than 1 µA supply current and the current going directly into the load. No power is wasted in a pull-up resistor when the output is low. The LMC7225 is only recommended where a level shifting function from one logic level to another is desired, where the LMC7225 is being used as a drop-in lower power replacement for an older comparator or in circuits where more than one output will be paralleled.

POWER DISSIPATION

The large output current ability makes it possible to exceed the maximum operating junction temperature of 85°C and possibly even the absolute maximum junction temperature of 150°C.

The thermal resistance of the 8-pin SOIC package is 165°C/W. Shorting the output to ground with a 2.7V supply will only result in about 5°C rise above ambient.

The thermal resistance of the much smaller 5-Pin SOT-23 package is 325°C/W. With a 2.7V supply, the raise is only 10.5°C but if the supply is 5V and the short circuit current is 50 mA, this will cause a raise of 41°C in the 8-Pin SOIC and 81°C in the 5-Pin SOT-23. This should be kept in mind if driving very low resistance loads.

SHOOT-THROUGH

Shoot-through is a common occurrence on digital circuits and comparators where there is a push-pull output stage. This occurs when a signal is applied at the same time to both the N-channel and P-channel output transistors to turn one off and turn the other on. (See Figure 15.) If one of the output devices responds slightly faster than the other, the fast one can be turned on before the other has turned off. For a very short time, this allows supply current to flow directly through both output transistors. The result is a short spike of current drawn from the supply.

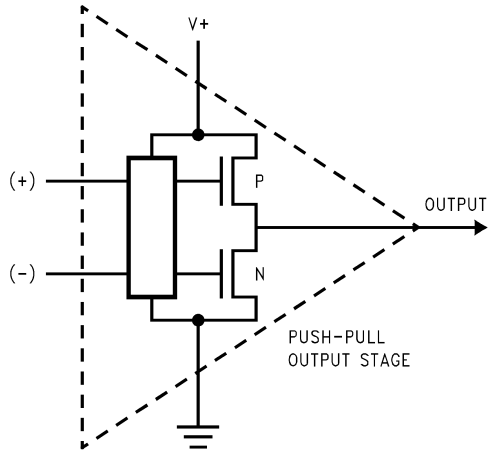


Figure 15.

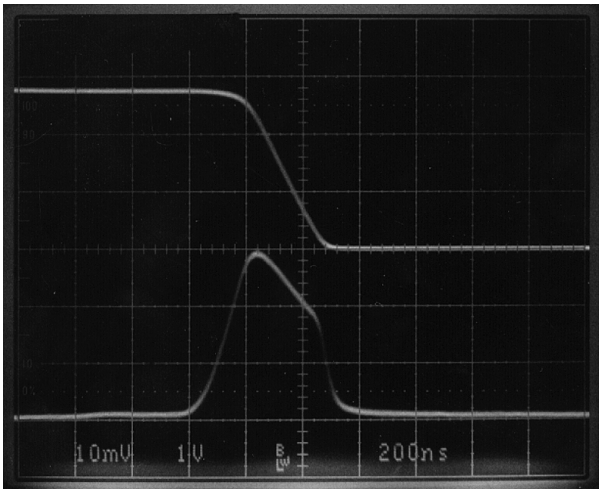


Figure 16. R_S = 100Ω

The LMC7215 produces a small current spike of 300 µA peak for about 400 ns with 2.7V supply and 1.8 mA peak for 400 ns with a 5V supply. This spike only occurs when the output is going from high to low. It does not occur when going from low to high. Figure 16 and Figure 17 show what this current pulse looks like on 2.7V and 5V supplies. The upper trace is the output voltage and the lower trace is the supply current as measured with the circuit in Figure 18.

If the power supply has a very high impedance, a bypass capacitor of 0.01 µF should be more than enough to minimize the effects of this small current pulse.

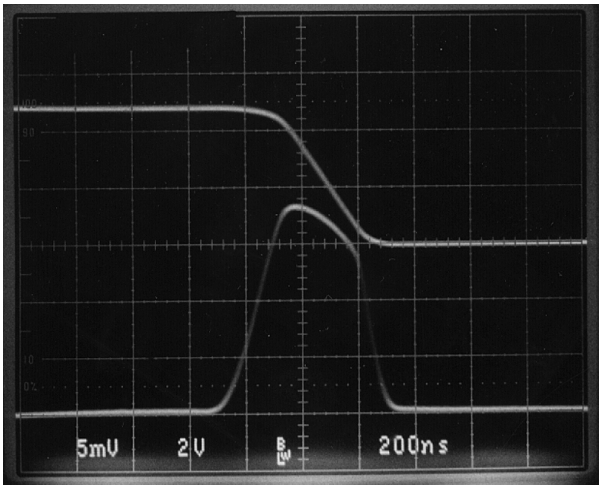


Figure 17. R_S = 10Ω

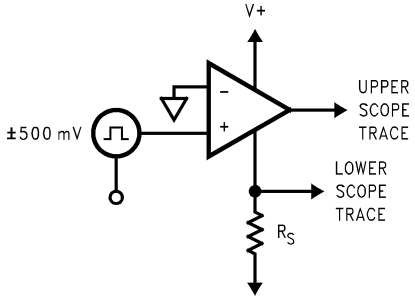


Figure 18.

LATCH-UP

In the past, most CMOS IC's were susceptible to a damaging phenomena known as latch-up. This occurred when an ESD current spike or other large signal was applied to any of the pins of an IC. The LMC7215 and LMC7225 both are designed to make them highly resistant to this type of damage. They have passed qualification tests with input currents on any lead up to 300 mA at temperatures up to 125°C.

SPICE MODELS

For a SPICE model of the LMC7215, LMC7225 and many other op amps and comparators, visit www.ti.com.

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC7215IM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC72 15IM	Samples
LMC7215IM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C02B	Samples
LMC7215IM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C02B	Samples
LMC7215IMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC72 15IM	Samples
LMC7215QIM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C02Q	Samples
LMC7215QIM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C02Q	Samples
LMC7225IM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C03B	Samples
LMC7225IM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C03B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LMC7215, LMC7215-Q1 :

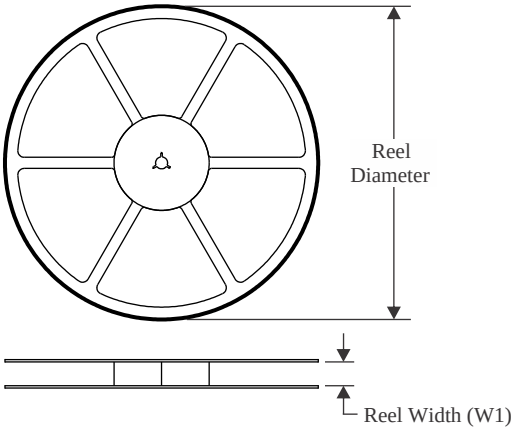
- Catalog : LMC7215
- Automotive : LMC7215-Q1

NOTE: Qualified Version Definitions:

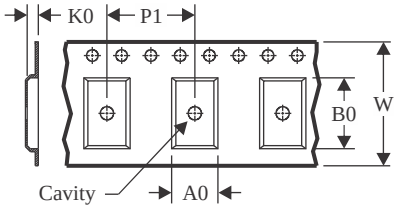
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

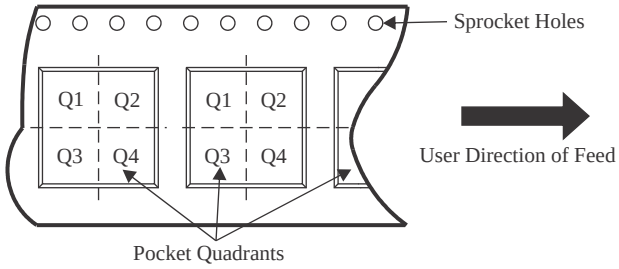


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

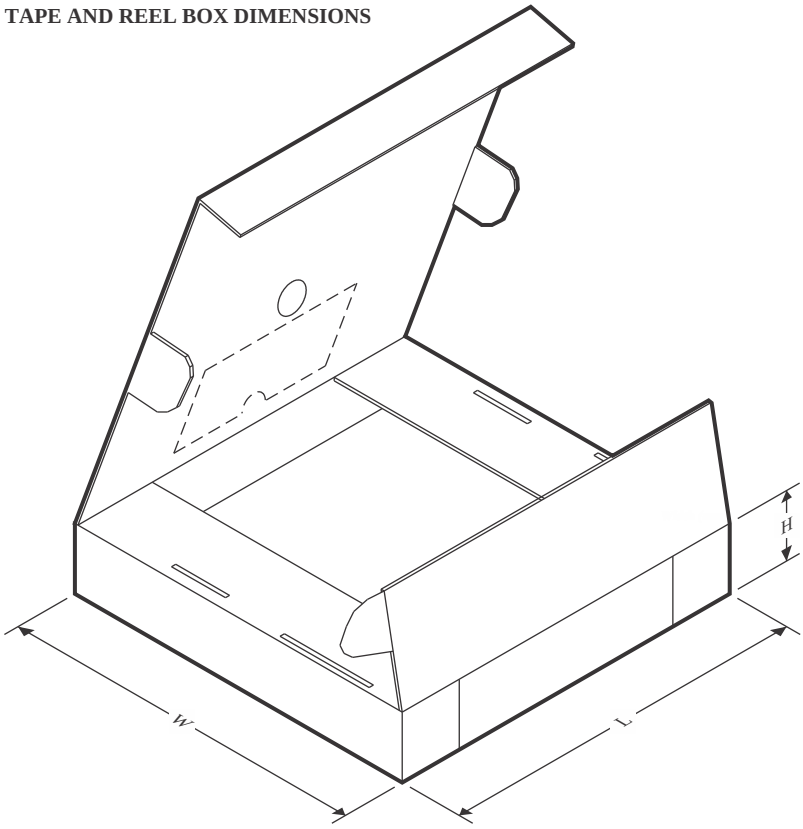
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC7215IM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7215IM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7215IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC7215QIM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7215QIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7225IM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7225IM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

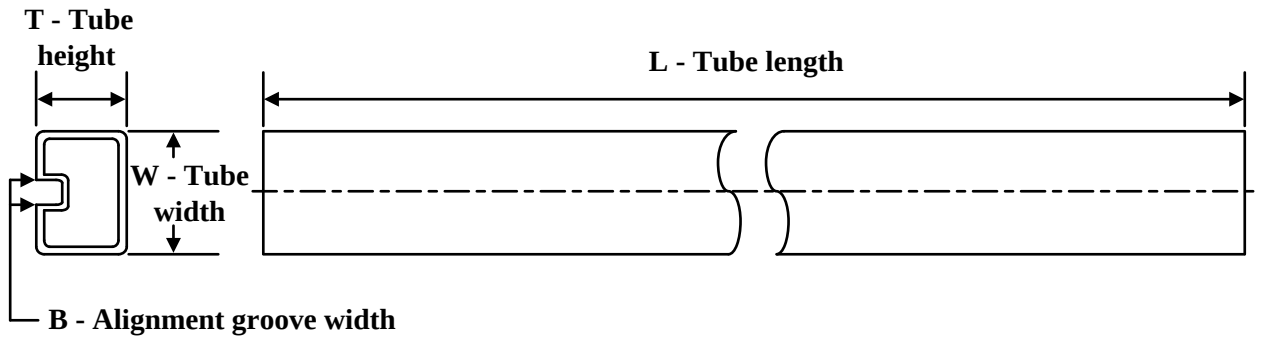
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC7215IM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMC7215IM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMC7215IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC7215QIM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMC7215QIM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMC7225IM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMC7225IM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

TUBE



*All dimensions are nominal

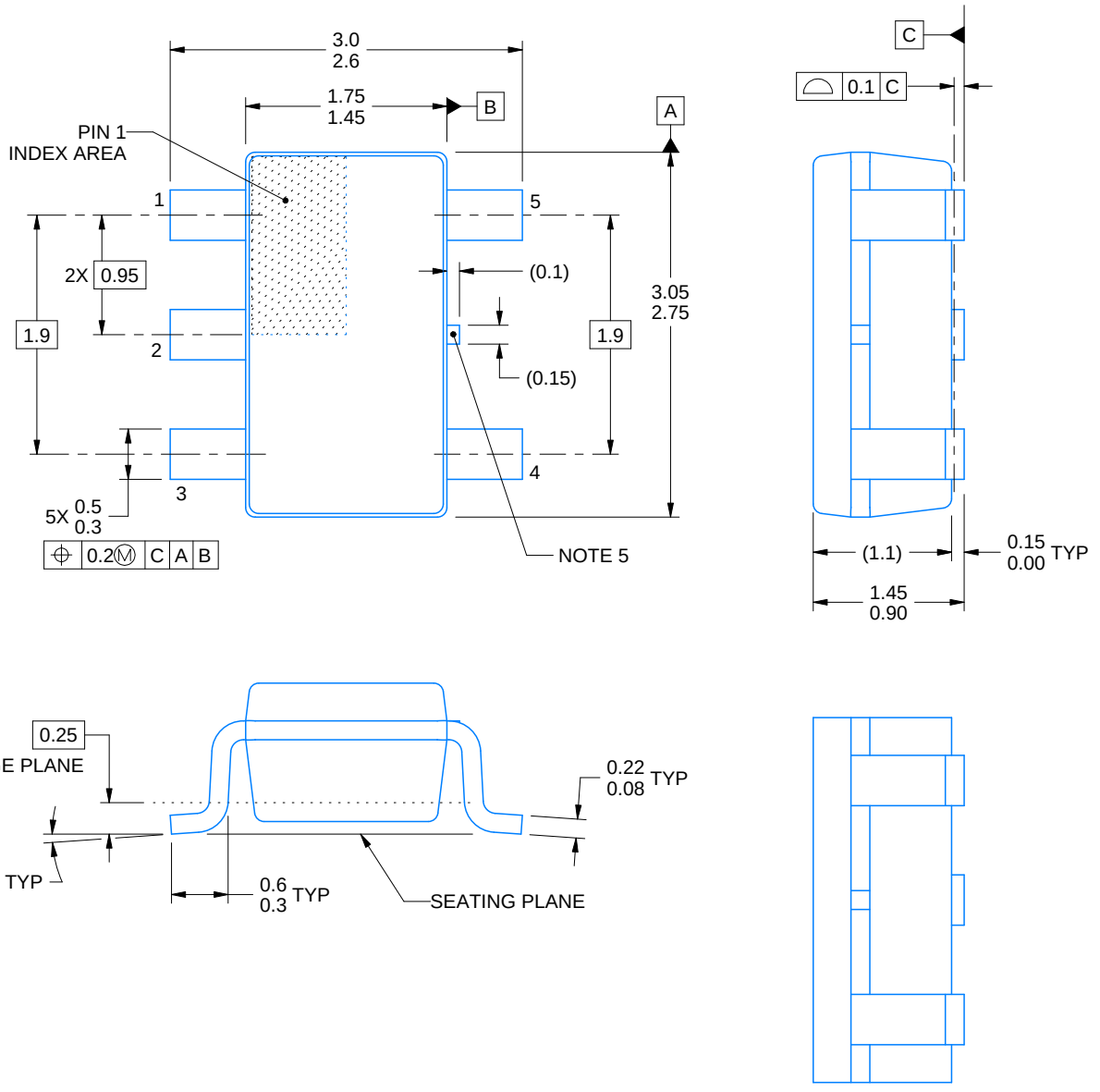
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC7215IM/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

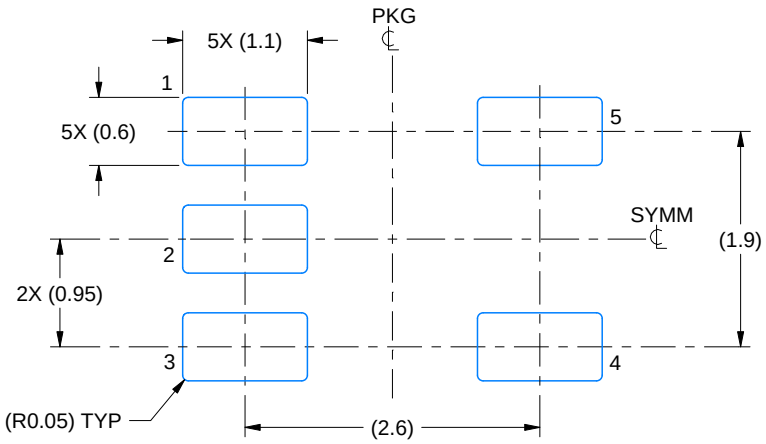


ALTERNATIVE PACKAGE SINGULATION VIEW

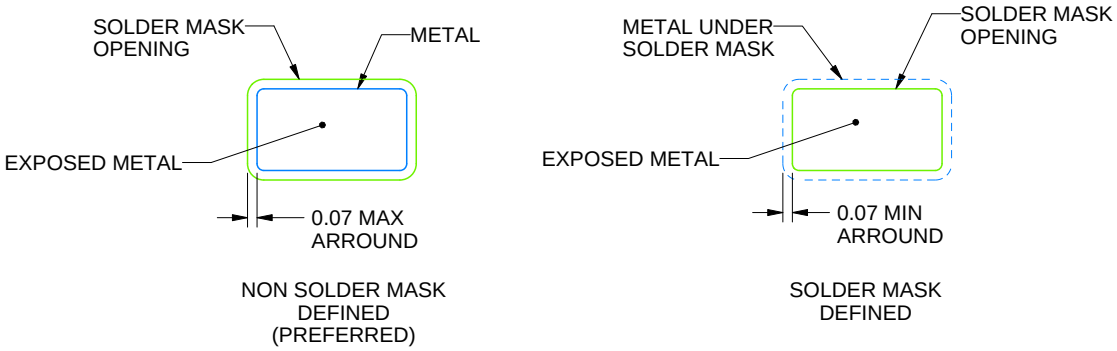
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

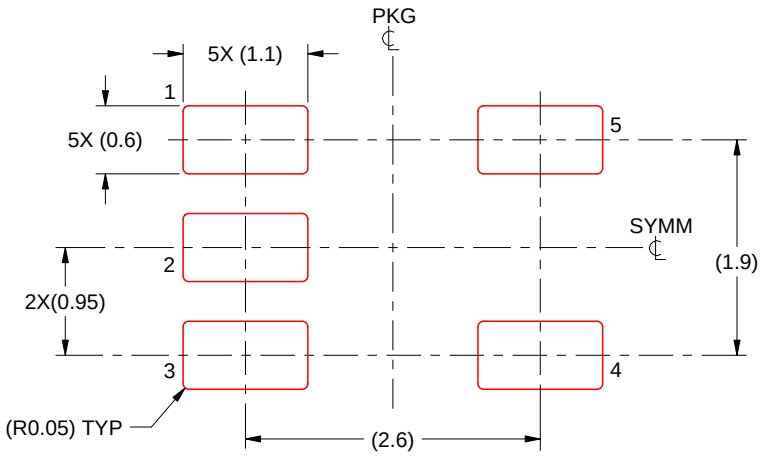


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

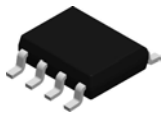


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

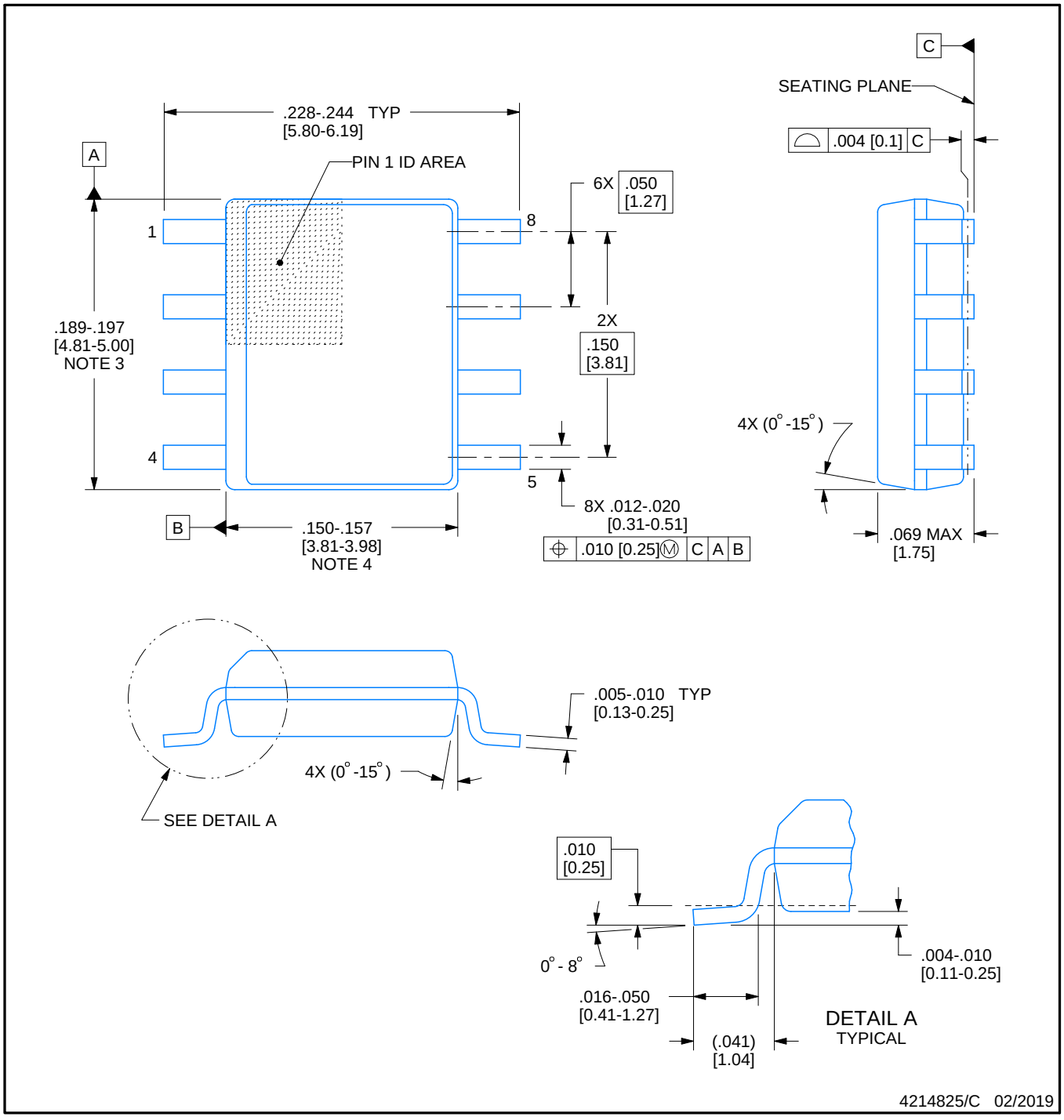


PACKAGE OUTLINE

D0008A

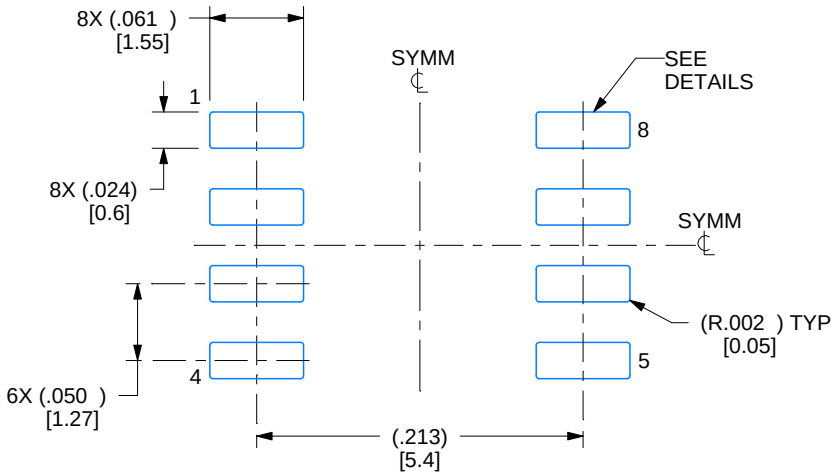
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

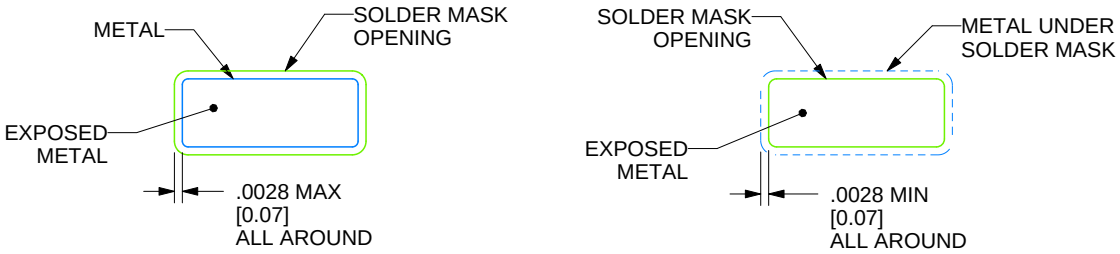


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

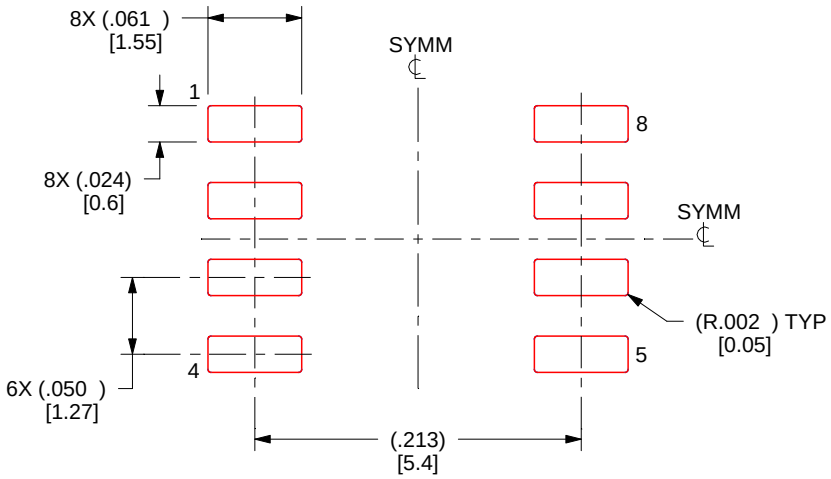
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265