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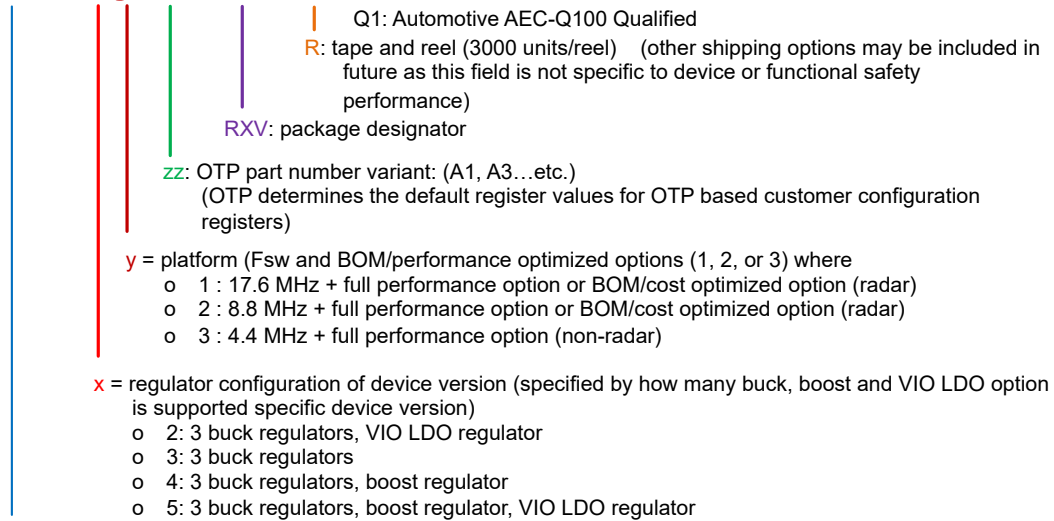
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4 Description (continued)

The LP8774x-Q1 device supports programmable start-up and shutdown delays and sequences which are synchronized to the ENABLE signal. The sequences can also include GPO signals to control external regulators, load switches, and processor reset. The default settings for the device are programmed into nonvolatile memory (NVM). The device controls the output slew rate to minimize output voltage overshoot and in-rush current during device start-up.

This data sheet applies to the superset device, including all register settings, as was validated and covers the following generic part number LP8774x-Q1 with orderable part numbers **LP8774xyzzRXVR Q1** where:

LP8774xyzzRXVRQ1



LP8774: device family and base part number

Figure 4-1. LP8774x-Q1 Orderable Part Numbers Scheme

5 Pin Configuration and Functions

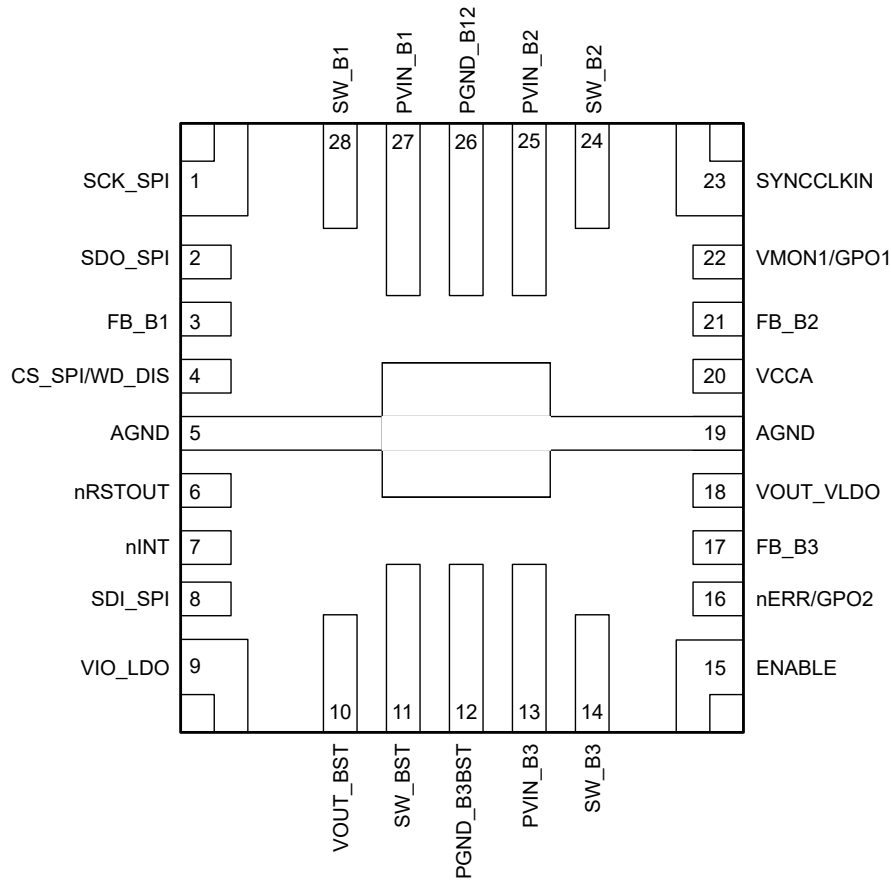


Figure 5-1. RXV Package, 28-Pin VQFN-HR (Top View)

Table 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.				
SCK_SPI	1	I	Digital	Clock signal for SPI interface.	Ground
SDO_SPI	2	O	Digital	Output data signal for SPI interface.	Floating
FB_B1	3	—	Analog	Output voltage feedback (positive) for BUCK1.	Ground
CS_SPI/ WD_DIS	4	I	Digital	Primary function: Chip select signal for SPI interface.	VCCA
		I	Digital	Alternative programmable function: Watchdog Deactivation Input.	Not applicable
AGND	5	—	Ground	Ground.	Ground
NRSTOUT	6	O	Digital	Reset output.	Floating
nINT	7	O	Digital	Interrupt output and CAN PHY control or both.	Floating
SDI_SPI	8	I	Digital	Input data signal for SPI interface.	Ground
VIO_LDO	9	—	Analog	IO supply from the internal LDO or from external source. LDO active: regulator filter node. LDO inactive: input for connecting to an external IO supply source, with input filtering capacitor placed.	Not applicable
VOUT_BST	10	—	Analog	BOOST active: BOOST output (internally connected as VIO_LDO input). BOOST inactive and VIO_LDO inactive: short with VIO_LDO. BOOST inactive and VIO_LDO active: input for connecting to an external supply used as VIO_LDO input.	External supply
SW_BST	11	—	Analog	When BOOST active: BOOST input. When BOOST inactive: short with VOUT_BST.	VOUT_BST

Table 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.				
PGND_B3BST	12	—	Ground	Power ground for BUCK3 and BOOST.	Ground
PVIN_B3	13	—	Power	Power input for BUCK3. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
SW_B3	14	—	Analog	BUCK3 switch node.	Floating
ENABLE	15	I	Digital	Programmable ENABLE signal.	Not applicable
nERR/GPO2	16	I	Digital	Primary function: System MCU Error Monitoring Input.	Ground
		O	Digital	Alternative programmable function: General Purpose Output signal (GPO2).	Floating
		O	Digital	Alternative programmable function: Fault Communication Output signal (FAULT2).	Floating
FB_B3	17	—	Analog	Output voltage feedback (positive) for BUCK3.	Ground
VOUT_VLDO	18	—	Power	LDO regulator filter node. LDO is used for internal purposes. No external load allowed.	-
AGND	19	—	Ground	Ground.	Ground
VCCA	20	—	Power	Supply voltage for internal LDO. VCCA and PVIN_Bxx pins must be connected together in the application and be locally bypassed.	System supply
FB_B2	21	—	Analog	Output voltage feedback (positive) for BUCK2.	Ground
VMON1/ GPO1	22	—	Analog	Voltage monitoring input.	Ground
		O	Digital	Alternative programmable function: General Purpose Output signal (GPO1).	Floating
		O	Digital	Alternative programmable function: Fault Communication Output signal (FAULT1).	Floating
		O	Digital	Alternative programmable function: CAN PHY control (CAN_DIS).	Floating
SYNCCLKIN	23	I	Digital	External clock input.	Ground
SW_B2	24	—	Analog	BUCK2 switch node.	Floating
PVIN_B2	25	—	Power	Power input for BUCK2. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
PGND_B12	26	—	Ground	Power ground for BUCK1 and BUCK2.	Ground
PVIN_B1	27	—	Power	Power input for BUCK1. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
SW_B1	28	—	Analog	BUCK1 switch node.	Floating

6 Device and Documentation Support

6.1 Documentation Support

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

6.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2022) to Revision B (June 2024)	Page
• Changed the Device Information table to the Packaging Information table.....	1
• Added Figure 4-1	3

Changes from Revision * (October 2021) to Revision A (November 2022)	Page
• Changed the document status from <i>Advance Information</i> to <i>Production Data</i>	1

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP87745101RXVRQ1	ACTIVE	VQFN-HR	RXV	28	3000	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	LP8774 5101-Q1	Samples
LP877451A1RXVRQ1	ACTIVE	VQFN-HR	RXV	28	3000	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	LP8774 51A1-Q1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LP87745-Q1 :

- Catalog : [LP87745](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP87745101RXVRQ1	VQFN-HR	RXV	28	3000	330.0	12.4	4.8	5.3	1.15	8.0	12.0	Q1
LP877451A1RXVRQ1	VQFN-HR	RXV	28	3000	330.0	12.4	4.8	5.3	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP87745101RXVRQ1	VQFN-HR	RXV	28	3000	367.0	367.0	35.0
LP877451A1RXVRQ1	VQFN-HR	RXV	28	3000	367.0	367.0	35.0

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