OPA1671 13-MHz, Low-Noise, Rail-to-Rail, Audio Operational Amplifier

Texas Instruments
Burr-Brown Audio

1 Features

- Low noise:
  4 nV/√Hz at 10 kHz
  4.7 fA/√Hz at 1 kHz
- Low distortion: –109 dB (0.00035%)
- Wide gain bandwidth: 13 MHz
- Rail-to-rail input and output
- Low supply-voltage operation: 1.7 V to 5.5 V
- Low input capacitance
  - Differential: 6 pF
  - Common-mode: 2.5 pF
- Low input-bias current: 10 pA
- Low power supply current: 940 µA
- Industry-standard packages: SC-70 and SOT-23

2 Applications

- Microphone preamplifier
- Auxiliary line input and output
- Active filter circuit
- Transimpedance amplifier
- Voltage buffer

3 Description

The OPA1671 is a wide-bandwidth, low-noise, low-distortion, audio operational amplifier that provides rail-to-rail input and output operation. This device offers an excellent combination of low voltage noise, current noise, and input capacitance, allowing the device to deliver high performance in a wide array of audio and industrial applications. The unique internal topology of the OPA1671 delivers very low distortion (–109 dB), while only consuming 940 µA of power supply current. The wide bandwidth (13 MHz) and high slew rate (5 V/µs) of OPA1671 makes this device an excellent choice for high gain audio and industrial signal conditioning.

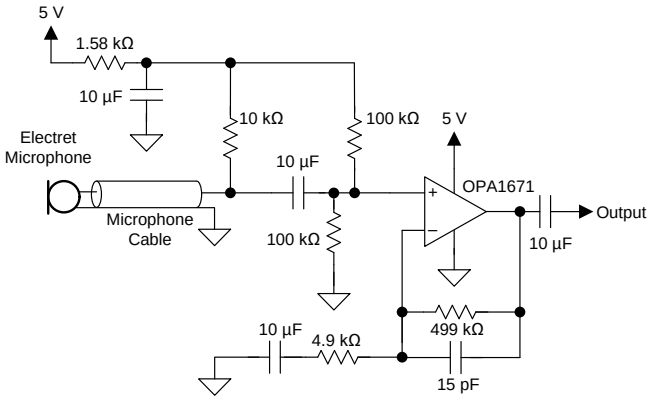
The OPA1671 is available in the SC-70 and SOT-23 packages and is specified over the industrial temperature range (–40°C to +125°C).

Device Information(1)

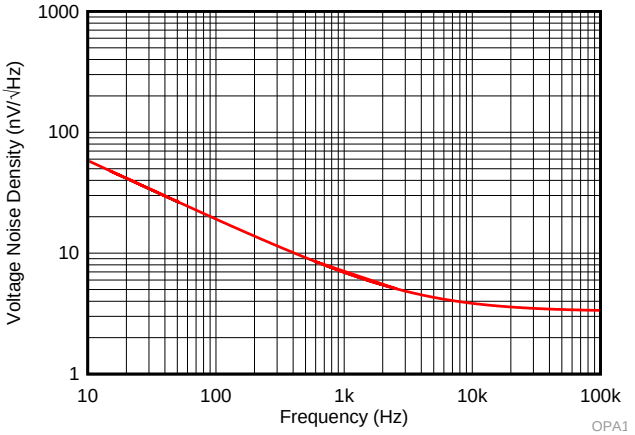
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1671	SC-70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Electret Microphone Preamplifier



OPA1671 Voltage Noise Density



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2019) to Revision B **Page**

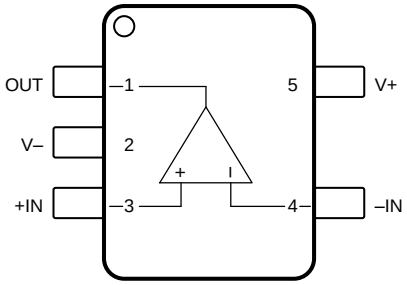
- Added SOT-23 (DBV) package and associated content to data sheet ... 1
- Added input offset voltage specification for V_{CM} = (V+), (V–) ... 5

Changes from Original (November 2018) to Revision A **Page**

- Changed from advanced information (preview) to production data (active) ... 1

5 Pin Configuration and Functions

DBV and DCK Packages
5-Pin SOT-23 and SC-70
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		6	V
Input voltage	(V–) –0.3	(V+) +0.3	V
Output short-circuit(2)	Continuous		
Operating temperature, T_A	–55	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	1.7 (±0.85)		5.5 (±2.75)	V
Specified temperature, T_A	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA1671		UNIT
		DBV (SOT-23)	DCK (SC-70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.1	214.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.4	127.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	60.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.5	33.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.1	59.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at V_S = ±0.85 V to ±2.75 V (V_S = 1.7 V to 5.5 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 1 V_{RMS}, V_S = 5.5 V			0.00035%		
					–109		dB
IMD	Intermodulation distortion	G = 1, V_O = 1 V_{RMS}, V_S = 5.5 V	SMPTE/DIN Two-Tone, 4:1, (60 Hz and 7 kHz)		0.00158%		
					–96		dB
			CCIF Two-Tone (19 kHz and 20 kHz)		0.0005%		
					–106		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				13		MHz
SR	Slew rate	4-V step, G = 1			5		V/µs
t_S	Settling time	To 0.1%, 2-V step , G = 1			0.75		µs
		To 0.01%, 2-V step , G = 1			1		
	Overload recovery time	V_{IN} × gain > V_S			0.35		µs
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			2.4		μV_{PP}
e_N	Input voltage noise density	f = 10 Hz			45		nV/√Hz
		f = 1 kHz			7		
		f = 10 kHz			4.0		
i_N	Input current noise	f = 1 kHz			4.7		fA/√Hz
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = (V+)				±1.6	mV
		V_{CM} = (V–)				±1.6	
					±0.25	±1.25	
		T_A = –40°C to 125°C			±0.25		
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			±0.3	±2.2	µV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = (V–)			±30	±130	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			V–		V+	V
CMRR	Common-mode rejection ratio	V_S = 1.7 V, (V–) < V_{CM} < (V+) – 1.25 V		74	91		dB
		V_S = 5.5 V, (V–) < V_{CM} < (V+) – 1.25 V		80	96		
		V_S = 1.7 V, V_{CM} = 0 V to 1.7 V		60	88		
		V_S = 5.5 V, V_{CM} = 0 V to 5.5 V		68	102		
INPUT CAPACITANCE							
Z_{ID}	Differential				10^{13} || 6		MΩ || pF
Z_{ICM}	Common-mode				10^{13} || 2.5		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 50 mV < V_O < (V+) – 50 mV, R_L = 10 kΩ		97	113		dB
			T_A = –40°C to 125°C		106		
		(V–) + 200 mV < V_O < (V+) – 200 mV, R_L = 2 kΩ		97	112		
			T_A = –40°C to 125°C		105		

Electrical Characteristics (continued)

at V_S = ±0.85 V to ±2.75 V (V_S = 1.7 V to 5.5 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	V_S = 5.5 V, R_L = 10 kΩ		10	20	mV
I_{SC}	Short-circuit current	Sinking, V_S = 5.5 V		–57		mA
		Sourcing, V_S = 5.5 V		66		
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		0.94	1.3	mA
		I_O = 0 mA, T_A = –40°C to 125°C			1.4	

6.6 Typical Characteristics

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

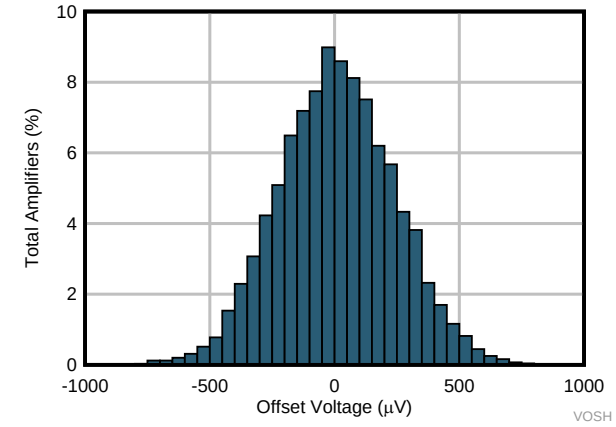


Figure 1. Offset Voltage Production Distribution

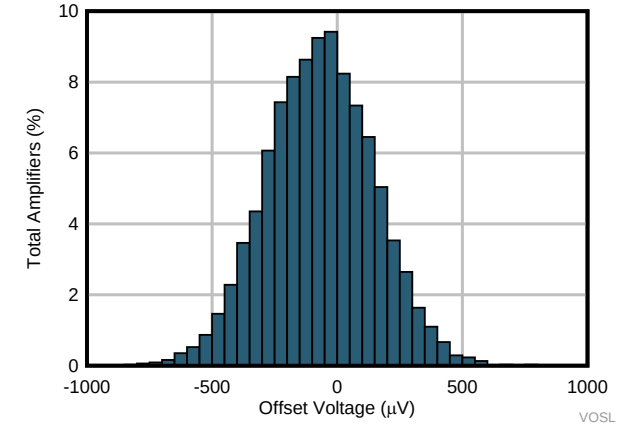


Figure 2. Offset Voltage Production Distribution

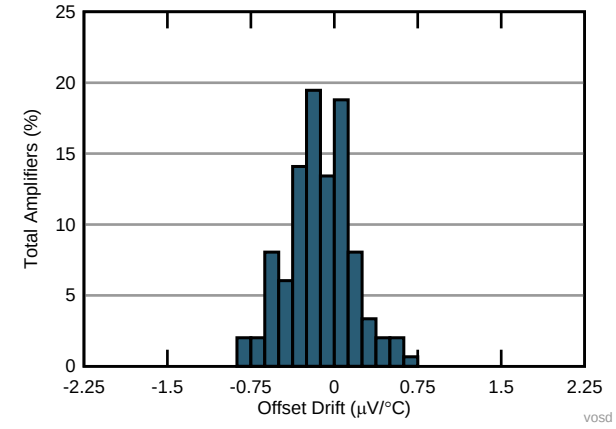


Figure 3. Offset Voltage Drift Distribution

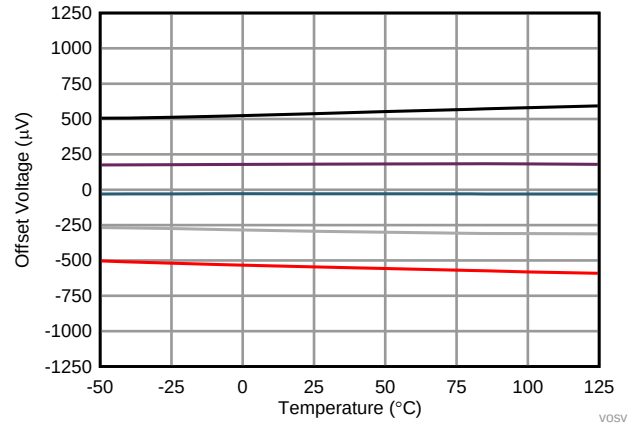


Figure 4. Offset Voltage vs Temperature

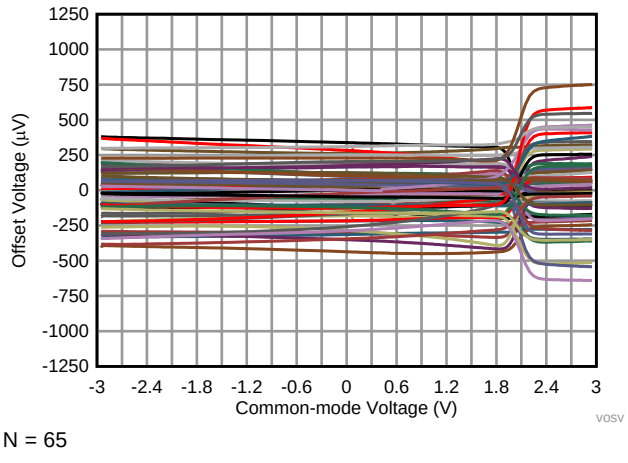


Figure 5. Offset Voltage vs Common Mode Voltage

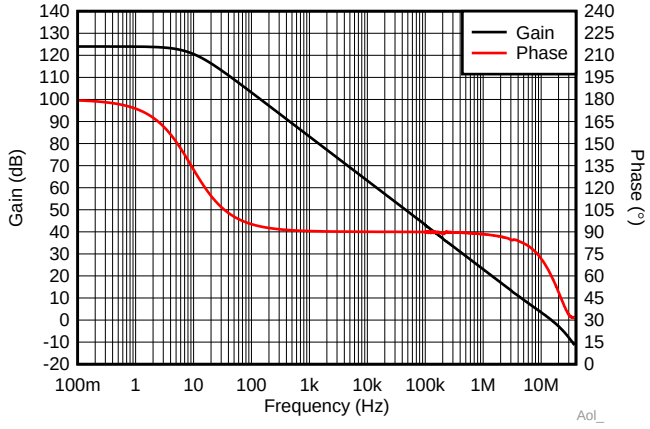


Figure 6. Open-Loop Gain and Phase vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

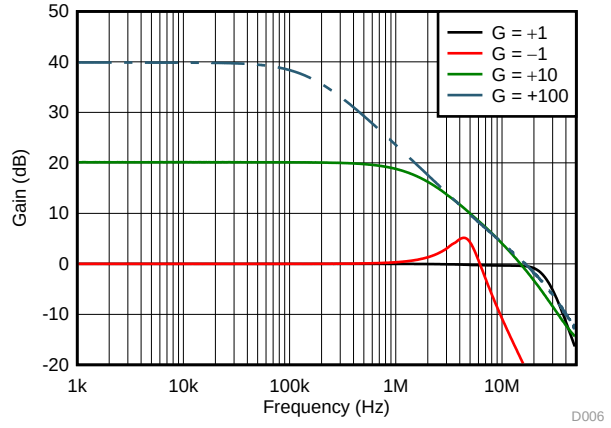


Figure 7. Closed-Loop Gain and Phase vs Frequency

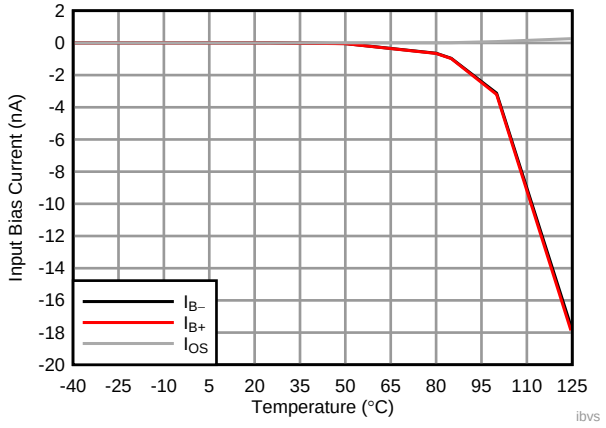


Figure 8. Input Bias Current vs Temperature

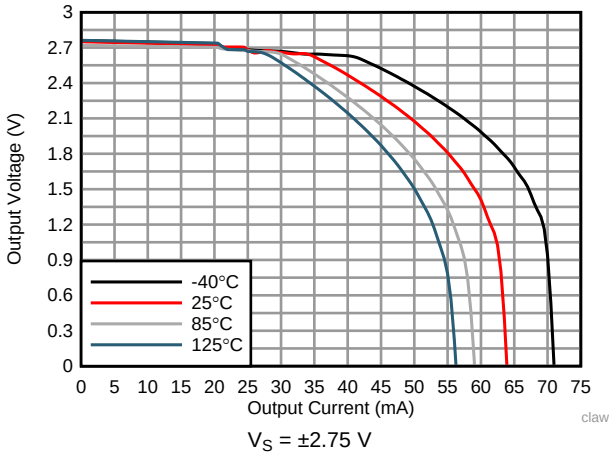


Figure 9. Output Voltage Swing vs Sourcing Output Current (Maximum Supply)

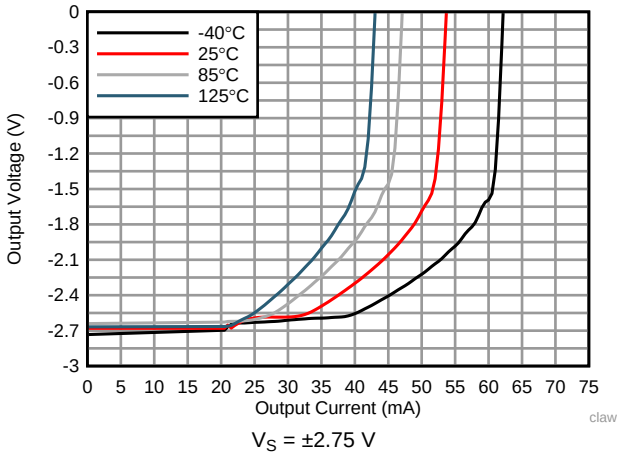


Figure 10. Output Voltage Swing vs Sinking Output Current (Maximum Supply)

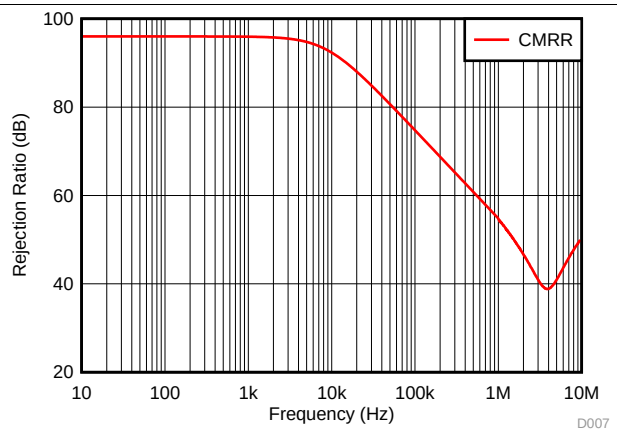


Figure 11. CMRR vs Frequency

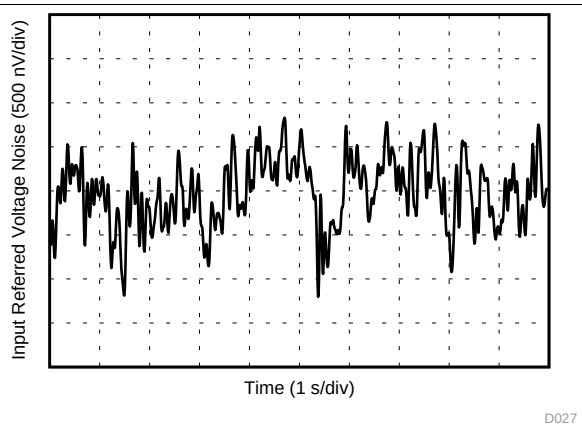


Figure 12. 0.1-Hz to 10-Hz Noise

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

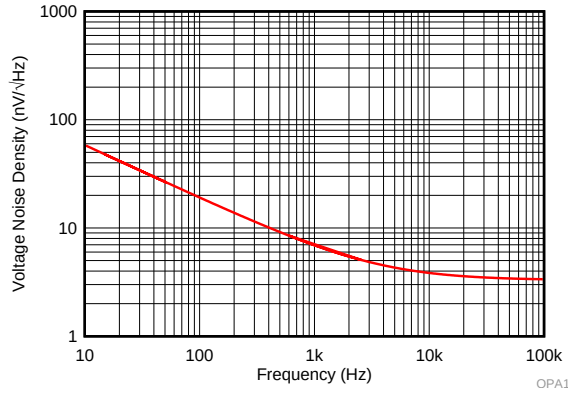
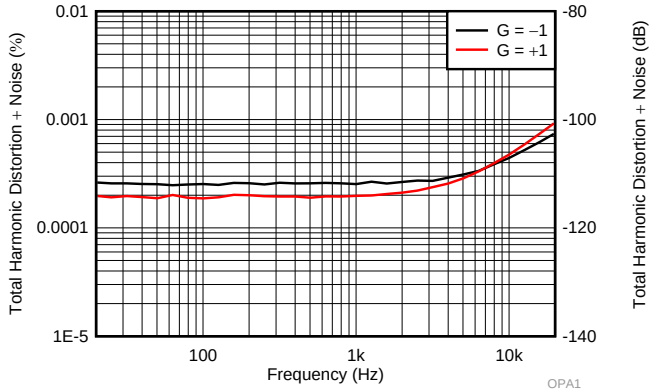


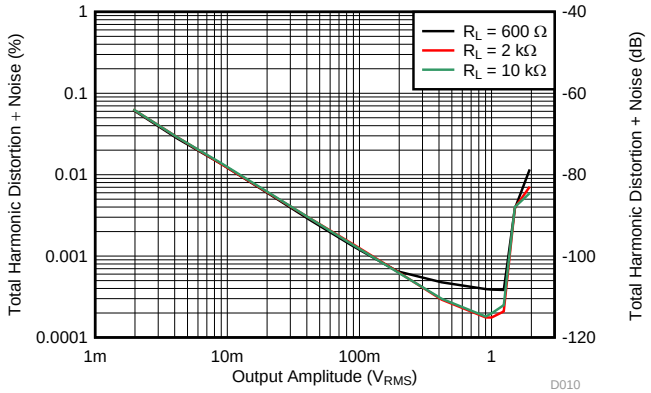
Figure 13. Input Voltage Noise Spectral Density vs Frequency



BW = 80 kHz

V_O = 1 V_{RMS}

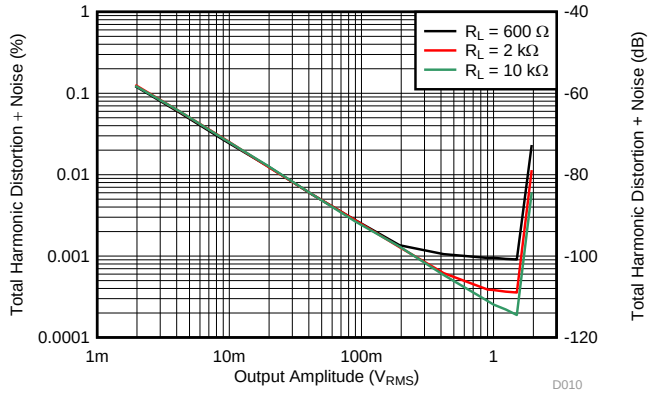
Figure 14. THD+N Ratio vs Frequency



Gain = 1 BW = 80 kHz

f_{TEST} = 1 kHz

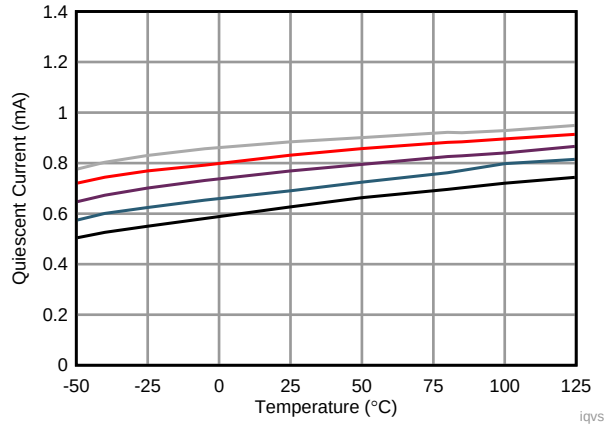
Figure 15. THD+N vs Output Amplitude



Gain = –1 BW = 80 kHz

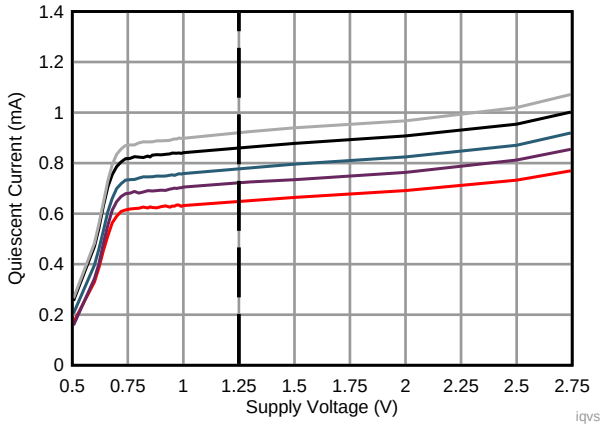
f_{TEST} = 1 kHz

Figure 16. THD+N vs Output Amplitude



5 typical units

Figure 17. Quiescent Current vs Temperature



5 typical units

Figure 18. Quiescent Current vs Supply

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

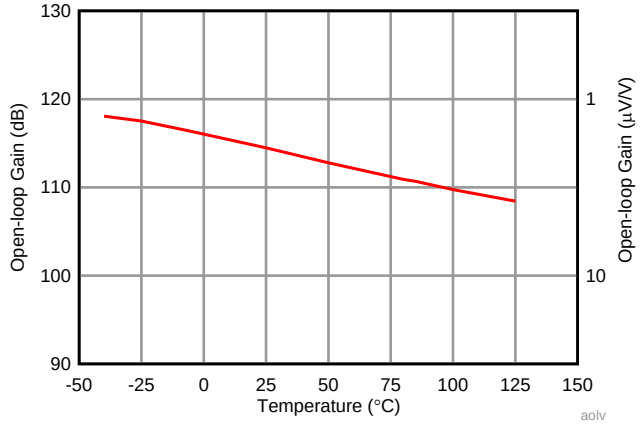


Figure 19. Open-Loop Gain vs Temperature

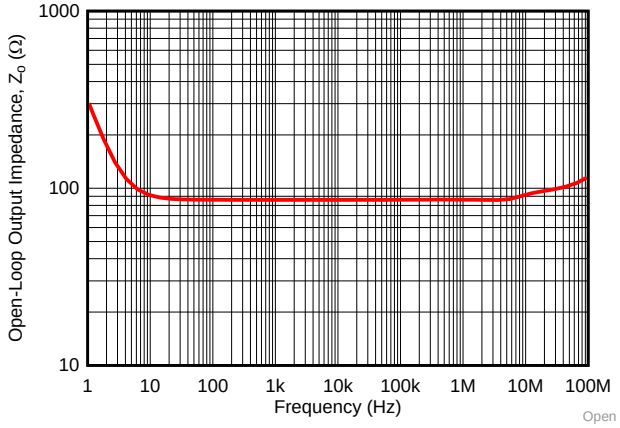


Figure 20. Open-Loop Output Impedance vs Frequency

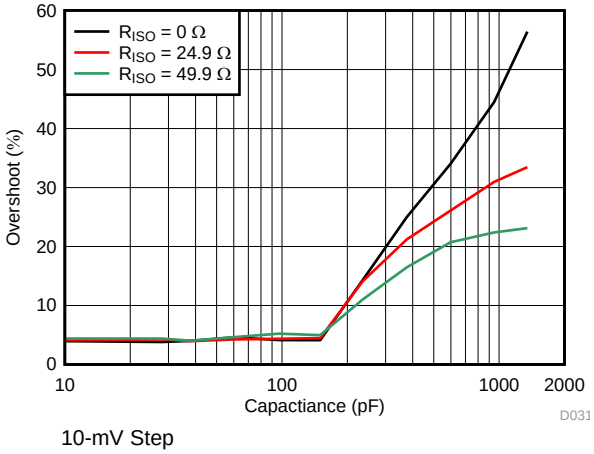


Figure 21. Small-Signal Overshoot vs Capacitive Load

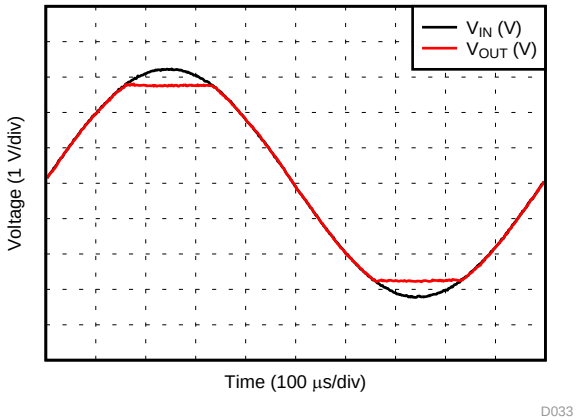


Figure 22. No Phase Reversal

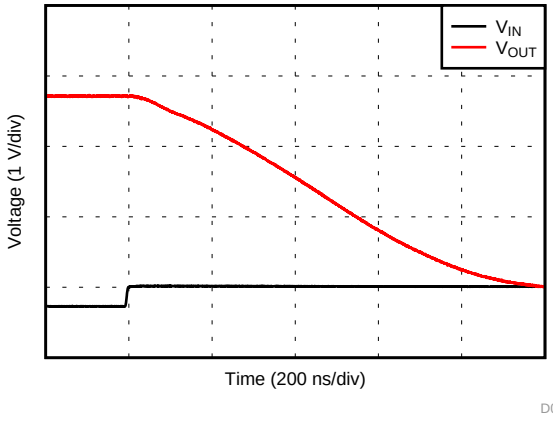


Figure 23. Positive Overload Recovery

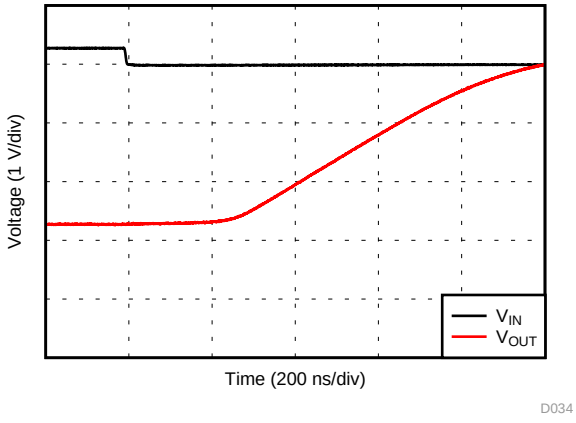
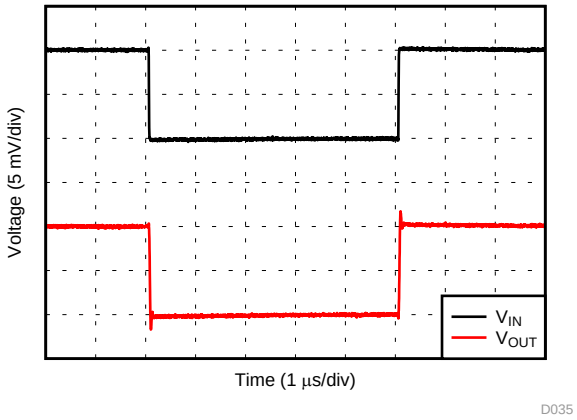


Figure 24. Negative Overload Recovery

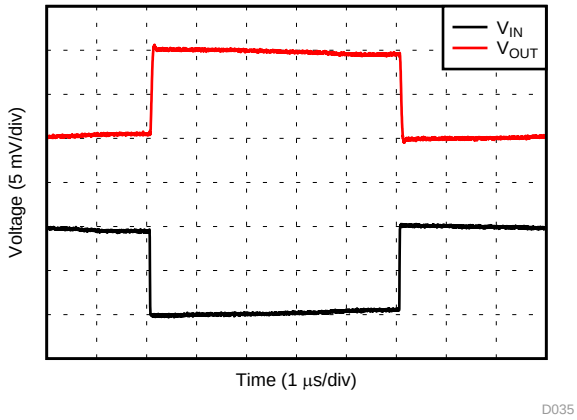
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)



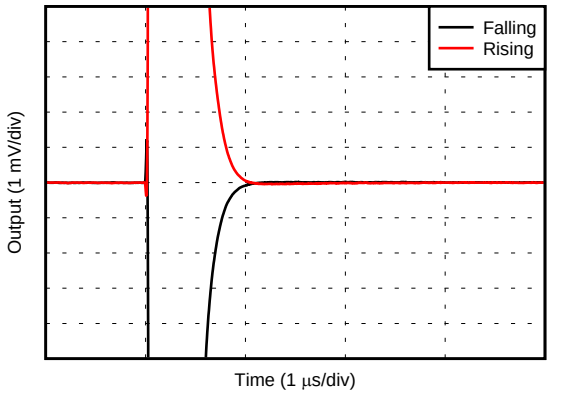
10-mV step G = +1

Figure 25. Small-Signal Step Response



10-mV step G = –1

Figure 26. Small-Signal Step Response



2-V Step

Figure 27. Settling Time

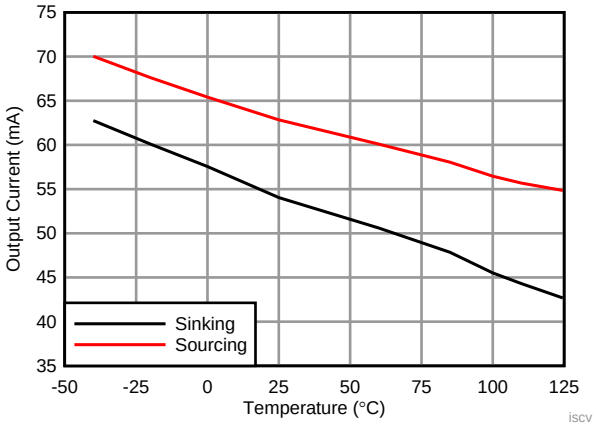


Figure 28. Short-Circuit Current vs Temperature

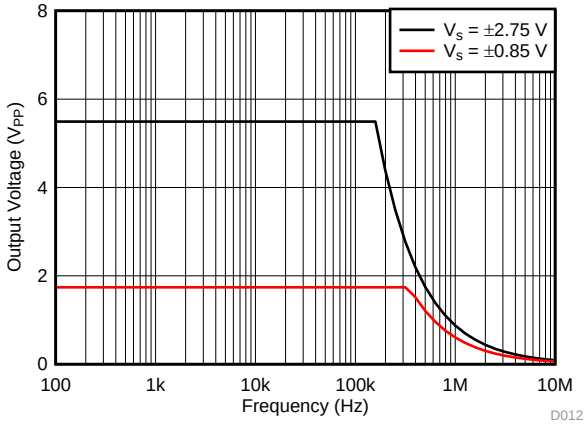


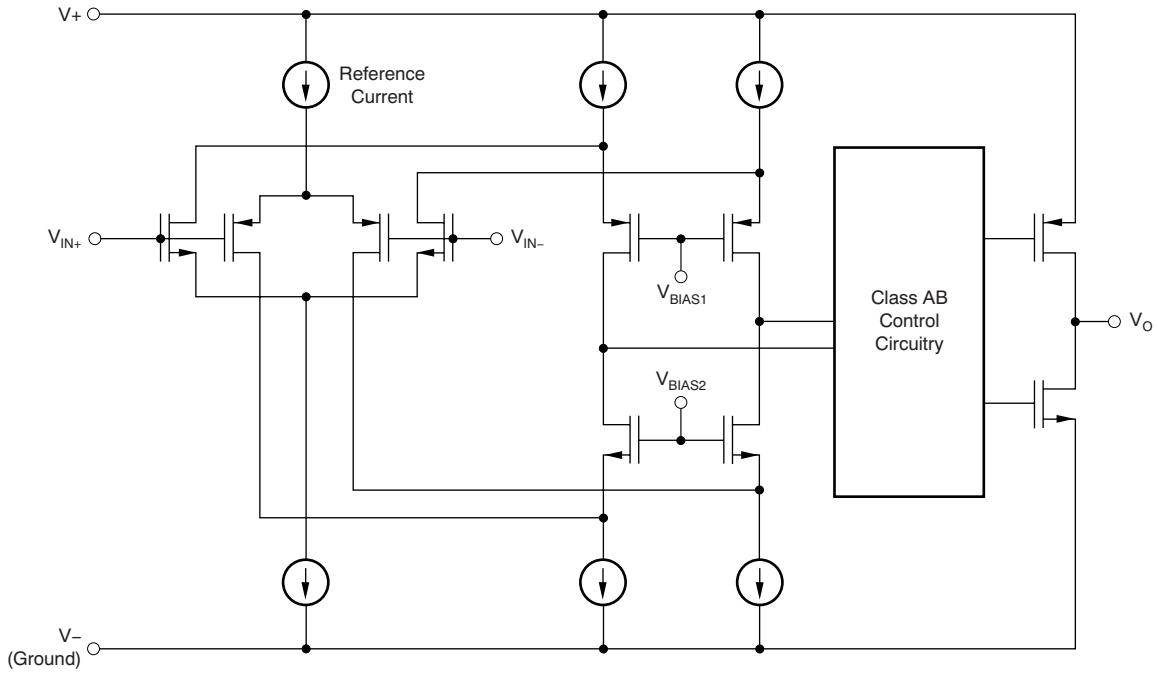
Figure 29. Maximum Output Voltage vs Frequency

7 Detailed Description

7.1 Overview

The OPA1671 is a rail-to-rail input, very low noise operational amplifier (op amp). The OPA1671 operates from 1.7 V to 5.5 V, is unity-gain stable, and is designed for a wide range of audio and general-purpose applications. The OPA1671 strengths also include 13-MHz bandwidth and 4.0-nV/√Hz noise spectral density, with very low input bias current (10 pA). These strengths make the OPA1671 a great choice for a preamplifier in microphone circuits, sensor modules and buffering high-fidelity, digital-to-analog converters (DACs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA1671 op amp can be used with single or dual supplies from an operating range of V_S = 1.7 V (±0.85 V) up to 5.5 V (±2.75 V).

CAUTION

Supply voltages greater than 6 V can permanently damage the device (see *Absolute Maximum Ratings*)

Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics* section.

7.3.2 Input Bias Current

Typically, input bias current is approximately ±10 pA. Input voltages exceeding the power supplies, however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 30.

Unlike many operational amplifiers, there are no diodes connected between the positive and negative input terminals. As a result, differential voltages up to the full supply voltage do not cause any significantly higher current flow into the inputs.

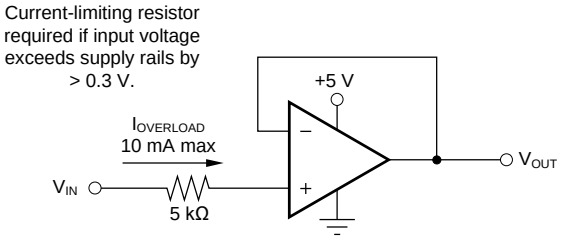


Figure 30. Input Current Protection

7.3.3 Common-Mode Voltage Range

The OPA1671 features true rail-to-rail inputs, allowing full common mode operation from the negative supply voltage to the positive supply voltage. This full common mode operation is achieved with complimentary N-channel and P-channel differential input pairs. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.25 V to (V+) The P-channel is active for common-mode inputs from (V–) to (V+) – 1.25 V. There is a small transition region, typically from (V+) – 1.25 V to (V+) – 1 V. In this region, the offset voltage transitions between the P-channel and N-channel offset values. Figure 5 shows the difference between offset in the P and N regions.

Feature Description (continued)

7.3.4 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA1671 operational amplifier incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 20 MHz (–3 dB), with a rolloff of 20 dB per decade.

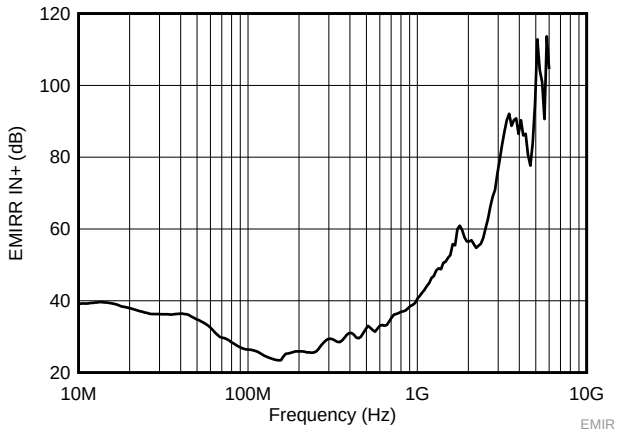


Figure 31. OPA1671 EMIRR vs Frequency

Table 1. OPA1671 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	30 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	38 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	60 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	59 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	90 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	100 dB

7.4 Device Functional Modes

The OPA1671 has a single functional mode and is operational when the power-supply voltage is greater than 1.7 V (±0.85 V). The maximum specified power-supply voltage for the OPA1671 is 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA1671 is a low-noise, rail-to-rail input and output operational amplifier specifically designed for portable applications. The device operates from 1.7 V to 5.5 V, is unity-gain stable, and suitable for a wide range of audio and general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA1671 device to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device a great choice for driving sampling analog-to-digital converters (ADCs).

8.1.1 Capacitive Loads

The dynamic characteristics of the OPA1671 amplifiers are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. Add a small resistor (for example, R_S = 50 Ω) in series with the output to isolate heavier capacitive loads.

8.1.2 Noise Performance

Figure 31 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The op amp itself contributes a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. For a CMOS-input device, the noise resulting from the input current is negligible; therefore, the total noise is dominated by the voltage noise of the OPA1671 at low source resistance, and the resistor noise > 1 kΩ.

Figure 31 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38 × 10^{-23} J/K
- T = temperature in kelvins (K)

For more details on calculating noise, see *Basic Noise Calculations*.

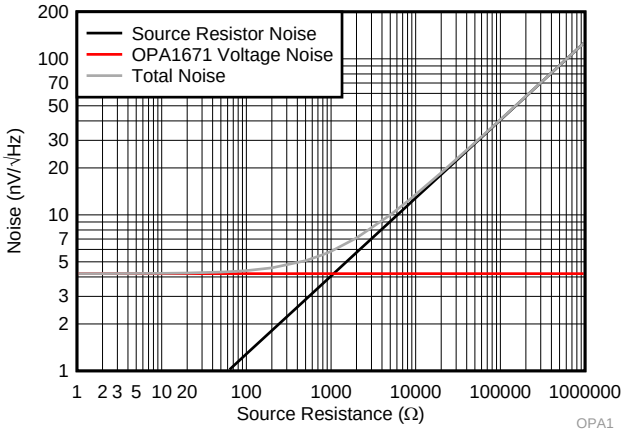


Figure 32. Noise Performance of the OPA1671 in a Unity-Gain Buffer Configuration

Application Information (continued)

8.1.3 Basic Noise Calculations

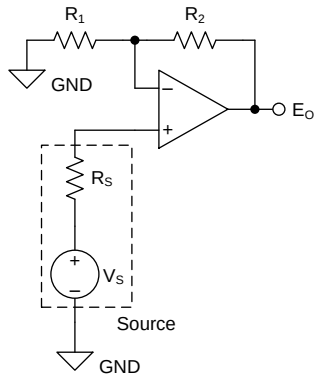
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 31. The source impedance is typically fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 33 shows noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components.

The selected feedback resistor values make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1+\frac{R_2}{R_1}\right)\cdot\sqrt{(e_S)^2+(e_N)^2+\left(e_{R_1\|R_2}\right)^2+(i_N\cdot R_S)^2+\left(i_N\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]\right)^2}\quad [\,V_{RMS}\,]$$

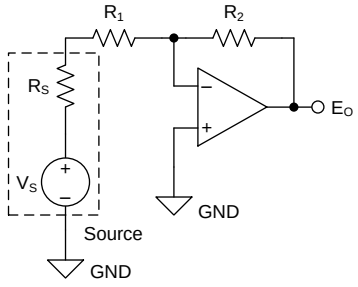
$$(2)\quad e_S = \sqrt{4\cdot k_B\cdot T(K)\cdot R_S}\quad \left[\frac{V}{\sqrt{Hz}}\right]\qquad \text{Thermal noise of } R_S$$

$$(3)\quad e_{R_1\|R_2} = \sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]}\quad \left[\frac{V}{\sqrt{Hz}}\right]\qquad \text{Thermal noise of } R_1 \parallel R_2$$

$$(4)\quad k_B = 1.38065\cdot 10^{-23}\quad \left[\frac{J}{K}\right]\qquad \text{Boltzmann Constant}$$

$$(5)\quad T(K) = 237.15 + T(°C)\quad [\,K\,]\qquad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O = \left(1+\frac{R_2}{R_S+R_1}\right)\cdot\sqrt{(e_N)^2+\left(e_{R_1+R_S\|R_2}\right)^2+\left(i_N\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]\right)^2}\quad [\,V_{RMS}\,]$$

$$(7)\quad e_{R_1+R_S\|R_2} = \sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]}\quad \left[\frac{V}{\sqrt{Hz}}\right]\qquad \text{Thermal noise of } (R_1+R_S) \parallel R_2$$

$$(8)\quad k_B = 1.38065\cdot 10^{-23}\quad \left[\frac{J}{K}\right]\qquad \text{Boltzmann Constant}$$

$$(9)\quad T(K) = 237.15 + T(°C)\quad [\,K\,]\qquad \text{Temperature in kelvins}$$

(1) e_N is the voltage noise of the amplifier. For the OPA1671 series of operational amplifiers, e_N = 4.0 nV/√Hz at 10 kHz.
(2) i_N is the current noise of the amplifier. For the OPA1671 series of operational amplifiers, i_N = 4.5 fA/√Hz at 1 kHz.
(3) For additional resources on noise calculations, see *TI's Precision Labs Series*.

Figure 33. Noise Calculation in Gain Configurations

8.2 Typical Application

This design uses an OPA1671 as a preamplifier for an electret microphone. Electret microphone types are common in many audio applications of varying performance levels. The OPA1671 offers very low noise in a tiny package, and is designed for use in electret preamplifier circuits.

Figure 34 shows the solution.

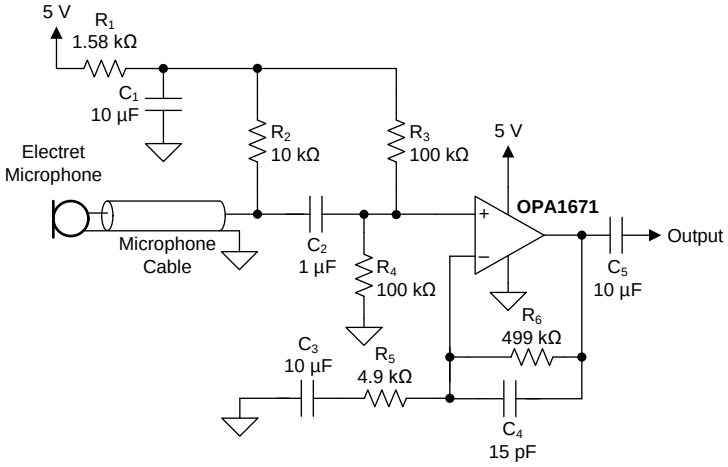


Figure 34. Electret Preamplifier Schematic

8.2.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 5 V
- Gain: 100 V/V
- Frequency response: 3 dB from 20 Hz to 20 kHz
- Output: 2.5 V ±1 V
- Output noise density: < 1 µV/$\sqrt{\text{Hz}}$ at 10 kHz

Typical Application (continued)

8.2.2 Detailed Design Procedure

The preamplifier circuit uses a noninverting gain configuration to allow for high input impedance, with independent gain-setting resistor values. DC bypass is accomplished with C_2 and C_3, with the low frequency poles set by C_2, R_4, C_3 and R_5; see Equation 1 and Equation 2.

$$p_{L1} = \frac{1}{2\pi \cdot (R_3 \,||\, R_4) \cdot C_2} = 3.18 \text{ Hz} \quad (1)$$

$$p_{L2} = \frac{1}{2\pi \cdot R_5 \cdot C_2} = 3.23 \text{ Hz} \quad (2)$$

The filter cutoff frequency is determined by a higher frequency pole, set by R_5 and C_4.

$$p_H = \frac{1}{2\pi \cdot R_6 \cdot C_4} = 21.3 \text{ kHz} \quad (3)$$

The gain of the circuit in the passband is set by R_5 and R_6.

$$A(V/V) = \frac{R_6}{R_5} = 100 (40 \text{ dB}) \quad (4)$$

The ouput noise of the circuit (ignoring the electret microphone intrinsic noise and impedance) is the RSS average noise contribution from R_5 and the input voltage noise of OPA1671. R_5 was selected for minimal noise contribution without requiring a dc blocking cap. (C3) larger than 10 µF. See Equation 5 for the output noise density calculation at 10 kHz.

$$e_{N\_OUT} = \text{Input Referred Noise} \cdot \text{Gain} = \sqrt{(4kTR_5)^2 + V_{N\_10k}{}^2} \cdot 100 = 0.96 \text{ µV}/\sqrt{\text{Hz}} \quad (5)$$

8.2.3 Application Curves

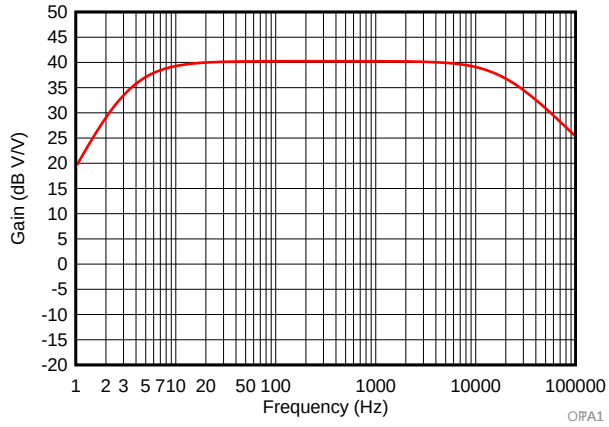


Figure 35. Electret Microphone Preamplifier Transfer Function

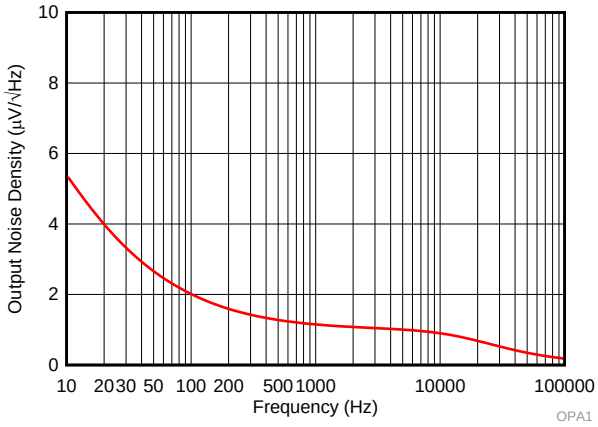


Figure 36. Electret Microphone Preamplifier Output Noise Density

9 Power Supply Recommendations

The OPA1671 device is specified for operation from 1.7 V to 5.5 V (±0.85 V to ±2.75 V).

10 Layout

10.1 Layout Guidelines

Paying attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

10.2 Layout Example

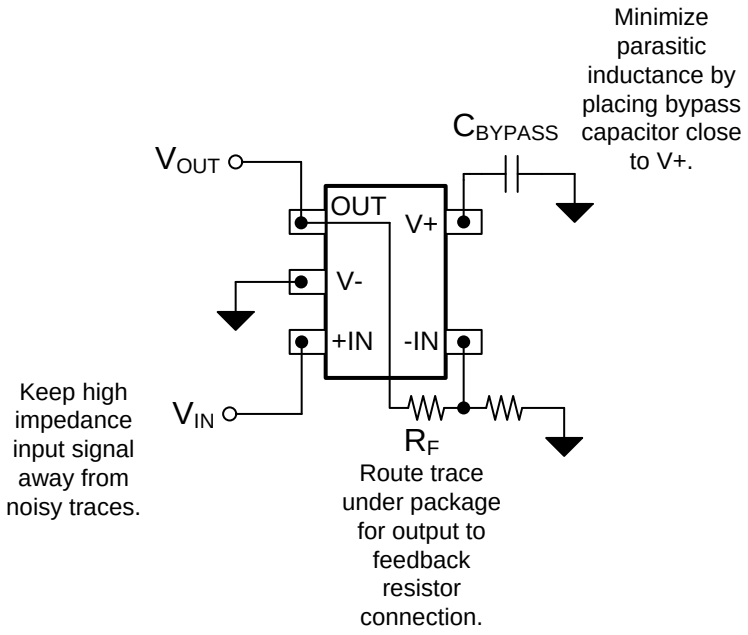


Figure 37. OPA1671 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI™ provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI™ offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI™ software be installed. Download the free TINA-TI™ software from the TINA-TI™ folder.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Circuit Board Layout Techniques*
- Texas, Instruments, *Analog Engineer's Circuit Cookbook*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1671IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	1X6T	Samples
OPA1671IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	1X6T	Samples
OPA1671IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	1D3	Samples
OPA1671IDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	1D3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

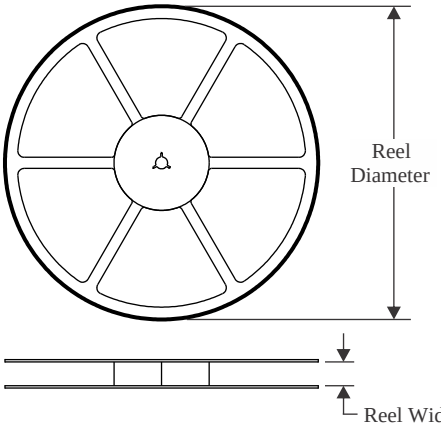
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

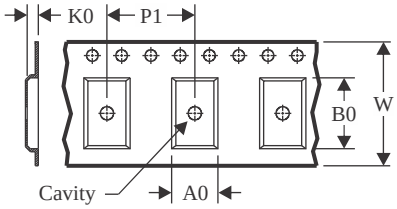
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

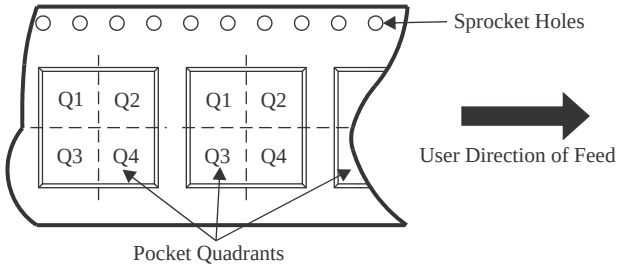


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

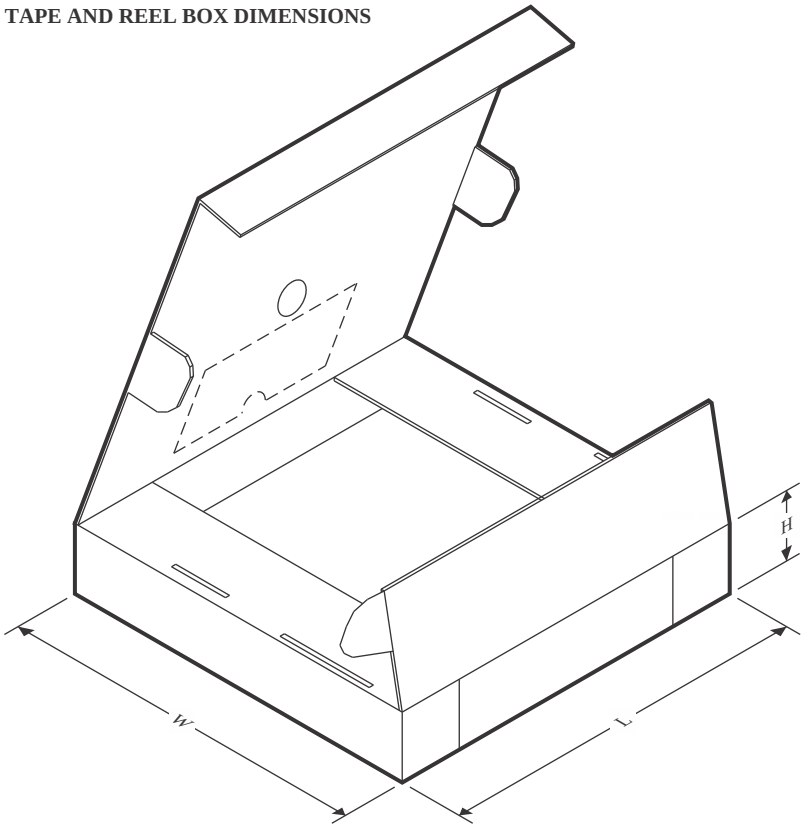
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1671IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA1671IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA1671IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA1671IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA1671IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA1671IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

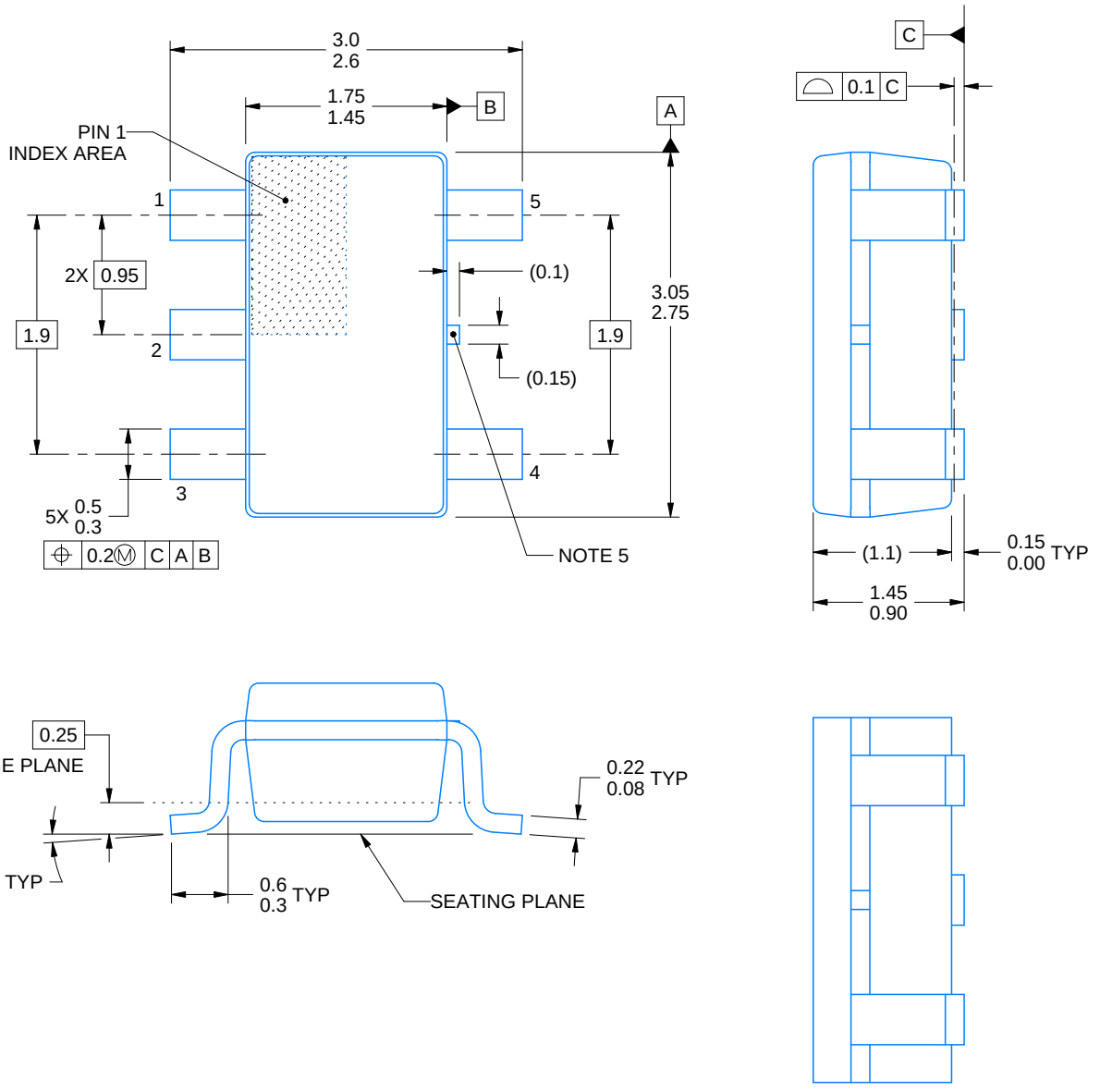
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1671IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA1671IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA1671IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA1671IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA1671IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
OPA1671IDCKT	SC70	DCK	5	250	190.0	190.0	30.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

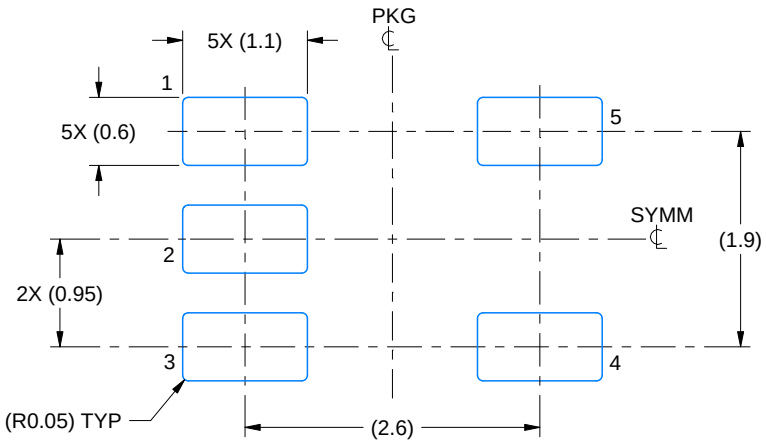


ALTERNATIVE PACKAGE SINGULATION VIEW

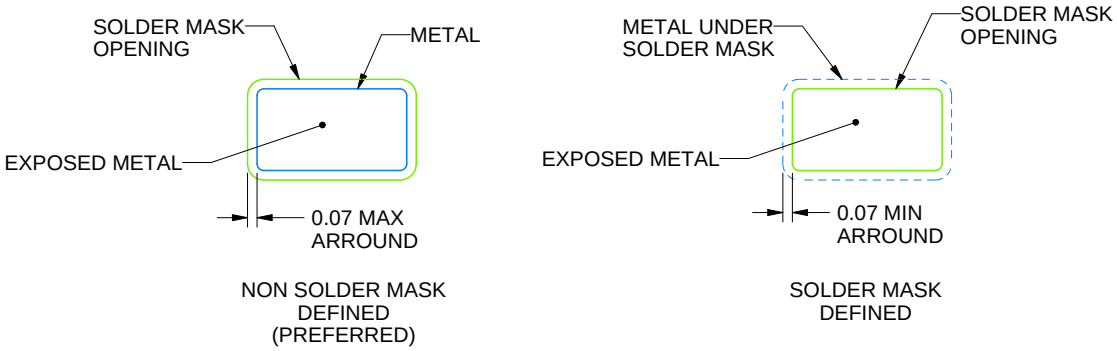
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

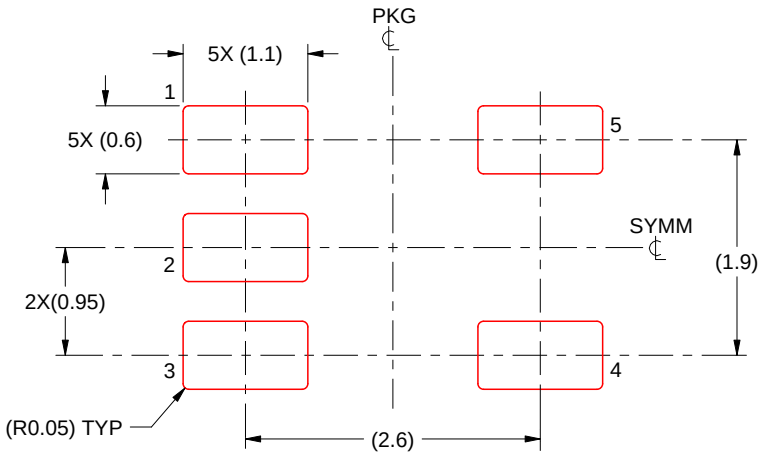


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

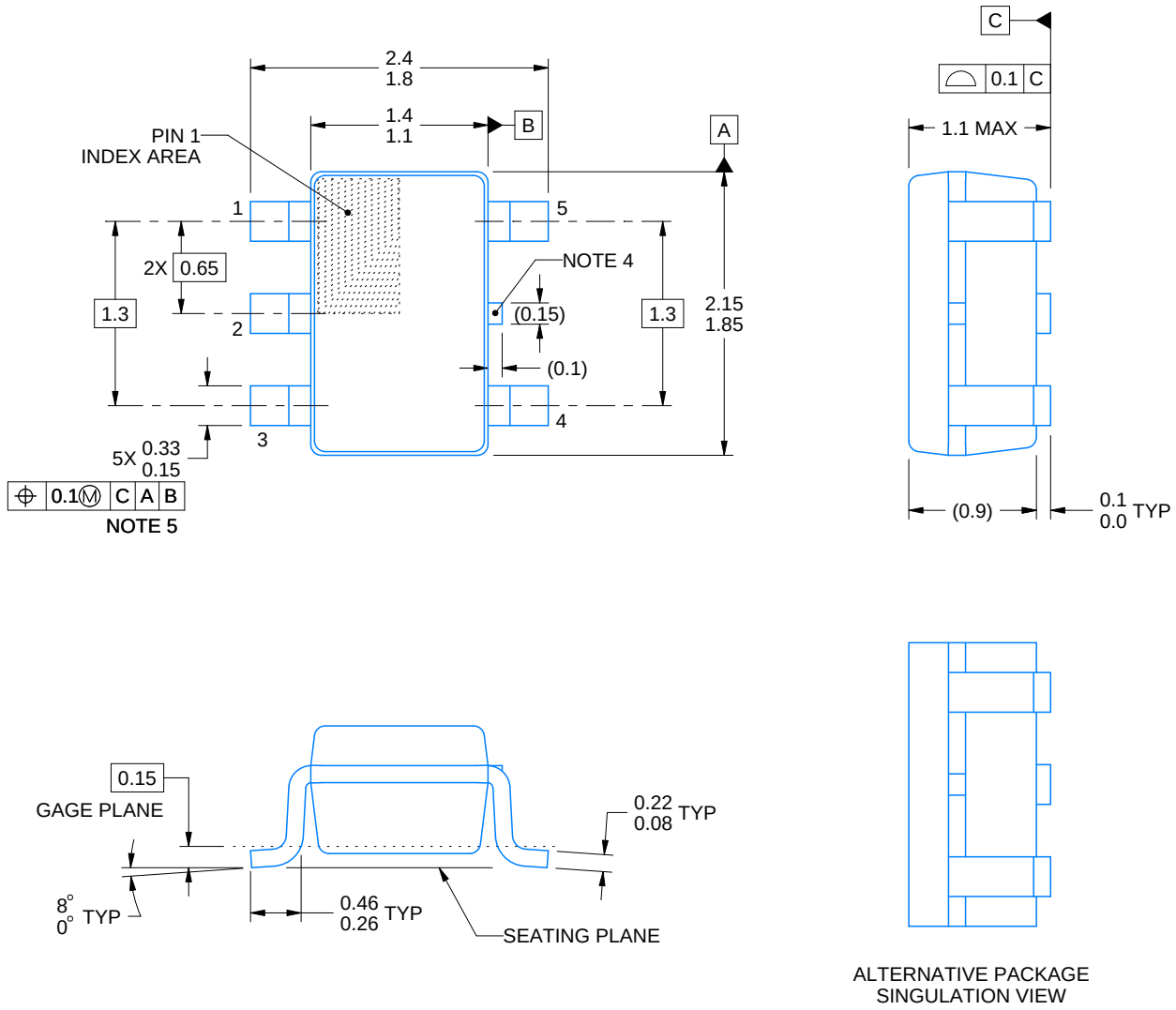
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

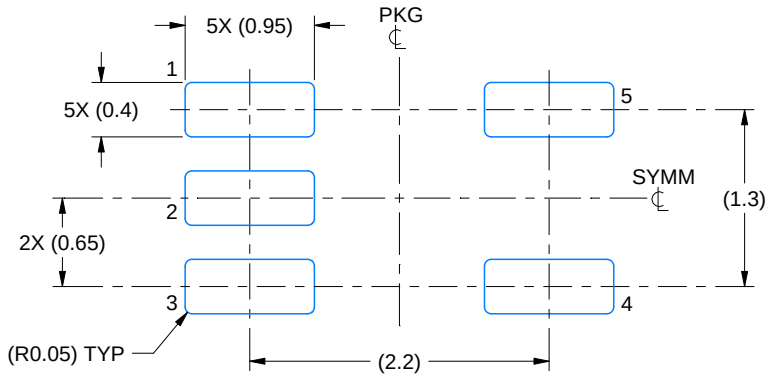
SMALL OUTLINE TRANSISTOR



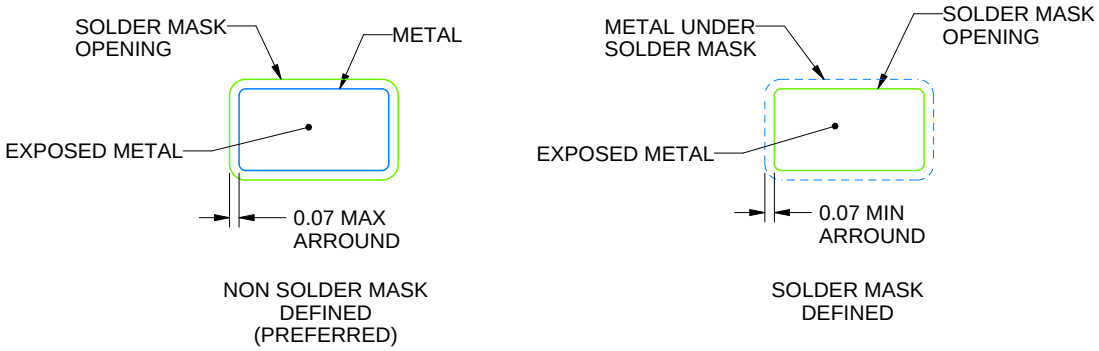
4214834/E 06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

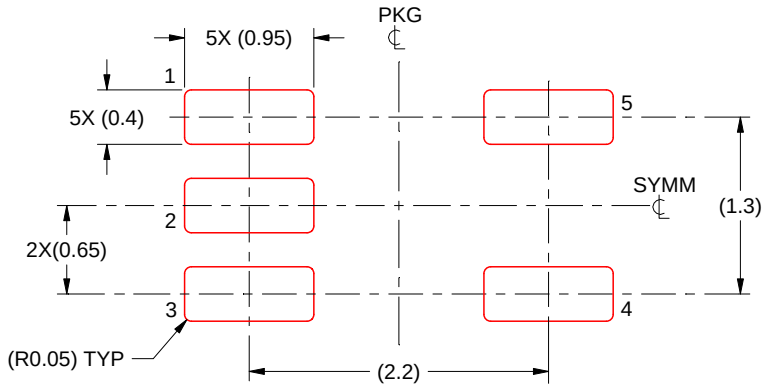


SOLDER MASK DETAILS

4214834/E 06/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/E 06/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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