TEXAS INSTRUMENTS

OPA348, OPA2348, OPA4348

SBOS213H – NOVEMBER 2001 – REVISED NOVEMBER 2016

OPAx348 1-MHz, 45-µA, CMOS, Rail-to-Rail Operational Amplifiers

1 Features

- Low I_Q: 45 µA (Typical)
- Rail-To-Rail Input and Output
- Single Supply: 2.1 V to 5.5 V
- Input Bias Current: 0.5 pA
- *Micro* Size Packages:
  - 5-Pin SC70
  - 8-Pin SOT-23
  - 14-Pin TSSOP
- Excellent Bandwidth-to-Power Consumption Trade-off
- Number of Channels:
  - OPA348: 1
  - OPA2348: 2
  - OPA4348: 4

2 Applications

- Portable Equipment
- Battery-Powered Equipment
- Smoke Alarms
- CO Detectors
- Medical Instrumentation

3 Description

The OPAx348 series of amplifiers are single-supply, low-power, CMOS operational amplifiers. Featuring an extended bandwidth of 1 MHz, and a supply current of 45 µA, the OPAx348 series is useful for low-power applications on single supplies of 2.1 V to 5.5 V.

A low supply current of 45 µA and an input bias current of 0.5 pA, makes the OPAx348 series an optimal candidate for low-power applications such as smoke detectors and other high-impedance sensors.

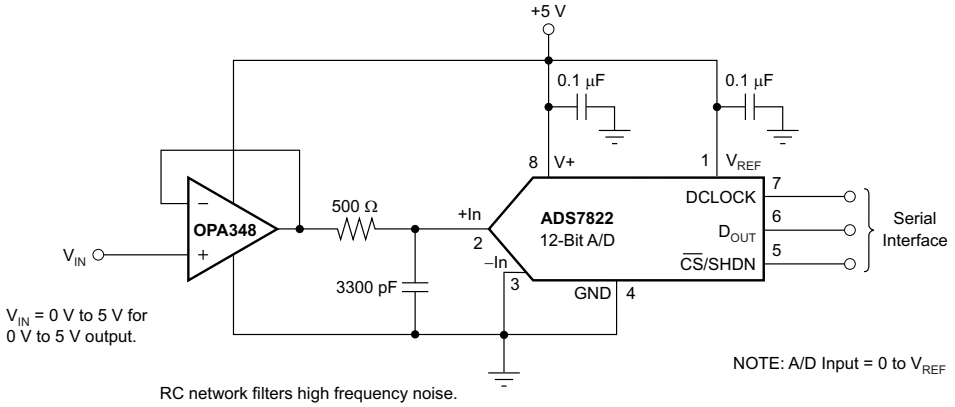
The OPA348 is available in the miniature 5-pin SC70 (SOT), 5-pin SOT-23 (SOT), and 8-pin SO (SOIC) packages. The OPA2348 is available in 8-pin SOT-23 (SOT) and 8-pin SO (SOIC) packages, and the OPA4348 is offered in space-saving 14-pin TSSOP and 14-pin SO (SOIC) packages. The extended temperature range of –40°C to +125°C over all supply voltages offers design flexibility.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA348	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
OPA2348	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (8)	2.90 mm × 1.63 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA4348	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADC Input Driver



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2013) to Revision H **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed OPA348 DCK package designator from SOT to SC70 to match Package Option Addendum information ... 3
- Deleted *Lead temperature* specification from *Absolute Maximum Ratings* table ... 6
- Reformatted *Thermal Information* table note ... 7
- Changed second and third paragraphs of *Driving A/D Converters* section to eliminate redundancy ... 17

Changes from Revision F (October 2012) to Revision G **Page**

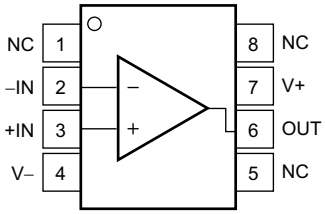
- Changed 2nd footnote for *Absolute Maximum Ratings* table ... 6

Changes from Revision E (September 2012) to Revision F **Page**

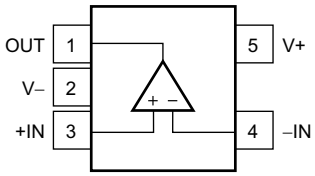
- Deleted Packaging and Ordering information table data ... 1

5 Pin Configuration and Functions

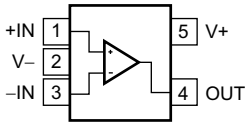
OPA348 D Package
8-Pin SOIC
Top View



OPA348 DBV Package
5-Pin SOT-23
Top View



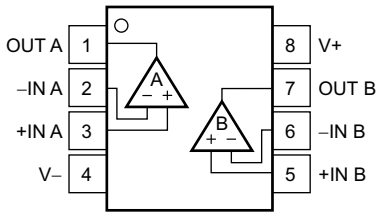
OPA348 DCK Package
5-Pin SC70 (*Micro* size)
Top View



Pin Functions: OPA348

NAME	PIN			I/O	DESCRIPTION
	DBV (SOT-23)	DCK (SC70)	D (SOIC)		
–IN	4	3	2	I	Negative (inverting) input
+IN	3	1	3	I	Positive (noninverting) input
NC	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	4	6	O	Output
V–	2	2	4	—	Negative (lowest) power supply
V+	5	5	7	—	Positive (highest) power supply

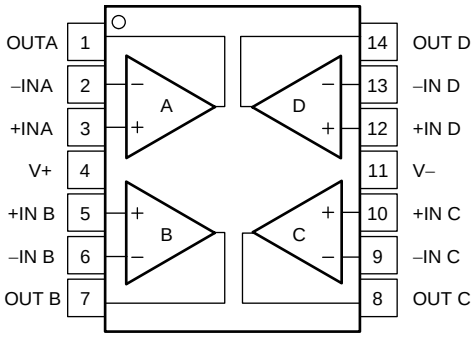
OPA2348 D, DCN, and DGK Packages
8-Pin SOIC, SOT, and VSSOP
Top View



Pin Functions: OPA2348

PIN				I/O	DESCRIPTION
NAME	D (SOIC)	DCN (SOT-23)	DGK (VSSOP)		
–IN A	2	2	2	I	Inverting input, channel A
–IN B	6	6	6	I	Inverting input, channel B
+IN A	3	3	3	I	Noninverting input, channel A
+IN B	5	5	5	I	Noninverting input, channel B
OUT A	1	1	1	O	Output, channel A
OUT B	7	7	7	O	Output, channel B
V–	4	4	4	—	Negative (lowest) power supply
V+	8	8	8	—	Positive (highest) power supply

OPA4348 D and PW Packages
14-Pin SOIC and TSSOP
Top View



Pin Functions: OPA4348

PIN			I/O	DESCRIPTION
NAME	D (SOIC)	PW (TSSOP)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	9	9	I	Inverting input, channel C
–IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V–	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		7.5	V
	Signal input terminals, voltage(2)	(V–) – 0.5	(V+) + 0.5	
Current	Signal input terminals, current(2)		10	mA
	Output short-circuit(3)	Continuous		
Temperature	Junction, T_J		150	°C
	Operating, T_A	–65	150	
	Storage, T_{stg}	–65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied.
(2) Input terminals are not diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	2.1	5.5	V
Specified temperature	–40	125	°C

6.4 Thermal Information: OPA348

THERMAL METRIC(1)		OPA348			UNIT
		DBV (SOT-23)	DCK (SC70)	D (SOIC)	
		5 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229	267	142	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99	81	90	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55	55	83	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.7	1.2	40	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54	54	82	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.5 Thermal Information: OPA2348

THERMAL METRIC(1)		OPA2348			UNIT
		D (SOIC)	DGK (VSSOP)	DCN (SOT-23)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134	191	147	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90	83	115	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79	112	32	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30	18	38	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78	110	33	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.6 Thermal Information: OPA4348

THERMAL METRIC(1)		OPA4348		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78	121	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35	49	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33	63	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	62	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.7 Electrical Characteristics

at V_S = 2.5 V to 5.5 V, T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V, V_{CM} = (V–) + 0.8 V		1	5	mV
		V_S = 5 V, V_{CM} = (V–) + 0.8 V, at T_A = –40°C to 125°C			6	
dV_{OS} /dT	Input offset voltage drift	At T_A = –40°C to 125°C		4		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 2.5 V to 5.5 V, V_{CM} < (V+) – 1.7 V		60	175	µV/V
		At T_A = –40°C to 125°C, V_S = 2.5 V to 5.5 V, V_{CM} < (V+) – 1.7 V			300	
	Channel separation	At dc		0.2		µV/V
		At f = 1 kHz		134		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.2		(V+) + 0.2	V

Electrical Characteristics (continued)

at V_S = 2.5 V to 5.5 V, T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	(V–) – 0.2 V < V_{CM} < (V+) – 1.7 V	70	82		dB
		(V–) < V_{CM} < (V+) – 1.7 V, at T_A = –40°C to 125°C	66			
		V_S = 5.5 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V	60	71		
		V_S = 5.5 V, (V–) < V_{CM} < (V+), at T_A = –40°C to 125°C	56			
INPUT BIAS CURRENT						
I_B	Input bias current			±0.5	±10	pA
I_{OS}	Input offset current			±0.5	±10	pA
INPUT IMPEDANCE						
	Differential			10^{13} || 3		Ω || pF
	Common-mode			10^{13} || 6		Ω || pF
NOISE						
	Input voltage noise	V_{CM} < (V+) – 1.7 V, f = 0.1 Hz to 10 Hz		10		μV_{PP}
e_n	Input voltage noise density	V_{CM} < (V+) – 1.7 V, f = 1 kHz		35		nV/√Hz
i_n	Input current noise density	V_{CM} < (V+) – 1.7 V, f = 1 kHz		4		fA/√Hz
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5 V, R_L = 100 kΩ, 0.025 V < V_O < 4.975 V	94	108		dB
		V_S = 5 V, R_L = 100 kΩ, 0.025 V < V_O < 4.975 V, at T_A = –40°C to 125°C	90			
		V_S = 5 V, R_L = 5 kΩ, 0.125 V < V_O < 4.875 V	90	98		
		V_S = 5 V, R_L = 5 kΩ, 0.125 V < V_O < 4.875 V, at T_A = –40°C to 125°C	88			
OUTPUT						
	Voltage output swing from rail	R_L = 100 kΩ, A_{OL} > 94 dB		18	25	mV
		R_L = 100 kΩ, A_{OL} > 90 dB, at T_A = –40°C to 125°C			25	
		R_L = 5 kΩ, A_{OL} > 90 dB		100	125	
		R_L = 5 kΩ, A_{OL} > 88 dB, at T_A = –40°C to 125°C			125	
I_{SC}	Short-circuit current			±10		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*		
FREQUENCY RESPONSE						
GBP	Gain-bandwidth product	C_L = 100 pF		1		MHz
SR	Slew rate	C_L = 100 pF, G = +1		0.5		V/µs
t_S	Settling time, 0.1%	C_L = 100 pF, V_S = 5.5 V, 2-V Step, G = +1		5		µs
	Settling time, 0.01%	C_L = 100 pF, V_S = 5.5 V, 2-V Step, G = +1		7		
	Overload recovery time	C_L = 100 pF, V_{IN} × Gain > V_S		1.6		µs
THD+N	Total harmonic distortion + noise	C_L = 100 pF, V_S = 5.5 V, V_O = 3 V_{PP}, G = +1, f = 1 kHz		0.0023%		
POWER SUPPLY						
V_S	Specified voltage		2.5		5.5	V
	Operating voltage			2.1	5.5	V
I_Q	Quiescent current (per amplifier)	I_O = 0 mA		45	65	µA
		I_O = 0 mA, at T_A = –40°C to 125°C			75	

6.8 Typical Characteristics

at T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

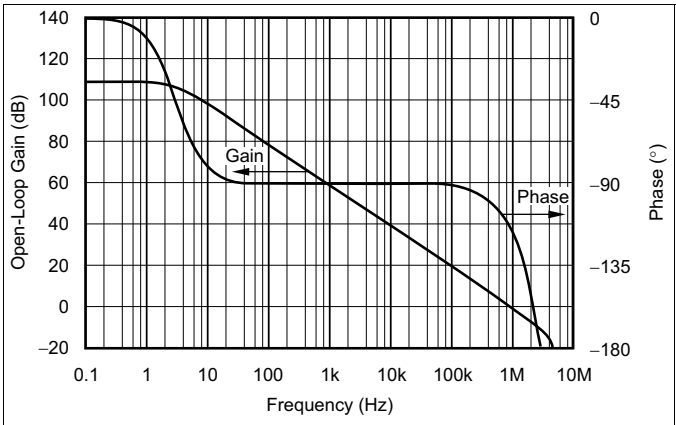


Figure 1. Open-Loop Gain and Phase vs Frequency

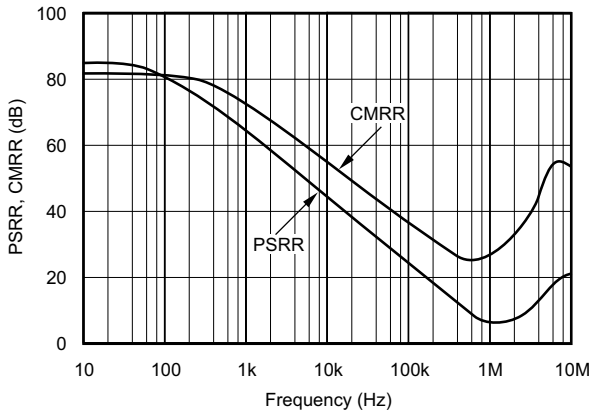


Figure 2. PSRR and CMRR vs Frequency

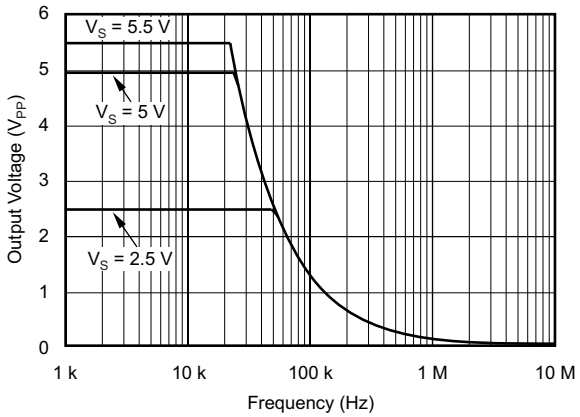


Figure 3. Maximum Output Voltage vs Frequency

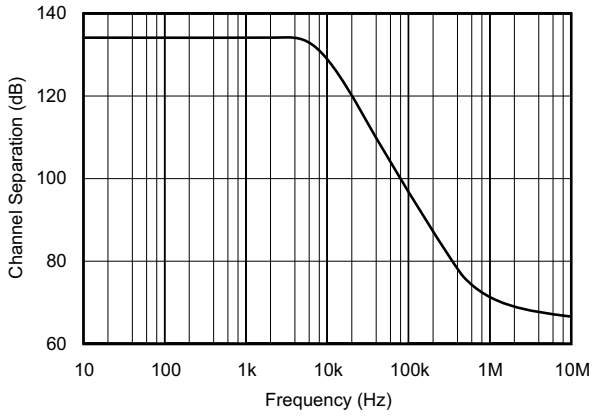


Figure 4. Channel Separation vs Frequency

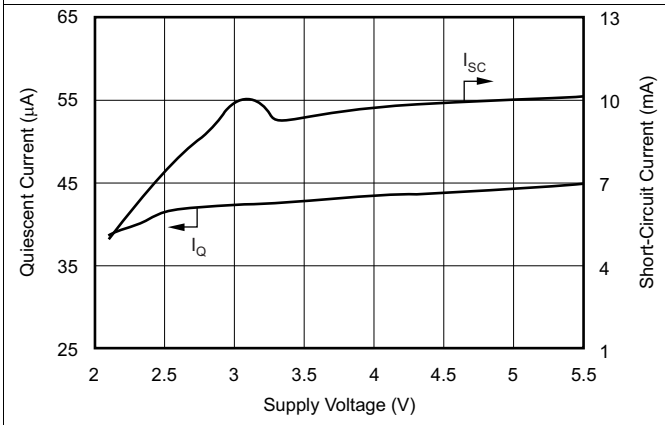


Figure 5. Quiescent and Short-Circuit Current vs Supply Voltage

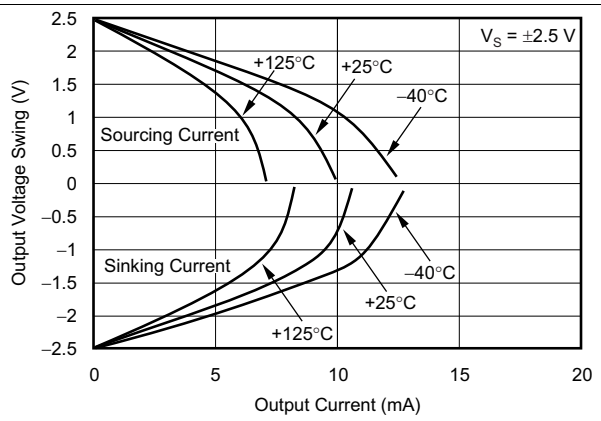


Figure 6. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

at T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

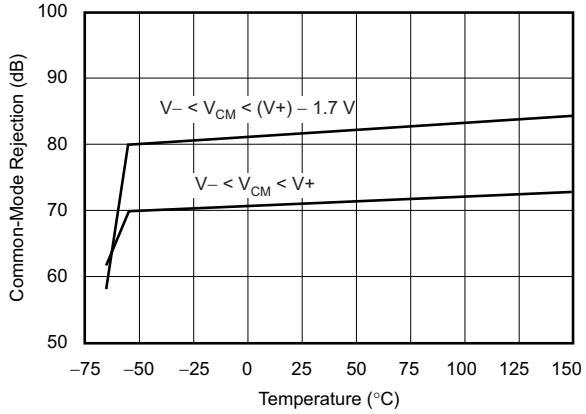


Figure 7. Common-Mode Rejection vs Temperature

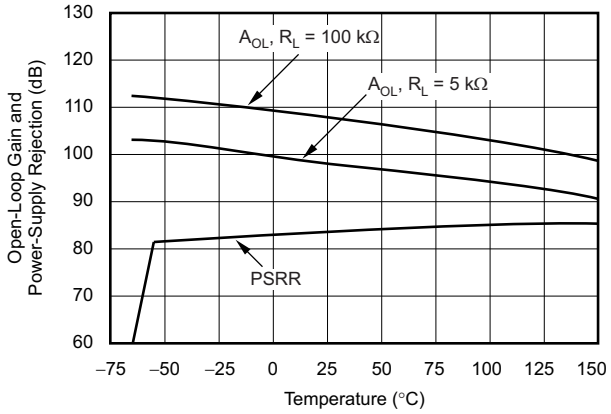


Figure 8. Open-Loop Gain and PSRR vs Temperature

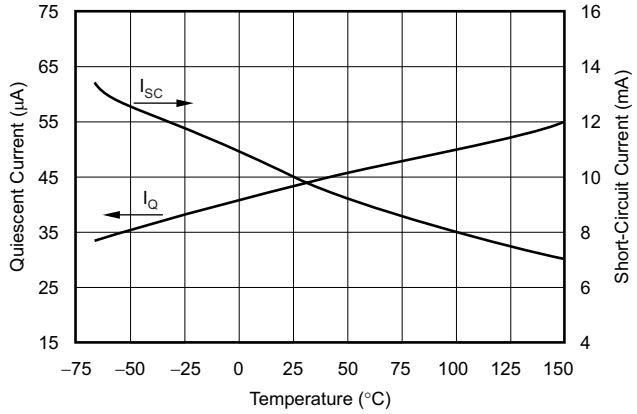


Figure 9. Quiescent and Short-Circuit Current vs Temperature

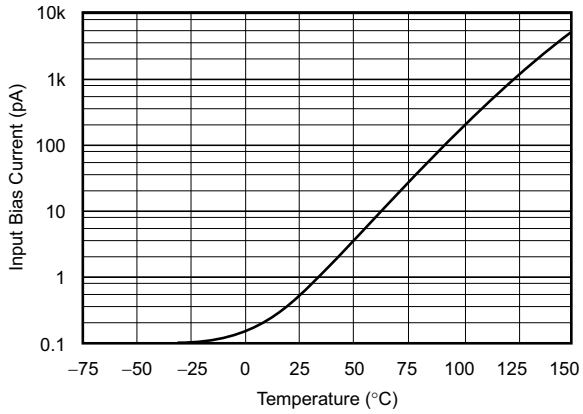


Figure 10. Input Bias (I_B) Current vs Temperature

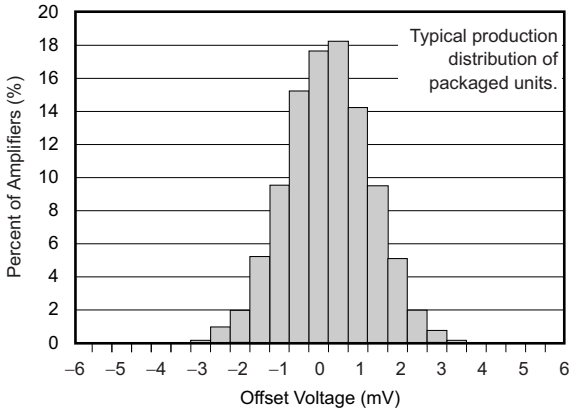


Figure 11. Offset Voltage Production Distribution

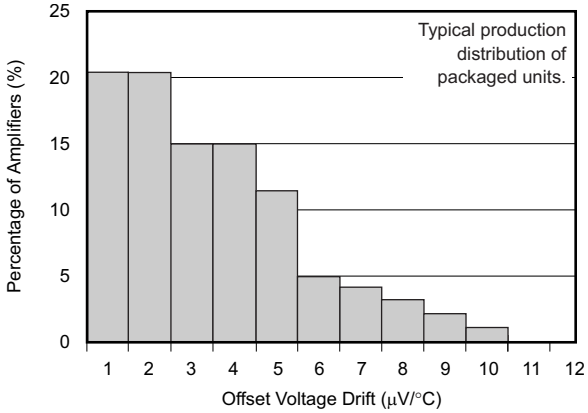


Figure 12. Offset Voltage Drift Magnitude Production Distribution

Typical Characteristics (continued)

at T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

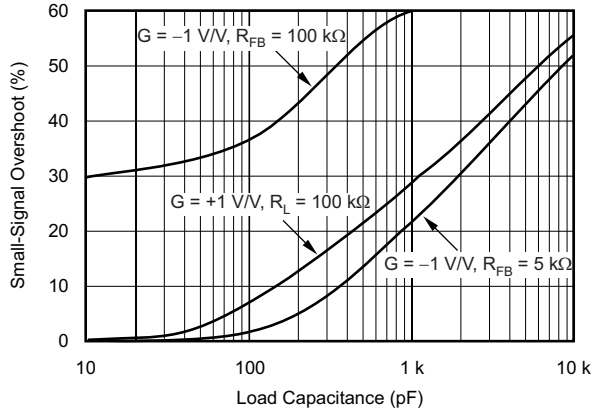


Figure 13. Small-Signal Overshoot vs Load Capacitance

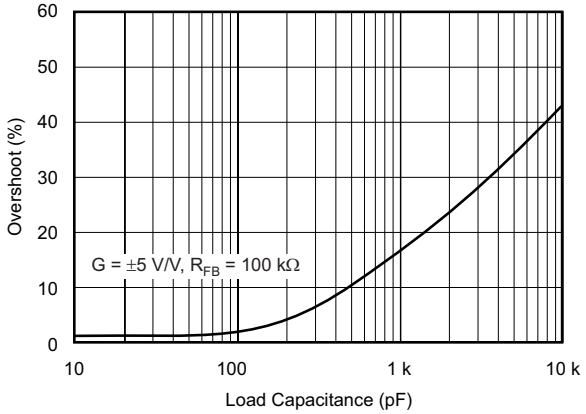
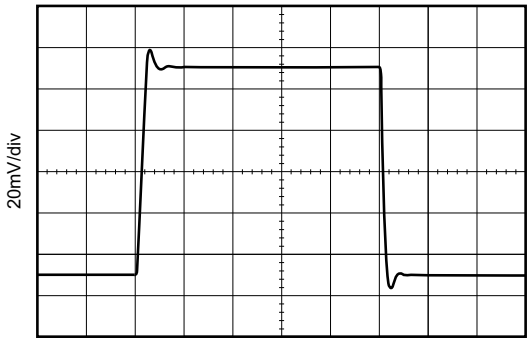
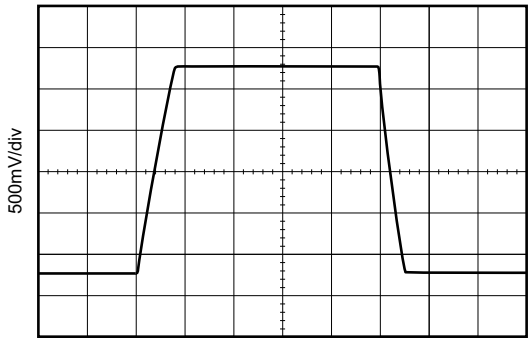


Figure 14. Percent Overshoot vs Load Capacitance



G = +1 V/V, R_L = 100 kΩ, C_L = 100 pF

Figure 15. Small-Signal Step Response



G = +1 V/V, R_L = 100 kΩ, C_L = 100 pF

Figure 16. Large-Signal Step Response

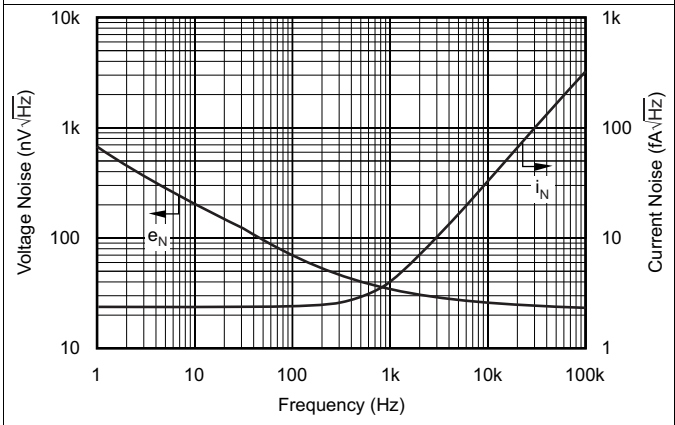


Figure 17. Input Current and Voltage Noise Spectral Density vs Frequency

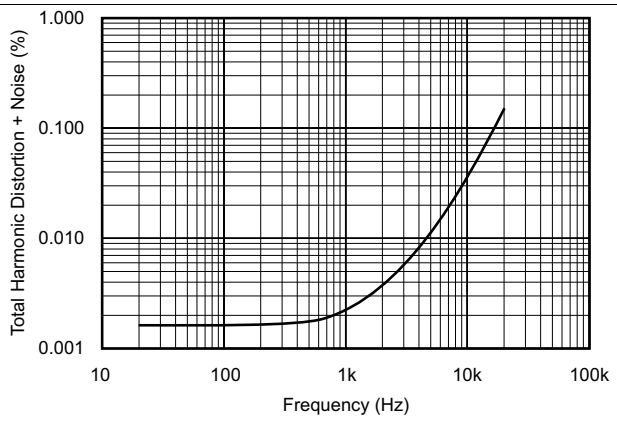


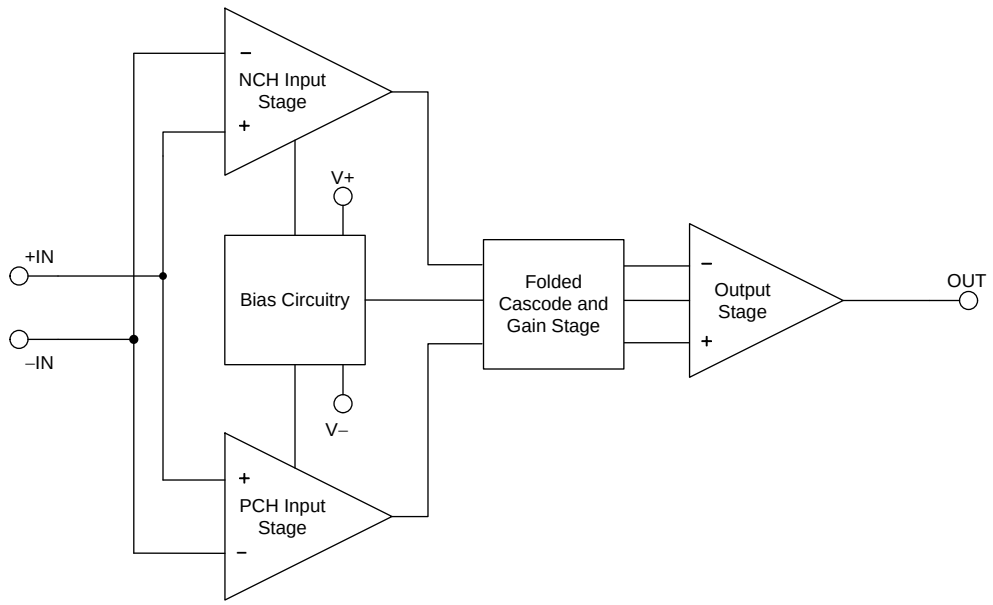
Figure 18. Total Harmonic Distortion + Noise vs Frequency

7 Detailed Description

7.1 Overview

The OPAx348 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The OPAx348 series features wide bandwidth with rail-to-rail input and output for increased dynamic range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPAx348 series op amps are fully specified and tested from 2.5 V to 5.5 V. However, supply voltage may range from 2.1 V to 5.5 V. Parameters are tested over the specified supply range which is an unique feature of the OPAx348 series. All temperature specifications apply from –40°C to +125°C. Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* section.

Feature Description (continued)

7.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPA348 series extends 200 mV beyond the supply rails. This extended range is achieved with a complementary input stage which is a N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.2 V to 300 mV above the positive supply, while the P-channel pair is on for inputs from 300 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region, shown in Figure 19, can vary ±300 mV with process variation. Thus, the transition region (both stages on) ranges from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within the 200-mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

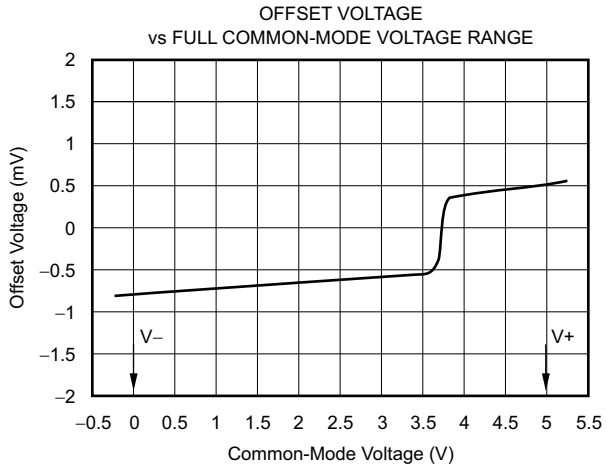


Figure 19. Behavior of Typical Transition Region at Room Temperature

7.3.3 Rail-To-Rail Input

The input common-mode range extends from (V–) – 0.2 V to (V+) + 0.2 V. For normal operation, inputs must be limited to this range. The absolute maximum input voltage is 500 mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, do not cause any damage to the op amp. Unlike some other op amps, if input current is limited the inputs may go beyond the power supplies without phase inversion; see Figure 20.

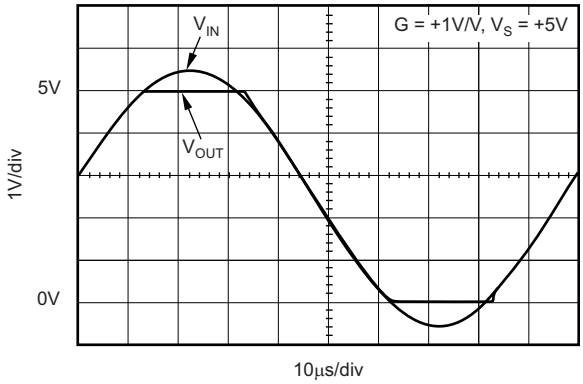


Figure 20. OPA348: No Phase Inversion with Inputs Greater Than The Power-Supply Voltage

Feature Description (continued)

Normally, input currents are 0.5 pA. However, large inputs (greater than 500 mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10 mA. This limiting is easily accomplished with an input voltage resistor, as shown in Figure 21.

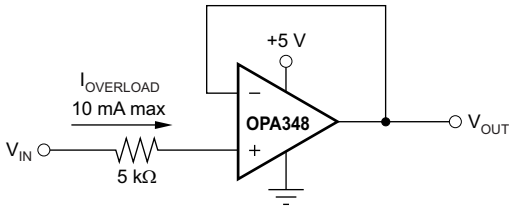


Figure 21. Input Current Protection for Voltages Exceeding the Supply Voltage

7.3.4 Rail-To-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 5-kΩ loads connected to any potential between V+ and ground. For light resistive loads (> 100 kΩ), the output voltage can typically swing to within 18 mV from supply rail. With moderately resistive loads (10 kΩ to 50 kΩ), the output voltage can typically swing to within 100 mV of the supply rails while maintaining high open-loop gain (see Figure 6).

7.3.5 Capacitive Load and Stability

The OPA348 in a unity-gain configuration can directly drive up to 250 pF pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see Figure 13). In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor, R_S, in series with the output, as shown in Figure 22. This small resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a direct current (dc) error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S / R_L, and is generally negligible.

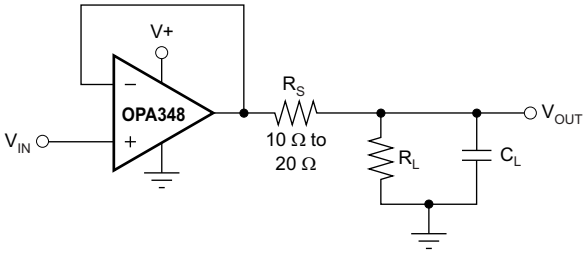


Figure 22. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

Feature Description (continued)

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input, and the gain setting resistors, thus degrading capacitive load drive. Best performance is achieved by using small valued resistors. For example, when driving a 500-pF load, reducing the resistor values from 100 kΩ to 5 kΩ decreases overshoot from 55% to 13% (see Figure 13). However, when large valued resistors cannot be avoided, a small (4-pF to 6-pF) capacitor, C_{FB}, can be inserted in the feedback, as shown in Figure 23. This configuration significantly reduces overshoot by compensating the effect of capacitance, C_{IN}, which includes the amplifier input capacitance and printed circuit board (PCB) parasitic capacitance.

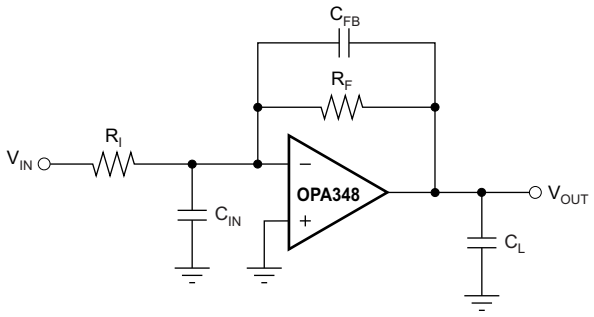


Figure 23. Improving Capacitive Load Drive

7.4 Device Functional Modes

The OPAx348 has a single functional mode and is operational when the power-supply voltage is greater than 2.1 V (±1.05 V). The maximum power supply voltage for the OPAx348 is 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA348 amplifier is a single-supply, CMOS op amp with 1-MHz unity-gain bandwidth and supply current of only 45 µA. Its performance is optimized for a lower power (2.1 V to 5.5 V), single-supply application, with its input common-mode voltage linear range extending 200 mV beyond the rails and the output voltage swing within 25 mV of either rail.

The OPA348 series features wide bandwidth and unity-gain stability with rail-to-rail input and output for increased dynamic range. Figure 24 shows the input and output waveforms for the OPA348 in unity-gain configuration. Operation is from a single 5-V supply with a 100-kΩ load connected to V_S / 2. The input is a 5-V_{PP} sinusoid. Output voltage is approximately 4.98 V_{PP}.

Power-supply pins must be bypassed with 0.01-µF ceramic capacitors.

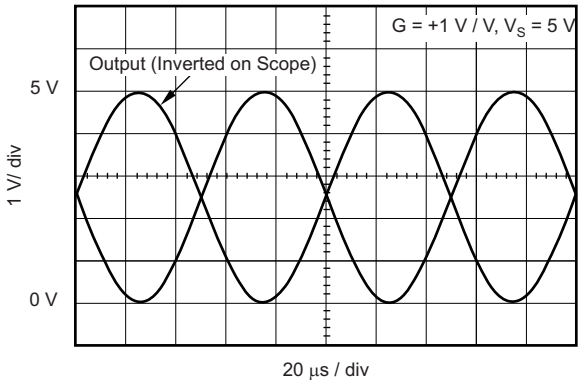


Figure 24. OPA348 Features Rail-to-Rail Input and Output

Application Information (continued)

8.1.1 Driving A/D Converters

The OPA348 series op amps are optimized for driving medium-speed sampling analog-to-digital converters (ADCs). The OPA348 op amps buffer the ADC input capacitance and resulting charge injection while providing signal gain.

Figure 25 shows the OPA348 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, *micro*POWER sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA348, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC input can be used to provide both an anti-aliasing filter and charge injection current.

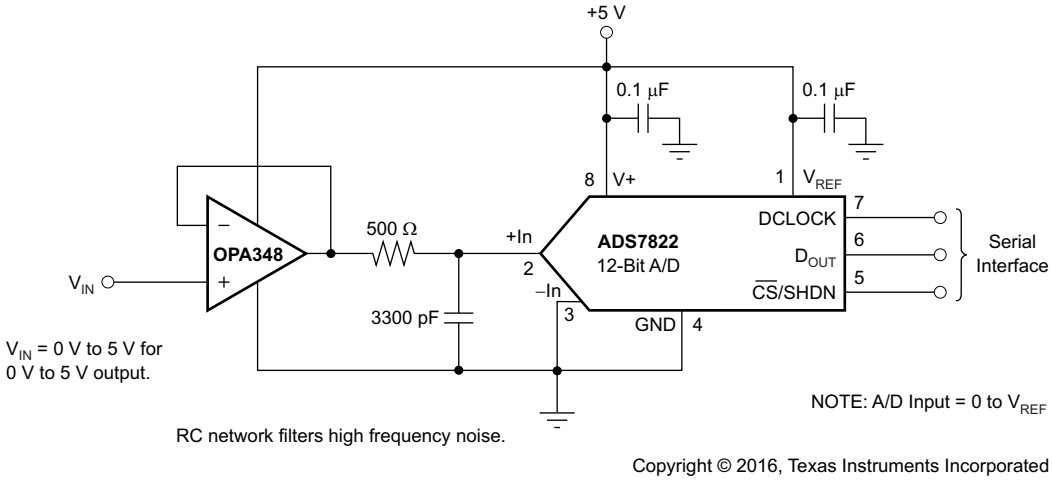


Figure 25. OPA348 in Noninverting Configuration Driving ADS7822

Figure 26 illustrates the OPA2348 driving an ADS7822 in a speech-bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit operates with V_S = 2.7 V to 5 V with less than 250-µA typical quiescent current.

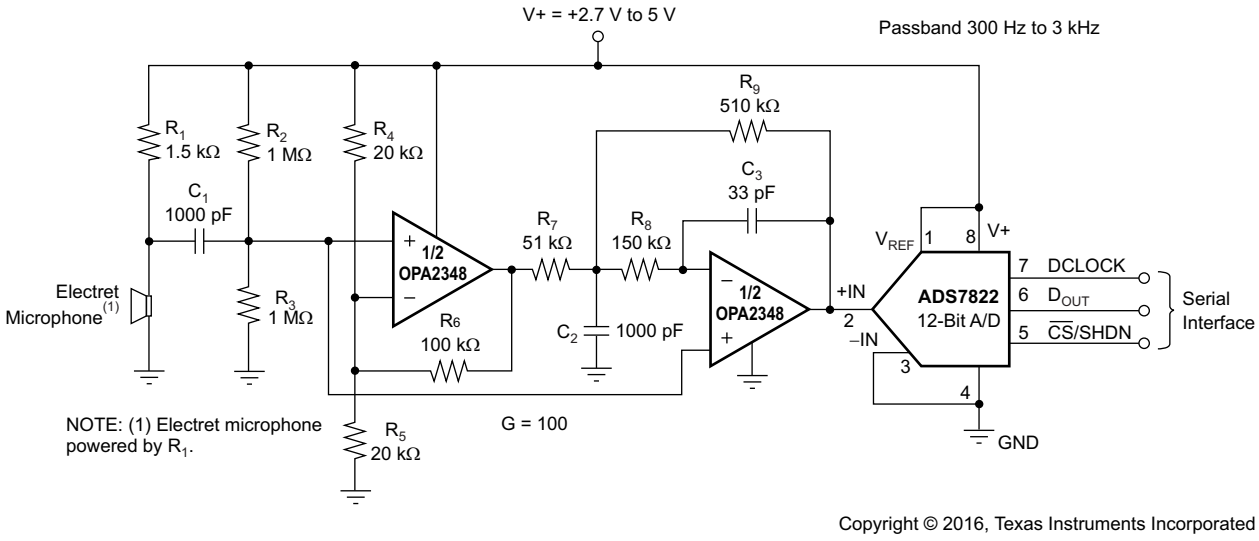


Figure 26. OPA2348 as a Speech-Bandpass Filtered Data Acquisition System

8.2 Typical Application

Figure 27 shows the OPA348 in a typical noninverting application with input signal bandwidth limited by the input low-pass filter.

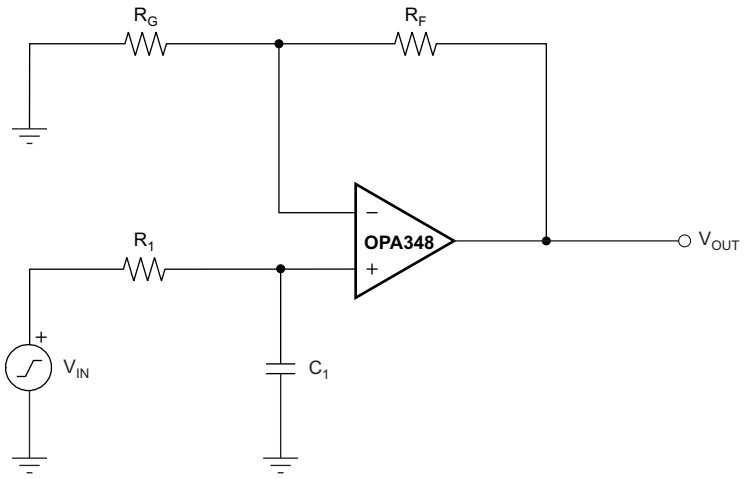


Figure 27. Single-Pole, Low-Pass Filter

Equation 1 and Equation 2 show the relationships for the low-pass cutoff frequency and the low frequency gain and the passive elements surrounding the amplifier.

$$f_{-3\,dB} = \frac{1}{2\pi R_1 C_1} \quad (1)$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right) \quad (2)$$

8.2.1 Design Requirements

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in Figure 27. If a steeper attenuation level is required, a two-pole or higher-order filter may be used.

8.2.2 Detailed Design Procedure

The design goals for this circuit include these parameters:

- A noninverting gain of 10 V/V (20 dB)
- Design a single-pole response circuit with –3-dB roll-off at 15.9 kHz and 159 Hz
- Modify the design to increase attenuation level to –40-dB/decade (Sallen-Key Filter)

Use these design values:

- C_1 = 0 nF, 10 nF, 1 µF
- R_1 = 1 kΩ
- R_G = 10 kΩ
- R_F = 90 kΩ

Typical Application (continued)

Figure 28 shows how the output voltage of OPA348 changes over frequency depending on the value of C_1 with a constant R_1 of 1 kΩ. Without any filtering of the input signal (C_1 = 0), the –3-dB effective bandwidth is a function of the OPA348 unity-gain bandwidth and closed-loop gain, $f_{(-3dB)}$ = UGBW/A_{CL}, where A_{CL} is closed-loop gain and UGBW denotes unity-gain bandwidth. Thus, for a closed-loop gain = 10, $f_{(-3dB)}$ = 1 MHz/10 =100 kHz; refer to Figure 28.

To further limit the output bandwidth, an appropriate choice of C_1 must be made: for C_1 = 10 nF, $f_C = \frac{1}{2\pi \times R_1 C_1} = \frac{1}{2\pi \times 1^3 \times 1^{-8}}$ = 15.9 kHz.

To further limit the bandwidth, a larger C_1 must be used:

choosing C_1 = 1 µF, $f_C = \frac{1}{2\pi \times R_1 C_1} = \frac{1}{2\pi \times 1^3 \times 1^{-6}}$ = 159 Hz. See Figure 28.

8.2.3 Application Curve

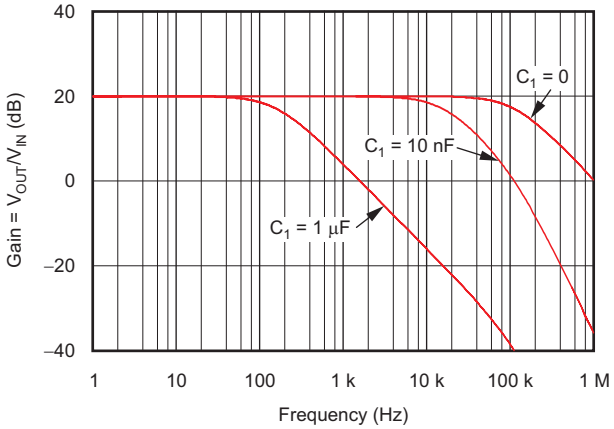


Figure 28. OPA348 Single-Pole AC Gain vs Frequency Response

If even more attenuation is required, a multiple pole filter is required. The Sallen-Key filter may be used for this task, as shown in Figure 29. For best results, the amplifier must have effective bandwidth that is at least 10 times higher than the filter cutoff frequency. Failure to follow this guideline results in a phase shift of the amplifier, which in turn leads to lower precision of the filter bandwidth. Additionally, in order to minimize the loading effect between multiple RC pairs on overall the filter cutoff frequency, choose R = 10 × R_1 and C_2 = C1/10; see Figure 29.

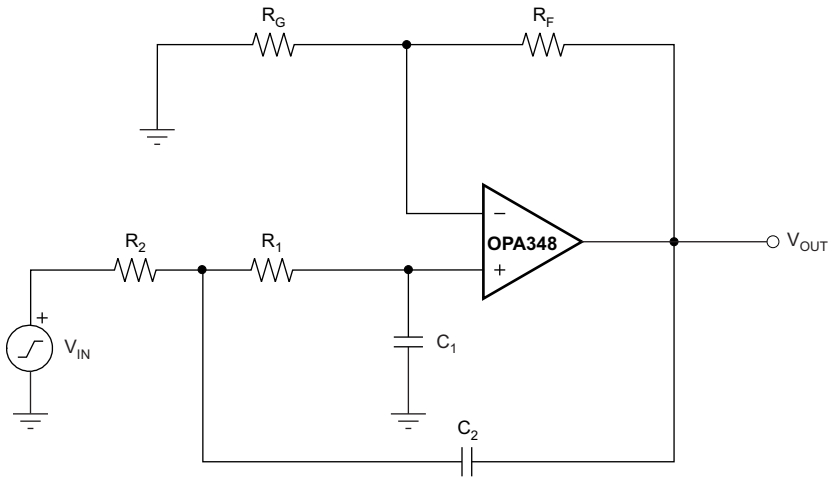


Figure 29. Two-Pole, Low-Pass Sallen-Key Filter

Typical Application (continued)

Equation 3, Equation 4, and Equation 5 show the relationships for low-pass cutoff frequency, filter transfer function, and low frequency gain, and the surrounding passive elements.

$$f_C = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} \tag{3}$$

$$\frac{V_{OUT(s)}}{V_{IN(s)}} = \frac{G(2\pi f_c)^2}{s^2 + 2\zeta(2\pi f_c)s + (2\pi f_c)^2} \tag{4}$$

$$G = \frac{R_G + R_F}{R_G} \tag{5}$$

Use these design values:

- C_1 = 10 nF and C_2 = 1 nF
- R_1 = 1 kΩ and R_2= 10 kΩ
- R_G = 10 kΩ
- R_F = 90 kΩ

Figure 30 shows the Sallen-Key filter second-order response for different RC values: for R and C values above, $f_C = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} = \frac{1}{2\pi\sqrt{1^3 \times 1^{-8} \times 1^4 \times 1^{-9}}}$ = 15.9 kHz.

To further limit the bandwidth, a larger RC value must be used: increasing C values 100 times, such as C_1 = 1 µF and C_2 = 0.1 µF, with unchanged resistors, results in the second-order roll-off at $f_C = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} = \frac{1}{2\pi\sqrt{1^3 \times 1^{-6} \times 1^4 \times 1^{-7}}}$ = 159 Hz. Refer to Figure 30.

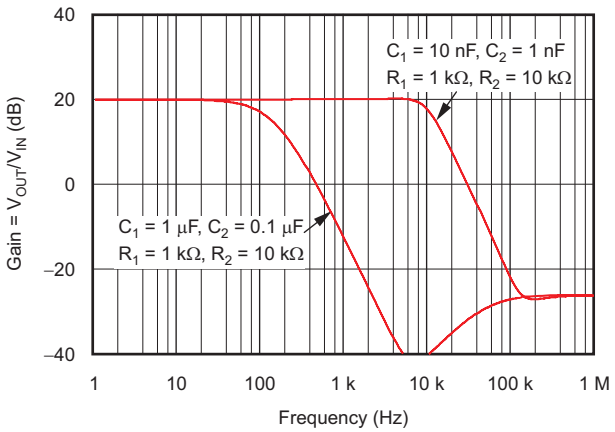


Figure 30. OPA348 Two-Pole, Low-Pass Sallen-Key AC Gain vs Frequency Response

9 Power Supply Recommendations

The OPAx348 is specified for operation from 2.1 V to 5.5 V (±1.05 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 5.5 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Connect low equivalent series resistance (ESR), 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 31, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

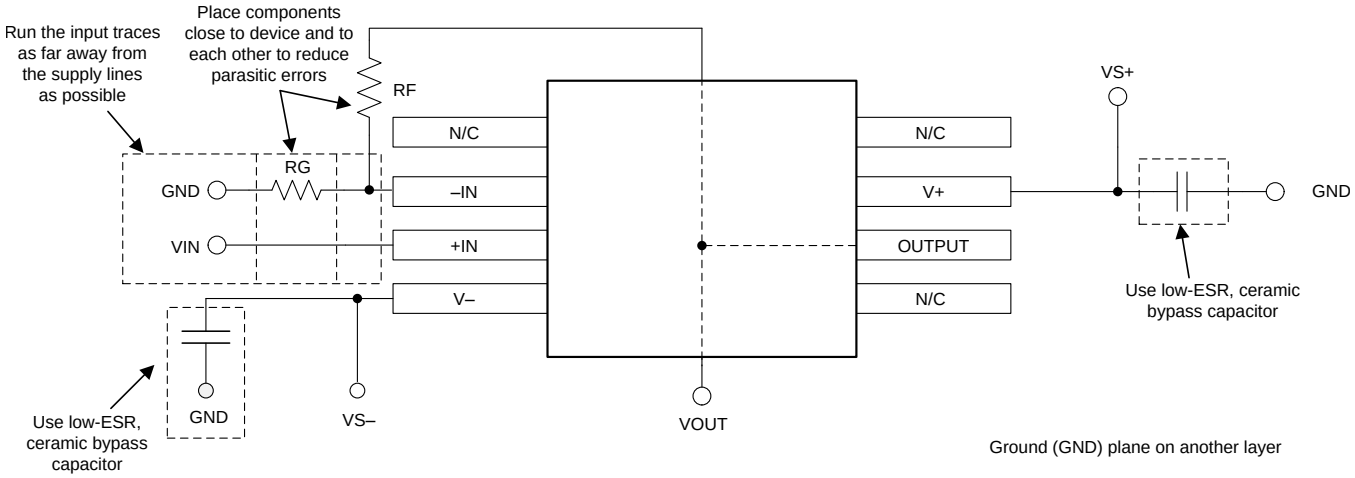


Figure 31. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount devices. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Op Amp EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of device package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own devices. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPAx348, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- *Hardware Pace Using Slope Detection* (SLAU511).
- *Mobile Phone Bank Card Reader Application Report* (TIDU399).
- *TPS61040 Inverter Design* (SLVA008).
- *Op Amp Performance Analysis* (SBOA054).
- *Single-Supply Operation of Operational Amplifiers* (SBOA059).
- *Tuning in Amplifiers* (SBOA067).

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA348	Click here	Click here	Click here	Click here	Click here
OPA2348	Click here	Click here	Click here	Click here	Click here
OPA4348	Click here	Click here	Click here	Click here	Click here

11.5 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.7 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.9 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2348AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2348A	Samples
OPA2348AIDCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B48	Samples
OPA2348AIDCNRG4	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B48	Samples
OPA2348AIDCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B48	Samples
OPA2348AIDCNTG4	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B48	Samples
OPA2348AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2348A	Samples
OPA2348AIDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OUTQ	Samples
OPA2348AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OUTQ	Samples
OPA2348AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2348A	Samples
OPA2348AIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2348A	Samples
OPA348AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 348A	Samples
OPA348AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A48	Samples
OPA348AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A48	Samples
OPA348AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A48	Samples
OPA348AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A48	Samples
OPA348AIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S48	Samples
OPA348AIDCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S48	Samples
OPA348AIDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S48	Samples
OPA348AIDCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S48	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA348AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 348A	Samples
OPA4348AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4348A	Samples
OPA4348AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4348A	Samples
OPA4348AIPWR	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4348A	Samples
OPA4348AIPWRG4	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4348A	Samples
OPA4348AIPWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4348A	Samples
OPA4348AIPWTG4	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4348A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2348, OPA348, OPA4348 :

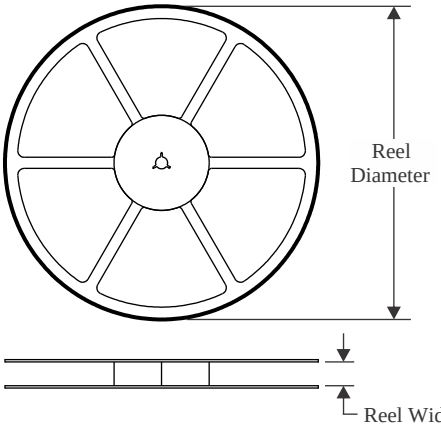
- Automotive : OPA2348-Q1, OPA348-Q1, OPA4348-Q1

NOTE: Qualified Version Definitions:

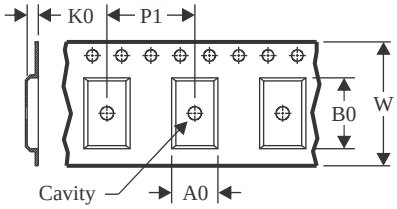
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

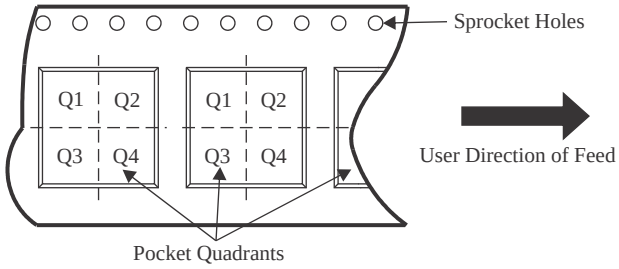


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

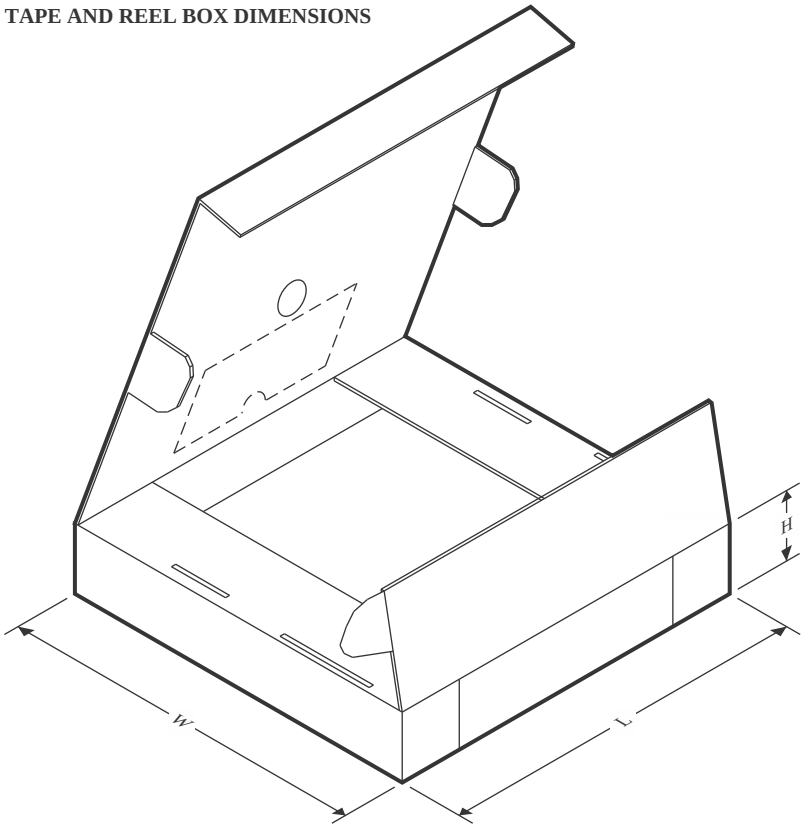
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2348AIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2348AIDCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2348AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2348AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA348AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA348AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA348AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA348AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA348AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA348AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA348AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4348AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4348AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4348AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

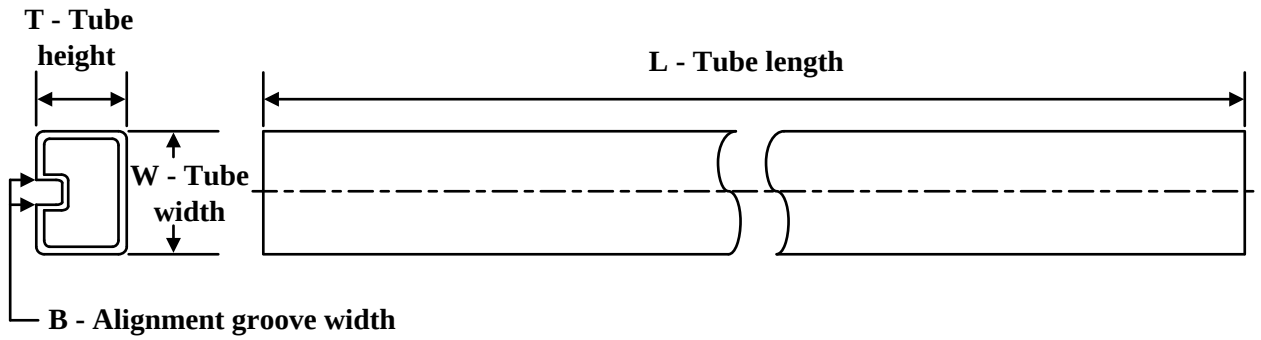
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

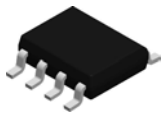
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2348AIDCNR	SOT-23	DCN	8	3000	200.0	183.0	25.0
OPA2348AIDCNT	SOT-23	DCN	8	250	200.0	183.0	25.0
OPA2348AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2348AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA348AIDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA348AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA348AIDBVT	SOT-23	DBV	5	250	445.0	220.0	345.0
OPA348AIDBVT	SOT-23	DBV	5	250	195.0	200.0	45.0
OPA348AIDCKR	SC70	DCK	5	3000	200.0	183.0	25.0
OPA348AIDCKT	SC70	DCK	5	250	200.0	183.0	25.0
OPA348AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4348AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4348AIPWR	TSSOP	PW	14	2500	356.0	356.0	35.0
OPA4348AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2348AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2348AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2348AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA348AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4348AID	D	SOIC	14	50	506.6	8	3940	4.32

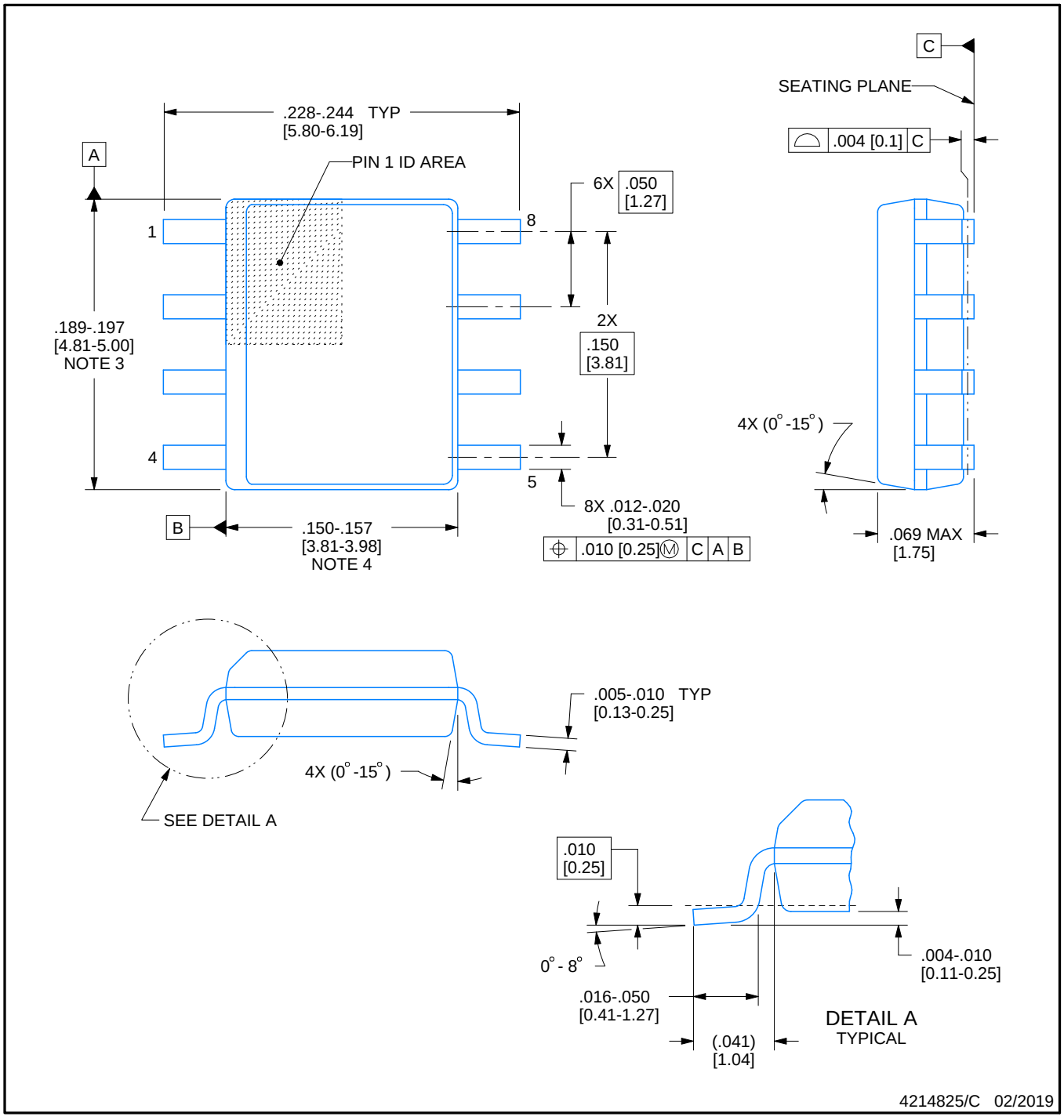


PACKAGE OUTLINE

D0008A

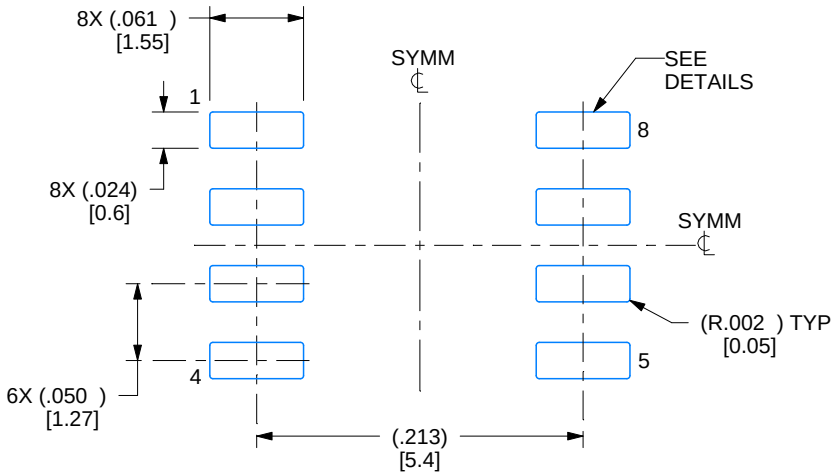
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

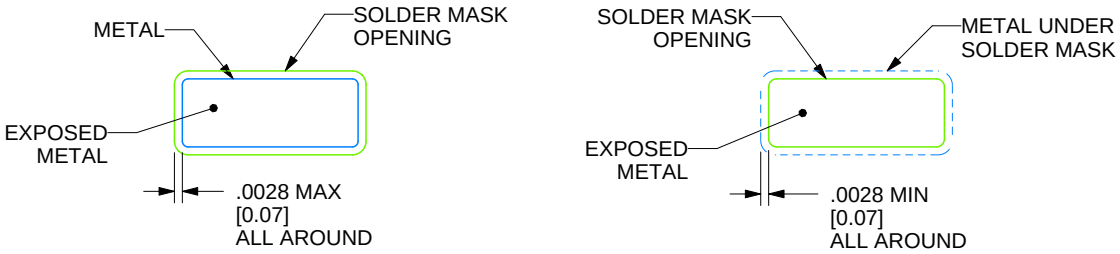


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

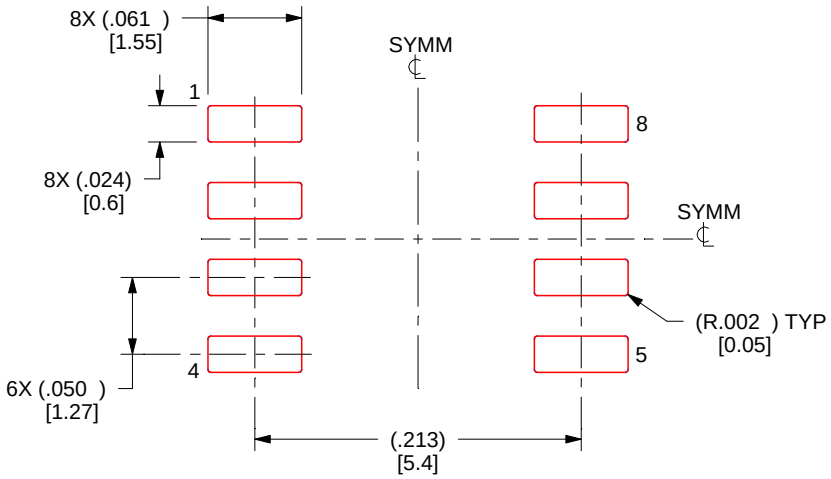
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

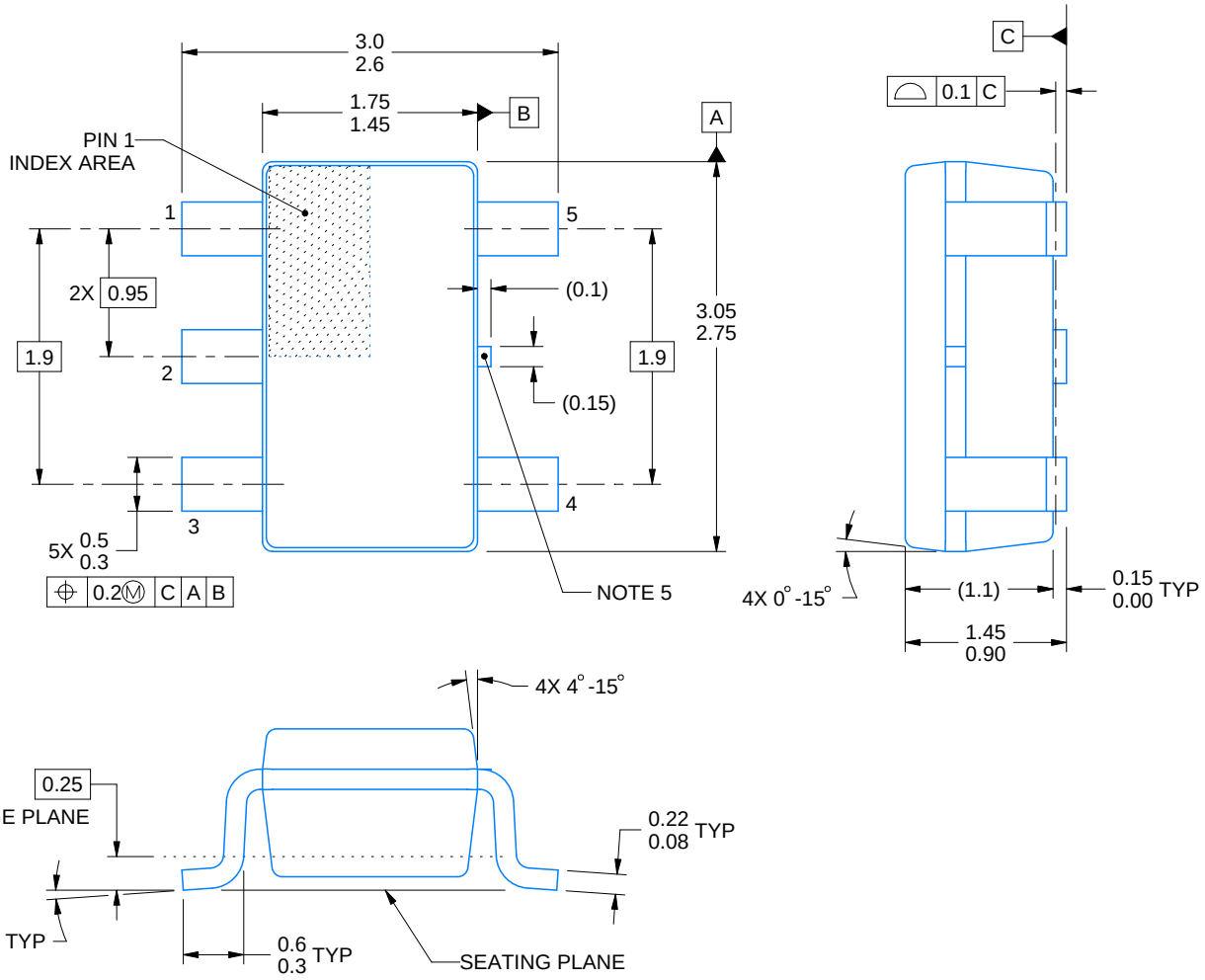
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

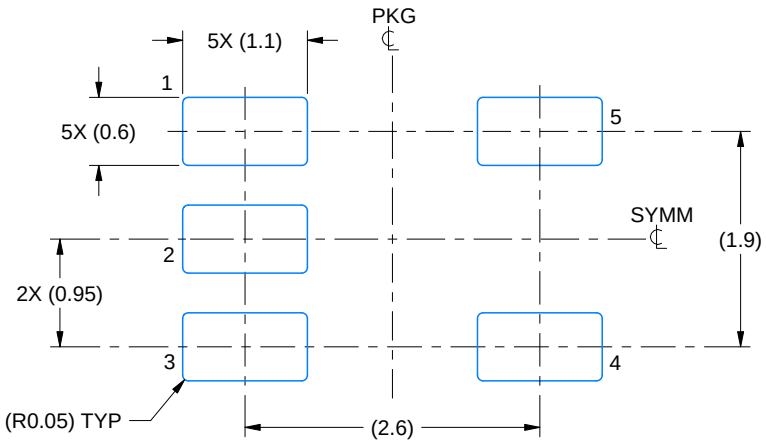
SMALL OUTLINE TRANSISTOR



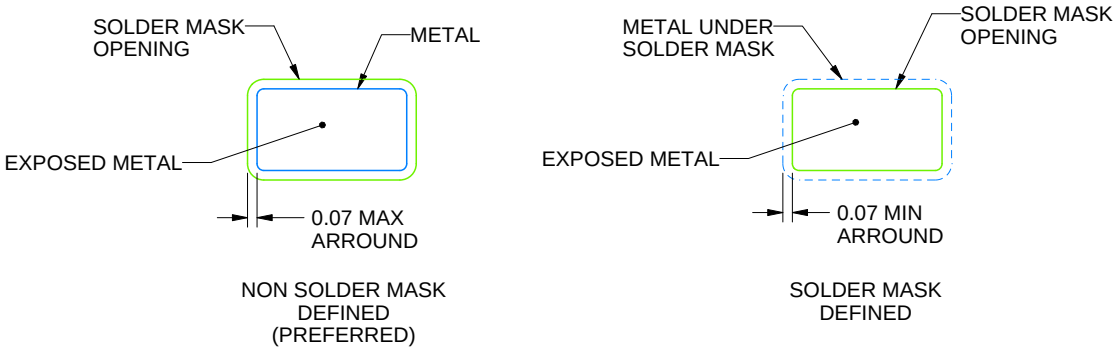
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

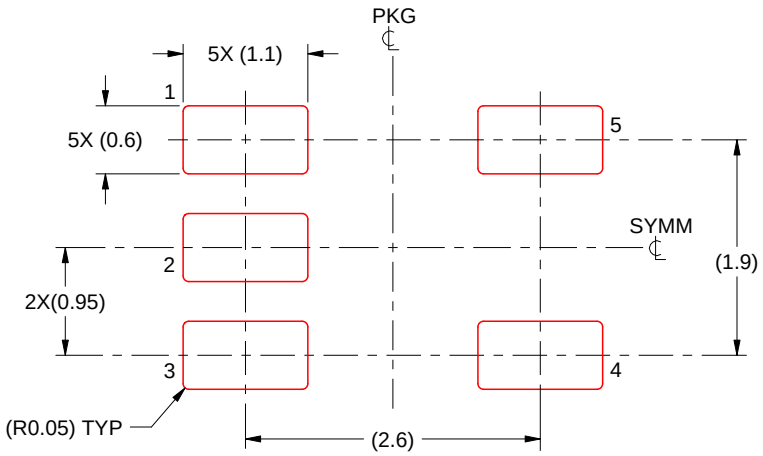


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

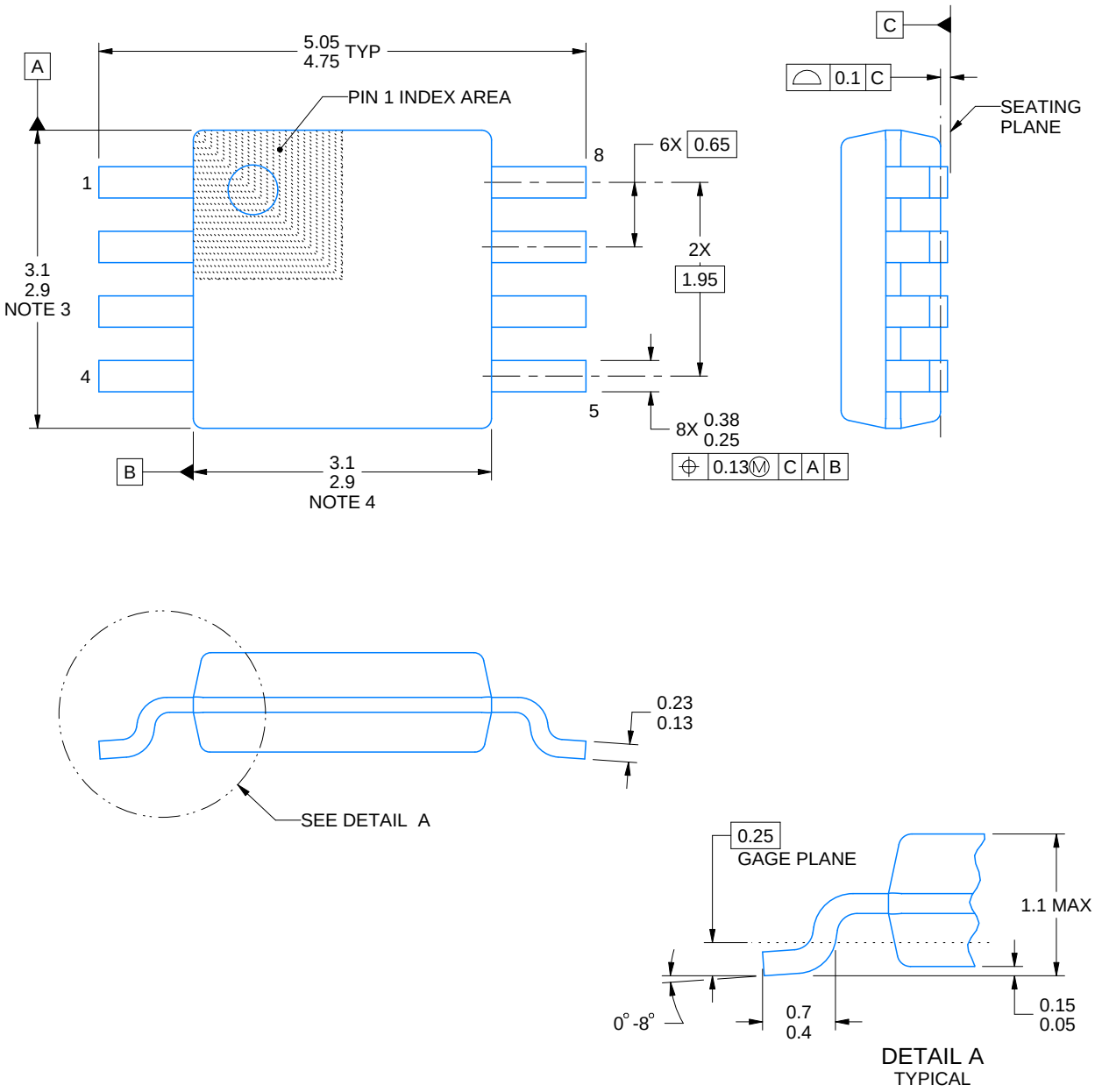
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

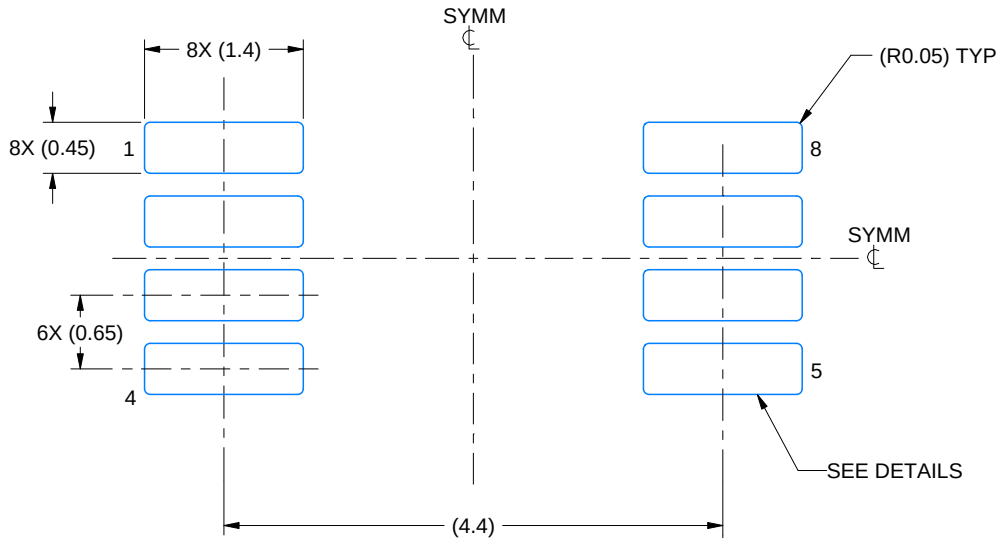
SMALL OUTLINE PACKAGE



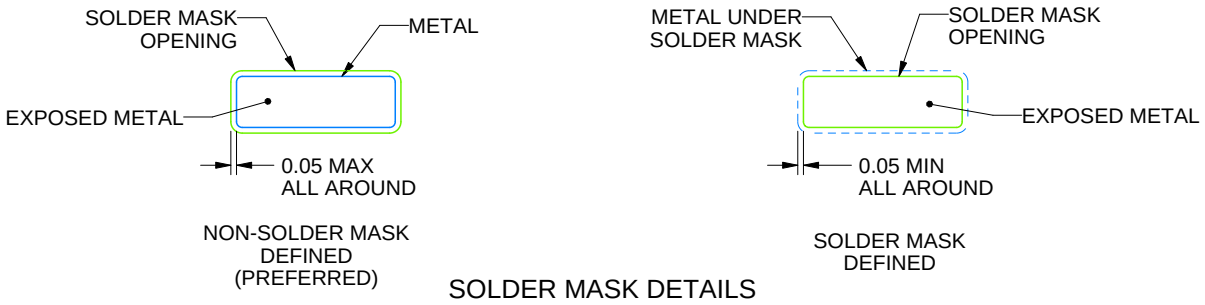
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

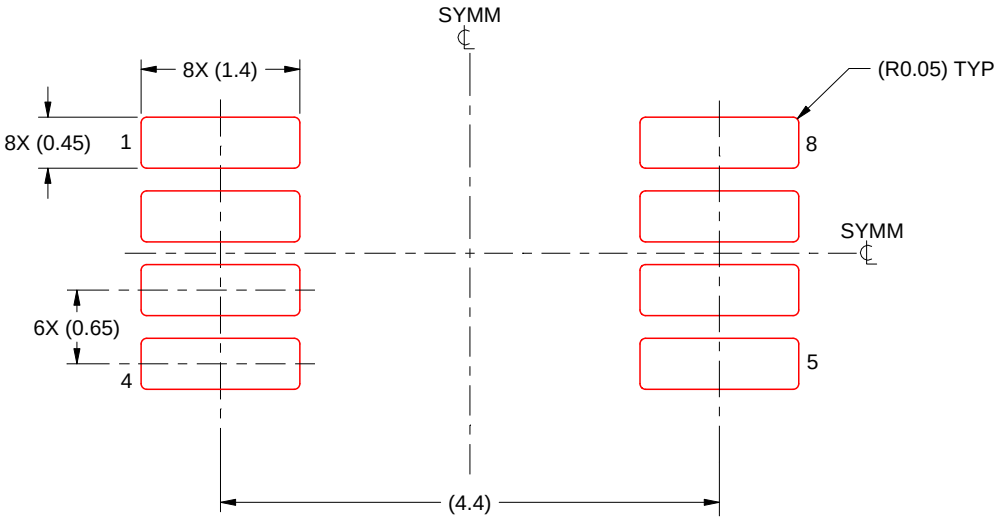


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

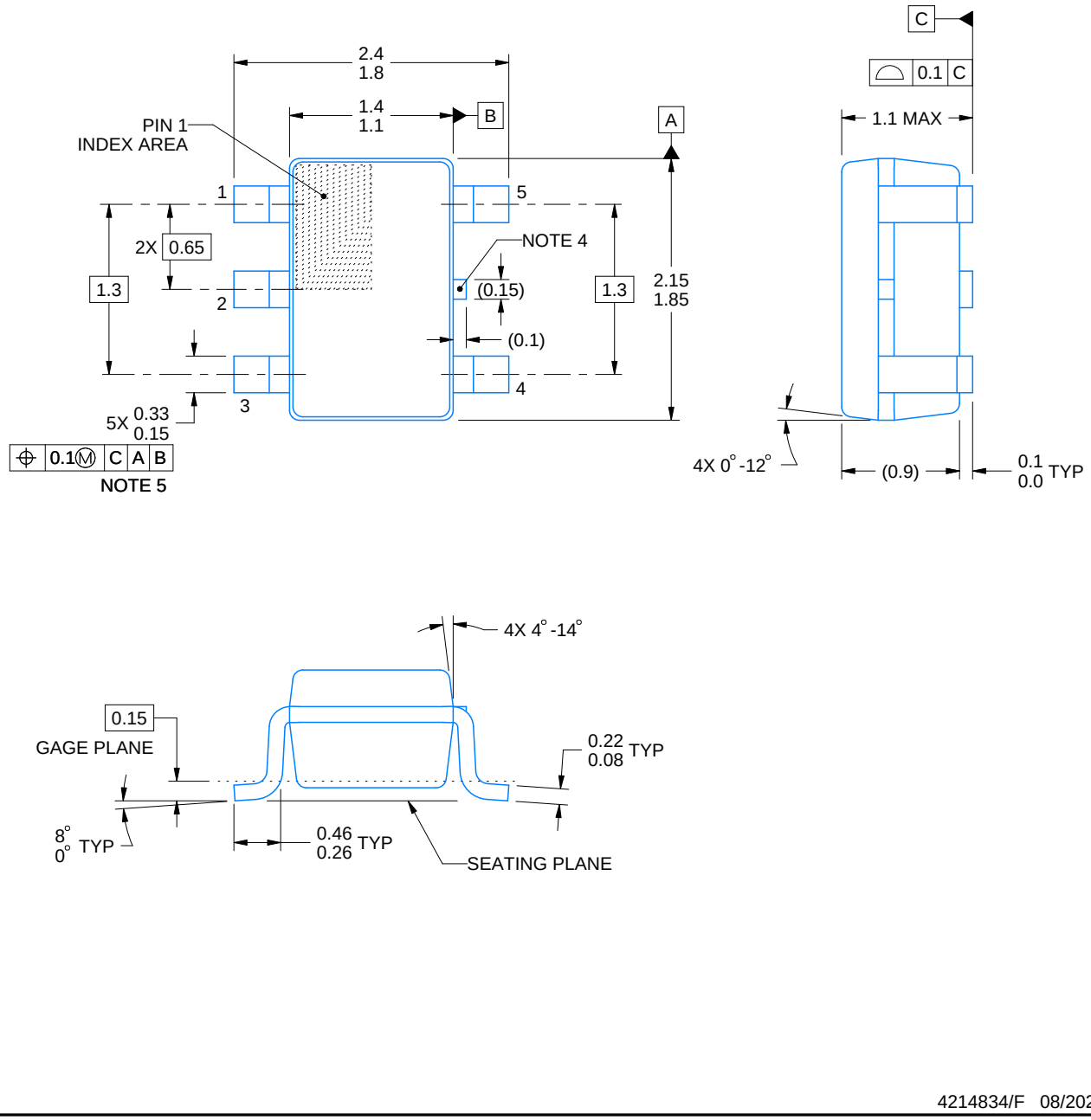
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

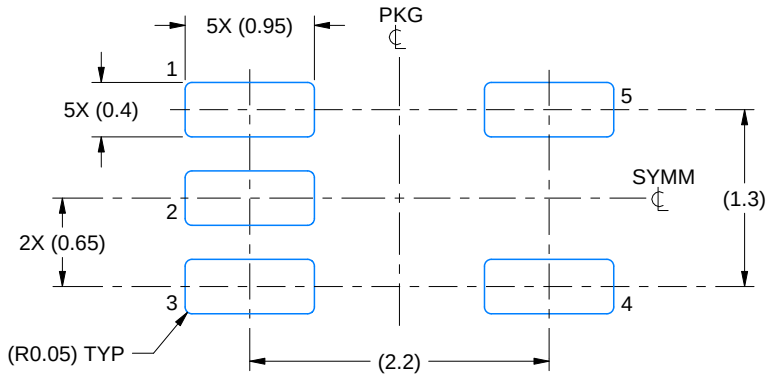
SMALL OUTLINE TRANSISTOR



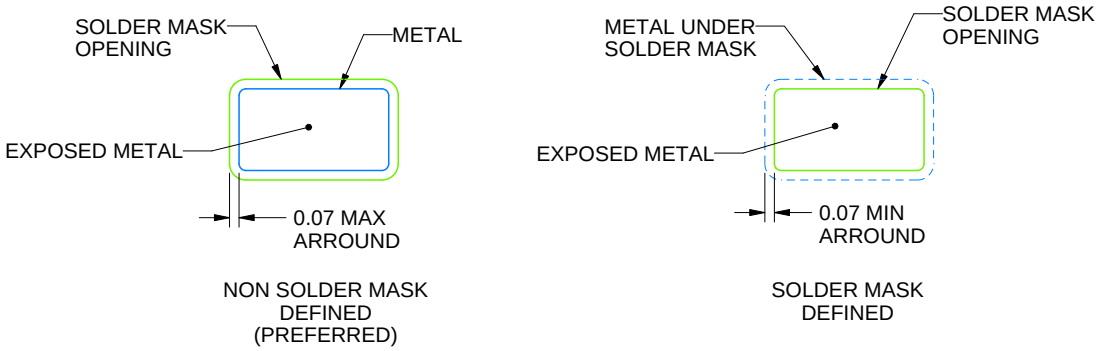
4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

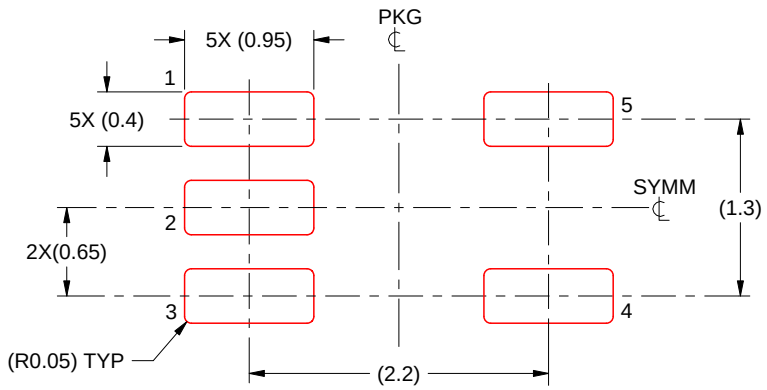


SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

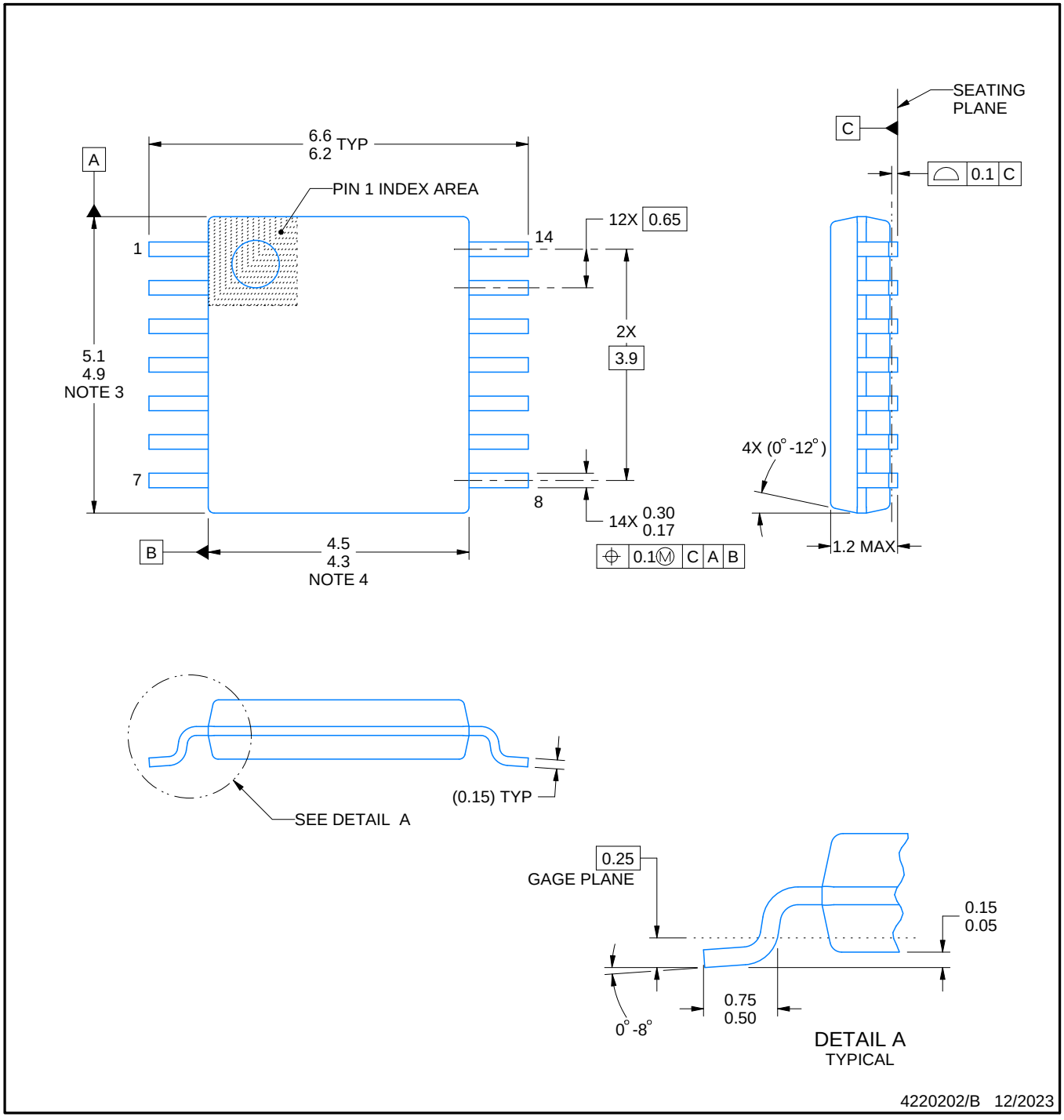
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

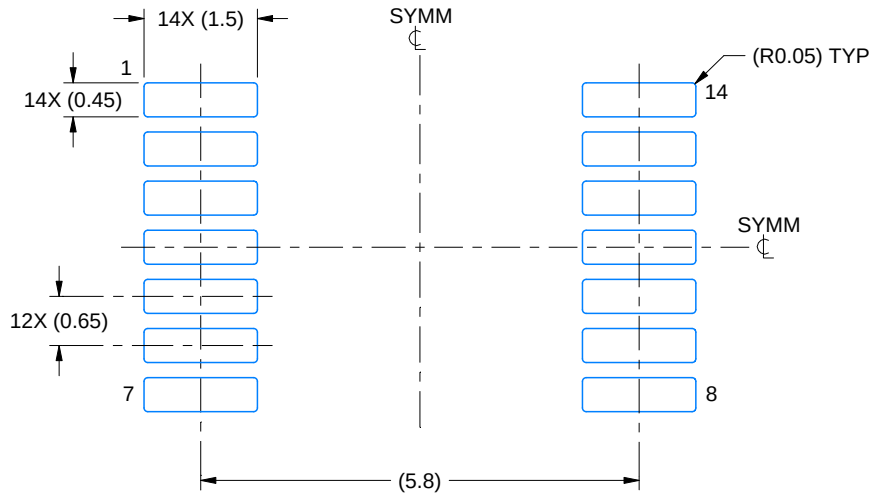
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

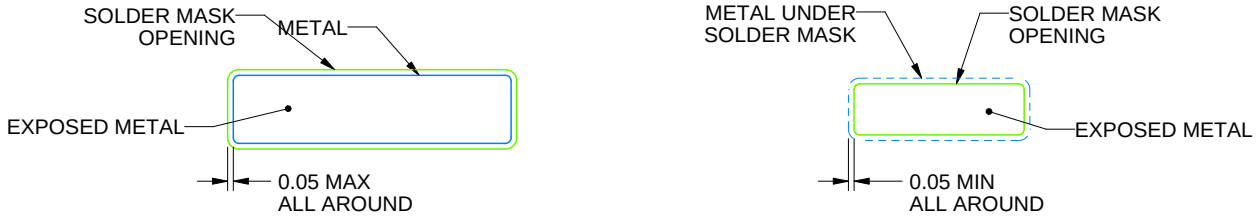


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

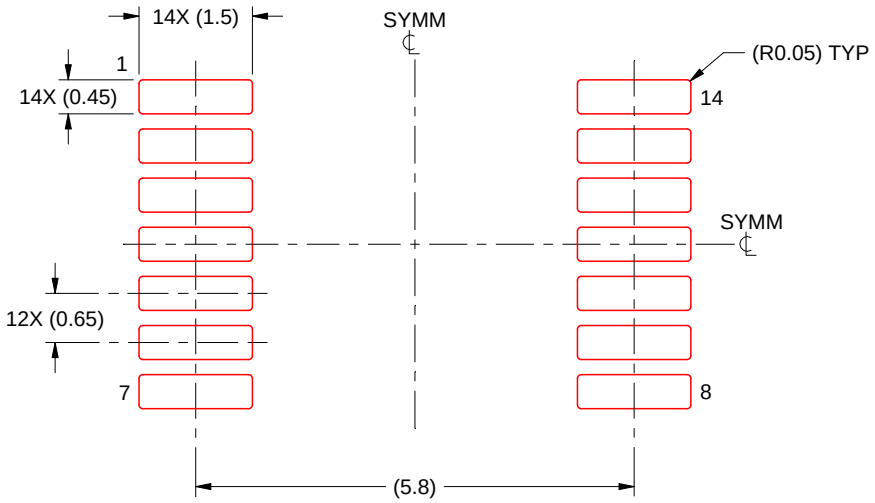


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



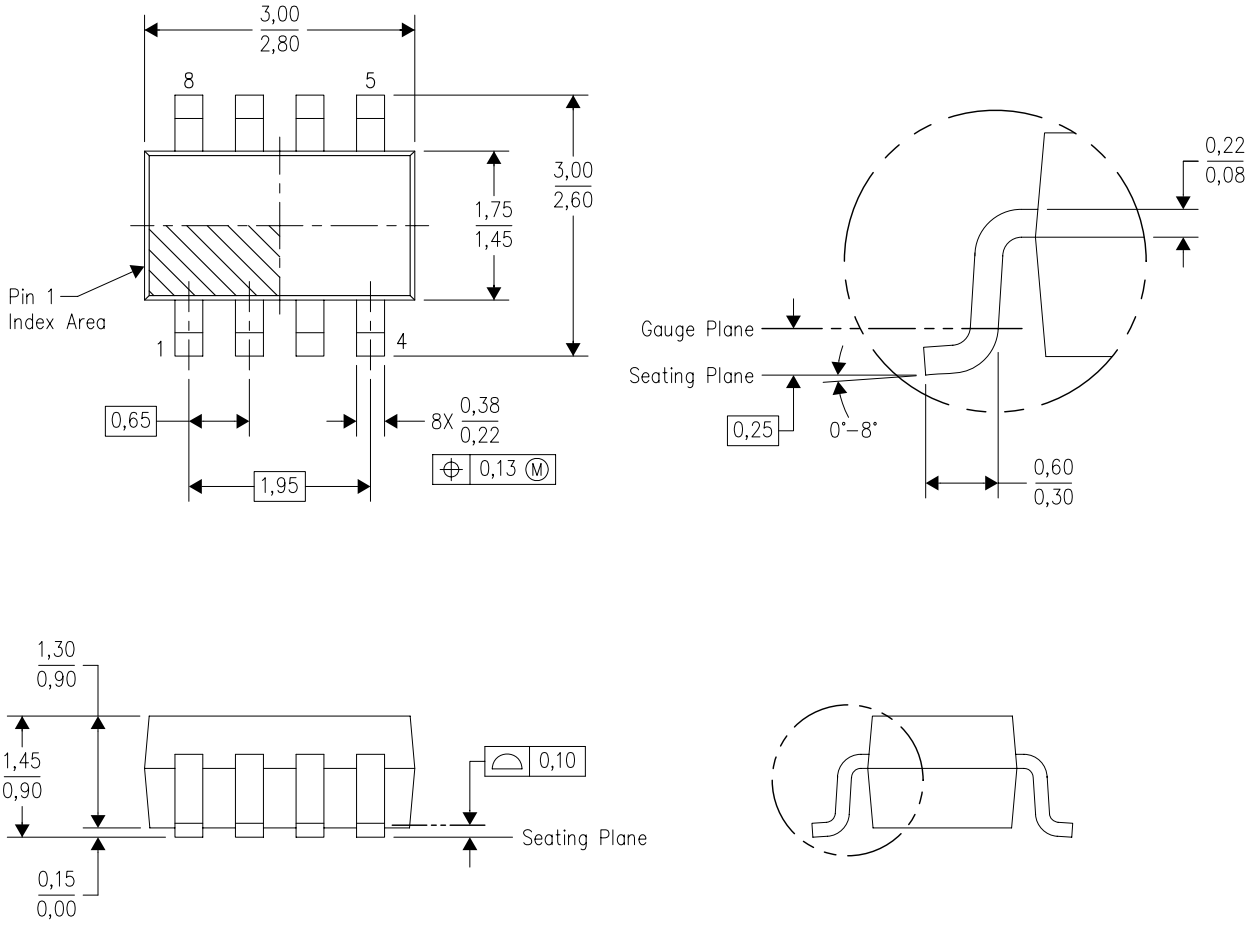
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

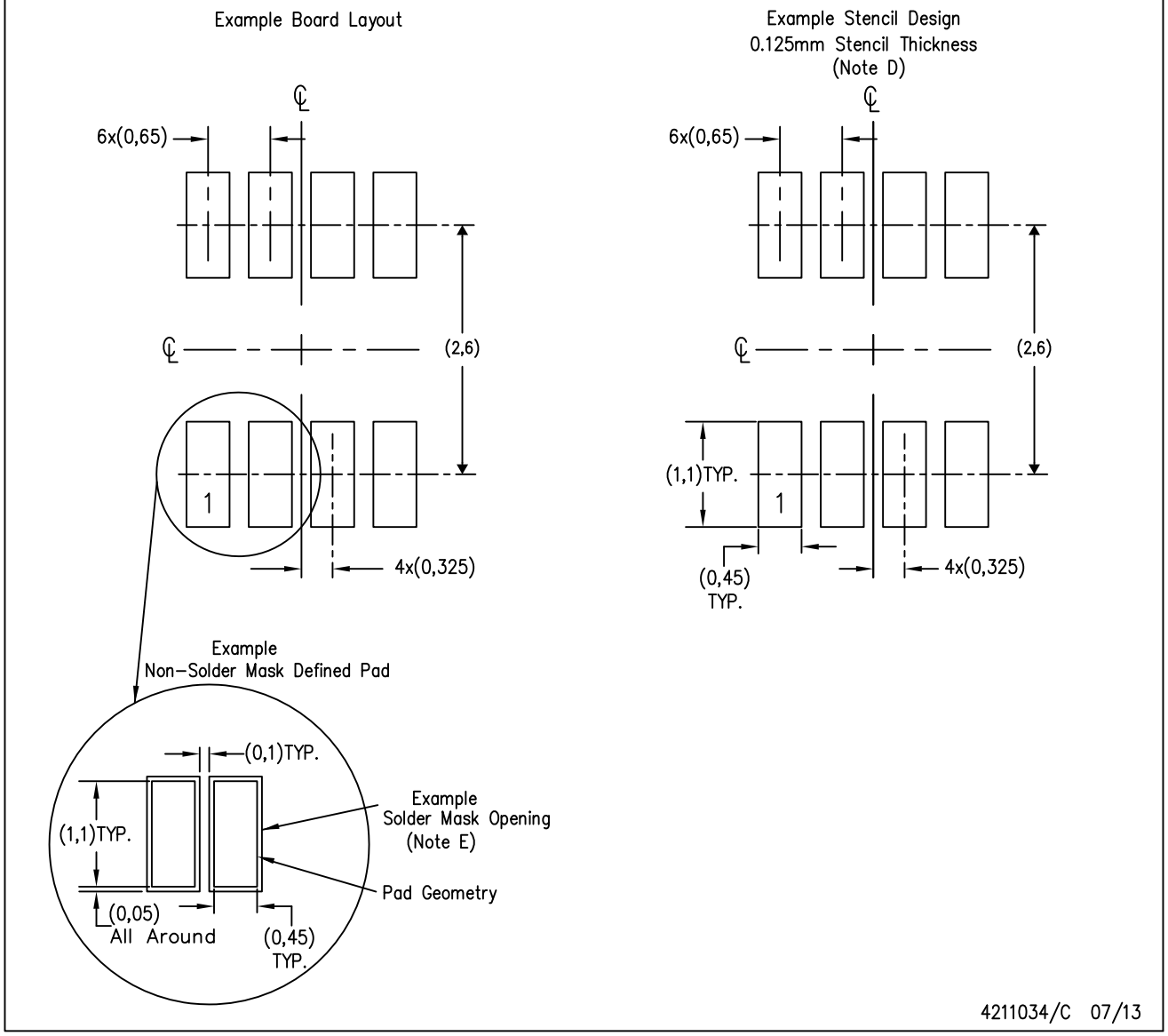
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)

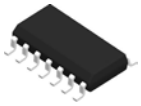


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

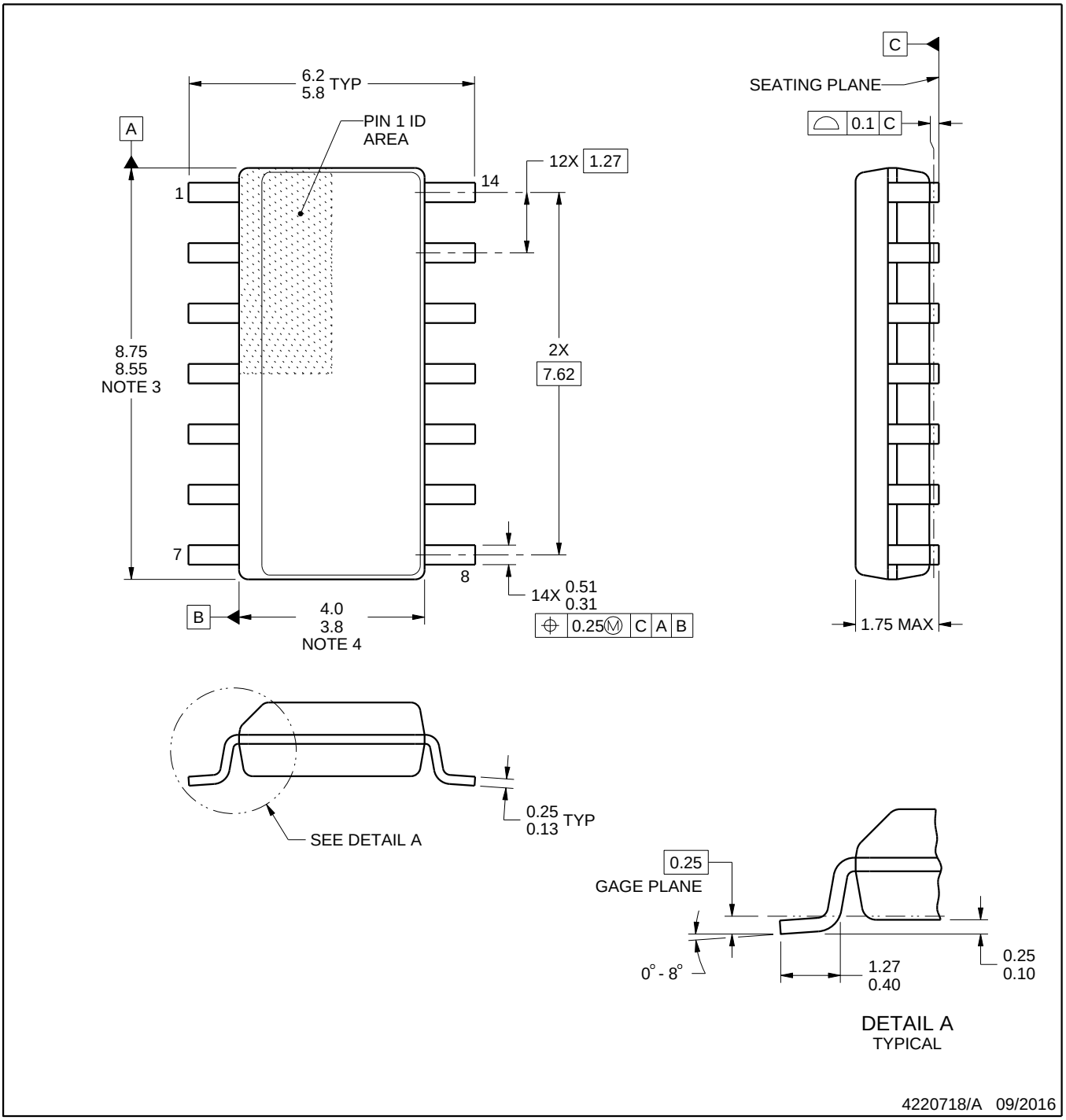


PACKAGE OUTLINE

D0014A

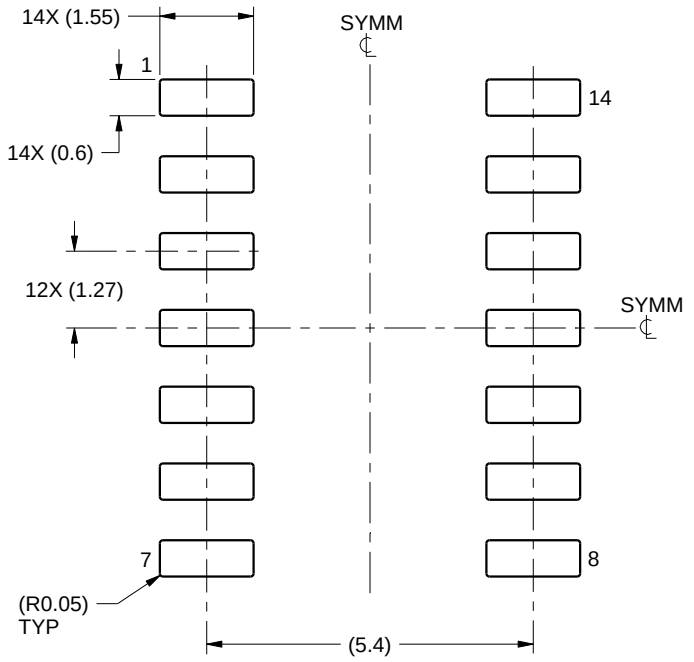
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

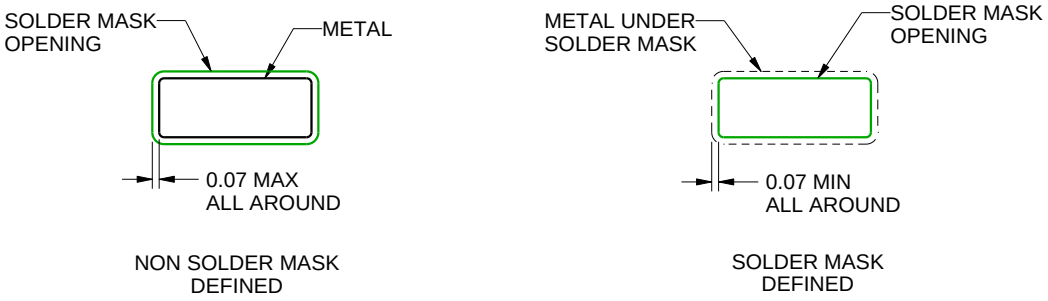


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

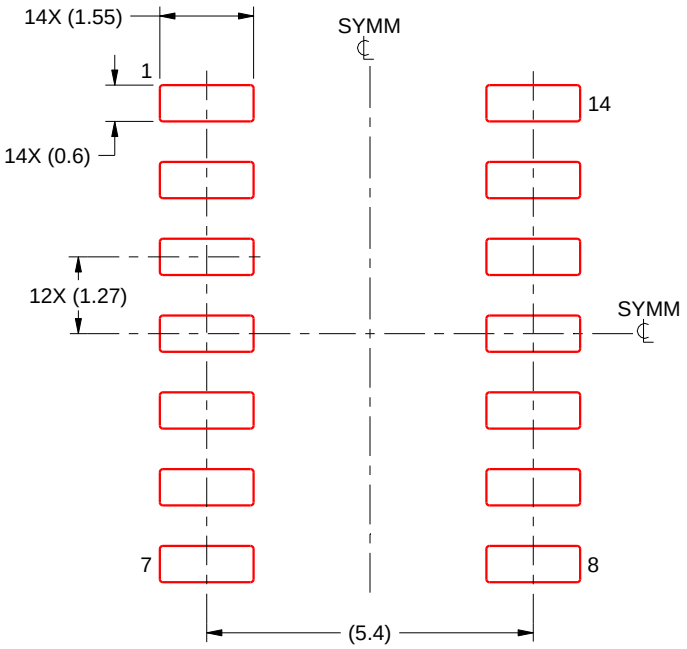
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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