OPA349
OPA2349

SBOS121B – JUNE 2000 – REVISED JANUARY 2004

1μA, Rail-to-Rail I/O CMOS OPERATIONAL AMPLIFIERS

FEATURES

- **LOW SUPPLY CURRENT: 1μA**
- **GAIN-BANDWIDTH: 70kHz**
- **UNITY-GAIN STABLE**
- **LOW INPUT BIAS CURRENT: 10pA (max)**
- **WIDE SUPPLY RANGE: 1.8V to 5.5V**
- **INPUT RANGE: 200mV Beyond Rails**
- **OUTPUT SWINGS TO 350mV OF RAILS**
- **OUTPUT DRIVE CURRENT: 8mA**
- **OPEN-LOOP GAIN: 90dB**
- ***Micro*PACKAGES: SC70, SOT23-5, SOT23-8**

APPLICATIONS

- **BATTERY PACKS AND POWER SUPPLIES**
- **PORTABLE PHONES, PAGERS, AND CAMERAS**
- **SOLAR-POWERED SYSTEMS**
- **SMOKE, GAS, AND FIRE DETECTION SYSTEMS**
- **REMOTE SENSORS**
- **PCMCIA CARDS**
- **DRIVING ANALOG-TO-DIGITAL (A/D) CONVERTERS**
- ***Micro*POWER FILTERS**

OPAx349 RELATED PRODUCTS

FEATURES	PRODUCT
1μA, 5.5kHz, Rail-To-Rail	TLV240x
1μA, 5.5kHz, Rail-To-Rail	TLV224x
7μA, 160kHz, Rail-To-Rail, 2.7V to 16V Supply	TLV238x
7μA, 160kHz, Rail-To-Rail, Micro Power	TLV27Lx
20μA, 500kHz, Rail-To-Rail, 1.8V Micro Power	TLV276x
20μA, 350kHz, Rail-To-Rail, Micro Power	OPAx347
45μA, 1MHz, Rail-To-Rail, 2.1V to 5.5V Supply	OPAx348

DESCRIPTION

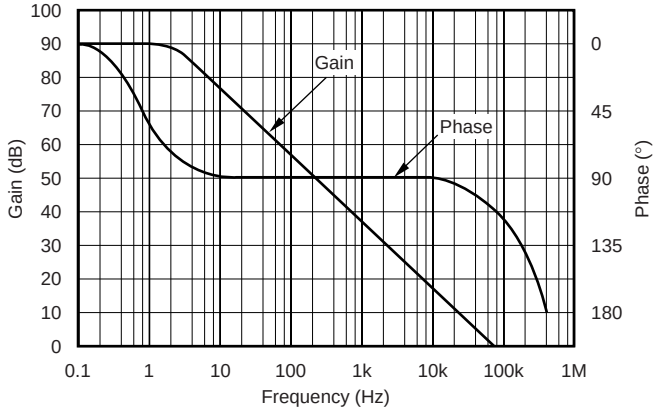
The OPA349 and OPA2349 are ultra-low power operational amplifiers that provide 70kHz bandwidth with only 1μA quiescent current. These rail-to-rail input and output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends 200mV beyond the power-supply rails and the output swings to within 350mV of the rails, maintaining wide dynamic range. Unlike some micropower op amps, these parts are unity-gain stable and require no external compensation to achieve wide bandwidth. The OPA349 features a low input bias current that allows the use of large source and feedback resistors.

The OPA349 can be operated with power supplies from 1.8V to 5.5V with little change in performance, ensuring continuing superior performance even in low battery situations.

The OPA349 comes in miniature SOT23-5, SC70, and SO-8 surface-mount packages. The OPA2349 dual is available in SOT23-8, and SO-8 surface-mount packages. These tiny packages are ideal for use in high-density applications, such as PCMCIA cards, battery packs, and portable instruments.

The OPA349 is specified for 0°C to +70°C. The OPA2349 is specified for –40°C to +70°C.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	5.5V
Signal Input Terminals, Voltage[2]	(V–) – 0.5V to (V+) + 0.5V
Current[2]	10mA
Output Short Circuit[3]	Continuous
Operating Temperature, OPA2349	–55°C to +125°C
Operating Temperature, OPA349	0°C to +85°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 3s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these, or any other conditions beyond those specified, is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

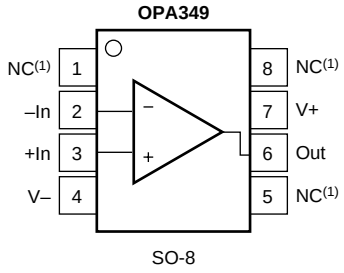
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

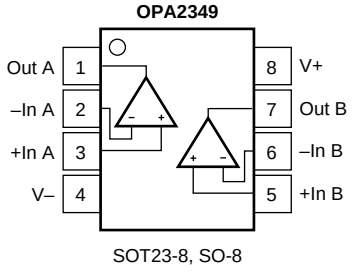
PRODUCT	PACKAGE	PACKAGE DESIGNATOR[1]	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Single					
OPA349NA	SOT23-5	DBV	A49	OPA349NA/250	Tape and Reel, 250
"	"	"	"	OPA349NA/3K	Tape and Reel, 3000
OPA349UA	SO-8	D	OPA349UA	OPA349UA	Rails, 100
"	"	"	"	OPA349UA/2K5	Tape and Reel, 2500
OPA349SA	SC70-5	DCK	S49	OPA349SA/250	Tape and Reel, 250
"	"	"	"	OPA349SA/3K	Tape and Reel, 3000
Dual					
OPA2349EA	SOT23-8	DCN	C49	OPA2349EA/250	Tape and Reel, 250
"	"	"	"	OPA2349EA/3K	Tape and Reel, 3000
OPA2349UA	SO-8	D	OPA2349UA	OPA2349UA	Rails, 100
"	"	"	"	OPA2349UA/2K5	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

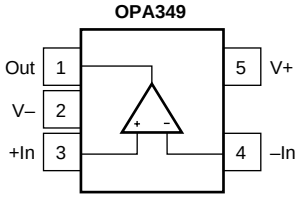
PIN CONFIGURATIONS



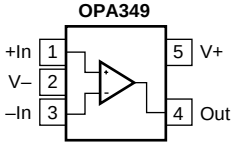
SO-8



SOT23-8, SO-8



SOT23-5



SC70-5

NOTE: (1) NC indicates no internal connection.

ELECTRICAL CHARACTERISTICS (Single): V_S = +1.8V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = 0°C to +70°C.**

At T_A = +25°C, and R_L = 1MΩ connected to V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA349 MIN	OPA349 TYP(1)	OPA349 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V, V_{CM} = 2.5V		±2	±10	mV
Over Temperature				**±2**	**±13**	**mV**
Drift	**dV_{OS}/dT**			**±15**		**µV/°C**
vs Power-Supply Rejection Ratio	PSRR	V_S = 1.8V to 5.5V, V_{CM} = (V–) + 0.3V		350	1000	µV/V
Over Temperature					**3000**	**µV/V**
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.2		(V+) + 0.2	V
Common-Mode Rejection Ratio	CMRR	V_S = +5V, –0.2V < V_{CM} < 5.2V	48	60		dB
Over Temperature			**46**			**dB**
		V_S = +5V, –0.2V < V_{CM} < 3.5V	52	72		dB
Over Temperature			**50**			**dB**
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.5	±10	pA
Input Offset Current	I_{OS}			±1	±10	pA
INPUT IMPEDANCE						
Differential				10^{13} || 2		Ω || pF
Common-Mode				10^{13} || 4		Ω || pF
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz				8		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			300		nV/√Hz
Current Noise Density, f = 1kHz	i_n			4		fA/√Hz
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 1MΩ, V_S = +5.5V, +0.3V < V_O < +5.2V	74	90		dB
Over Temperature			**72**			**dB**
Open-Loop Voltage Gain	A_{OL}	R_L = 10kΩ, V_S = +5.5V, +0.35V < V_O < +5.15V	74	90		dB
Over Temperature			**60**			**dB**
OUTPUT						
Voltage Output Swing from Rail		R_L = 1MΩ, V_S = +5.5V, A_{OL} > 74dB			300	mV
Over Temperature					**300**	**mV**
		R_L = 10kΩ, V_S = +5.5V, A_{OL} > 74dB			350	mV
Over Temperature					**350**	**mV**
Output Current				±8		mA
Short-Circuit Current	I_{SC}			±10		mA
Capacitive Load Drive	C_{LOAD}	See Typical Characteristics				
FREQUENCY RESPONSE		C_L = 10pF				
Gain-Bandwidth Product	GBW	G = +1		70		kHz
Slew Rate	SR	V_S = +5V, G = +1		0.02		V/µs
Settling Time, 0.1%	t_S	V_S = 5V, 1V Step		65		µs
0.01%		V_S = 5V, 1V Step		80		µs
Overload Recovery Time		V_{IN} • Gain = V_S		5		µs
POWER SUPPLY						
Specified Voltage Range	V_S		+1.8		+5.5	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		1	2	µA
Over Temperature					**10**	**µA**
TEMPERATURE RANGE						
Specified Range			0		+70	°C
Operating Range			0		+85	°C
Storage Range			–65		+150	°C
Thermal Resistance	θ_{JA}					
SOT23-5 Surface-Mount				200		°C/W
SO-8 Surface-Mount				150		°C/W
SC70-5 Surface-Mount				250		°C/W

NOTE: (1) Refer to Typical Characteristic curves.

ELECTRICAL CHARACTERISTICS (Dual): V_S = +1.8V to +5.5V

Boldface limits apply over the specified temperature range, T_A = –40°C to +70°C.

At T_A = +25°C, and R_L = 1MΩ connected to V_S/2, unless otherwise noted.

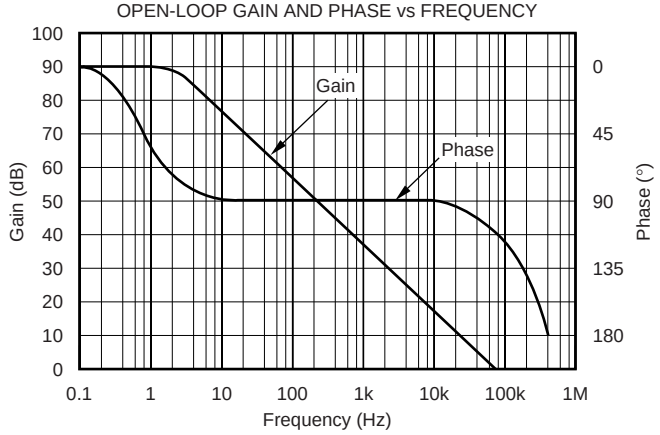
PARAMETER		CONDITION	OPA2349 MIN	OPA2349 TYP(1)	OPA2349 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V, V_{CM} = 2.5V		±2	±10	mV
Over Temperature				**±2**	**±13**	**mV**
Drift	**dV_{OS}/dT**			**±15**		**µV/°C**
vs Power Supply	PSRR	V_S = 1.8V to 5.5V, V_{CM} = (V–) + 0.3V		350	1000	µV/V
Over Temperature					**3000**	**µV/V**
Channel Separation, dc		R_L = 100kΩ		10		µV/V
		f = 1kHz		66(1)		dB
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.2		(V+) + 0.2	V
Common-Mode Rejection Ratio	CMRR	V_S = +5V, –0.2V < V_{CM} < 5.2V	48	60		dB
Over Temperature			**46**			**dB**
		V_S = +5V, –0.2V < V_{CM} < 3.5V	52	72		dB
Over Temperature			**50**			**dB**
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.5	±10	pA
Input Offset Current	I_{OS}			±1	±10	pA
INPUT IMPEDANCE						
Differential				10^{13} || 2		Ω || pF
Common-Mode				10^{13} || 4		Ω || pF
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz				8		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			300		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz	i_n			4		$fA/\sqrt{Hz}$
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 1MΩ, V_S = +5.5V, +0.3V < V_O < +5.2V	74	90		dB
Over Temperature			**72**			**dB**
Open-Loop Voltage Gain	A_{OL}	R_L = 10kΩ, V_S = +5.5V, +0.35V < V_O < +5.15V	74	90		dB
Over Temperature			**60**			**dB**
OUTPUT						
Voltage Output Swing from Rail		R_L = 1MΩ, V_S = +5.5V, A_{OL} > 74dB		150	300	mV
Over Temperature					**300**	**mV**
		R_L = 10kΩ, V_S = +5.5V, A_{OL} > 74dB		200	350	mV
Over Temperature					**350**	**mV**
Output Current				±8		mA
Short-Circuit Current	I_{SC}			±10		mA
FREQUENCY RESPONSE		C_L = 10pF				
Gain-Bandwidth Product	GBW	G = +1		70		kHz
Slew Rate	SR	V_S = +5V, G = +1		0.02		V/µs
Settling Time, 0.1%	t_S	V_S = 5V, 1V Step		65		µs
0.01%		V_S = 5V, 1V Step		80		µs
Overload Recovery Time		V_{IN} • Gain = V_S		5		µs
POWER SUPPLY						
Specified Voltage Range	V_S		+1.8		+5.5	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		1	2	µA
Over Temperature					**10**	**µA**
TEMPERATURE RANGE						
Specified Range			–40		+70	°C
Operating Range			–40		+85	°C
Storage Range			–65		+150	°C
Thermal Resistance	θ_{JA}					
SOT23-8 Surface-Mount				200		°C/W
SO-8 Surface-Mount				150		°C/W

NOTE: (1) Refer to Typical Characteristic curves.

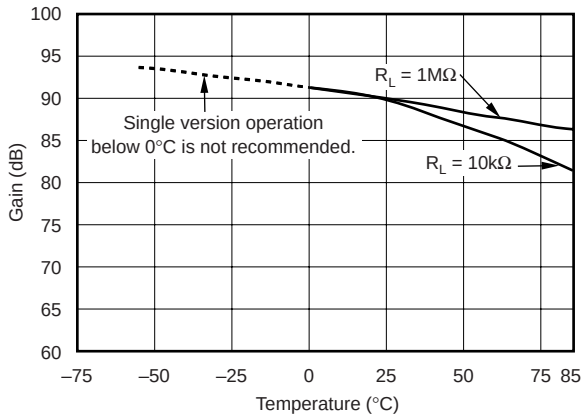
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, and R_L = 1MΩ connected to V_S/2, unless otherwise noted.

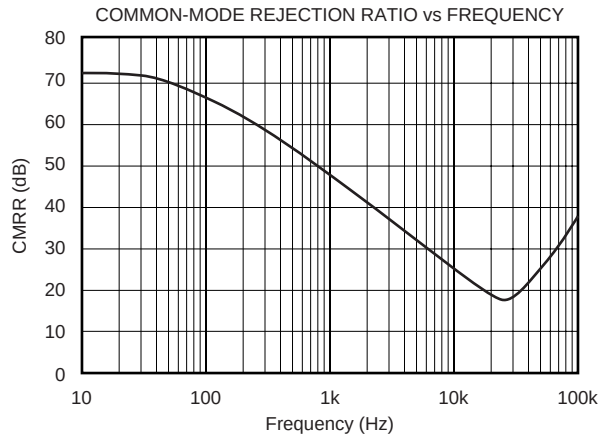
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



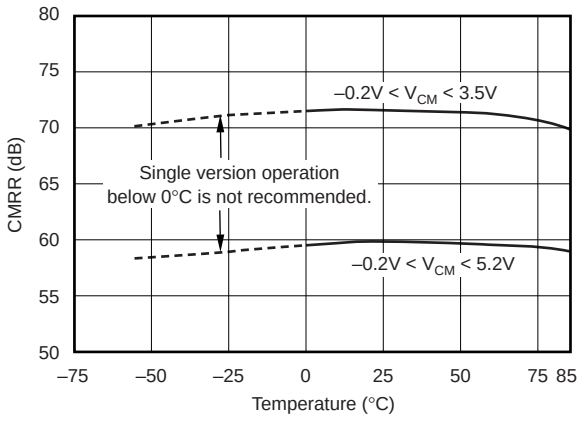
OPEN-LOOP GAIN vs TEMPERATURE



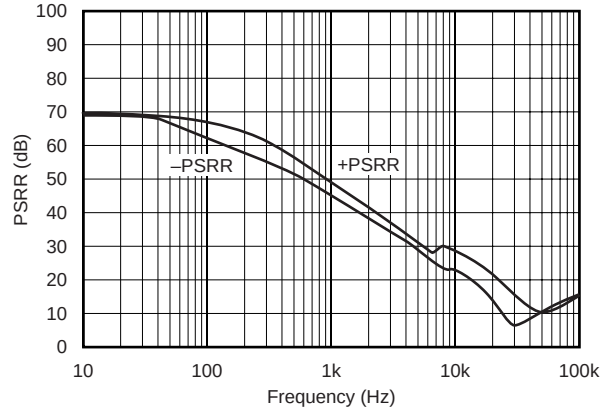
COMMON-MODE REJECTION RATIO vs FREQUENCY



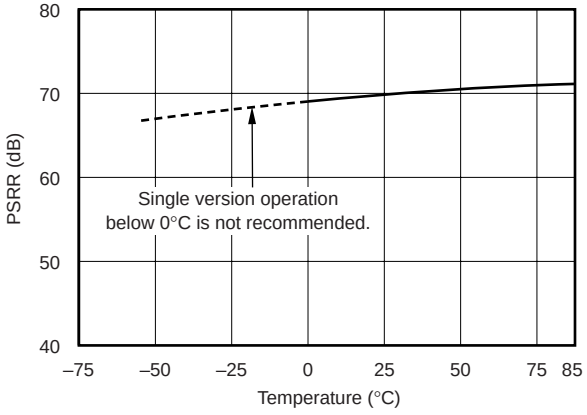
COMMON-MODE REJECTION RATIO
vs TEMPERATURE



POWER-SUPPLY REJECTION RATIO vs FREQUENCY



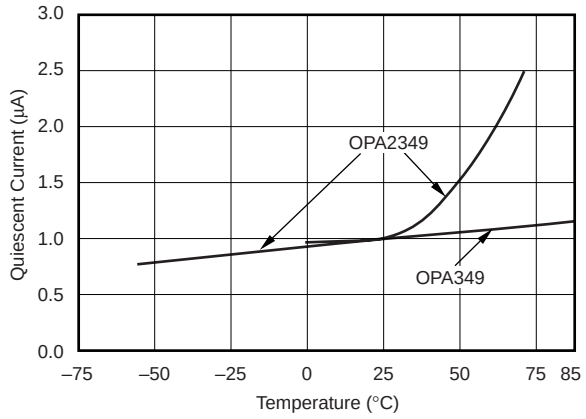
POWER-SUPPLY REJECTION RATIO
vs TEMPERATURE



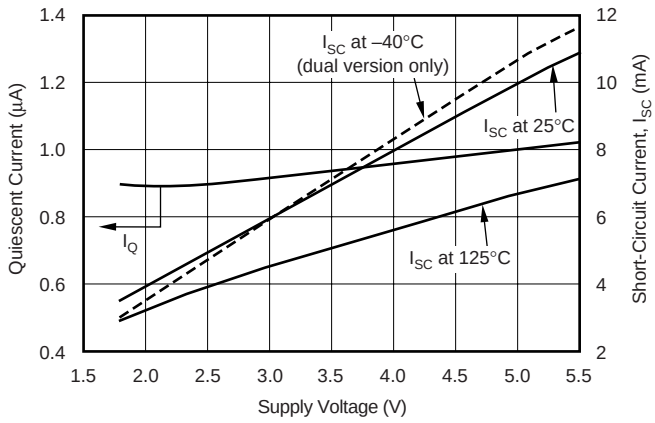
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 1MΩ connected to V_S/2, unless otherwise noted.

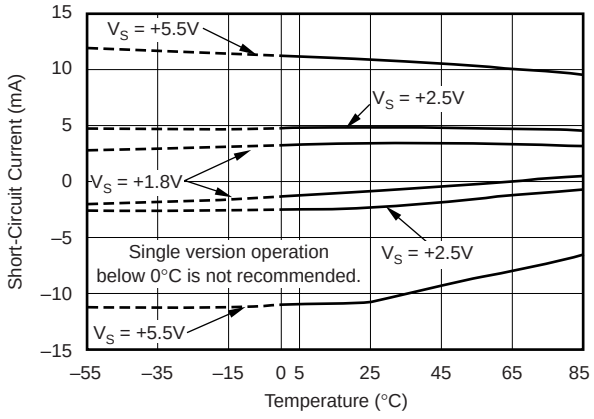
QUIESCENT CURRENT vs TEMPERATURE



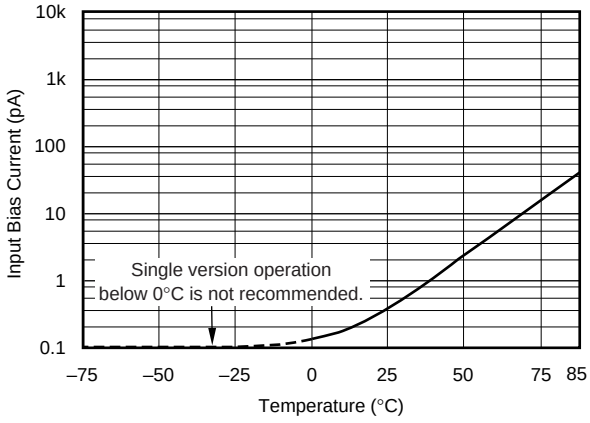
QUIESCENT AND SHORT-CIRCUIT vs SUPPLY VOLTAGE



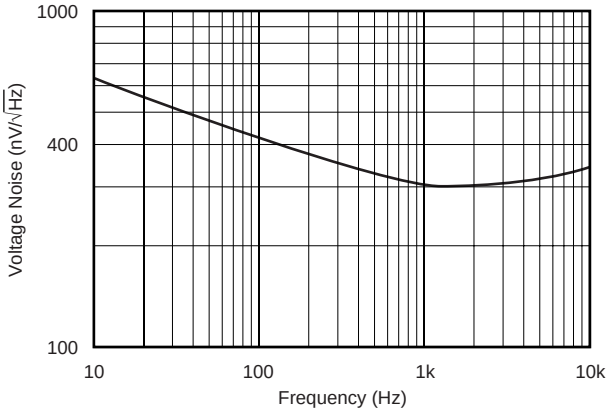
SHORT-CIRCUIT CURRENT vs TEMPERATURE



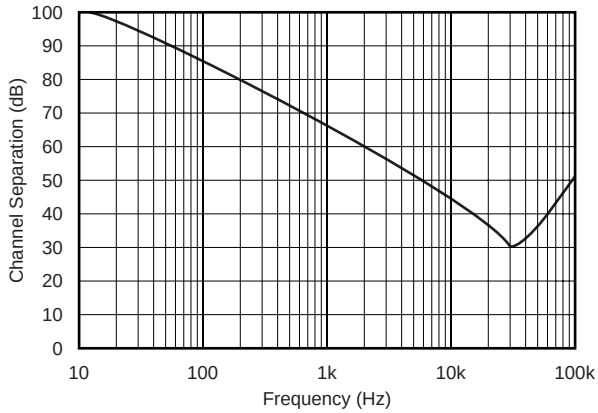
INPUT BIAS CURRENT vs TEMPERATURE



INPUT VOLTAGE NOISE DENSITY



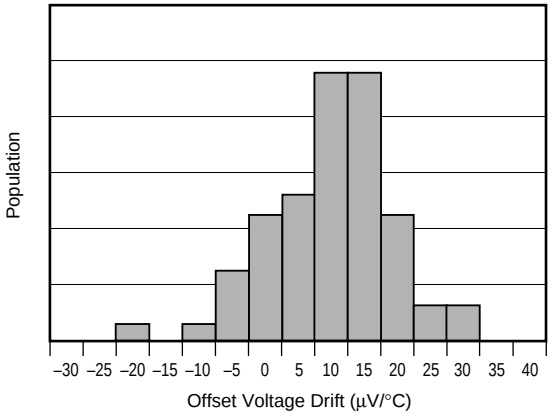
CHANNEL SEPARATION vs FREQUENCY



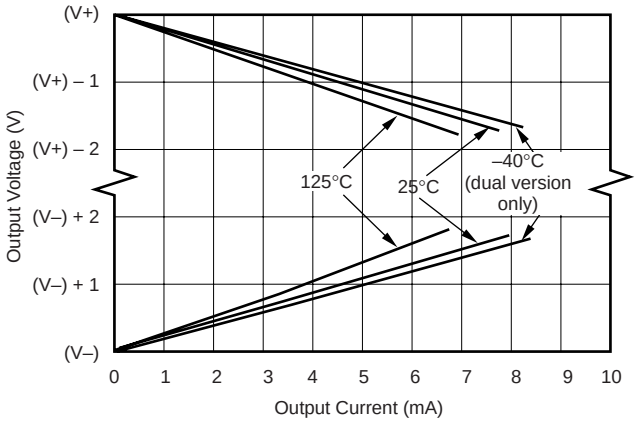
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 1MΩ connected to V_S/2, unless otherwise noted.

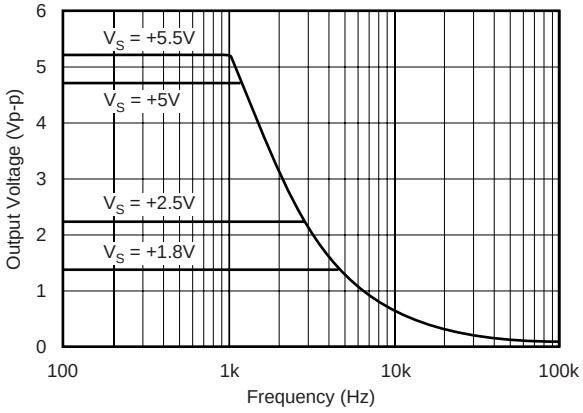
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



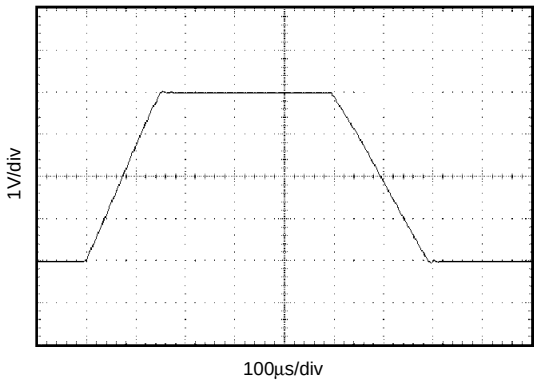
OUTPUT VOLTAGE vs OUTPUT CURRENT



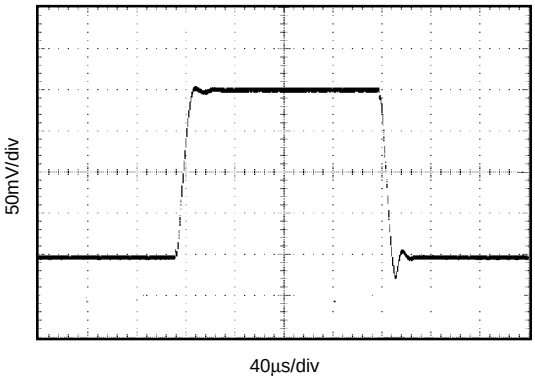
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



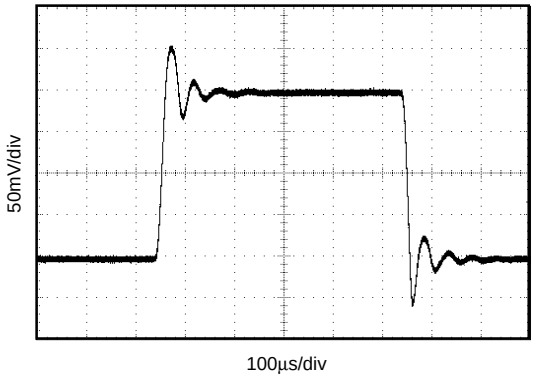
LARGE-SIGNAL STEP RESPONSE
G = 1, R_L = 1MΩ



SMALL-SIGNAL STEP RESPONSE
G = 1, R_L = 1MΩ, C_L = 20pF



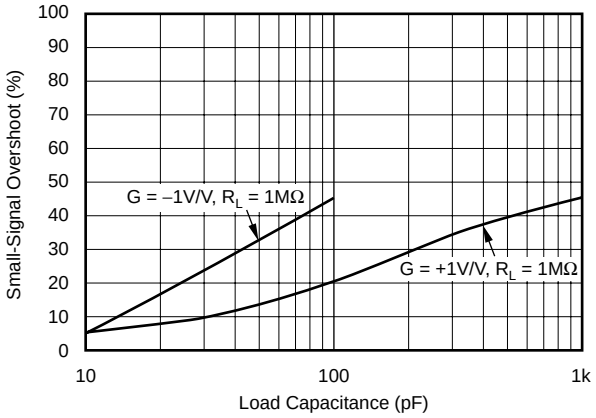
SMALL-SIGNAL STEP RESPONSE
G = 1, R_L = 1MΩ, C_L = 500pF



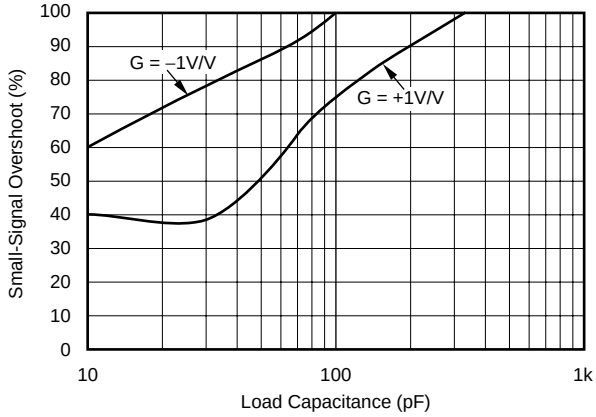
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 1MΩ connected to V_S/2, unless otherwise noted.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE
(SC70)



SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE
(SOT23, SO-8)



APPLICATIONS INFORMATION

The OPA349 series op amps are unity-gain stable and can operate on a single supply, making them highly versatile and easy to use. Power-supply pins should be bypassed with 0.01µF ceramic capacitors.

The OPA349 series op amps are fully specified and tested from +1.8V to +5.5V. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristic curves.

The ultra-low quiescent current of the OPA349 requires careful application circuit techniques to achieve low overall current consumption. Figure 1 shows an ac-coupled amplifier biased with a voltage divider. Resistor values must be very large to minimize current. The large feedback resistor value reacts with input capacitance and stray capacitance to produce a pole in the feedback network. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking. Check circuit performance carefully to assure that biasing and feedback techniques meet signal and quiescent current requirements.

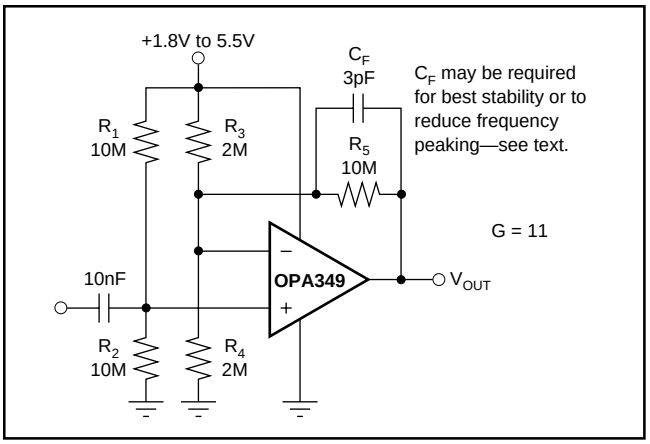


FIGURE 1. AC-Coupled Amplifier.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA349 series extends 200mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair (as shown in Figure 2). The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3V to 200mV above the positive supply, while the P-channel pair is on for inputs from 200mV below the negative supply to approximately (V+) – 1.3V. There is a small transition region, typically (V+) – 1.5V to (V+) – 1.1V, in which both pairs are on. This 400mV transition region can vary 300mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.8V to (V+) – 1.4V on the low end, up to (V+) – 1.2V to (V+) – 0.8V on the high end. Within the 400mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region. For more information on designing with rail-to-rail input op amps, see Figure 3, *Design Optimization with Rail-to-Rail Input Op Amps*.

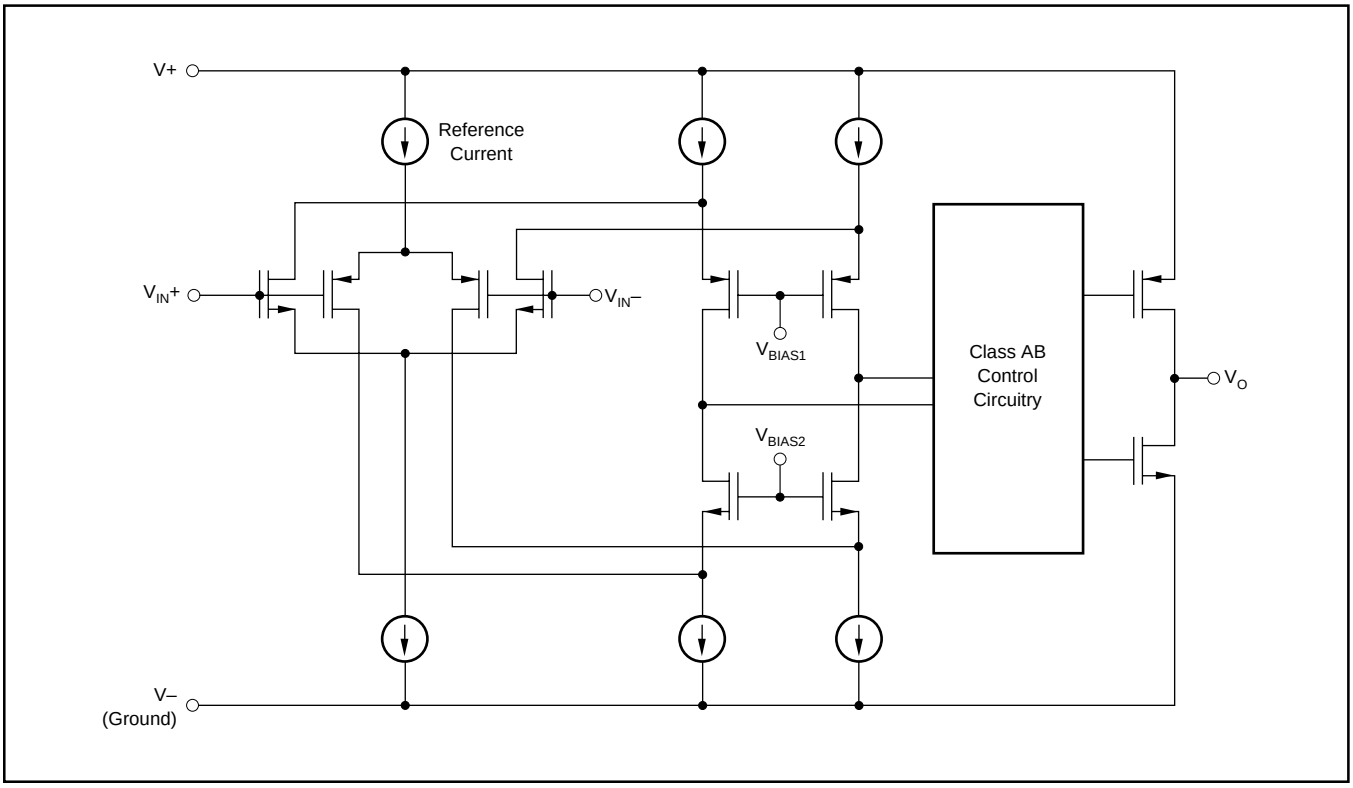


FIGURE 2. Simplified Schematic.

DESIGN OPTIMIZATION WITH RAIL-TO-RAIL INPUT OP AMPS

In most applications, operation is within the range of only one differential pair. However, some applications can subject the amplifier to a common-mode signal in the transition region. Under this condition, the inherent mismatch between the two differential pairs may lead to degradation of the CMRR and THD. The unity-gain buffer configuration is the most problematic—it will traverse through the transition region if a sufficiently wide input swing is required. A design option would be to configure the op amp as a unity-gain inverter as shown below and hold the noninverting input at a set common-mode voltage outside the transition region. This can be accomplished with a voltage divider from the supply. The voltage divider should be designed such that the biasing point for the noninverting input is outside the transition region.

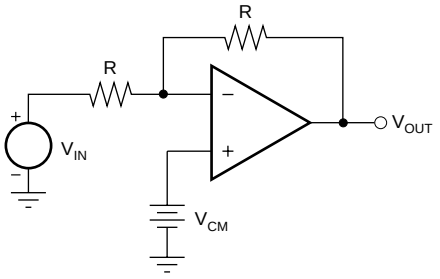


FIGURE 3. Design Optimization.

COMMON-MODE REJECTION

The CMRR for the OPA349 is specified in two ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region (V_{CM} < (V+) – 1.5V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at V_S = 5V over the entire common-mode range is specified.

OUTPUT DRIVEN TO V– RAIL

Loads that connect to single-supply ground (or the V– supply pin) can cause the OPA349 or OPA2349 to oscillate if the output voltage is driven into the negative rail (as shown in Figure 4a). Similarly, loads that can cause current to flow out of the output pin when the output voltage is near V– can cause oscillations. The op amp will recover to normal operation a few microseconds after the output is driven positively out of the rail.

Some op amp applications can produce this condition even without a load connected to V–. The integrator in Figure 4b shows an example of this effect. Assume that the output ramps negatively, and saturates near 0V. Any negative-going step at V_{IN} will produce a positive output current pulse through R_1 and C_1. This may incite the oscillation. Diode D_1 prevents the input step from pulling output current when the output is saturated at the rail, thus preventing the oscillation.

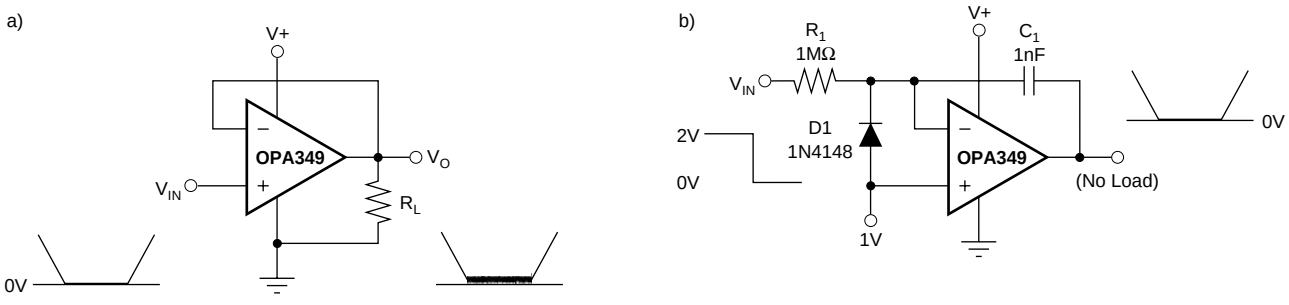


FIGURE 4. Output Driven to Negative Rail.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2349EA/250	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	C49	Samples
OPA2349EA/3K	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	C49	Samples
OPA2349UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2349UA	Samples
OPA2349UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2349UA	Samples
OPA349NA/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	A49	Samples
OPA349NA/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		A49	Samples
OPA349SA/250	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		S49	Samples
OPA349SA/3K	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		S49	Samples
OPA349UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		OPA 349UA	Samples
OPA349UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 349UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

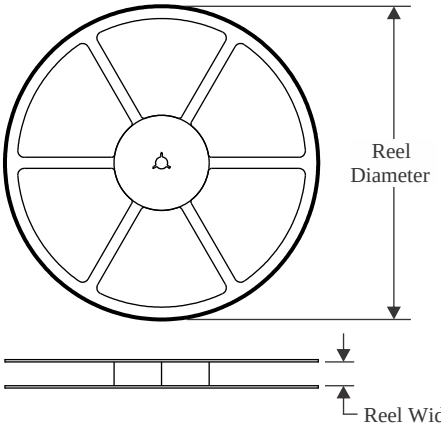
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

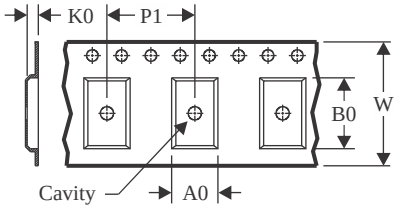
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

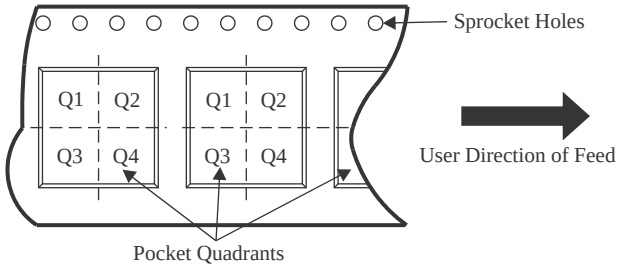


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

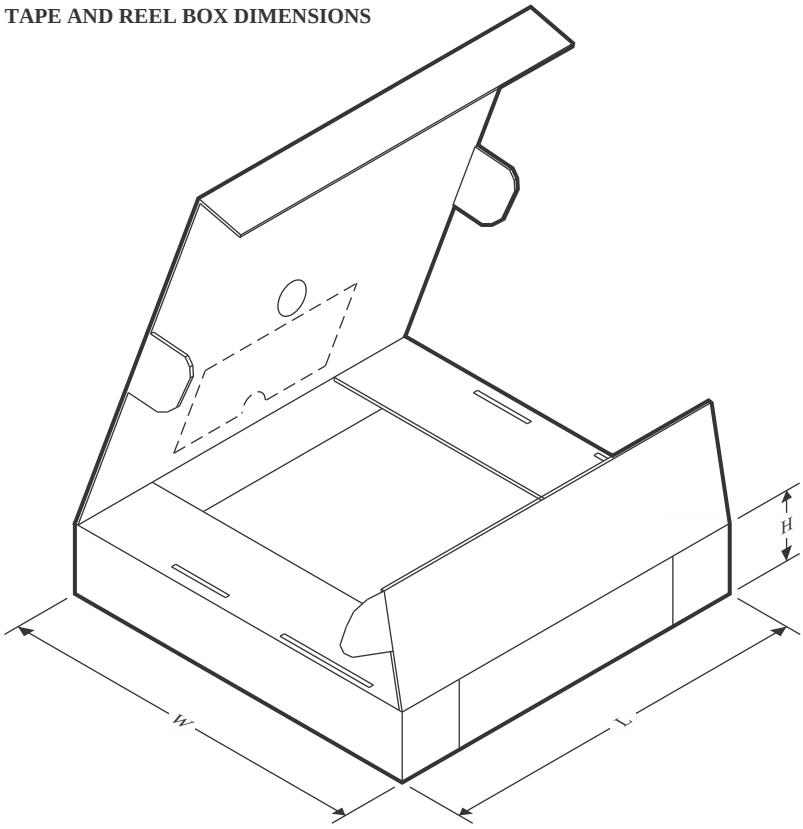
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2349EA/250	SOT-23	DCN	8	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA2349EA/3K	SOT-23	DCN	8	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA2349UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA349NA/250	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA349NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA349SA/250	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA349SA/3K	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA349UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

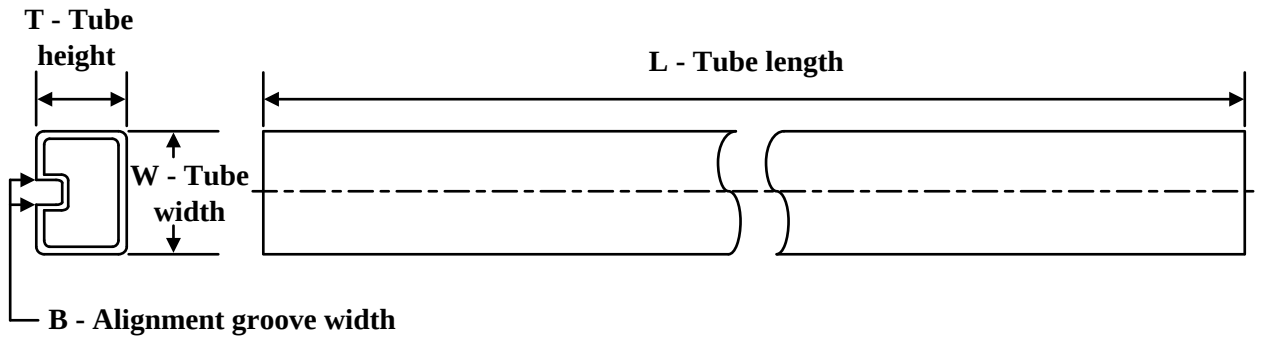
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2349EA/250	SOT-23	DCN	8	250	210.0	185.0	35.0
OPA2349EA/3K	SOT-23	DCN	8	3000	210.0	185.0	35.0
OPA2349UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA349NA/250	SOT-23	DBV	5	250	445.0	220.0	345.0
OPA349NA/3K	SOT-23	DBV	5	3000	445.0	220.0	345.0
OPA349SA/250	SC70	DCK	5	250	180.0	180.0	18.0
OPA349SA/3K	SC70	DCK	5	3000	180.0	180.0	18.0
OPA349UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

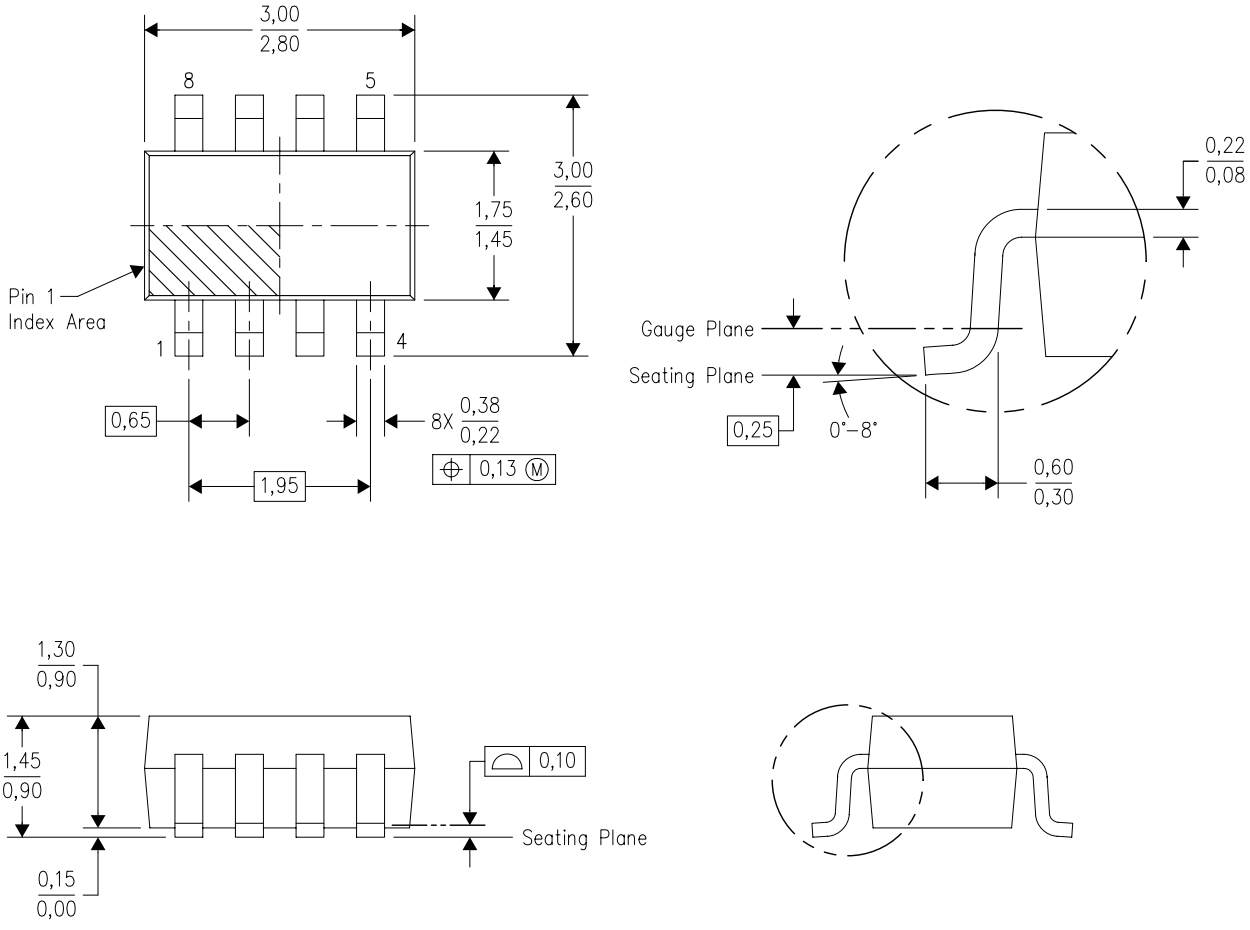
TUBE



*All dimensions are nominal

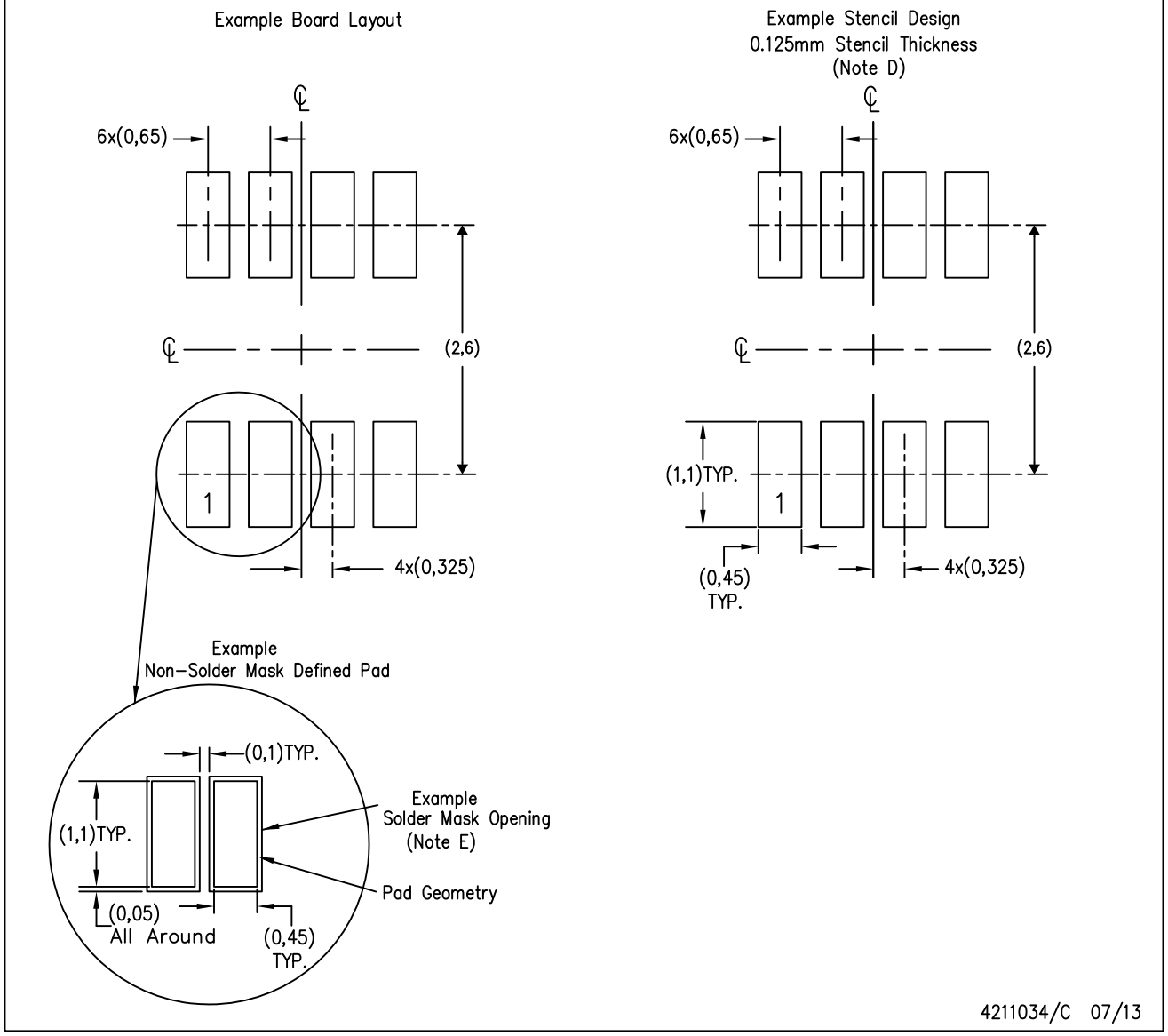
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2349UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA349UA	D	SOIC	8	75	506.6	8	3940	4.32

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



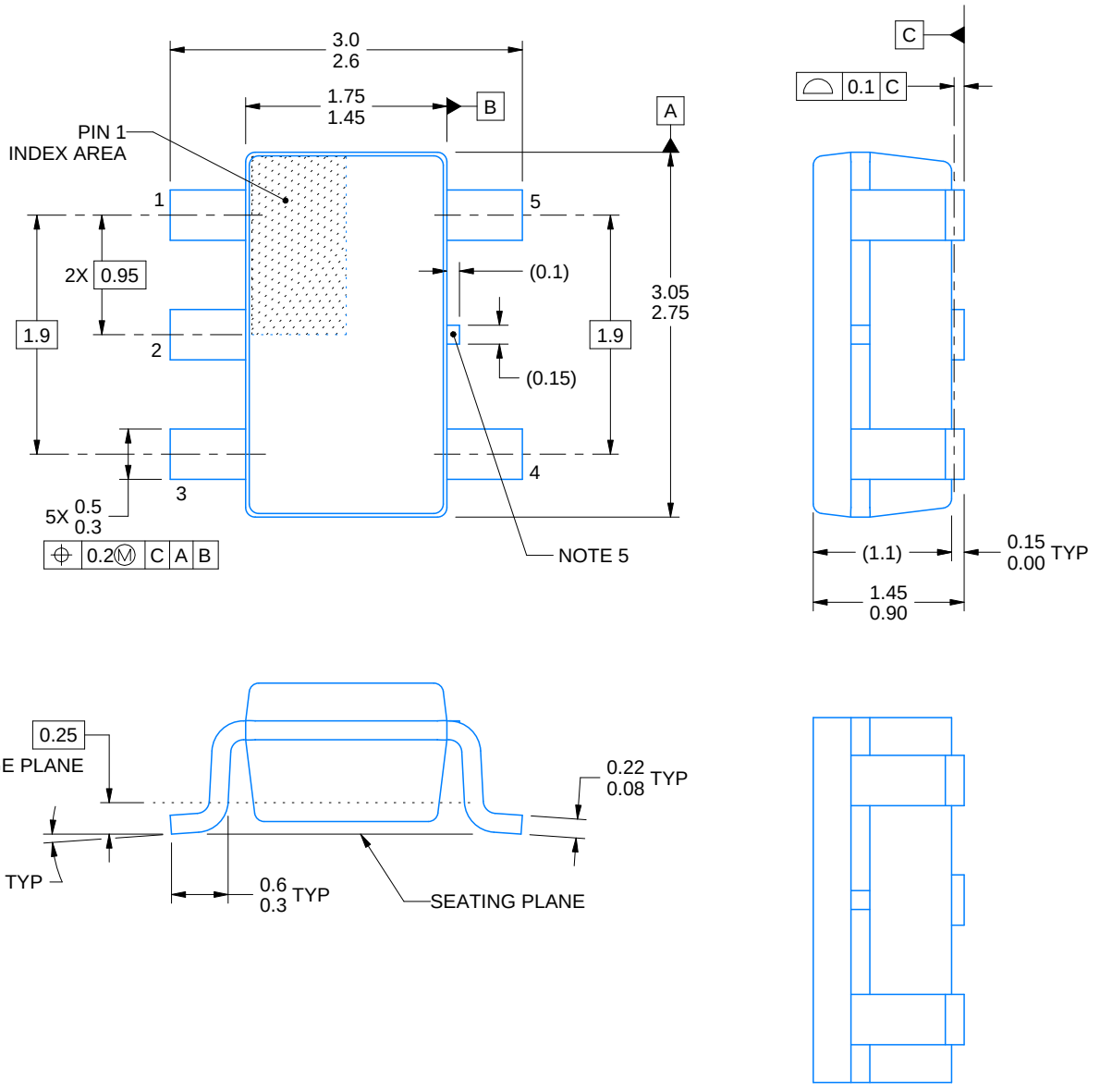
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

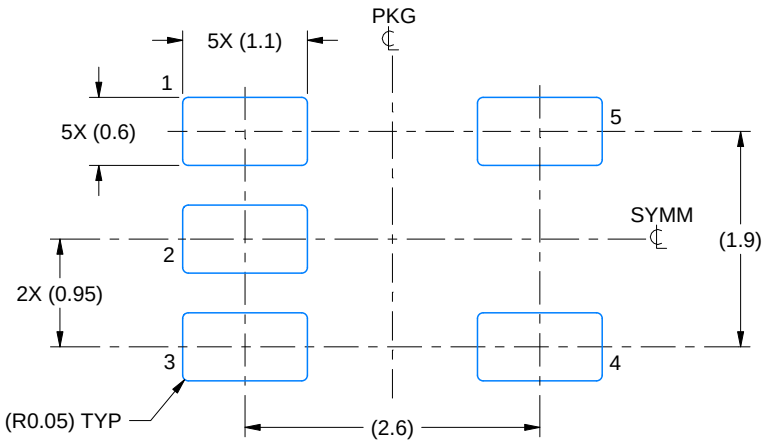


ALTERNATIVE PACKAGE SINGULATION VIEW

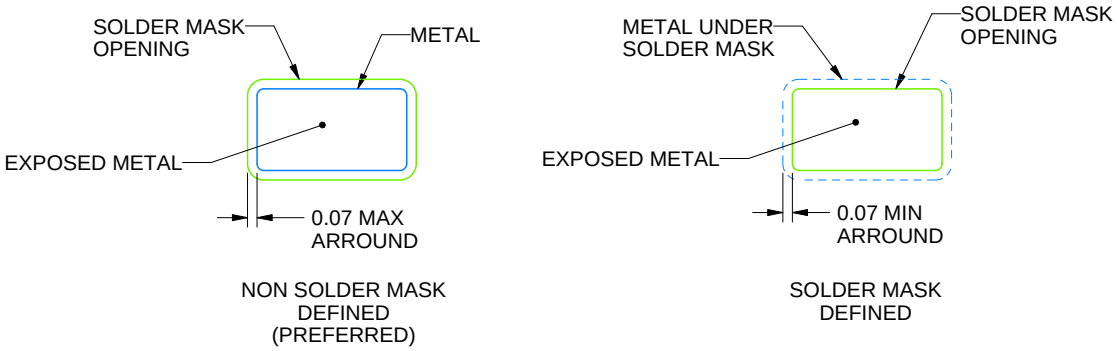
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

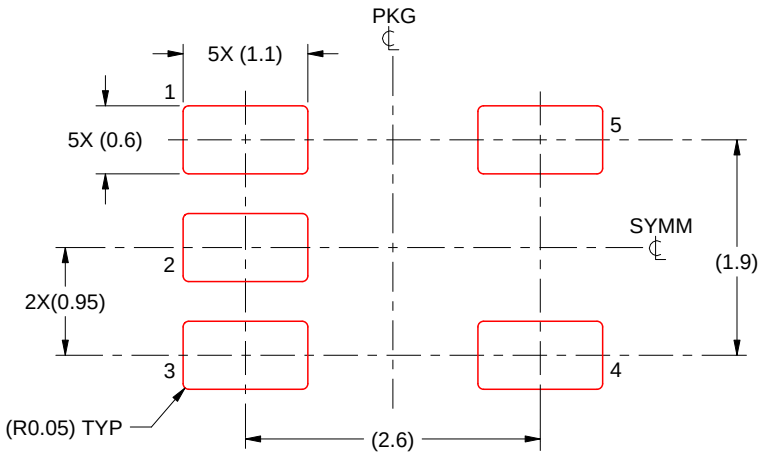


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

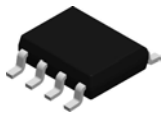


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

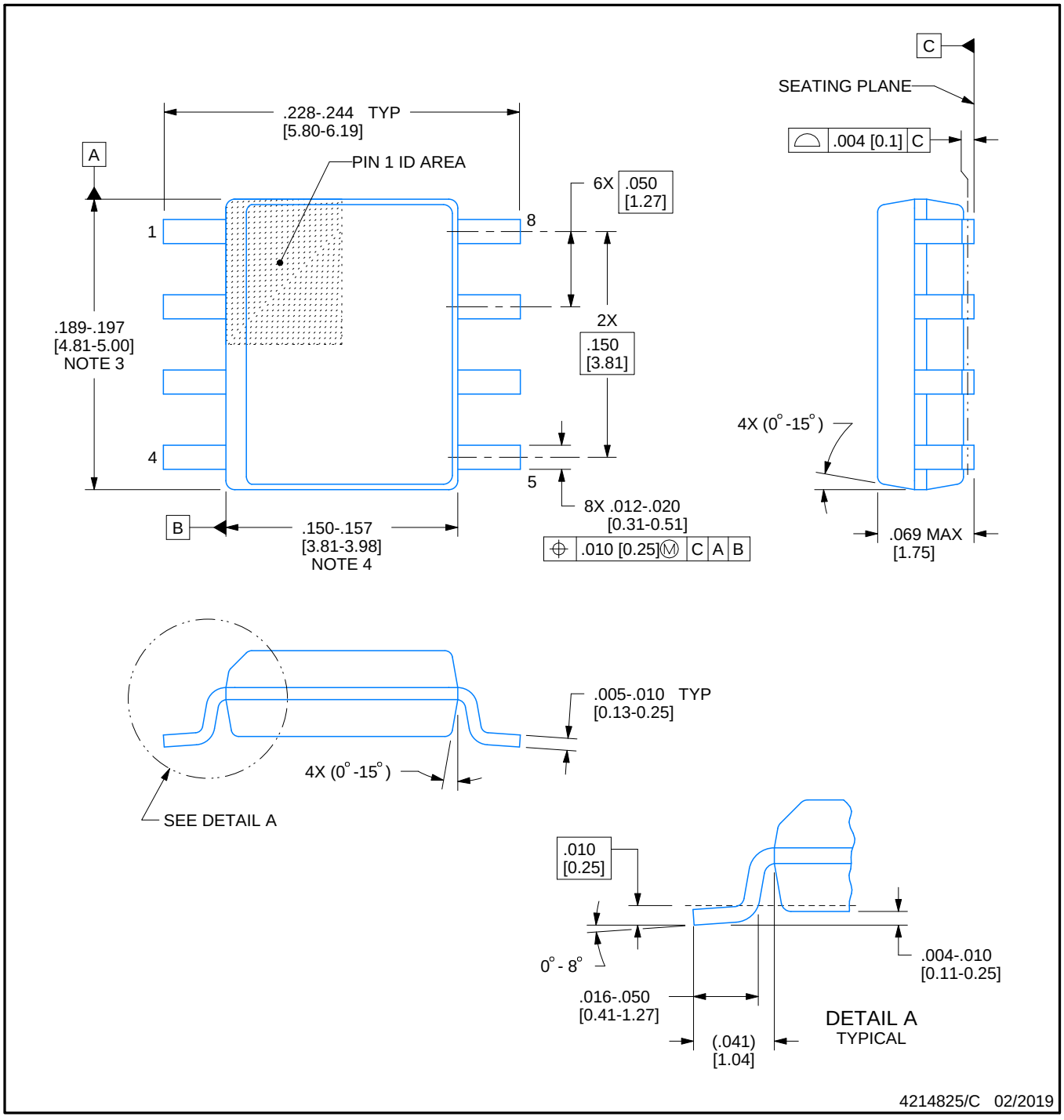


PACKAGE OUTLINE

D0008A

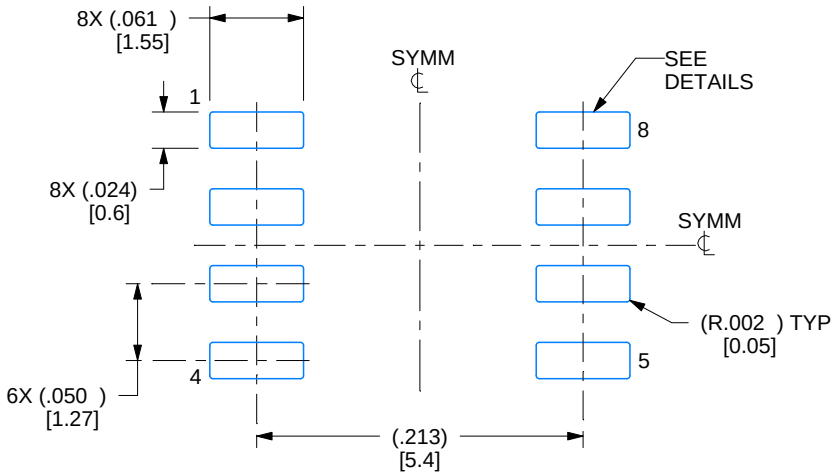
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

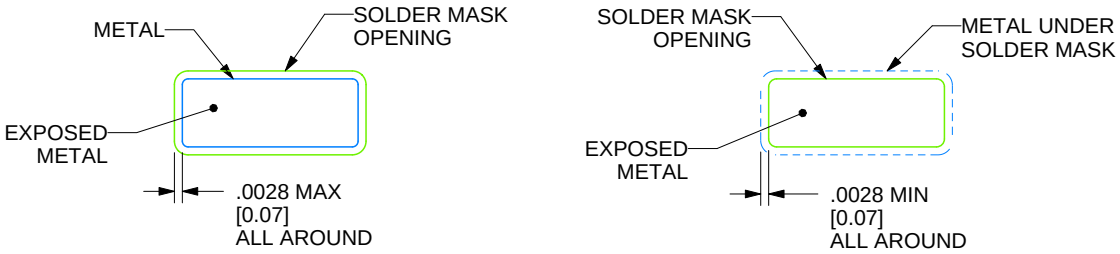


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

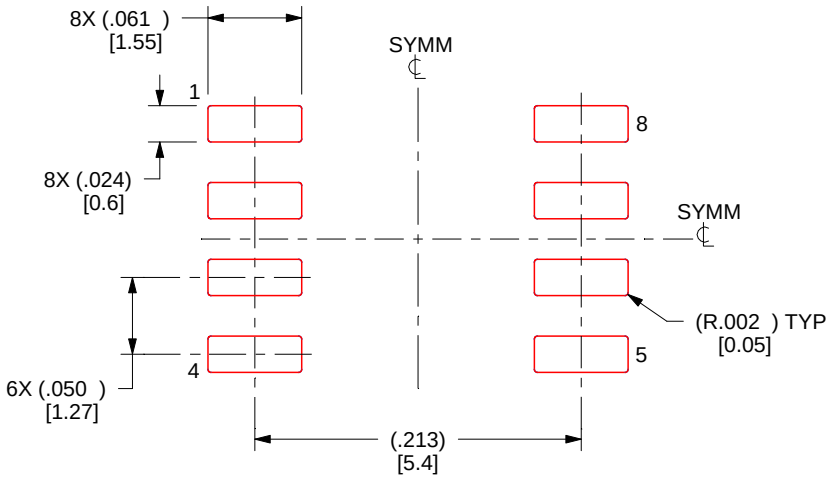
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

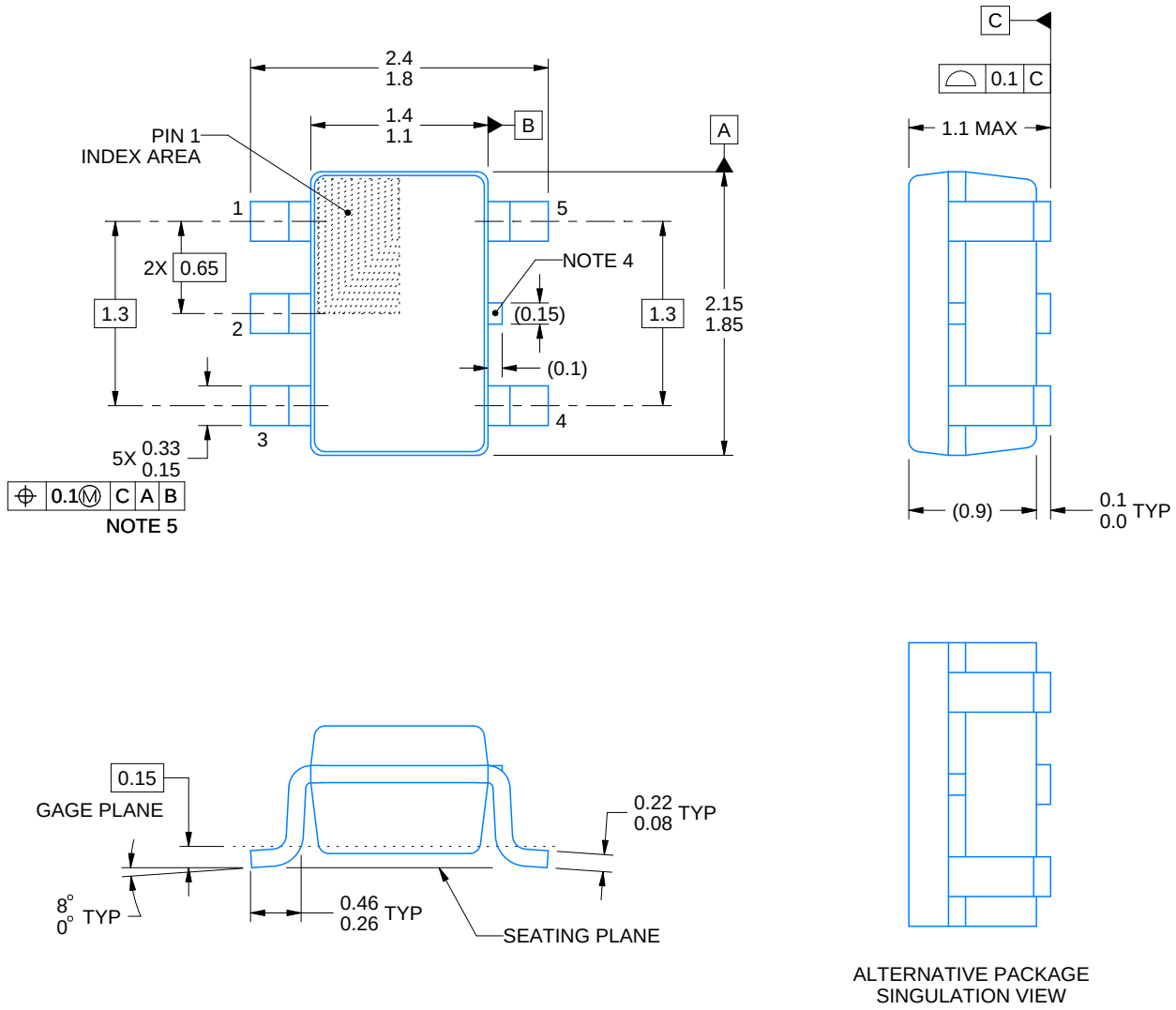
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

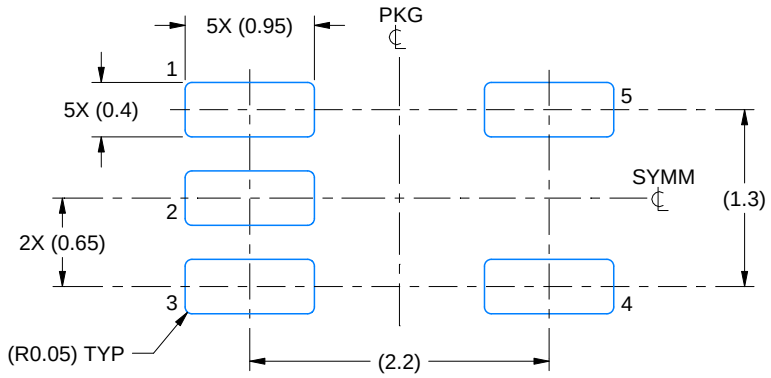
SMALL OUTLINE TRANSISTOR



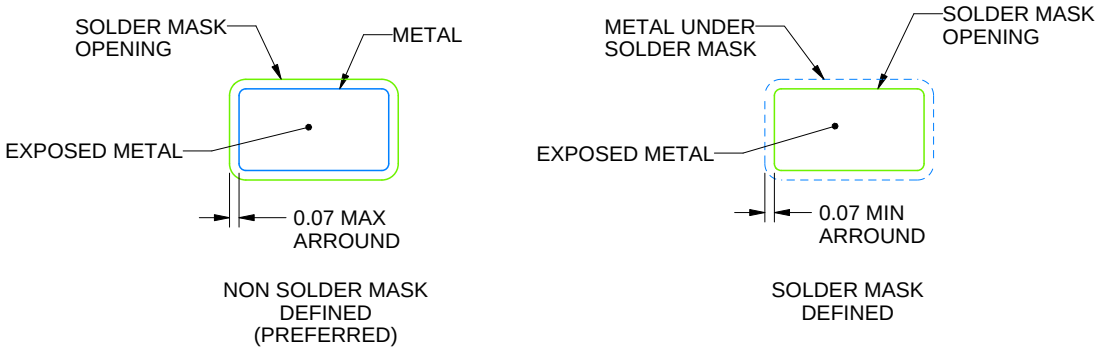
4214834/E 06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

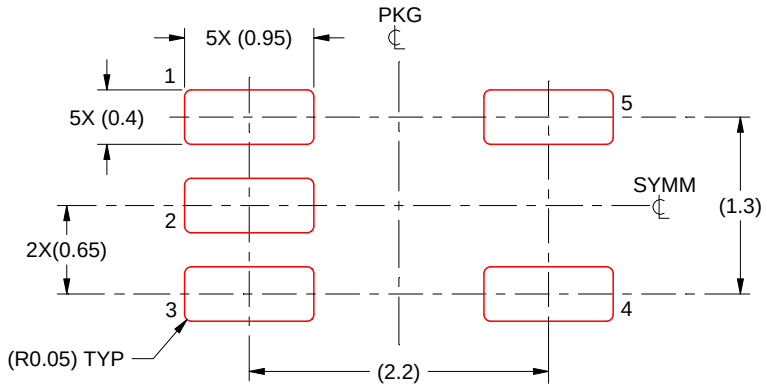


SOLDER MASK DETAILS

4214834/E 06/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/E 06/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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