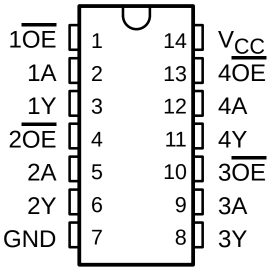
SN74F125
QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SDFS016B – JANUARY 1989 – REVISED JULY 2002

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**

**D, DB, N, OR NS PACKAGE
(TOP VIEW)**



description/ordering information

The SN74F125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{\mathrm{OE}}$) input is high.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F125N	SN74F125N
	SOIC – D	Tube	SN74F125D	F125
		Tape and reel	SN74F125DR	
	SOP – NS	Tape and reel	SN74F125NSR	74F125
	SSOP – DB	Tape and reel	SN74F125DBR	F125

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE
(each buffer)**

INPUTS		OUTPUT
$\overline{\mathrm{OE}}$	A	Y
L	H	H
L	L	L
H	X	Z

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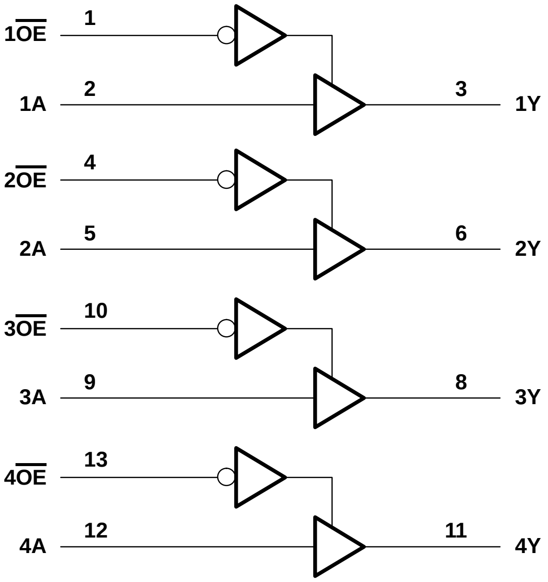
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		–0.5 V to 7 V
Input voltage range, V_I (see Note 1)		–1.2 V to 7 V
Input current range		–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state		–0.5 V to 5.5 V
Voltage range applied to any output in the high state		128 mA
Current into any output in the low state		±70 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	86°C/W
	DB package	96°C/W
	N package	80°C/W
	NS package	76°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			– 15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = – 3 mA	2.4	3.3		V
		I_{OH} = – 15 mA	2	3.1		
	V_{CC} = 4.75 V,	I_{OH} = – 3 mA	2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 64 mA		0.4	0.55	V
I_I	V_{CC} = 0,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			– 20	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			– 50	µA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	– 100		– 225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		17	24	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		28	40	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		25	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

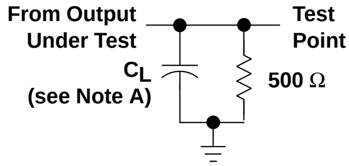
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

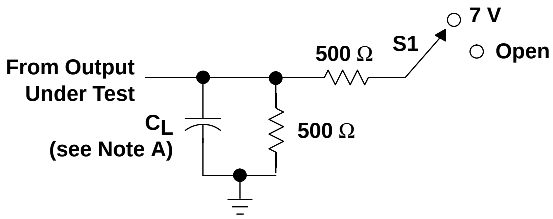
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1.2	3.6	6	1.2	6.5	ns
t_{PHL}			2.2	5.1	7.5	2.2	8	
t_{PZH}	$\overline{OE}$	Y	2.7	5.1	7.5	2.7	8.5	ns
t_{PZL}			3.2	5.6	8	3.2	9	
t_{PHZ}	$\overline{OE}$	Y	1	3.1	5	1	6	ns
t_{PLZ}			1	3.1	5.5	1	6	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION

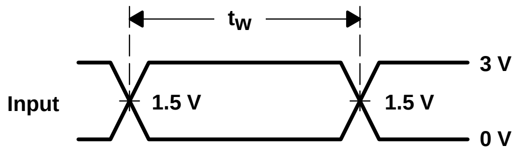


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



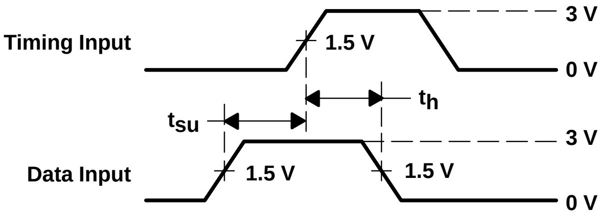
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
Open Collector	7 V

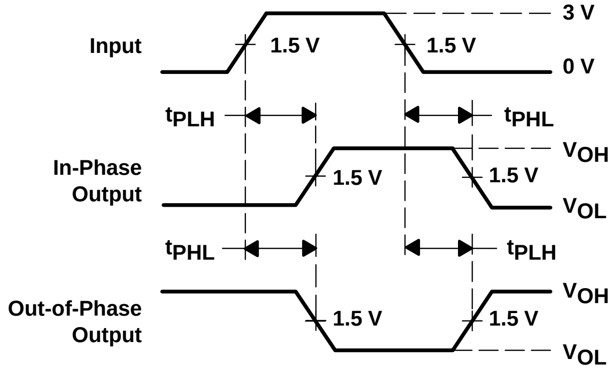


1.5 V

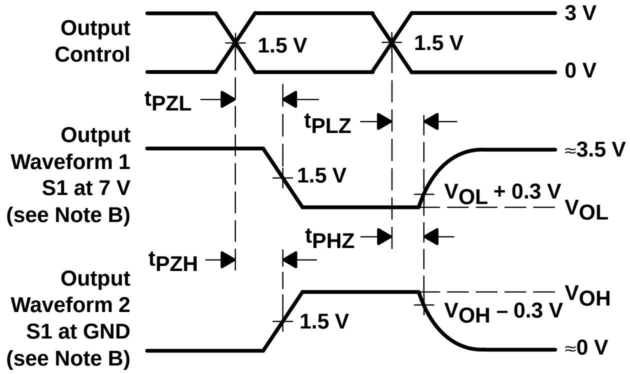
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, duty cycle = 50%.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F125DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F125	Samples
SN74F125N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F125N	Samples
SN74F125NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F125	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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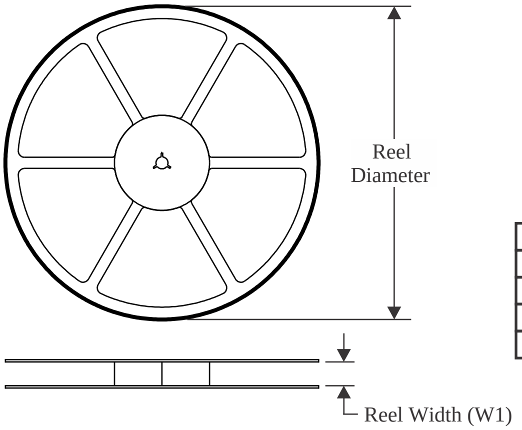
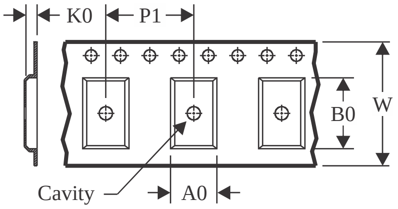
TAPE AND REEL INFORMATION

REEL DIMENSIONS

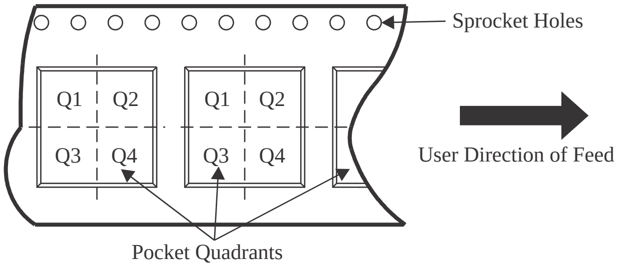


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

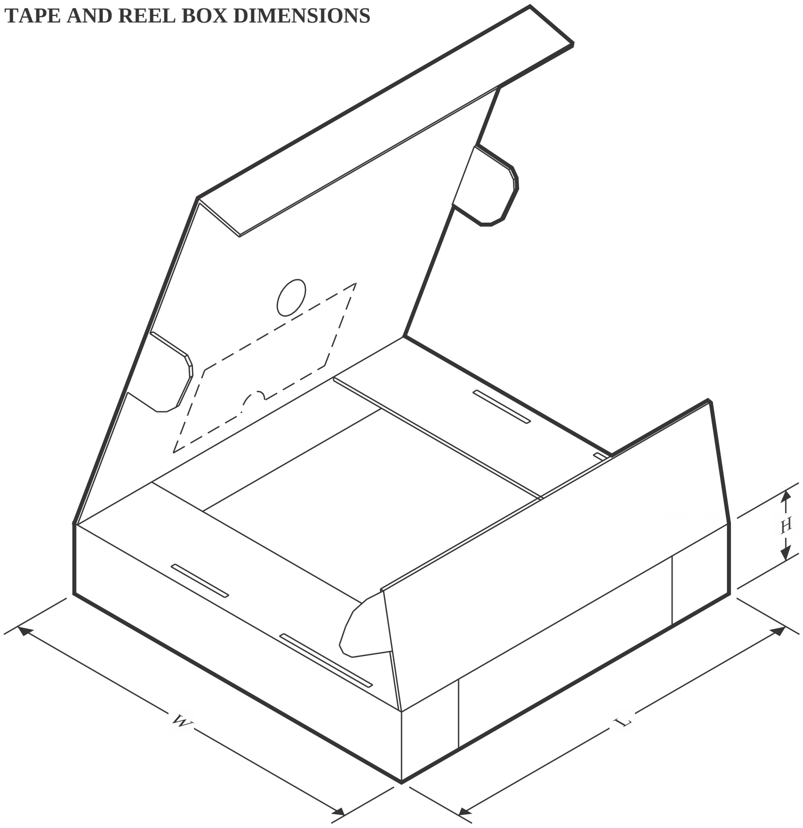
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74F125NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

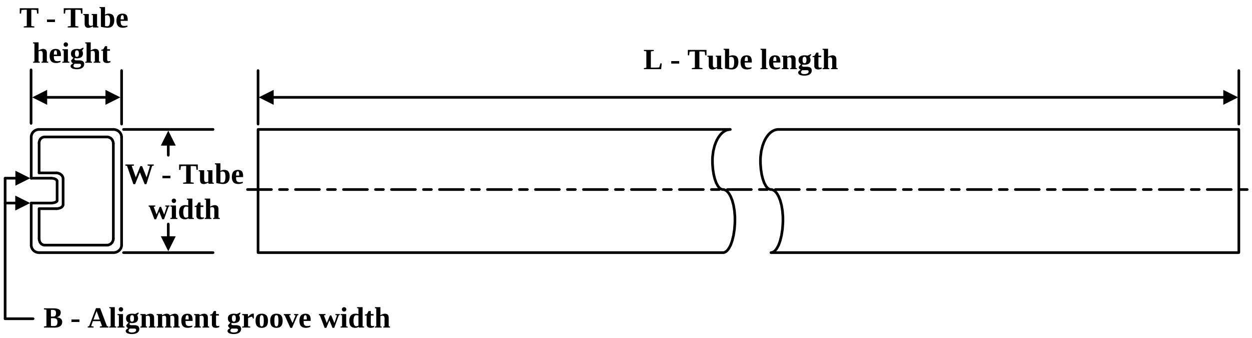
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F125DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74F125NSR	SO	NS	14	2000	356.0	356.0	35.0

TUBE



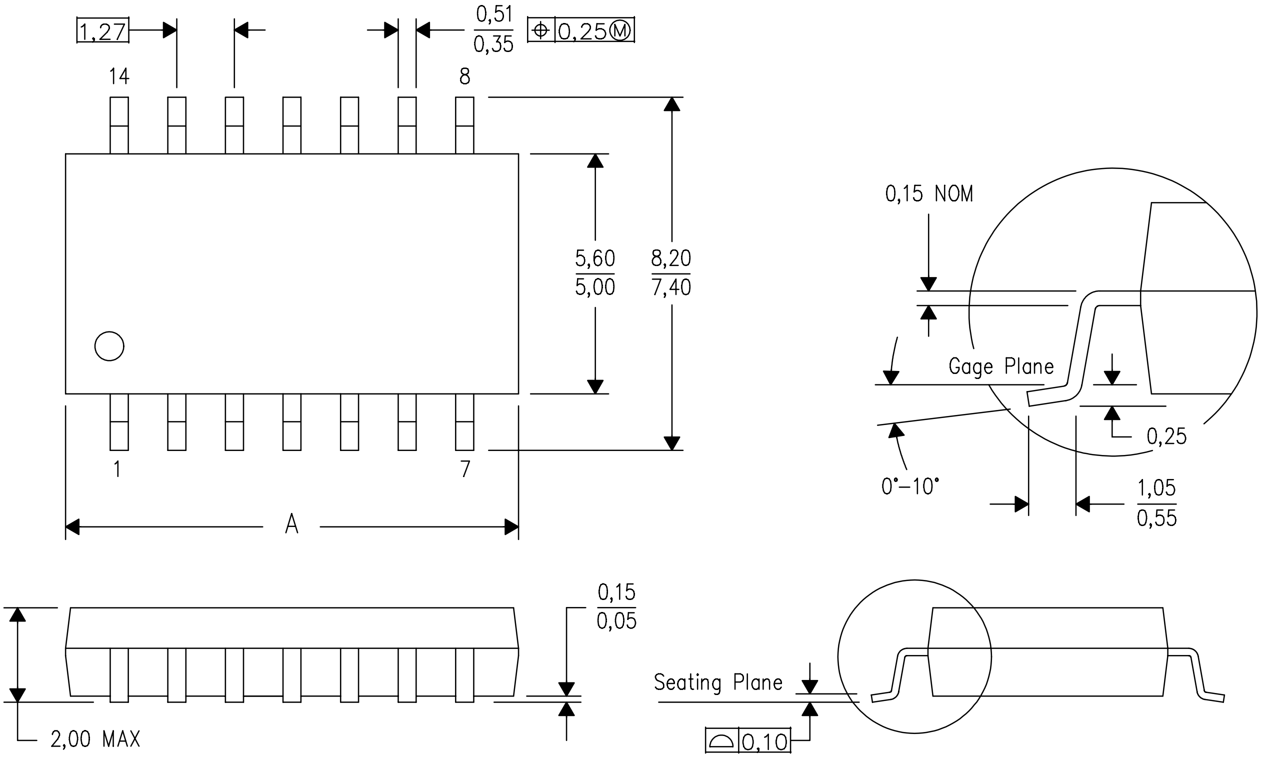
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74F125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F125N	N	PDIP	14	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

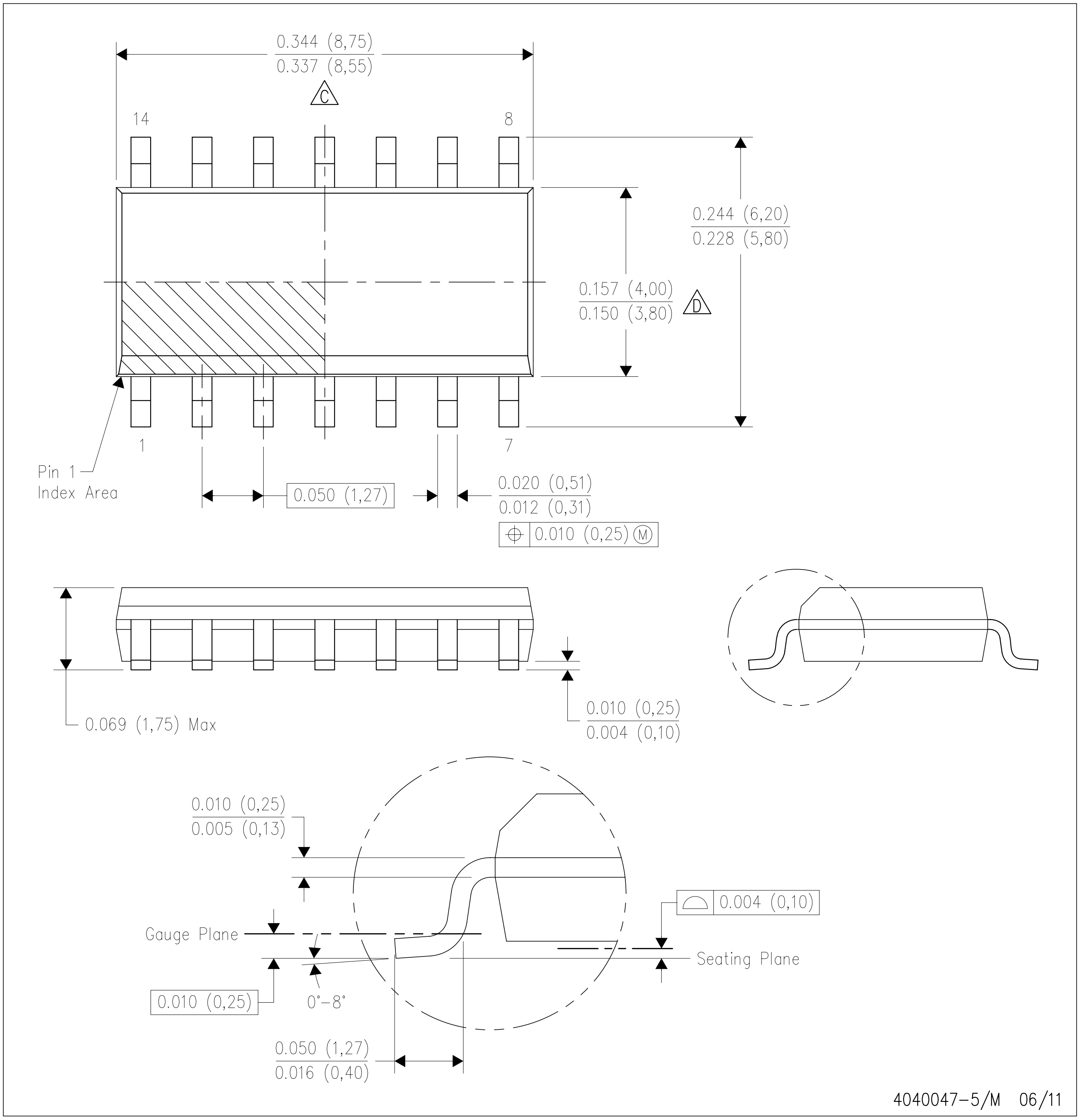


PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

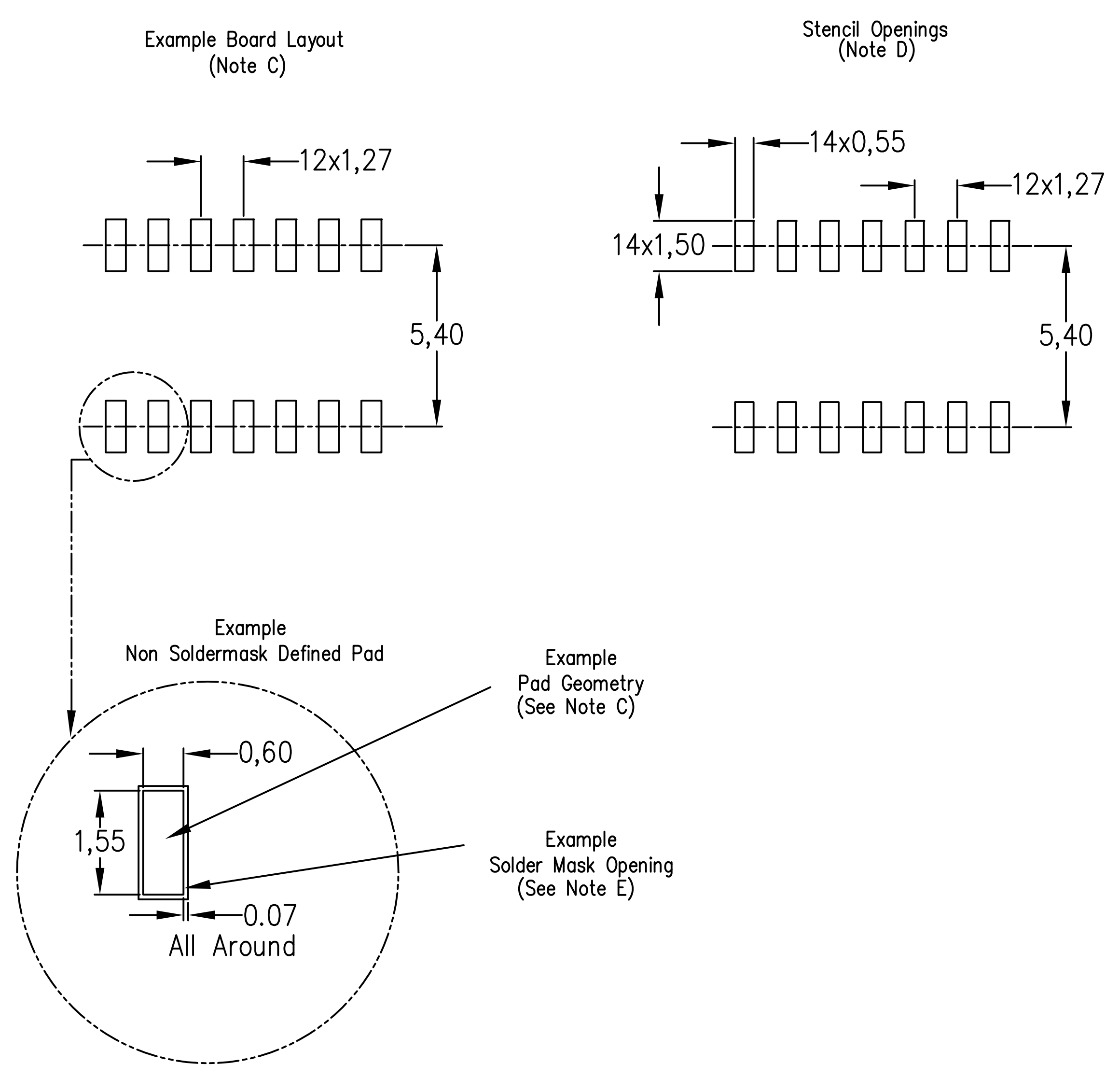
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



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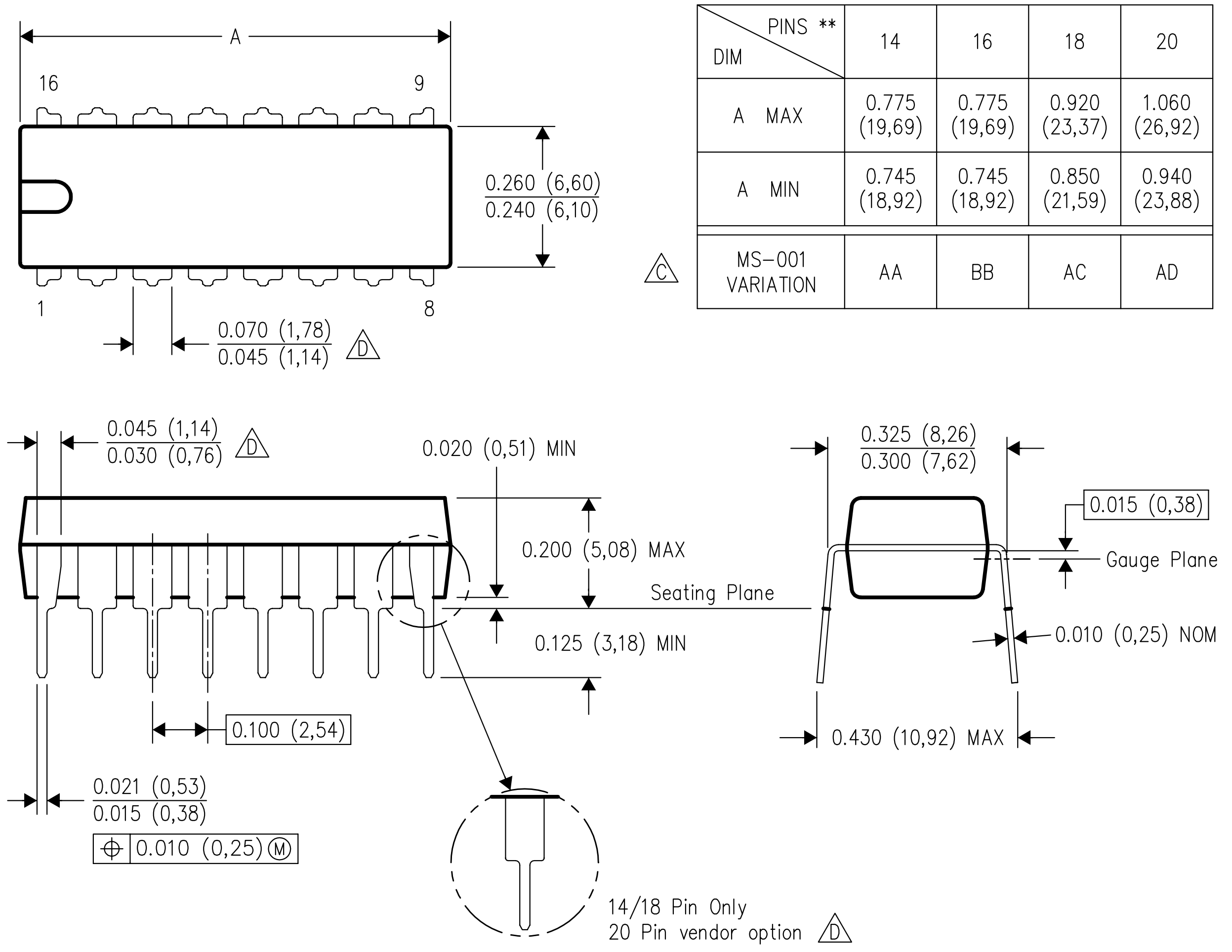
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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