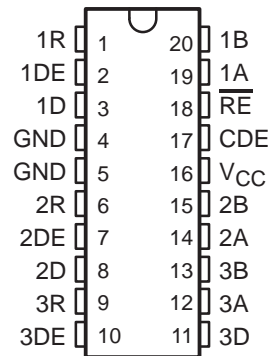


SN75ALS171, SN75ALS171A TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

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- Three Bidirectional Transceivers
- Driver Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and RS-485 and ITU Recommendation V.11
- Two Skew Limits Available
- Designed to Operate Up to 20 Million Data Transfers per Second (FAST-20 SCSI)
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Pulse Skew . . . 5 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Features Independent Driver Enables and Combined Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltages Ranges
- Driver Output Capacity . . . ± 60 mA
- Thermal Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedances . . . 12 k Ω Min
- Receiver Input Sensitivity . . . ± 300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection

DW OR J PACKAGE
(TOP VIEW)



description

The SN75ALS171 and the SN75ALS171A triple differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines, and each driver meets ANSI Standards EIA/TIA-422-B and RS-485 and both the drivers and receivers meet ITU Recommendation V.11. The SN75ALS171A is designed for FAST-20 SCSI and can transmit or receive data pulses as short as 30 ns with a maximum skew of 5 ns.

The SN75ALS171 and the SN75ALS171A operate from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} is at 0 V. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS171 and the SN75ALS171A are characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN75ALS171, SN75ALS171A

TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

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Function Tables

EACH DRIVER

INPUT D	ENABLES		OUTPUTS	
	DE	CDE	A	B
H	H	H	H	L
L	H	H	L	H
X	L	X	Z	Z
X	X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE \overline{RE}	OUTPUT R
$V_{ID} \geq 0.3 V$	L	H
$-0.3 V < V_{ID} < 0.3 V$	L	?
$V_{ID} \leq -0.3 V$	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

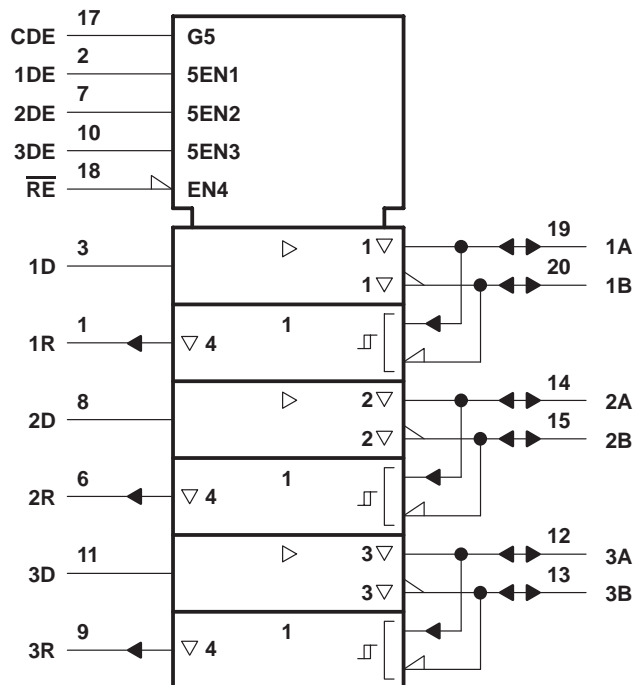
AVAILABLE OPTIONS

SKEW LIMIT	PART NUMBER	
10 ns	SN75ALS171DW	SN75ALS171J
5 ns	SN75ALS171ADW	

SN75ALS171, SN75ALS171A TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

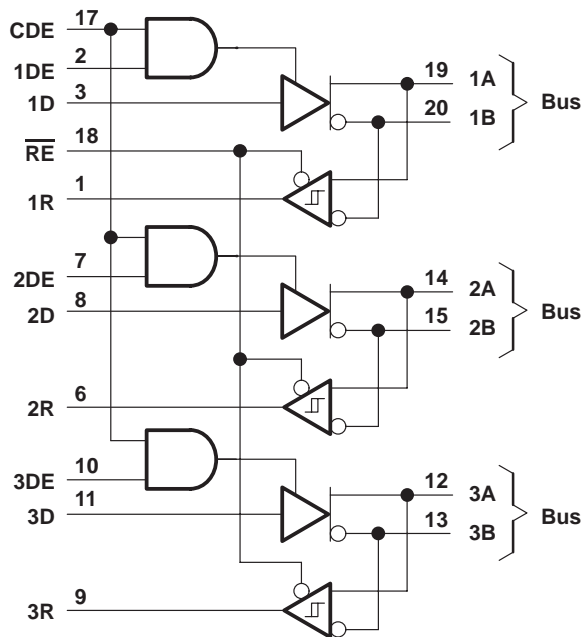
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logic symbol†

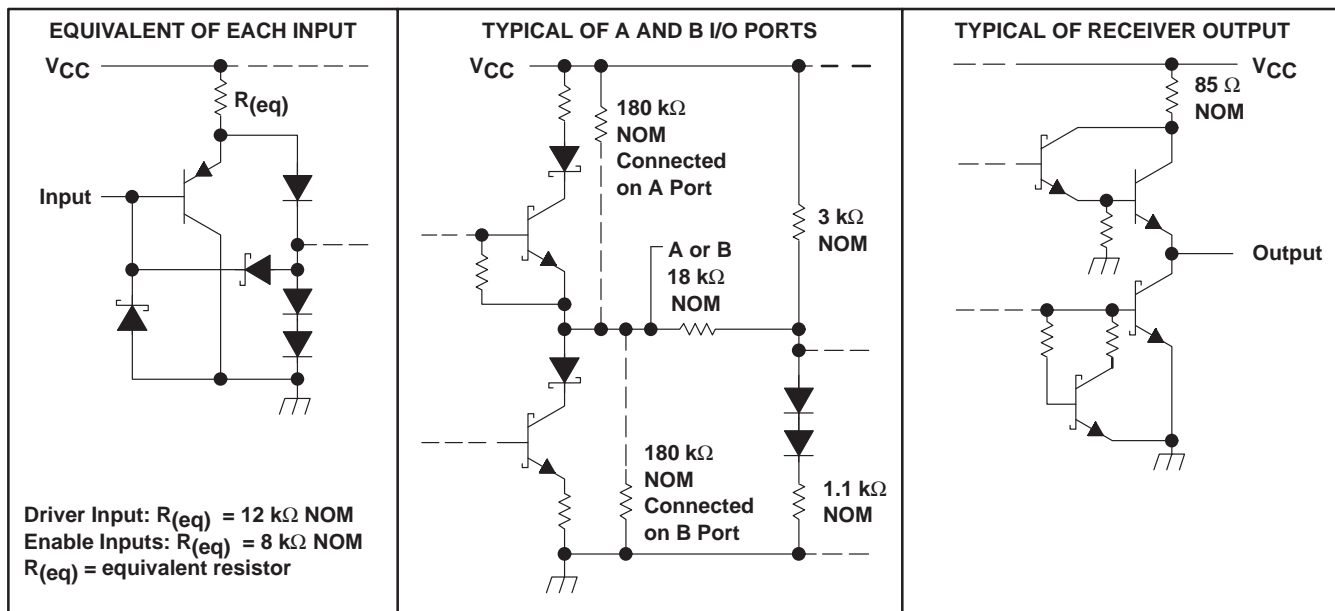


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



SN75ALS171, SN75ALS171A TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	-7 V to 12 V
Enable input voltage, V_I	7 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}	-7		12	V
High-level input voltage, V_{IH}	D, CDE, DE, and \overline{RE}		2	V
Low-level input voltage, V_{IL}	D, CDE, DE, and \overline{RE}		0.8	V
Differential input voltage, V_{ID} (see Note 2)			±12	V
High-level output current, I_{OH}	Driver		-60	mA
	Receiver		-400	µA
Low-level output current, I_{OL}	Driver		60	mA
	Receiver		8	
Operating free-air temperature, T_A	0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONST		MIN	TYP‡	MAX	UNIT		
V _{IK}	Input clamp voltage	I _I = -18 mA				-1.5	V		
V _O	Output voltage	I _O = 0		0		6	V		
V _{OH}	High-level output voltage	V _{CC} = 4.75 V, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OH} = -55 mA	2.7			V		
V _{OL}	Low-level output voltage	V _{CC} = 4.75 V, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OL} = 55 mA			1.7	V		
V _{OD1}	Differential output voltage	I _O = 0		1.5		6	V		
V _{OD2}	Differential output voltage	R _L = 100 Ω,	See Figure 1	1/2 V _{OD1} or 2§	2.5	5	V		
		R _L = 54 Ω,	See Figure 1	1.5	2.5	5			
V _{OD3}	Differential output voltage	V _{test} = -7 V to 12 V, See Figure 2		1.5		5	V		
Δ V _{OD}	Change in magnitude of differential output voltage¶	R _L = 54 Ω or 100 Ω, See Figure 1				±0.2	V		
V _{OC}	Common-mode output voltage					3	-1	V	
Δ V _{OC}	Change in magnitude of common-mode output voltage¶							±0.2	V
I _O	Output current	Output disabled, See Note 3		V _O = 12 V		1	mA		
				V _O = -7 V		-0.8			
I _{IH}	High-level enable-input current	D and DE CDE		V _{IH} = 2.7 V		20	μA		
						60			
I _{IL}	Low-level enable-input current	D and DE CDE		V _{IL} = 0.4 V		-100	μA		
						-900			
I _{OS}	Short-circuit output current					V _O = -6 V	-250		
						V _O = 0	-150		
						V _O = V _{CC}	250		
						V _O = 8 V	250		
I _{CC}	Supply current	No load				Outputs enabled	69	90	mA
						Outputs disabled	57	78	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

§ The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.

¶ Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

SN75ALS171, SN75ALS171A

TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
t _{d(OD)}	Differential output delay time	ALS171	R _L = 54 Ω, See Figure 3, C _L = 50 pF	3		13	ns	
		ALS171A						6
		ALS171	R _{L1} = R _{L3} = 165 Ω, C _L = 60 pF, R _{L2} = 75 Ω, V _{TERM} = 5 V, See Figure 6	3		13		
		ALS171A						6
t _{sk(p)}	Pulse skew‡	R _L = 54 Ω, See Figure 3	C _L = 50 pF,		1	5	ns	
		R _{L1} = R _{L3} = 165 Ω, C _L = 60 pF,	R _{L2} = 75 Ω, See Figure 6		1	5	ns	
t _{sk(lim)}	Skew limit§	ALS171	R _L = 54 Ω, See Figure 3			10	ns	
		ALS171A						5
		ALS171	R _{L1} = R _{L3} = 165 Ω, C _L = 60 pF, See Figure 6	R _{L2} = 75 Ω, See Figure 6				10
		ALS171A						
t _{t(OD)}	Differential-output transition time	R _L = 54 Ω, See Figure 3	C _L = 50 pF,	3	8	13	ns	
		R _{L1} = R _{L3} = 165 Ω, C _L = 60 pF, See Figure 6	R _{L2} = 75 Ω, V _{TERM} = 5 V, See Figure 6	3	8	13		
t _{pZH}	Output enable time to high level	R _L = 110 Ω,	See Figure 4		30	50	ns	
t _{pZL}	Output enable time to low level	R _L = 110 Ω,	See Figure 5		30	50	ns	
t _{PHZ}	Output disable time from high level	R _L = 110 Ω,	See Figure 4	3	8	13	ns	
t _{PLZ}	Output disable time from low level	R _L = 110 Ω,	See Figure 5	3	8	13	ns	
t _{pDE}	Differential-output enable time	R _{L1} = R _{L3} = 165 Ω, C _L = 60 pF,	R _{L2} = 75 Ω, See Figure 7	8	30	45	ns	
t _{pDZ}	Differential-output disable time			5	10	45	ns	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ Pulse skew is defined as the |t_{d(ODH)} - t_{d(ODL)}| of each channel.

§ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	EIA/TIA-422-B	RS-485
V _O	V _{0a} , V _{0b}	V _{0a} , V _{0b}
V _{OD1}	V ₀	V ₀
V _{OD2}	V _t (R _L = 100 Ω)	V _t (R _L = 54 Ω)
V _{OD3}		V _t (Test Termination Measurement 2)
V _{tst}		V _{tst}
Δ V _{OD}	V _t - V _t	V _t - V _t
V _{OC}	V _{os}	V _{os}
Δ V _{OC}	V _{os} - V _{os}	V _{os} - V _{os}
I _{OS}	I _{sa} , I _{sb}	
I _O	I _{xa} , I _{xb}	I _{ia} , I _{ib}



SN75ALS171, SN75ALS171A TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

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RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7\text{ V}$,	$I_O = -0.4\text{ mA}$			0.3	V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5\text{ V}$,	$I_O = 8\text{ mA}$	$-0.3\ddagger$			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18\text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 300\text{ mV}$, See Figure 8	$I_{OH} = -400\text{ }\mu\text{A}$,	2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = -300\text{ mV}$, See Figure 8	$I_{OL} = 8\text{ mA}$,			0.45	V
I_{OZ}	High-impedance-state output current	$V_O = 0.4\text{ V to }2.4\text{ V}$				± 20	μA
I_I	Line input current	Other input = 0 V, See Note 4	$V_I = 12\text{ V}$			1	mA
			$V_I = -7\text{ V}$			-0.8	
I_{IH}	High-level enable-input current	$V_{IH} = 2.7\text{ V}$				60	μA
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4\text{ V}$				-300	μA
r_i	Input resistance			12			k Ω
I_{OS}	Short-circuit output current	$V_{ID} = 300\text{ mV}$,	$V_O = 0$	-15		-85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$V_{ID} = -1.5\text{ V to }1.5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$, See Figure 9	9		19	ns
			11		16	
t_{PHL}	Propagation delay time, high- to low-level output	$V_{ID} = -1.5\text{ V to }1.5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$, See Figure 9	9		19	ns
			11		16	
$t_{sk(p)}$	Pulse skew§	$V_{ID} = -1.5\text{ V to }1.5\text{ V}$, $C_L = 15\text{ pF}$, See Figure 9		2	5	ns
$t_{sk(lim)}$	Skew limit¶		ALS171			10
		ALS171A			5	
t_{PZH}	Output enable time to high level	$C_L = 15\text{ pF}$, See Figure 10		7	14	ns
t_{PZL}	Output enable time to low level			7	14	ns
t_{PHZ}	Output disable time from high level	$C_L = 15\text{ pF}$, See Figure 10		20	35	ns
t_{PLZ}	Output disable time from low level			8	17	ns

† All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

§ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.

¶ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.



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PARAMETER MEASUREMENT INFORMATION

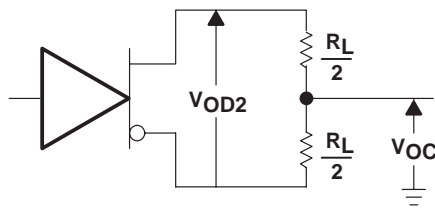


Figure 1. Driver V_{OD} and V_{OC}

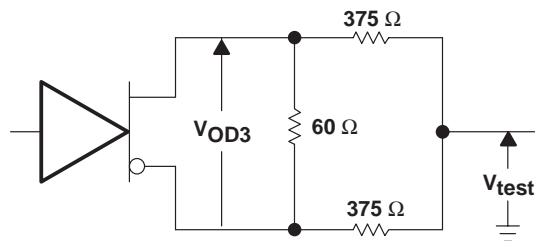
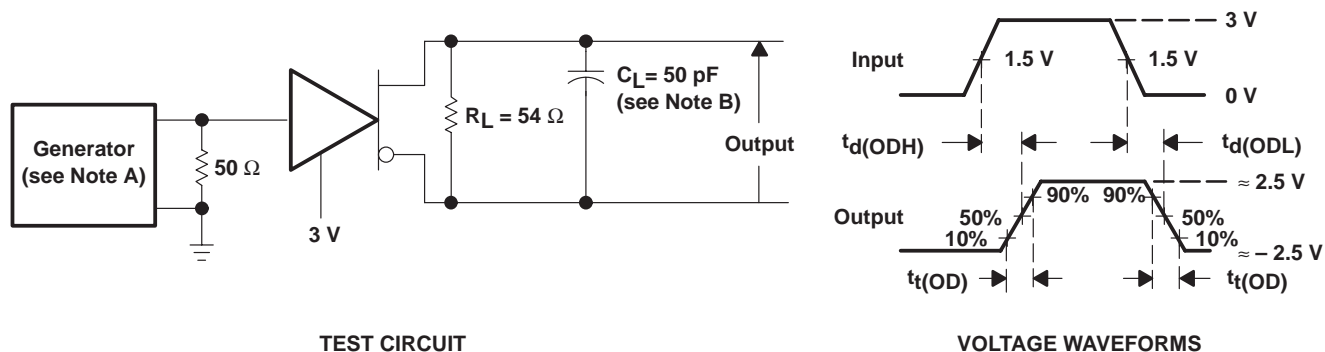


Figure 2. Driver V_{OD3}



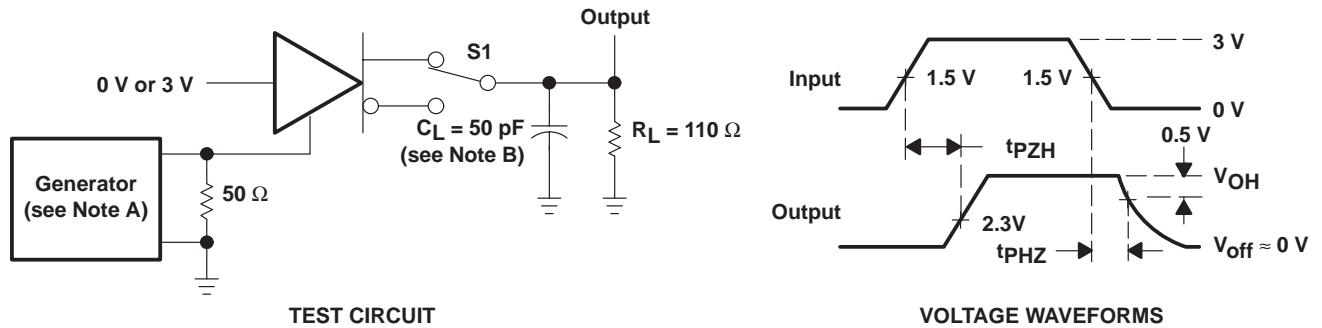
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

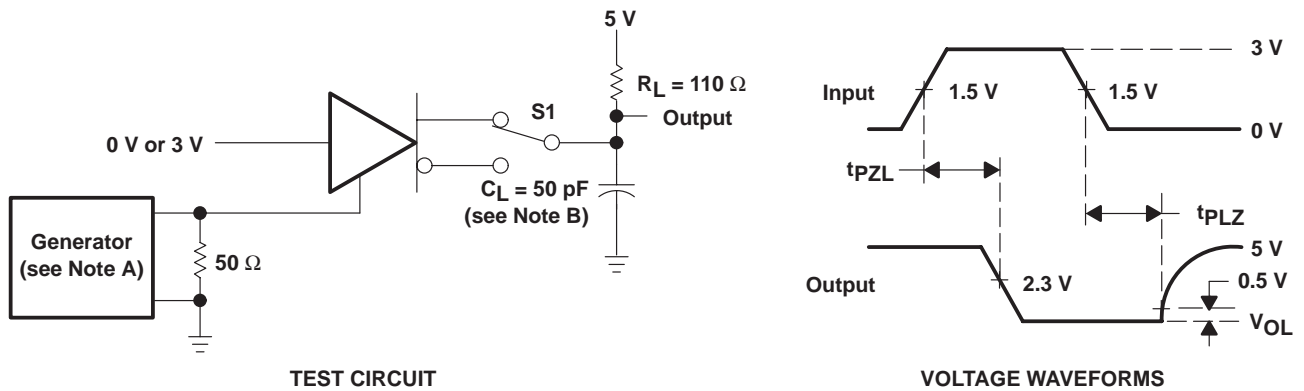
Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms



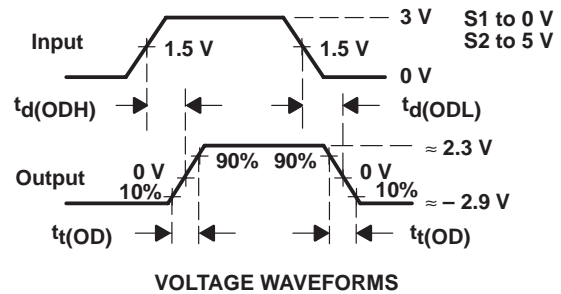
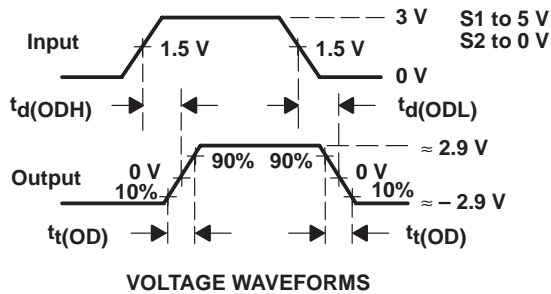
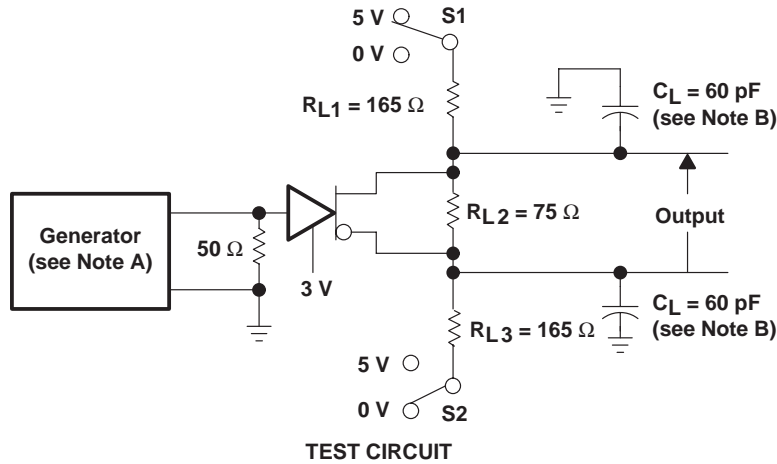
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

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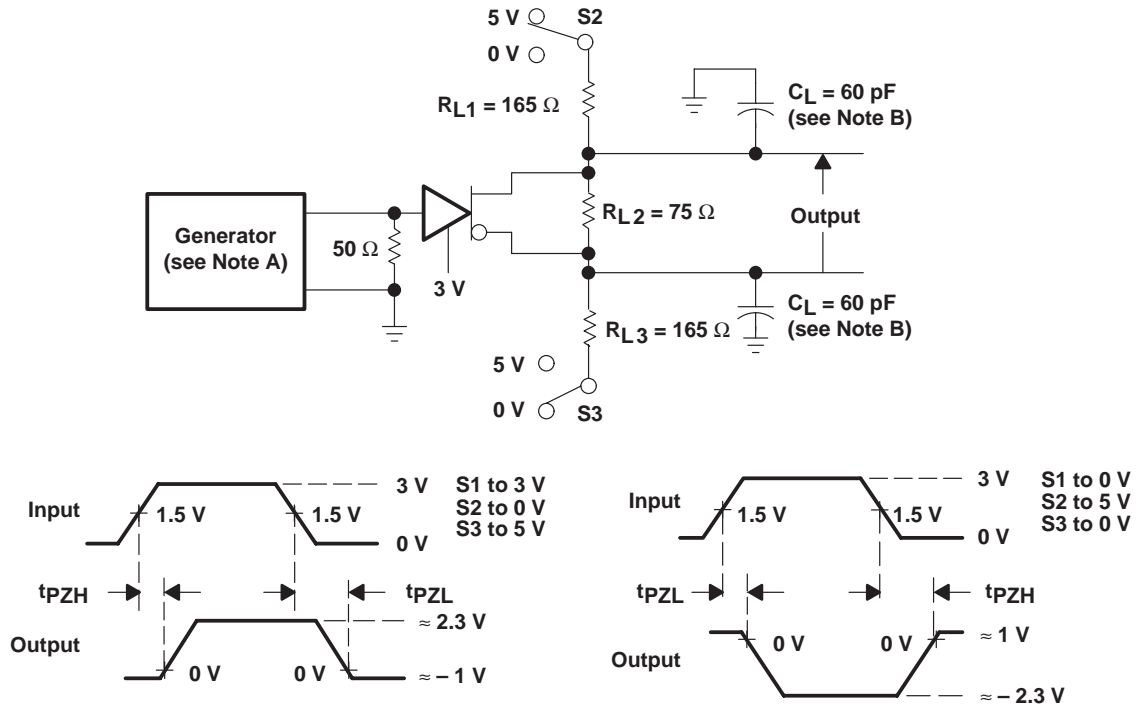
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

**Figure 6. Driver Test Circuit and Voltage Waveforms
With Double-Differential-SCSI Termination for the Load**

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Driver Differential-Enable and Disable Times With a Double-SCSI Termination

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PARAMETER MEASUREMENT INFORMATION

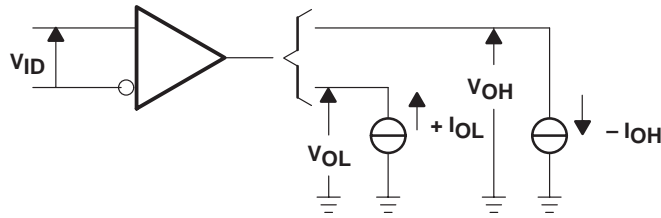
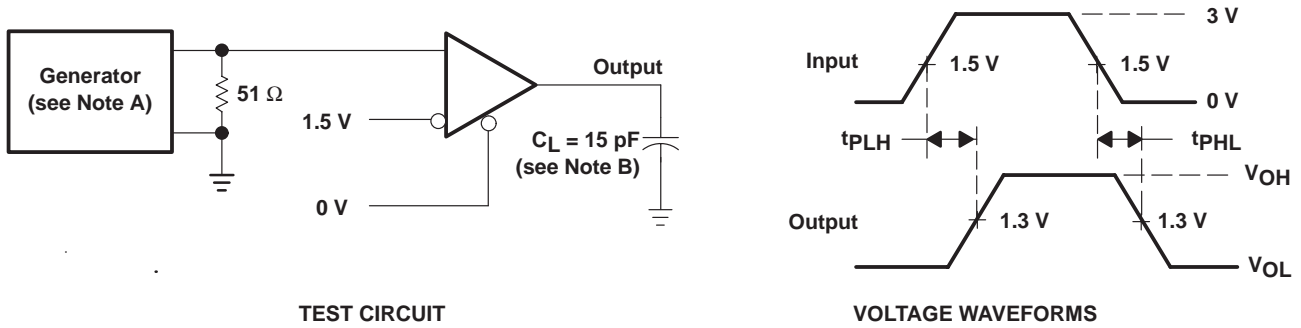


Figure 8. Receiver V_{OH} and V_{OL}



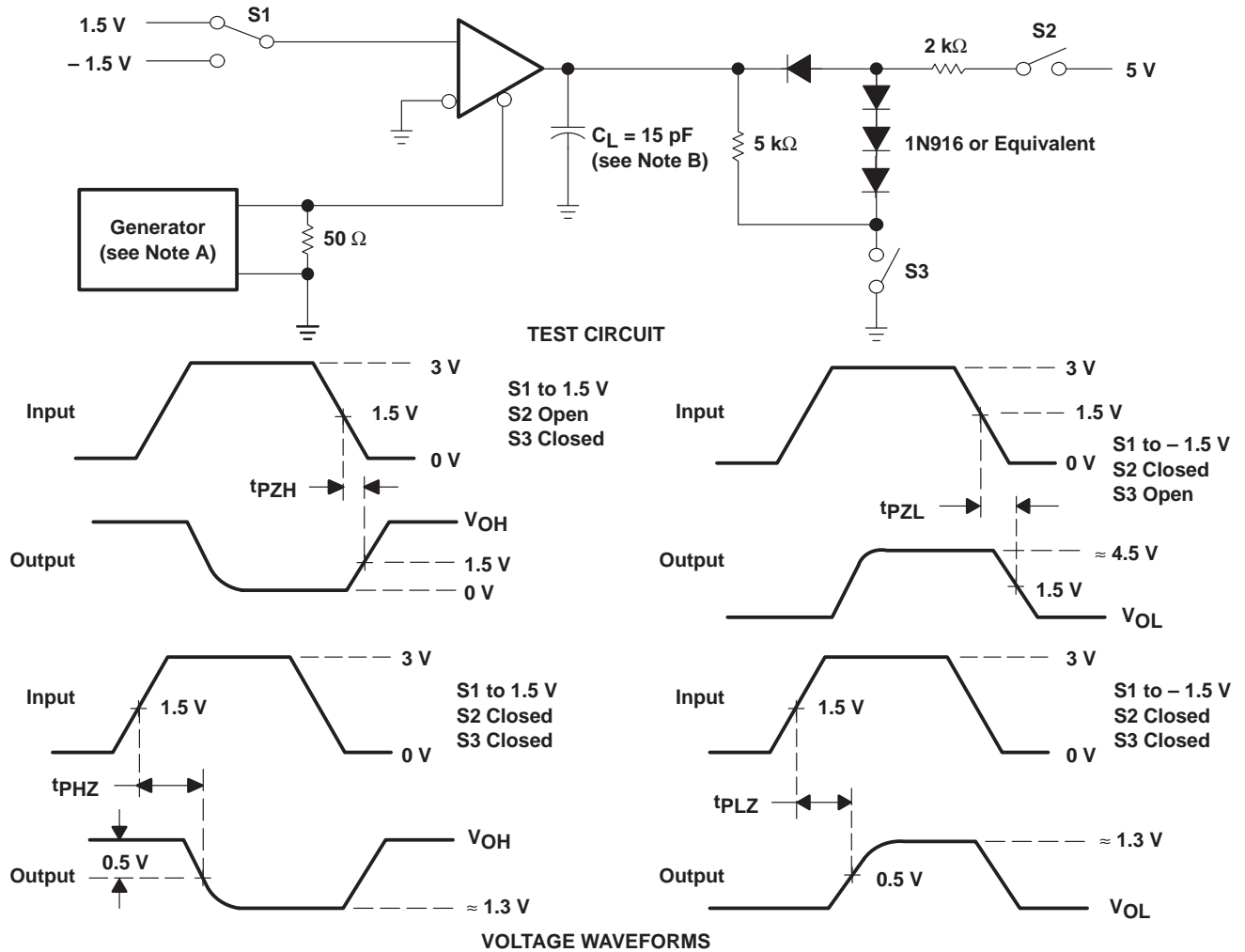
TEST CIRCUIT

VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 9. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 10. Receiver Test Circuit and Voltage Waveforms

SN75ALS171, SN75ALS171A TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

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TYPICAL CHARACTERISTICS

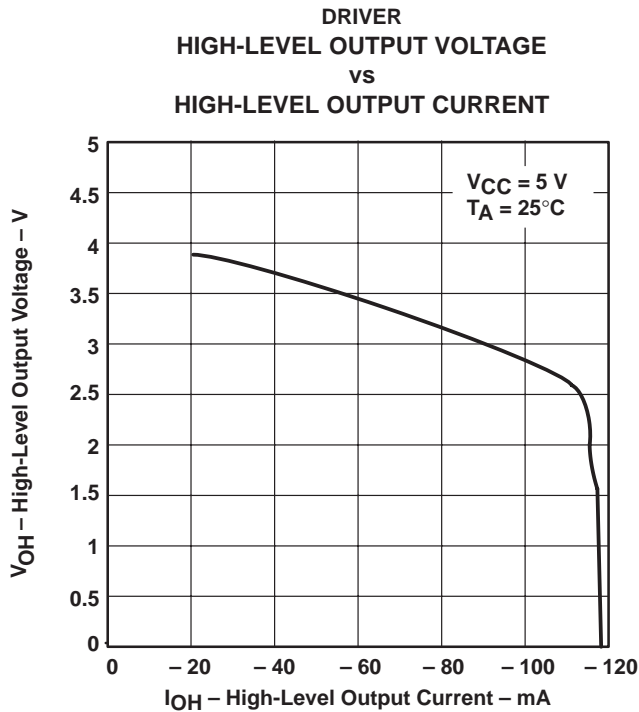


Figure 11

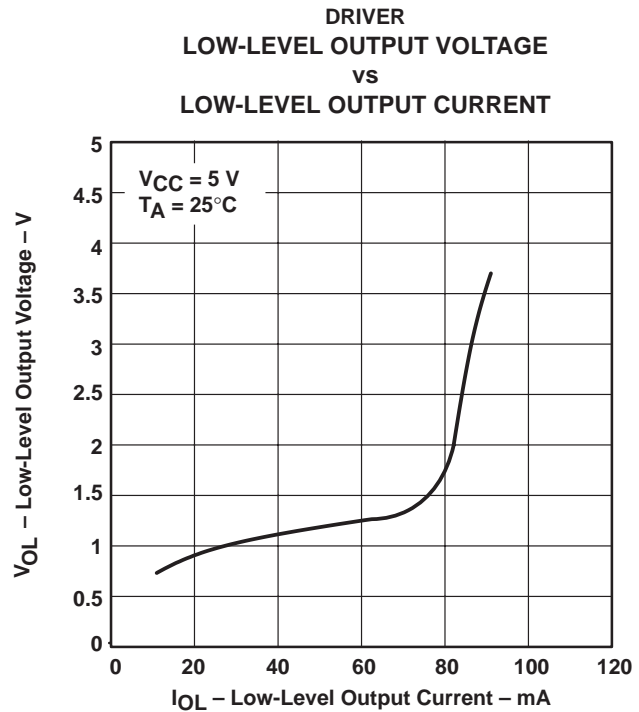


Figure 12

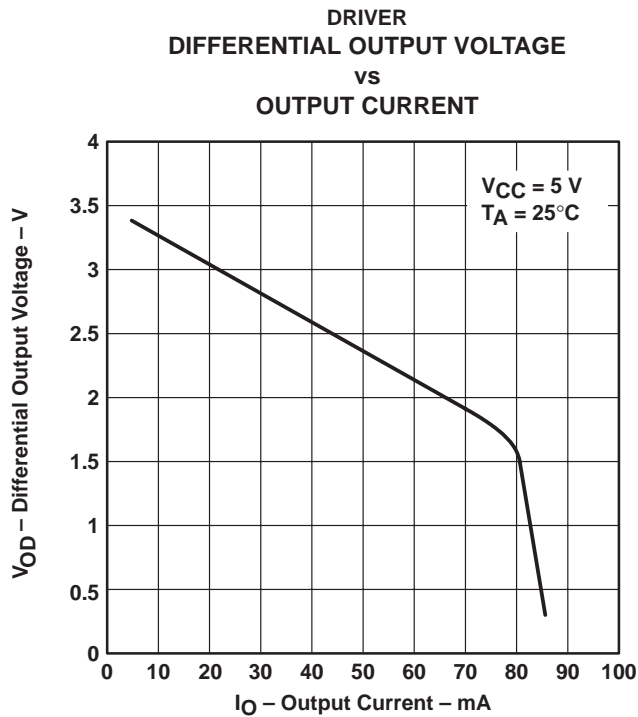


Figure 13



TYPICAL CHARACTERISTICS

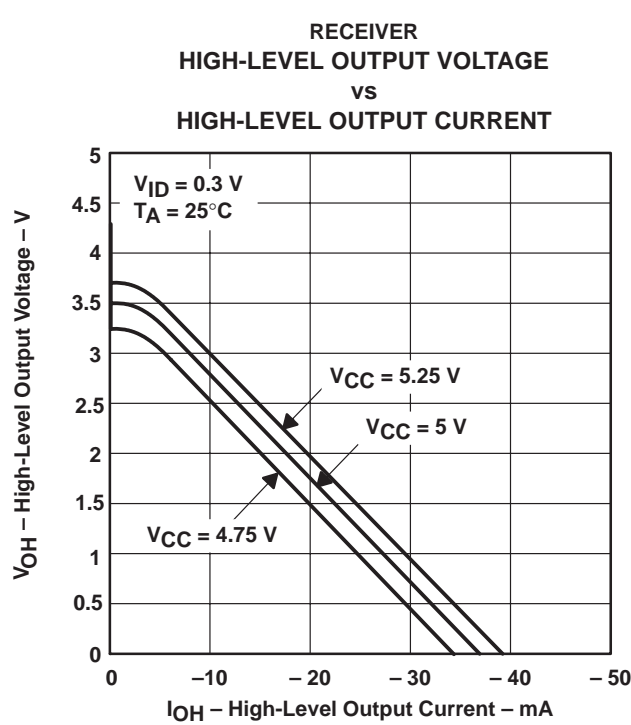


Figure 14

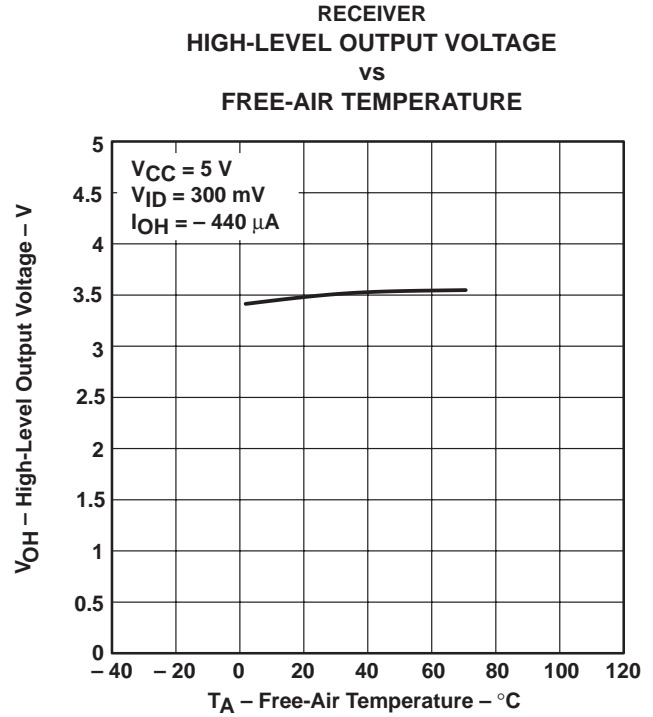


Figure 15

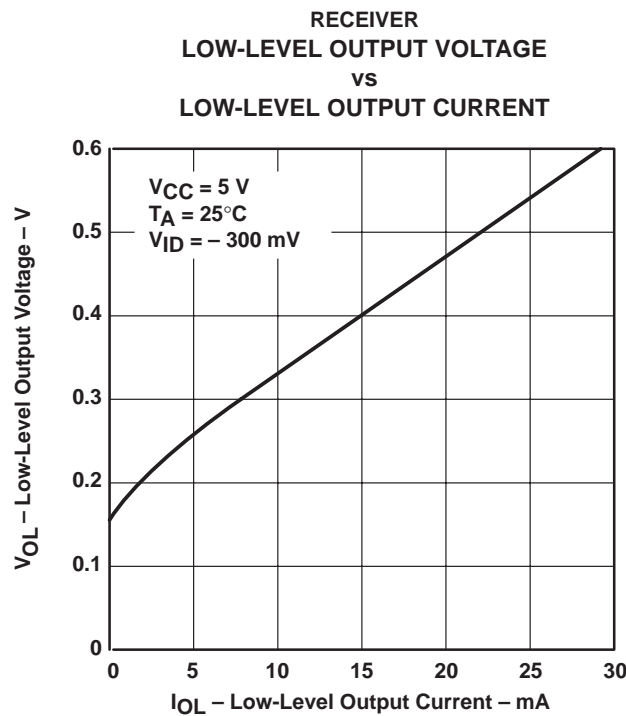


Figure 16

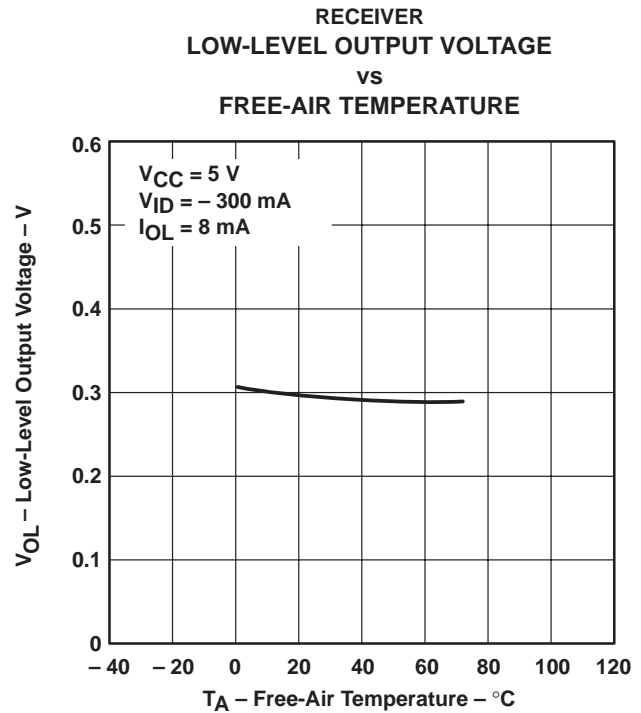


Figure 17

SN75ALS171, SN75ALS171A TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

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TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

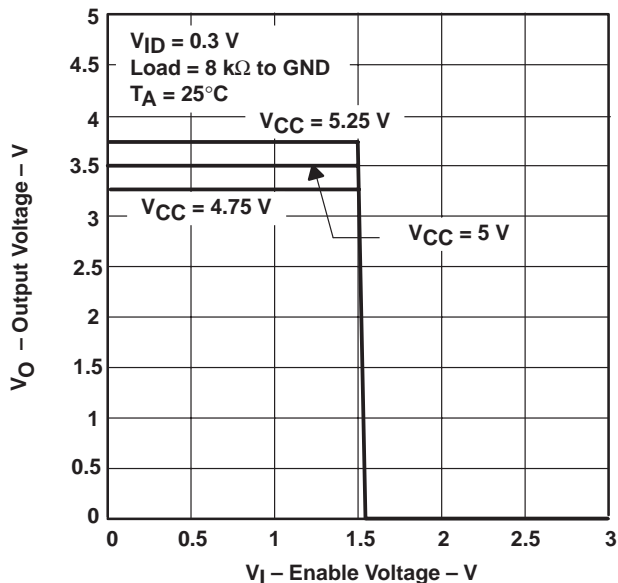


Figure 18

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

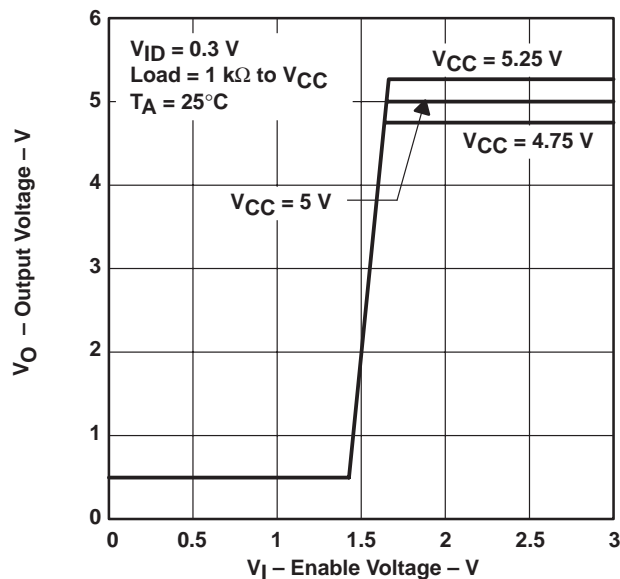
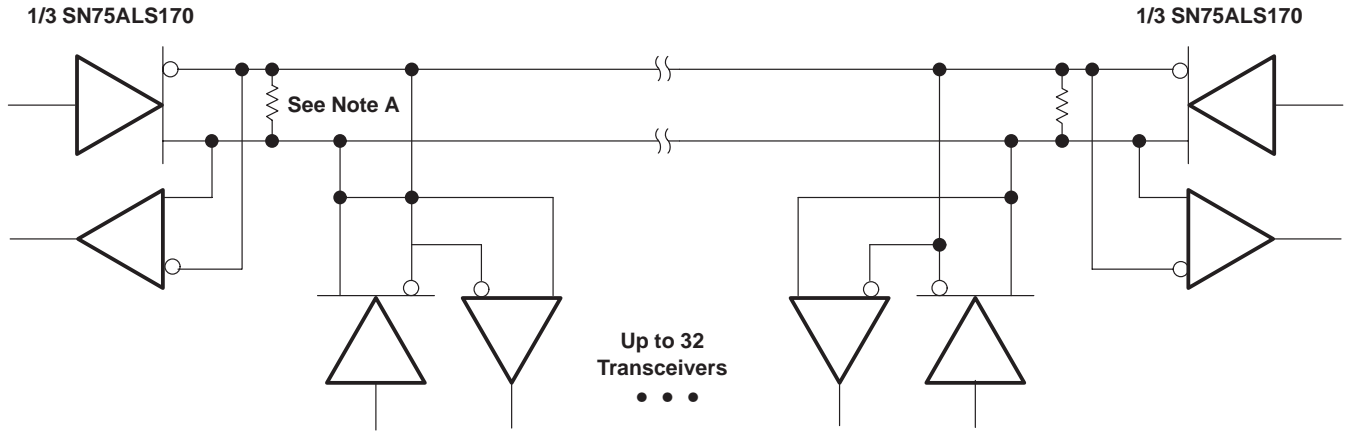


Figure 19

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 20. Typical Application Circuit

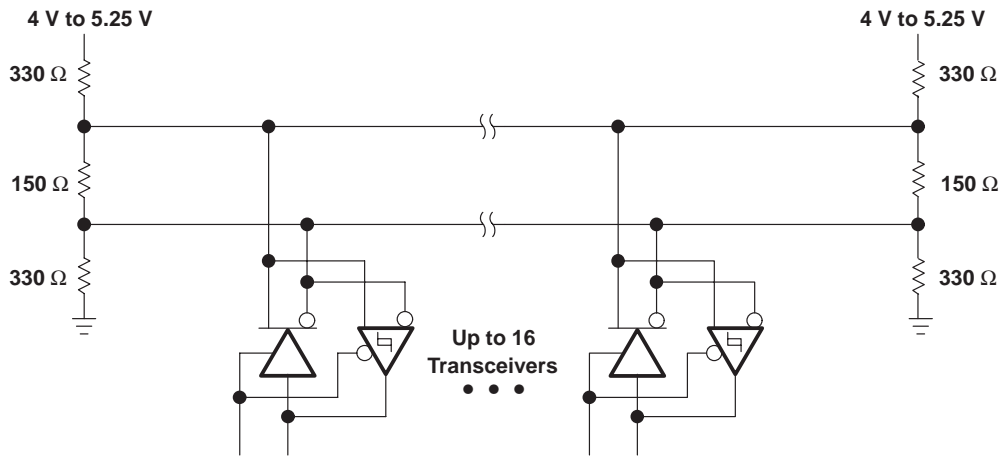


Figure 21. Typical Differential SCSI Application Circuit

SN75ALS171, SN75ALS171A TRIPLE DIFFERENTIAL BUS TRANSCEIVERS

SLLS056D – AUGUST 1987 – REVISED SEPTEMBER 1995

APPLICATION INFORMATION

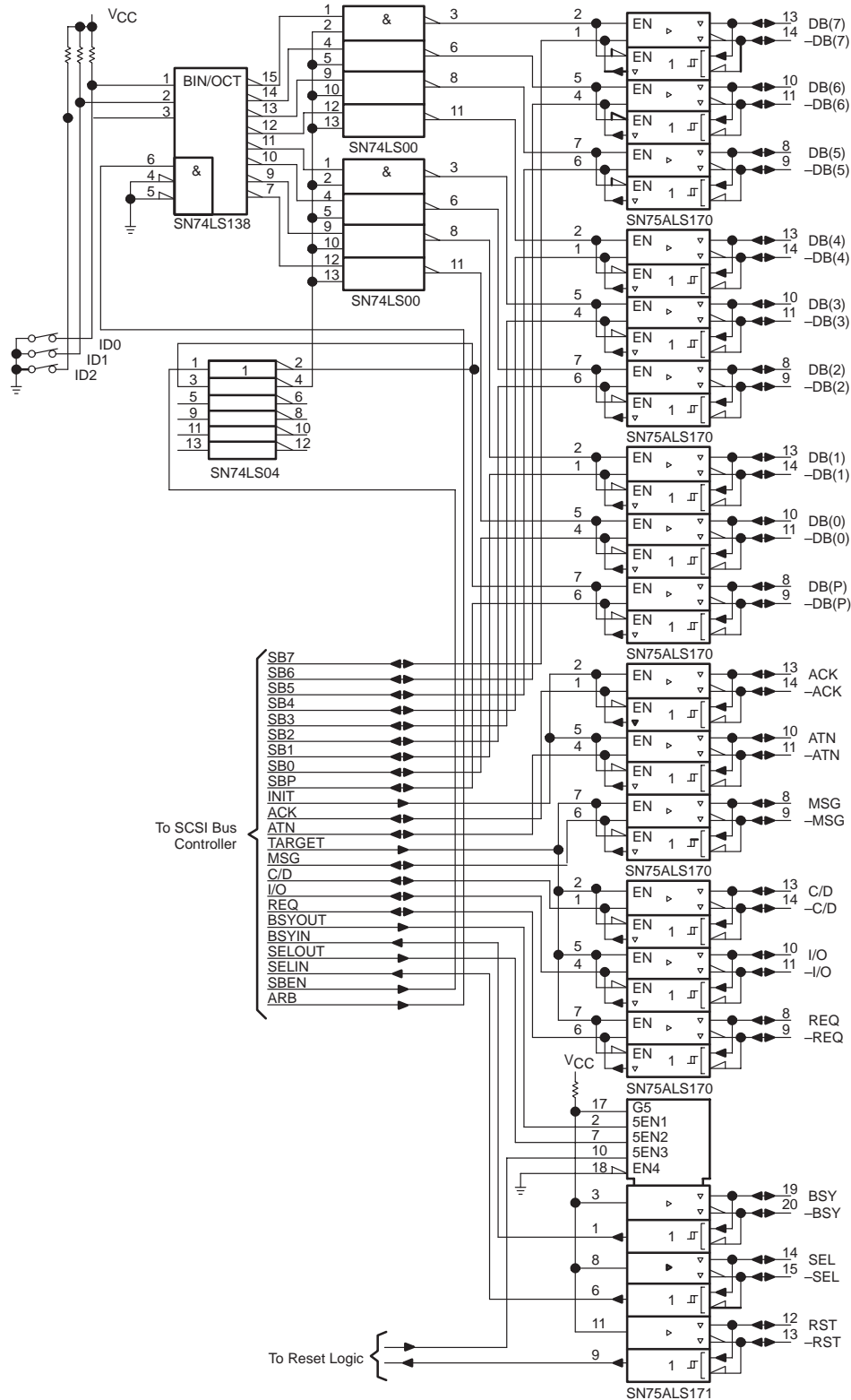


Figure 22. Typical Differential SCSI Bus Interface Implementation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS171ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS171A	Samples
SN75ALS171DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS171	Samples
SN75ALS171DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS171	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS171DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS171DWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS171ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75ALS171DW	DW	SOIC	20	25	506.98	12.7	4826	6.6

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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