420-MHz HIGH-SPEED CURRENT-FEEDBACK AMPLIFIER

Check for Samples: THS3001

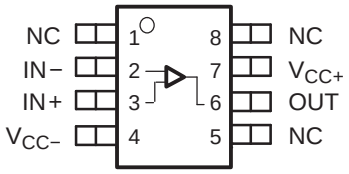
FEATURES

- **High Speed:**
  - **420-MHz Bandwidth (G = 1, -3 dB)**
  - **6500-V/µs Slew Rate**
  - **40-ns Settling Time (0.1%)**
- **High Output Drive: I_O = 100 mA**
- **Excellent Video Performance**
  - **115-MHz Bandwidth (0.1 dB, G = 2)**
  - **0.01% Differential Gain**
  - **0.02° Differential Phase**
- **Low 3-mV (max) Input Offset Voltage**
- **Very Low Distortion:**
  - **THD = –96 dBc at f = 1 MHz**
  - **THD = –80 dBc at f = 10 MHz**
- **Wide Range of Power Supplies:**
  - **V_{CC} = ±4.5 V to ±16 V**
- **Evaluation Module Available**

APPLICATIONS

- **Communication**
- **Imaging**
- **High-Quality Video**

THS3001
D OR DGN PACKAGE
(TOP VIEW)



NC – No internal connection

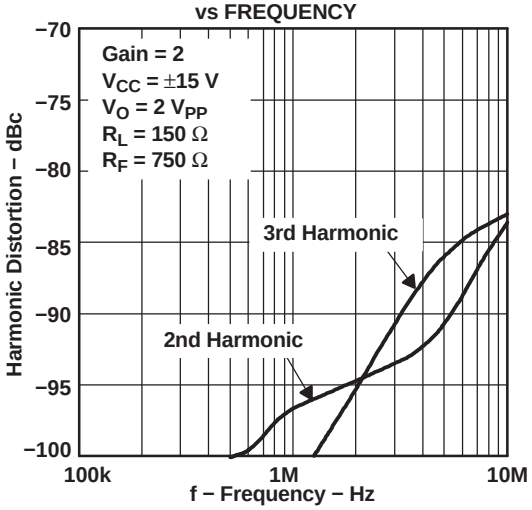
RELATED DEVICES

THS4011 /2	290-MHz VFB High-Speed Amplifier
THS6012	500-mA CFB HIgh-Speed Amplifier
THS6022	250-mA CFB High-Speed Amplifier

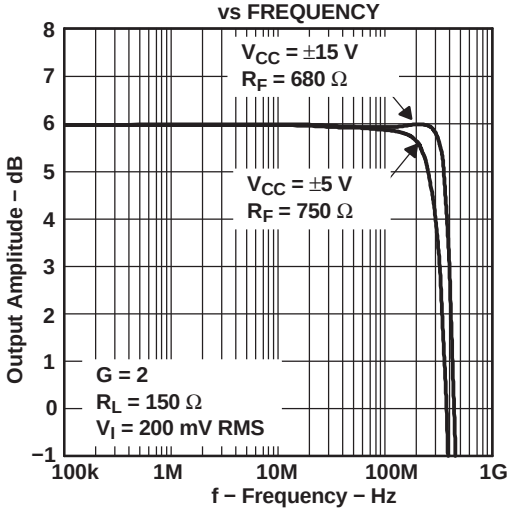
DESCRIPTION

The THS3001 is a high-speed current-feedback operational amplifier, ideal for communication, imaging, and high-quality video applications. This device offers a very fast 6500-V/µs slew rate, a 420-MHz bandwidth, and 40-ns settling time for large-signal applications requiring excellent transient response. In addition, the THS3001 operates with a very low distortion of –96 dBc, making it well suited for applications such as wireless communication basestations or ultrafast ADC or DAC buffers.

HARMONIC DISTORTION
vs FREQUENCY



OUTPUT AMPLITUDE
vs FREQUENCY



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICE			TRANSPORT MEDIA, QUANTITY	EVALUATION MODULE
	SOIC (D)	MSOP (DGN)	MSOP SYMBOL		
0°C to 70°C	THS3001CD	THS3001CDGN	ADP	Rails, 75	THS3001EVM
	THS3001CDR	THS3001CDGNR		Tape and Reel, 2500	--
		THS3001HVCDGN	BNK	Rails, 75	--
		THS3001HVCDGNR		Tape and Reel, 2500	--
-40°C to 85°C	THS3001ID	THS3001IDGN	ADQ	Rails, 75	--
	THS3001IDR	THS3001IDGNR		Tape and Reel, 2500	--
		THS3001HVIDGN	BNJ	Rails, 75	--
		THS3001HVIDGNR		Tape and Reel, 2500	--

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			THS3001	THS3001HV	UNITS
V_{SS}	Supply voltage, V_{CC+} to V_{CC-}		33	37	V
V_I	Input voltage		$\pm V_{CC}$	$\pm V_{CC}$	V
I_O	Output current		175	175	mA
V_{ID}	Differential input voltage		±6	±6	V
	Continuous total power dissipation		See Dissipation Rating Table		
T_J	Maximum junction temperature (2)		150	150	°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)		125	125	°C
T_A	Operating free-air temperature	THS3001C, THS3001HVC	0 to 70	0 to 70	°C
		THS3001I, THS3001HVI	–40 to 85	–40 to 85	°C
T_{stg}	Storage temperature		–65 to 125	–65 to 125	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (1) (°C/W)	POWER RATING (2)	
			$T_A \le 25°C$	$T_A = 85°C$
D (8)	38.3	97.5	1.02 W	410 mW
DGN (8)	4.7	58.4	1.71 W	685 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

RECOMMENDED OPERATING CONDITIONS

				MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage, V_{CC+} and V_{CC-}	Split supply	THS3001C, THS3001I	±4.5		±16	V
		Single supply		9		32	
		Split supply	THS3001HVC, THS3001HVI	±4.5		±18.5	
		Single supply		9		37	
T_A	Operating free-air temperature	THS3001C, THS3001HVC		0		70	°C
		THS3001I, THS3001HVI		-40		85	

ELECTRICAL CHARACTERISTICS

At T_A = 25°C, R_L = 150 Ω , R_F = 1 kΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS (1)		MIN	TYP	MAX	UNIT
V_{CC}	Power supply operating range		Split supply	THS3001C THS3001I	±4.5		±16.5	V
				THS3001HVx	±4.5		±18.5	
			Single supply	THS3001C THS3001I	9		33	
				THS3001HVx	9		37	
I_{CC}	Quiescent current		V_{CC} = ±5 V	T_A = 25°C		5.5	7.5	mA
				T_A = full range			8.5	
			V_{CC} = ±15 V	T_A = 25°C		6.6	9	
				T_A = full range			10	
			V_{CC} = ±18.5 V, THS3001HV	T_A = 25°C		6.9	9.5	
				T_A = full range			10.5	
V_O	Output voltage swing		V_{CC} = ±5 V	R_L = 150 Ω	±2.9	±3.2		V
				R_L = 1 kΩ	±3	±3.3		
			V_{CC} = ±15 V	R_L = 150 Ω	±12.1	±12.8		
				R_L = 1 kΩ	±12.8	±13.1		
I_O	Output current (2)		V_{CC} = ±5 V,	R_L = 20 Ω		100		mA
			V_{CC} = ±15 V,	R_L = 75 Ω	85	120		
V_{IO}	Input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	3	mV
				T_A = full range			4	
	Input offset voltage drift		V_{CC} = ±5 V or ±15 V			5		µV/°C
I_{IB}	Input bias current	Positive (IN+)	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	10	µA
				T_A = full range			15	
		Negative (IN-)		T_A = 25°C		1	10	
				T_A = full range			15	
V_{ICR}	Common-mode input voltage range		V_{CC} = ±5 V		±3	±3.2		V
			V_{CC} = ±15 V		±12.9	±13.2		
	Open loop transresistance		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ			1.3		MΩ
			V_{CC} = ±15 V, V_O = ±7.5 V, R_L = 1 kΩ			2.4		
CMRR	Common-mode rejection ratio		V_{CC} = ±5 V, V_{CM} = ±2.5 V		62	70		dB
			V_{CC} = ±15 V, V_{CM} = ±10 V		65	73		
PSRR	Power supply rejection ratio		V_{CC} = ±5 V	T_A = 25°C	65	76		dB
				T_A = full range	63			
			V_{CC} = ±15 V	T_A = 25°C	69	76		dB
				T_A = full range	67			

(1) Full range = 0°C to 70°C for the THS3001C and -40°C to 85°C for the THS3001I.
(2) Observe power dissipation ratings to keep the junction temperature below absolute maximum when the output is heavily loaded or shorted. See Absolute Maximum Ratings table.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = 25°C, R_L = 150 Ω , R_F = 1 kΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
R_I	Input resistance	Positive (IN+)			1.5		MΩ
		Negative (IN-)			15		Ω
C_I	Differential input capacitance				7.5		pF
R_O	Output resistance		Open loop at 5 MHz		10		Ω
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V, f = 10 kHz, G = 2		1.6		nV/√Hz
I_n	Input current noise	Positive (IN+)	V_{CC} = ±5 V or ±15 V, f = 10 kHz, G = 2		13		pA/√Hz
		Negative (IN-)			16		

OPERATING CHARACTERISTICS

T_A = 25°C, R_L = 150 Ω , R_F = 1 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate (1)	V_{CC} = ±5 V, $V_{O(PP)}$ = 4 V	G = –5		1700		V/µs
			G = 5		1300		
		V_{CC} = ±15 V, $V_{O(PP)}$ = 20 V	G = –5		6500		
			G = 5		6300		
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 0 V to 10 V Step	Gain = –1,		40		ns
	Settling time to 0.1%	V_{CC} = ±5 V, 0 V to 2 V Step,	Gain = –1,		25		
THD	Total harmonic distortion	V_{CC} = ±15 V, f_c = 10 MHz,	$V_{O(PP)}$ = 2 V, G = 2		–80		dBc
	Differential gain error	G = 2, 40 IRE modulation, ±100 IRE Ramp, NTSC and PAL	V_{CC} = ±5 V		0.015%		
			V_{CC} = ±15 V		0.01%		
	Differential phase error	G = 2, 40 IRE modulation, ±100 IRE Ramp, NTSC and PAL	V_{CC} = ±5 V		0.01°		
			V_{CC} = ±15 V		0.02°		
BW	Small signal bandwidth (-3 dB)	G = 1, R_F = 1 kΩ	V_{CC} = ±5 V		330		MHz
			V_{CC}= ±15 V		420		MHz
		G = 2, R_F = 750 Ω,	V_{CC} = ±5 V		300		MHz
		G = 2, R_F = 680 Ω,	V_{CC} = ±15 V		385		
		G = 5, R_F = 560 Ω,	V_{CC} = ±15 V		350		
	Bandwidth for 0.1 dB flatness	G = 2, R_F = 750 Ω,	V_{CC} = ±5 V		85		MHz
		G = 2, R_F = 680 Ω,	V_{CC} = ±15 V		115		
	Full power bandwidth (2)	V_{CC} = ±5 V, $V_{O(PP)}$ = 4 V, R_L = 500 Ω	G = –5		65		MHz
			G = 5		62		
		V_{CC} = ±15 V, $V_{O(PP)}$ = 20 V, R_L = 500 Ω	G = –5		32		
			G = 5		31		

(1) Slew rate is measured from an output level range of 25% to 75%.
(2) Full power bandwidth is defined as the frequency at which the output has 3% THD.

PARAMETER MEASUREMENT INFORMATION

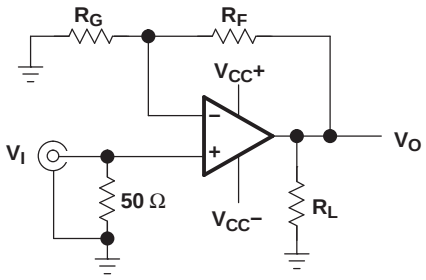


Figure 1. Test Circuit, Gain = 1 + (R_F/R_G)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$\|V_O\|$	Output voltage swing	vs Free-air temperature	2
I_{CC}	Current supply	vs Free-air temperature	3
I_{IB}	Input bias current	vs Free-air temperature	4
V_{IO}	Input offset voltage	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Common-mode input voltage	6
		vs Common-mode input voltage	7
		vs Frequency	8
	Transresistance	vs Free-air temperature	9
	Closed-loop output impedance	vs Frequency	10
V_n	Voltage noise	vs Frequency	11
I_n	Current noise	vs Frequency	11
PSRR	Power supply rejection ratio	vs Frequency	12
		vs Free-air temperature	13
SR	Slew rate	vs Supply voltage	14
		vs Output step peak-to-peak	15, 16
	Normalized slew rate	vs Gain	17
	Harmonic distortion	vs Peak-to-peak output voltage swing	18, 19
		vs Frequency	20, 21
	Differential gain	vs Loading	22, 23
	Differential phase	vs Loading	24, 25
	Output amplitude	vs Frequency	26-30
	Normalized output response	vs Frequency	31-34
	Small and large signal frequency response		35, 36
	Small signal pulse response		37, 38
	Large signal pulse response		39 - 46

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

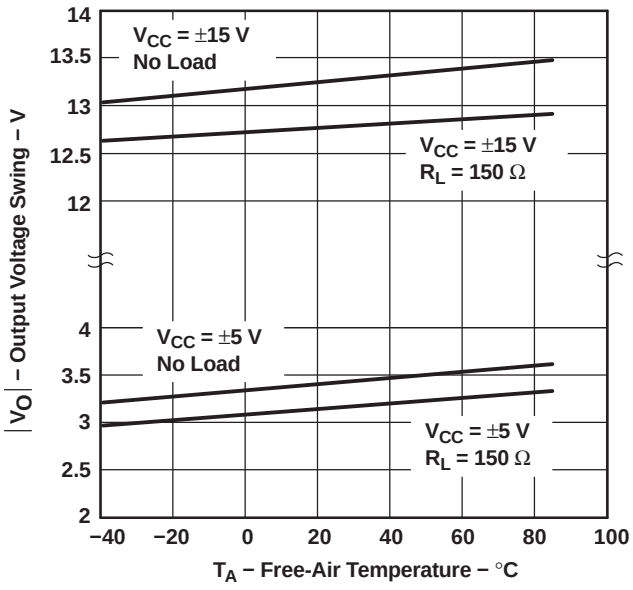


Figure 2.

CURRENT SUPPLY vs FREE-AIR TEMPERATURE

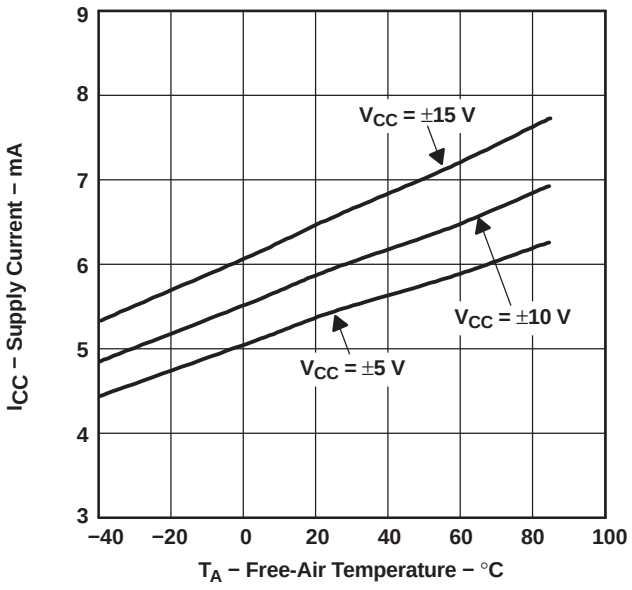


Figure 3.

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

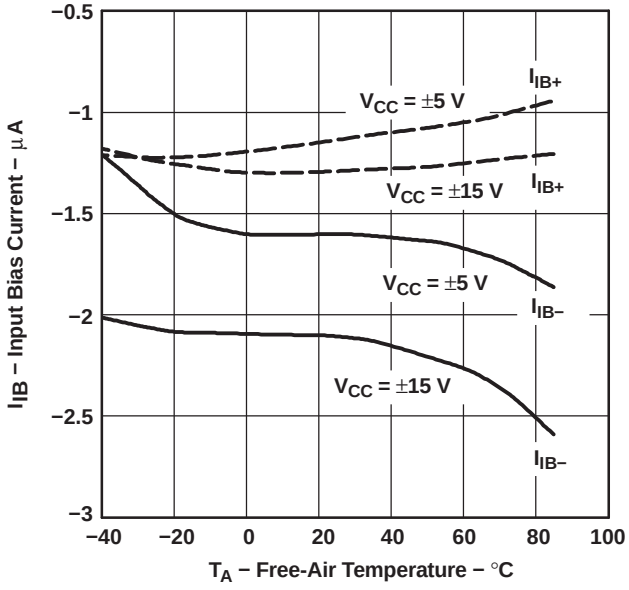


Figure 4.

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

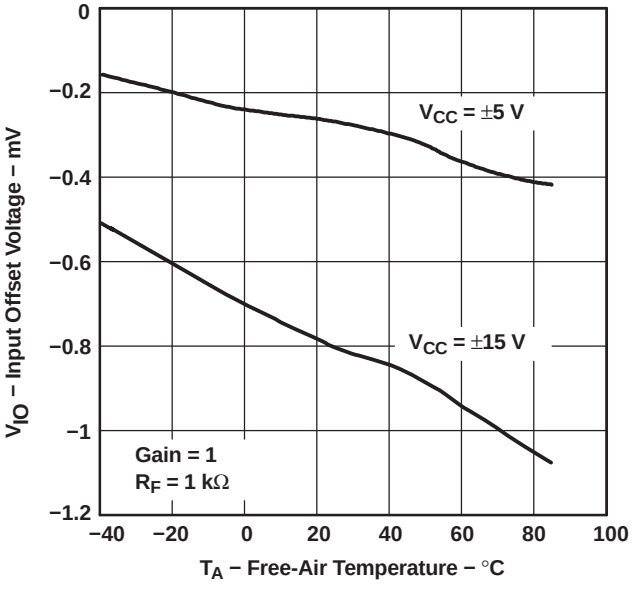


Figure 5.

TYPICAL CHARACTERISTICS (continued)

COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE

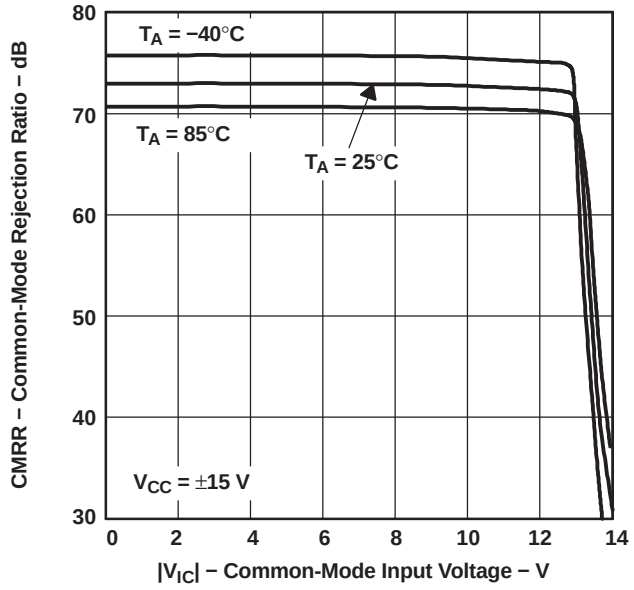


Figure 6.

COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE

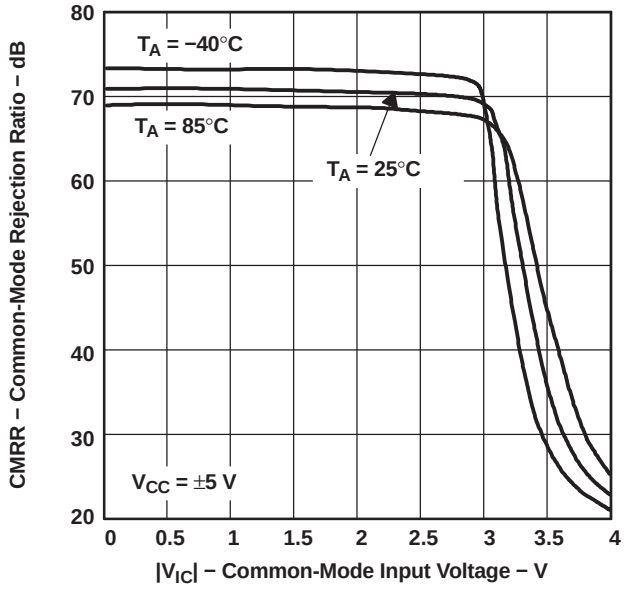


Figure 7.

COMMON-MODE REJECTION RATIO vs FREQUENCY

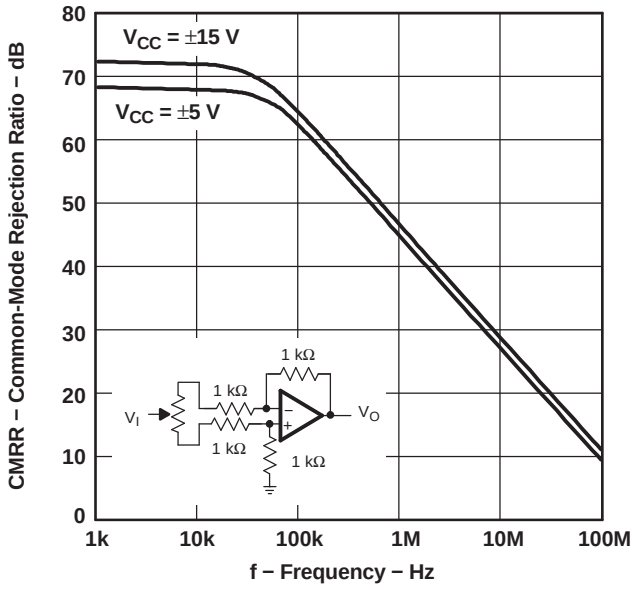


Figure 8.

TRANSRESISTANCE vs FREE-AIR TEMPERATURE

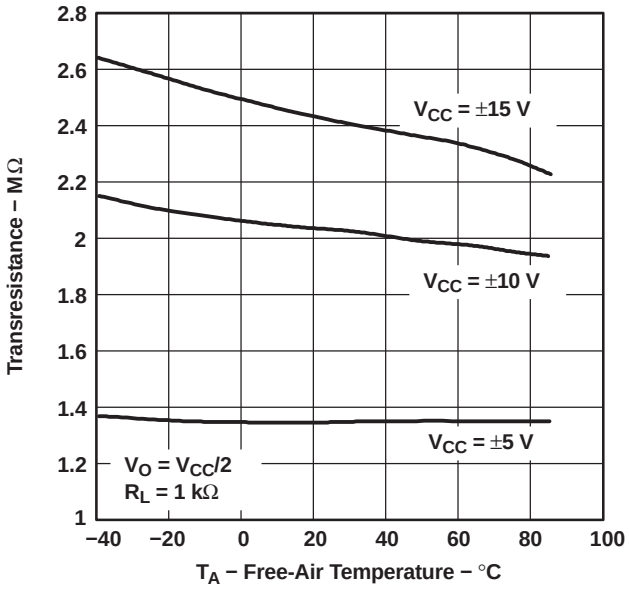


Figure 9.

TYPICAL CHARACTERISTICS (continued)

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

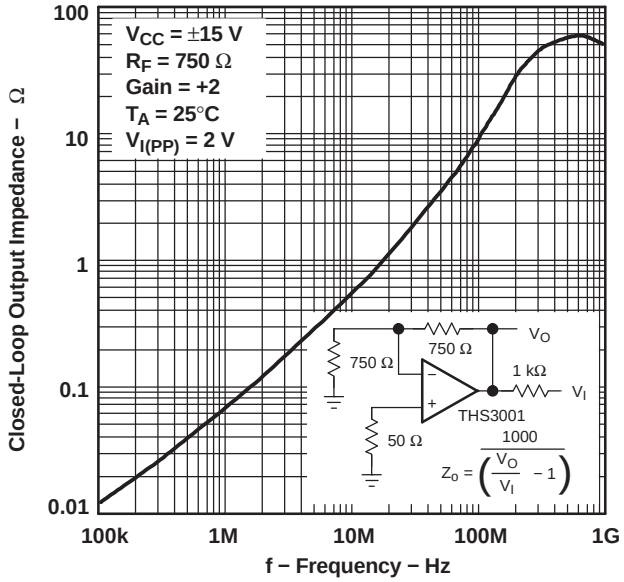


Figure 10.

VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY

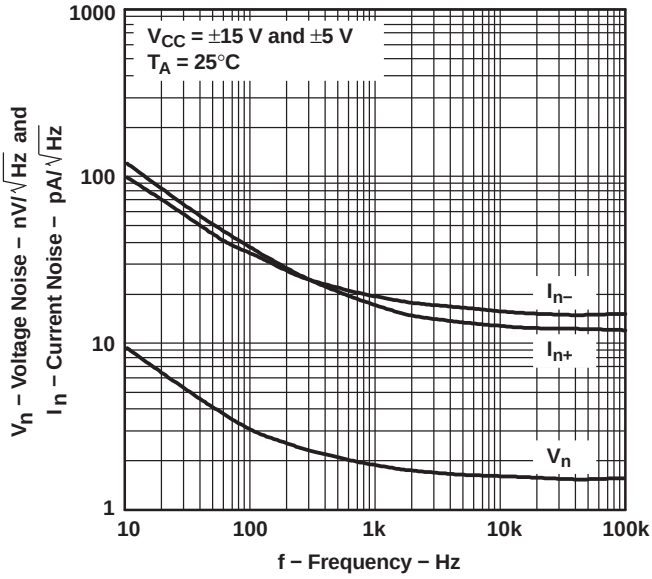


Figure 11.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

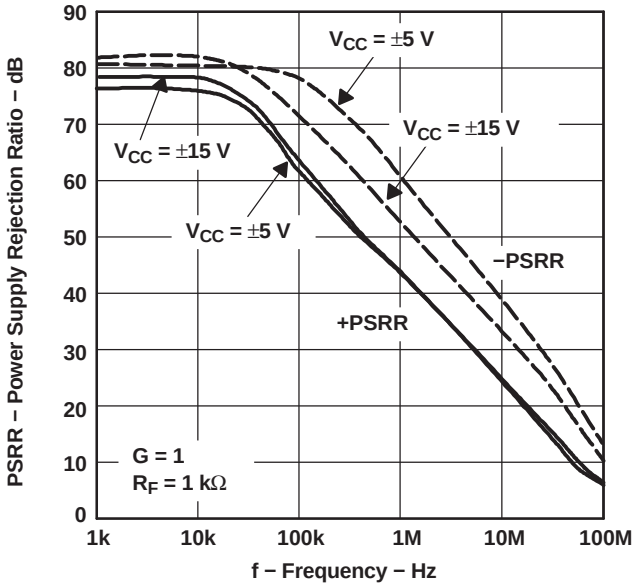


Figure 12.

POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

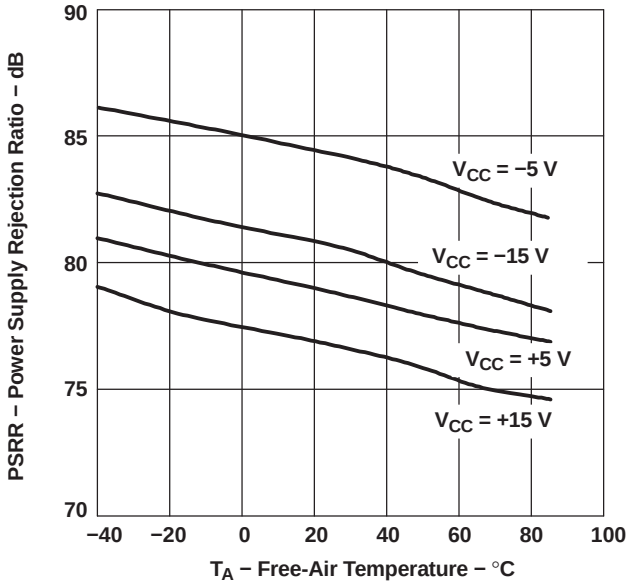


Figure 13.

TYPICAL CHARACTERISTICS (continued)

SLEW RATE vs SUPPLY VOLTAGE

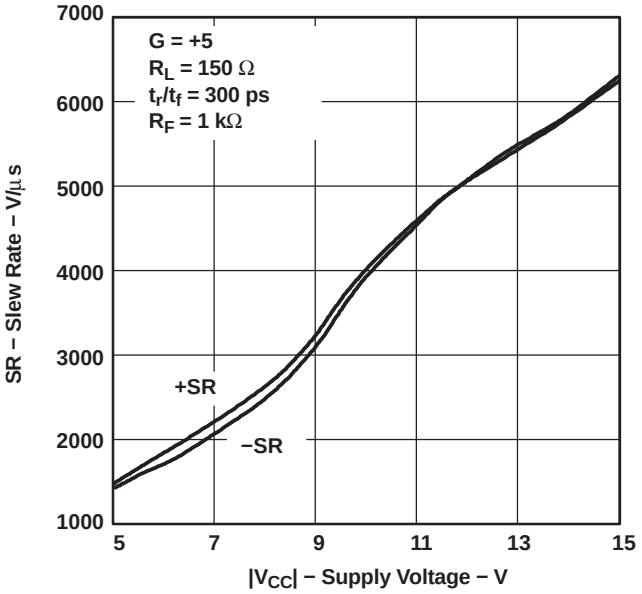


Figure 14.

SLEW RATE vs OUTPUT STEP

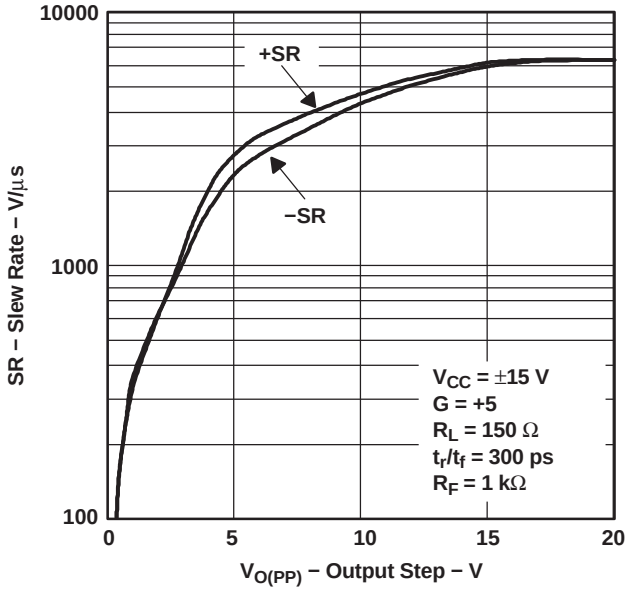


Figure 15.

SLEW RATE vs OUTPUT STEP

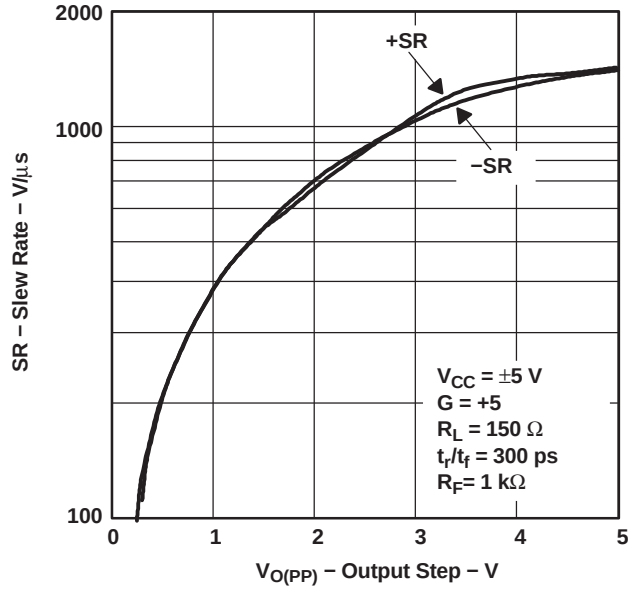


Figure 16.

NORMALIZED SLEW RATE vs GAIN

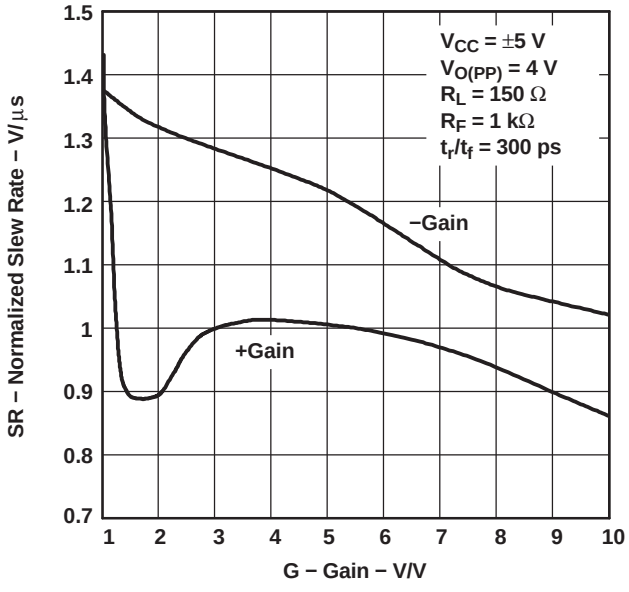


Figure 17.

TYPICAL CHARACTERISTICS (continued)

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE SWING

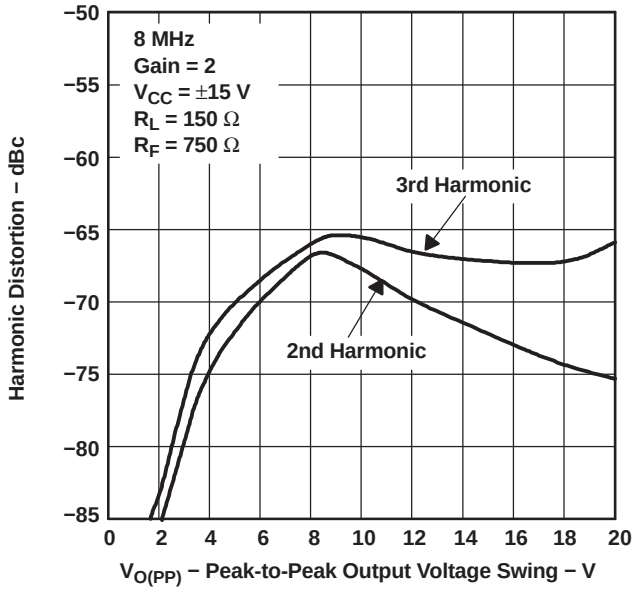


Figure 18.

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE SWING

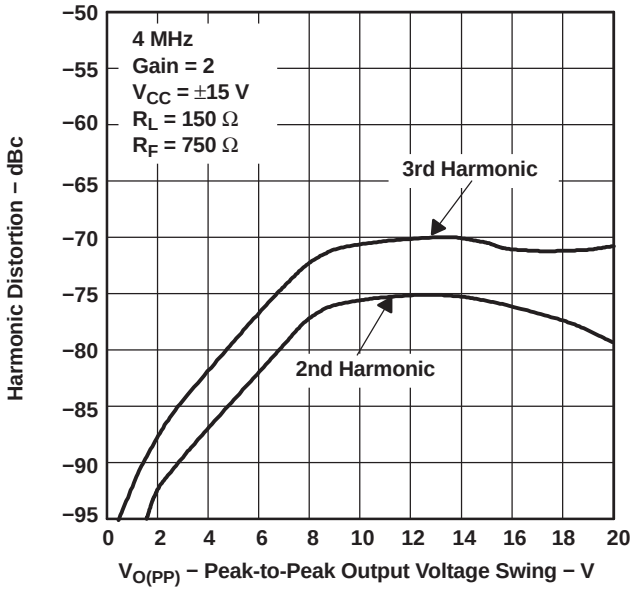


Figure 19.

HARMONIC DISTORTION
vs
FREQUENCY

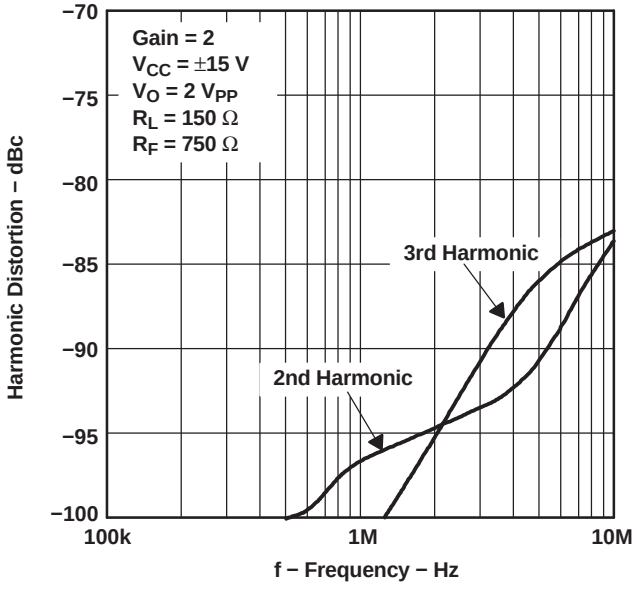


Figure 20.

HARMONIC DISTORTION
vs
FREQUENCY

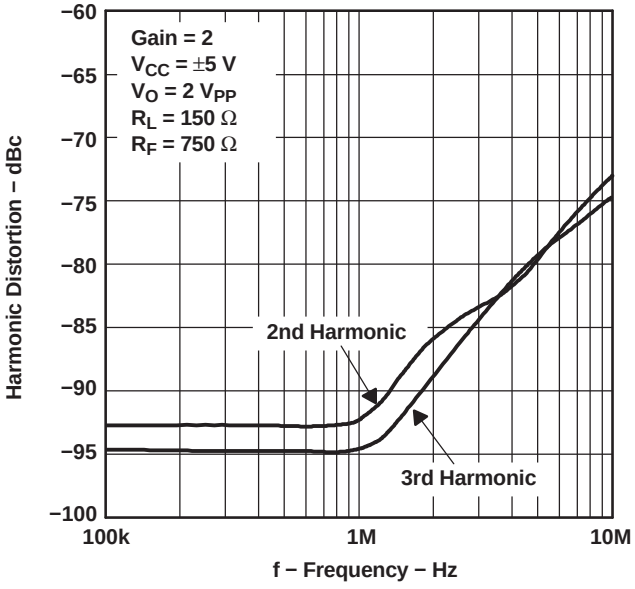


Figure 21.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL GAIN vs LOADING

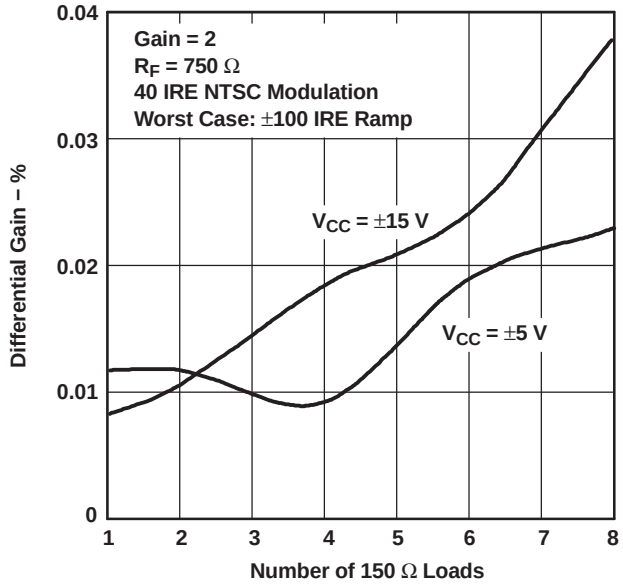


Figure 22.

DIFFERENTIAL GAIN vs LOADING

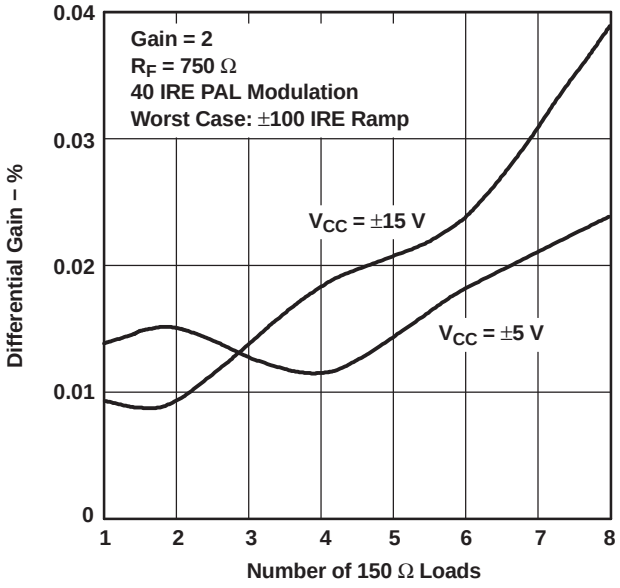


Figure 23.

DIFFERENTIAL PHASE vs LOADING

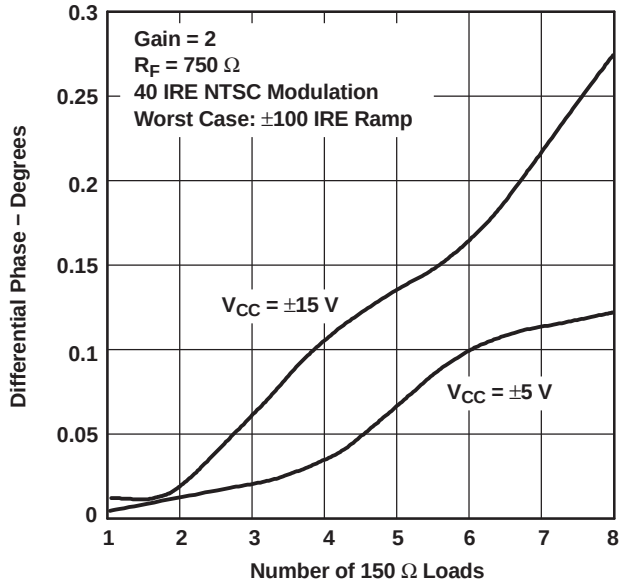


Figure 24.

DIFFERENTIAL PHASE vs LOADING

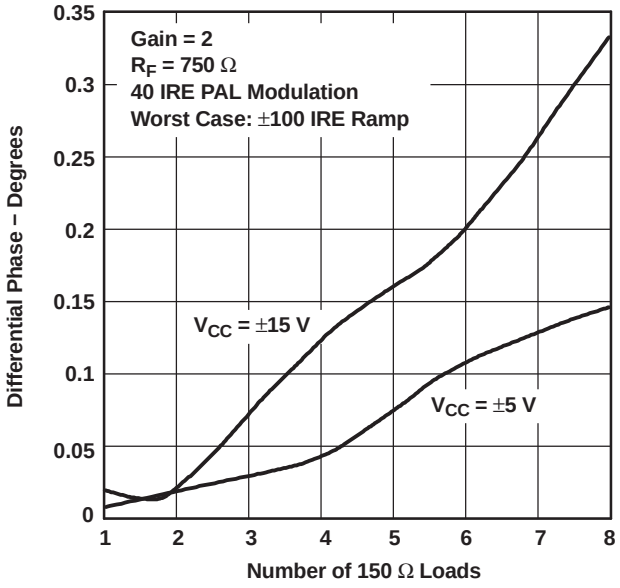


Figure 25.

TYPICAL CHARACTERISTICS (continued)

OUTPUT AMPLITUDE vs FREQUENCY

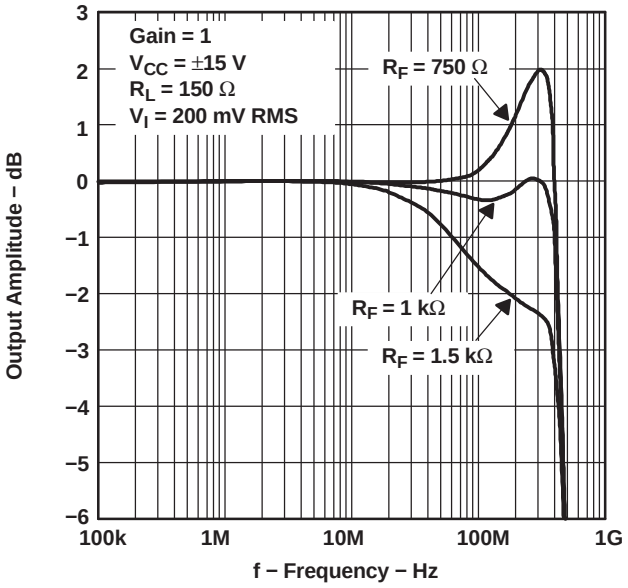


Figure 26.

OUTPUT AMPLITUDE vs FREQUENCY

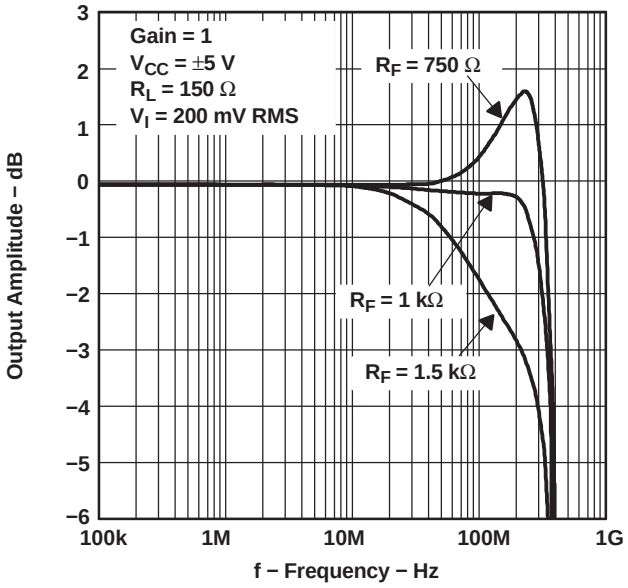


Figure 27.

OUTPUT AMPLITUDE vs FREQUENCY

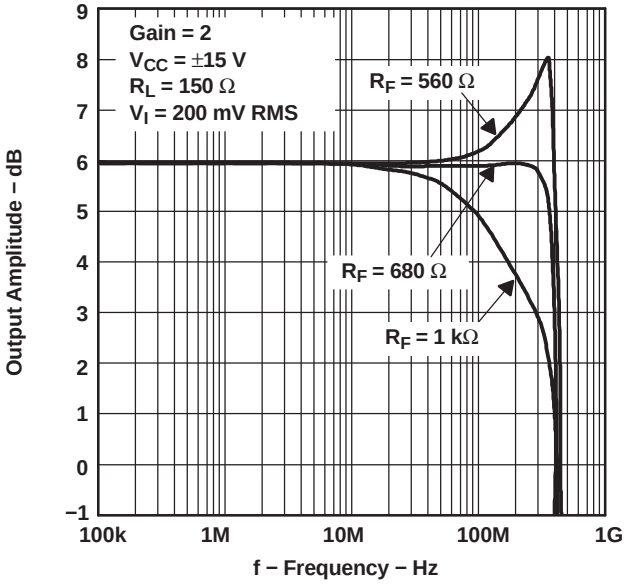


Figure 28.

OUTPUT AMPLITUDE vs FREQUENCY

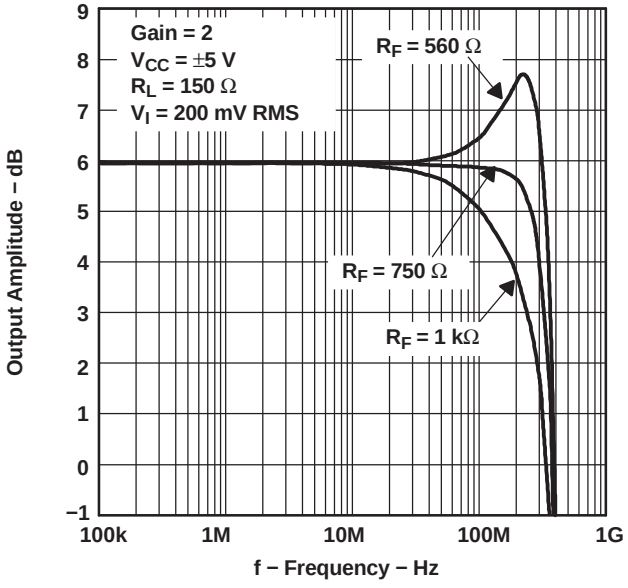


Figure 29.

TYPICAL CHARACTERISTICS (continued)

OUTPUT AMPLITUDE vs FREQUENCY

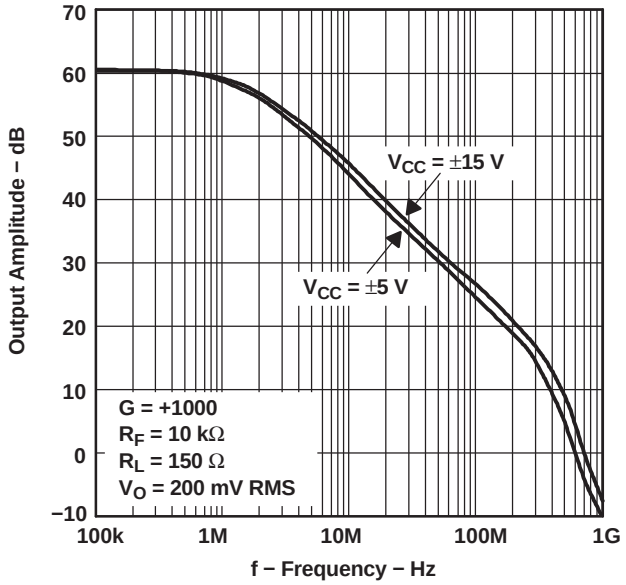


Figure 30.

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

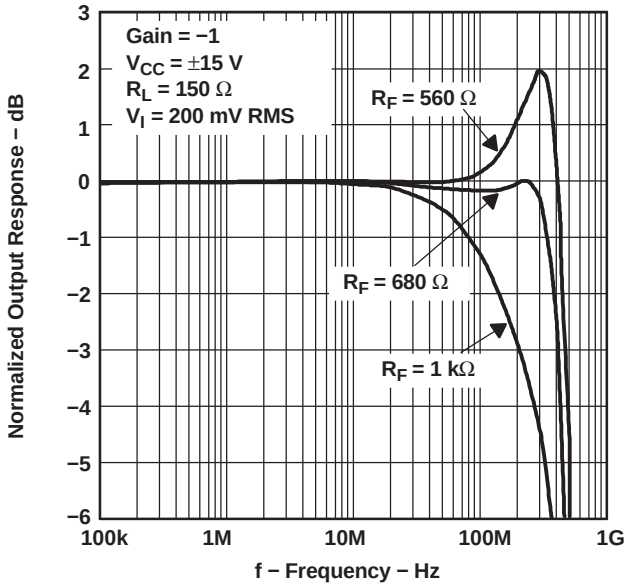


Figure 31.

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

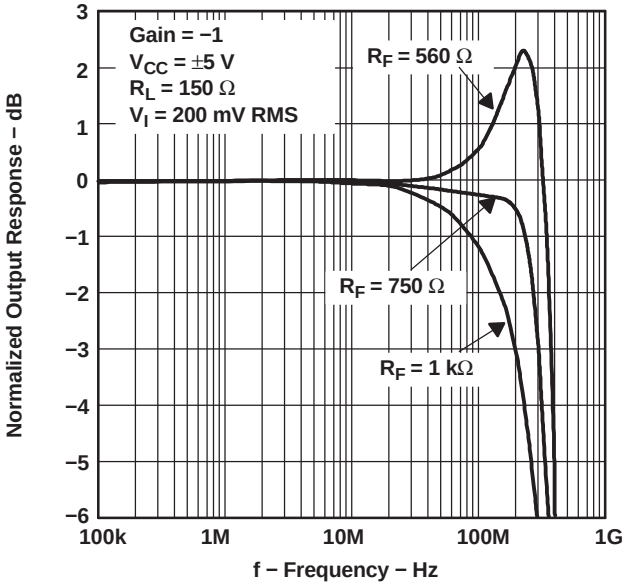


Figure 32.

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

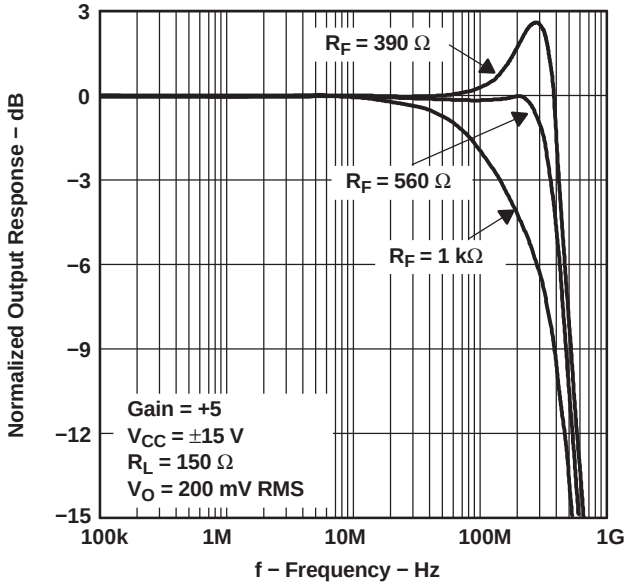


Figure 33.

TYPICAL CHARACTERISTICS (continued)

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

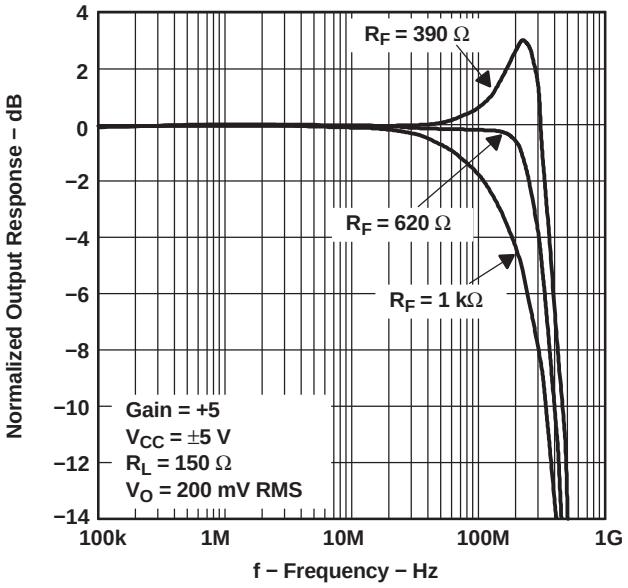


Figure 34.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

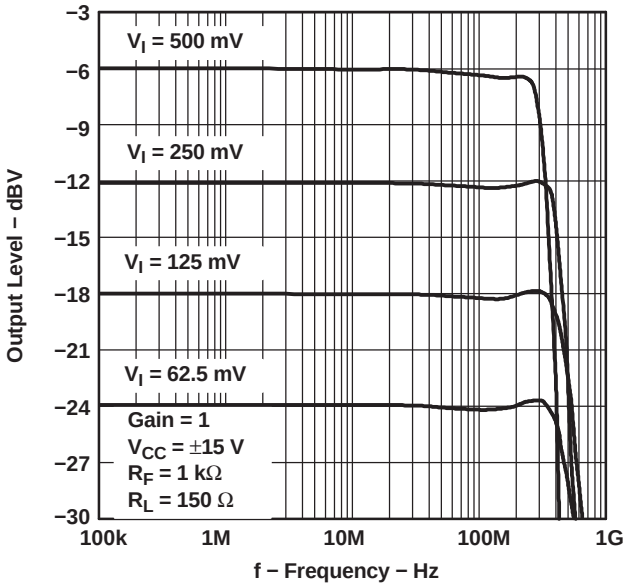


Figure 35.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

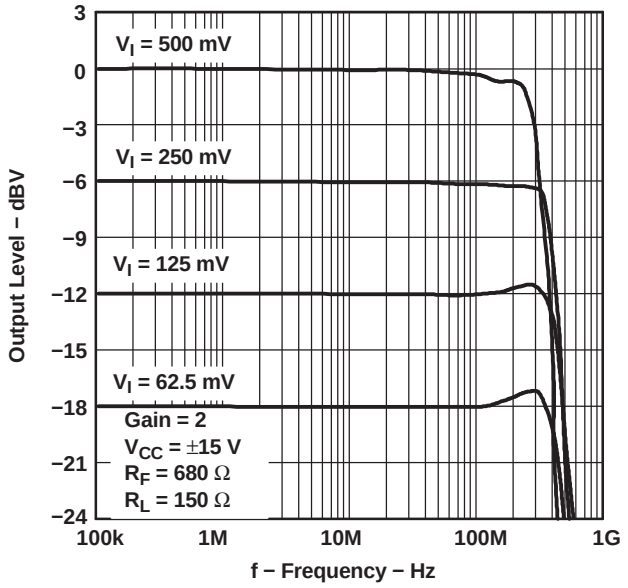


Figure 36.

SMALL SIGNAL PULSE RESPONSE

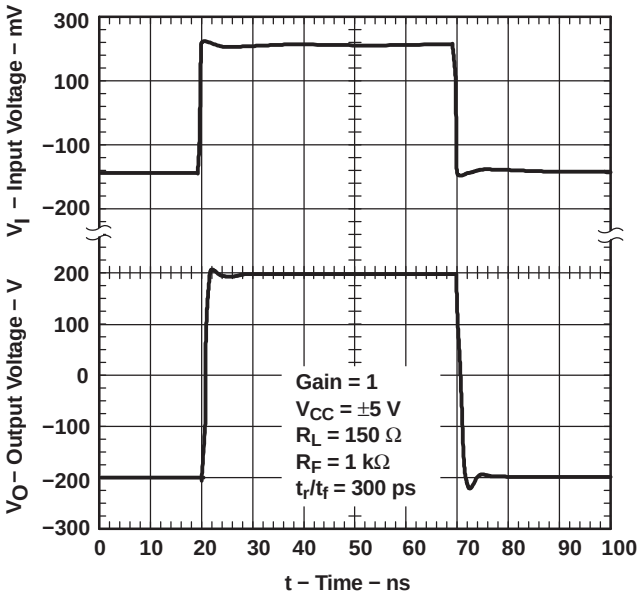


Figure 37.

TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL PULSE RESPONSE

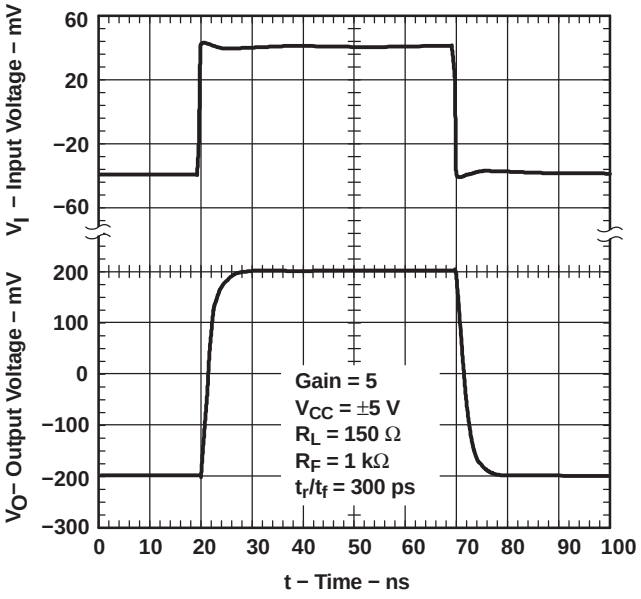


Figure 38.

LARGE SIGNAL PULSE RESPONSE

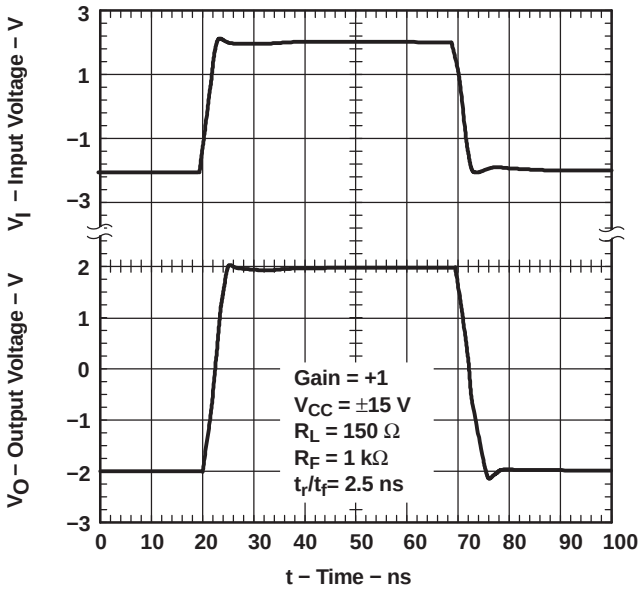


Figure 39.

LARGE SIGNAL PULSE RESPONSE

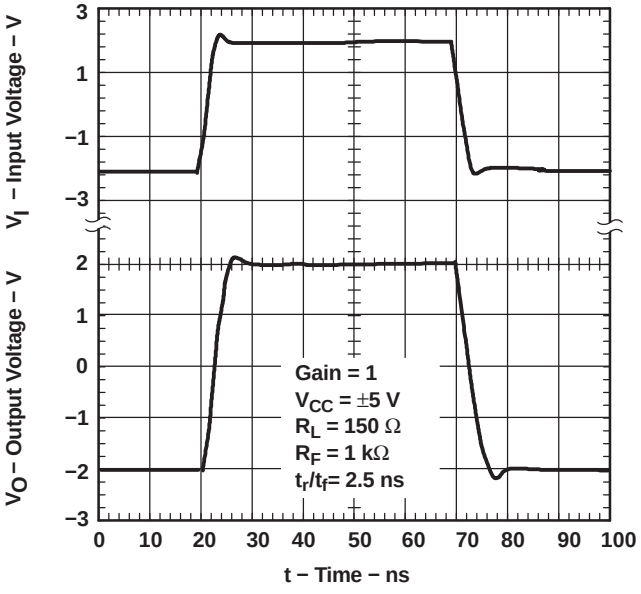


Figure 40.

LARGE SIGNAL PULSE RESPONSE

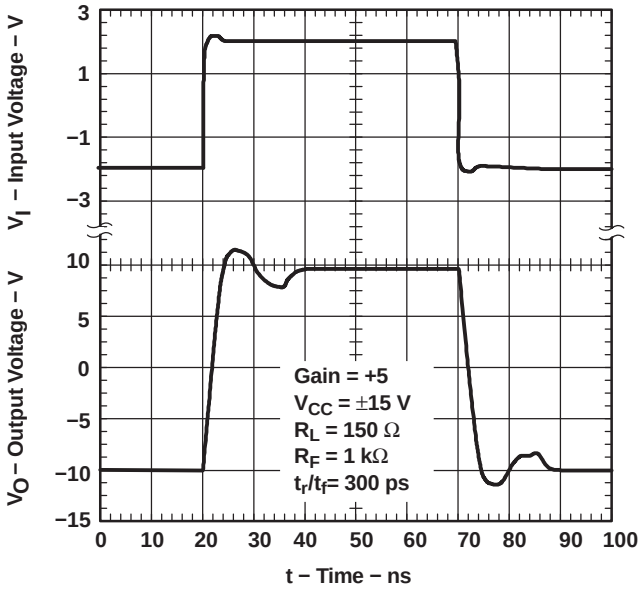


Figure 41.

TYPICAL CHARACTERISTICS (continued)

LARGE SIGNAL PULSE RESPONSE

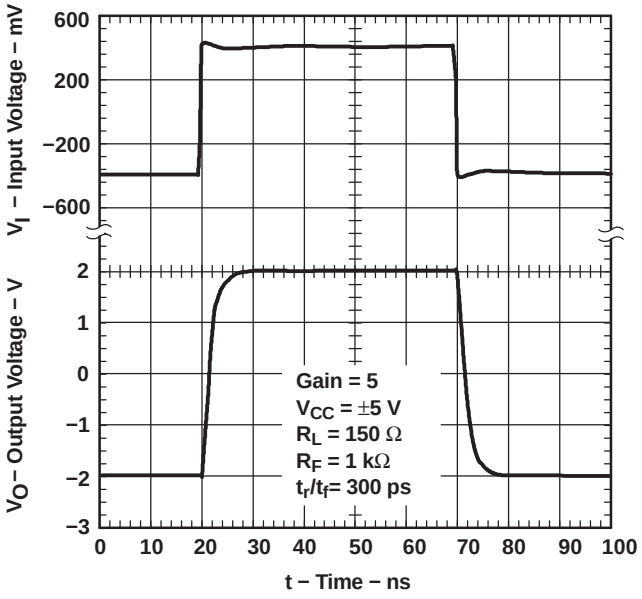


Figure 42.

LARGE SIGNAL PULSE RESPONSE

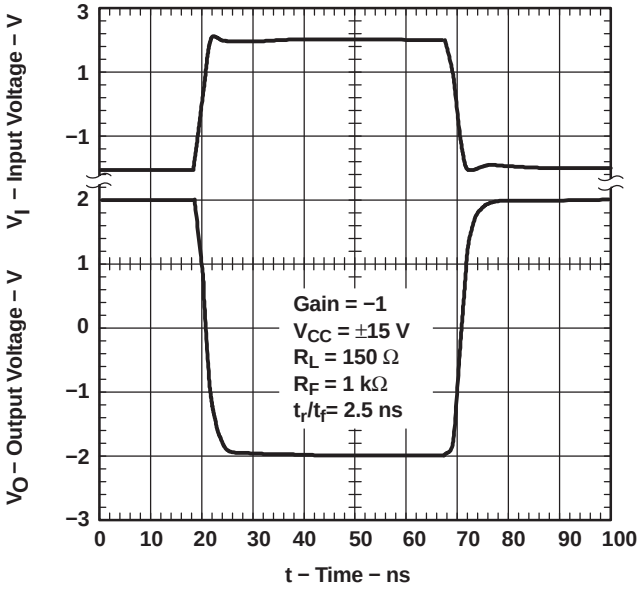


Figure 43.

LARGE SIGNAL PULSE RESPONSE

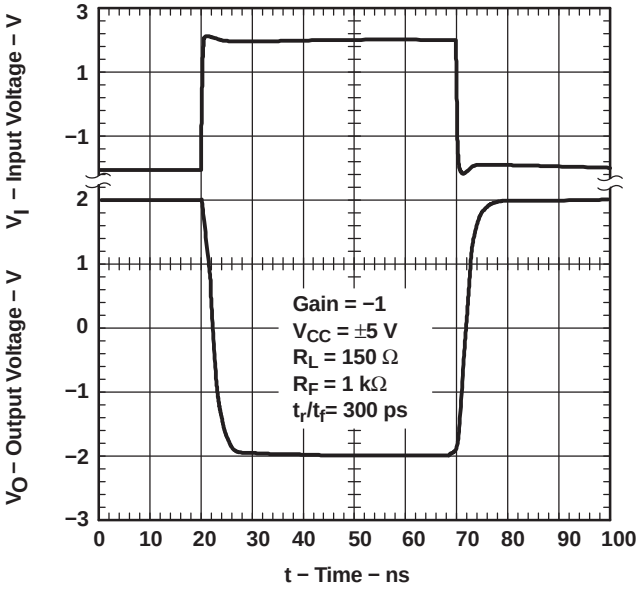


Figure 44.

LARGE SIGNAL PULSE RESPONSE

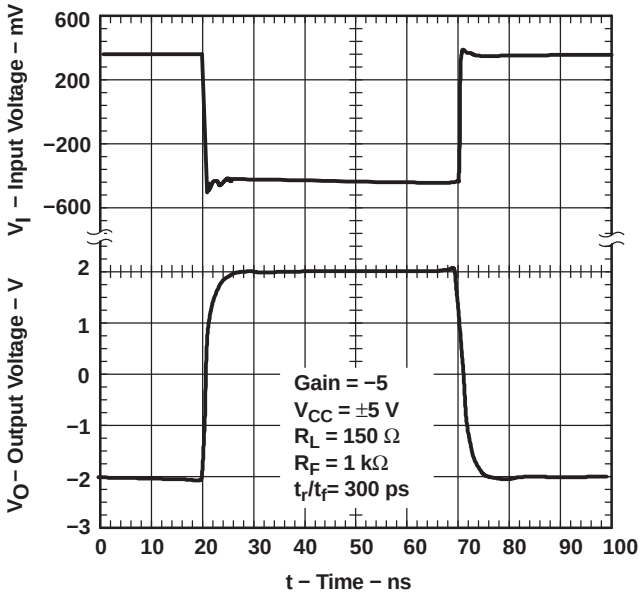


Figure 45.

TYPICAL CHARACTERISTICS (continued)

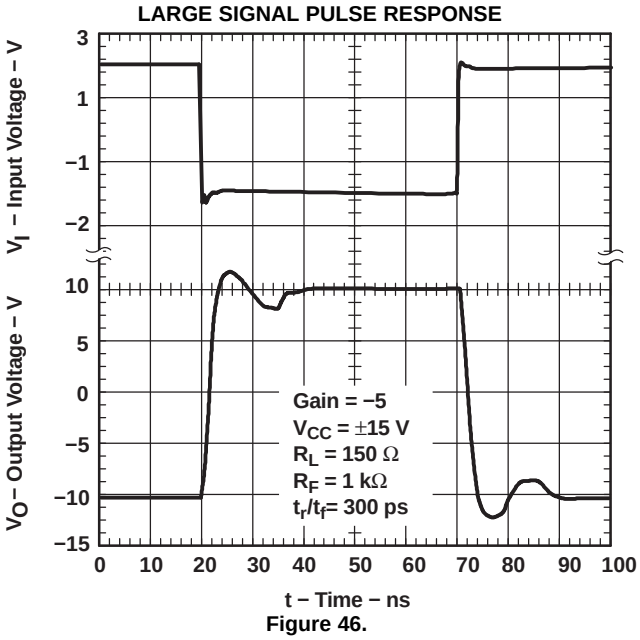


Figure 46.

APPLICATION INFORMATION

THEORY OF OPERATION

The THS3001 is a high-speed, operational amplifier configured in a current-feedback architecture. The device is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This configuration implements an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 47.

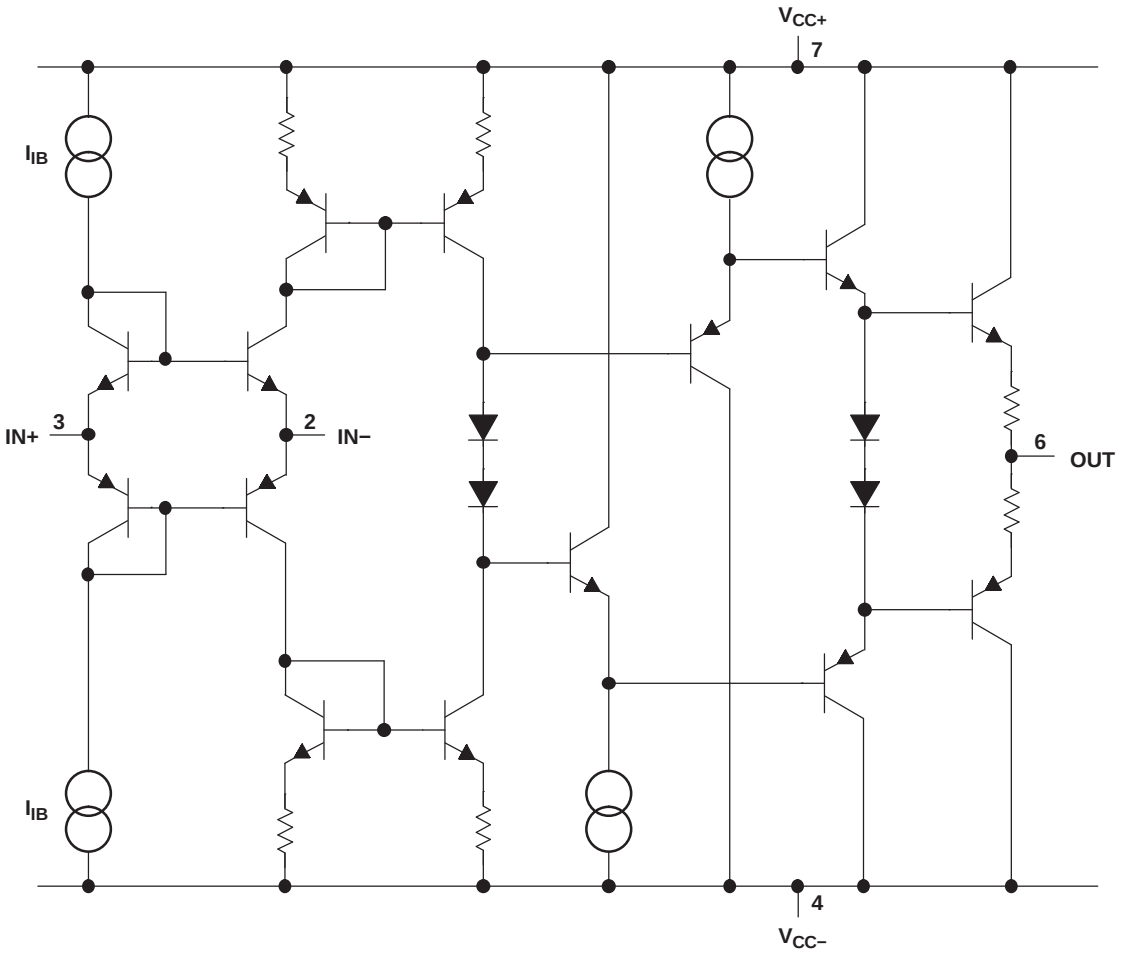


Figure 47. Simplified Schematic

RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

The THS3001 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides the excellent isolation and extremely high slew rates that result in superior distortion characteristics.

As with all current-feedback amplifiers, the bandwidth of the THS3001 is an inversely proportional function of the value of the feedback resistor (see Figures 26 to 34). The recommended resistors for the optimum frequency response are shown in Table 1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. For most applications, a feedback resistor value of 1 kΩ is recommended - a good compromise between bandwidth and phase margin that yields a stable amplifier.

Consistent with current-feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independent of the bandwidth constitutes a major advantage of current-feedback amplifiers over conventional voltage-feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

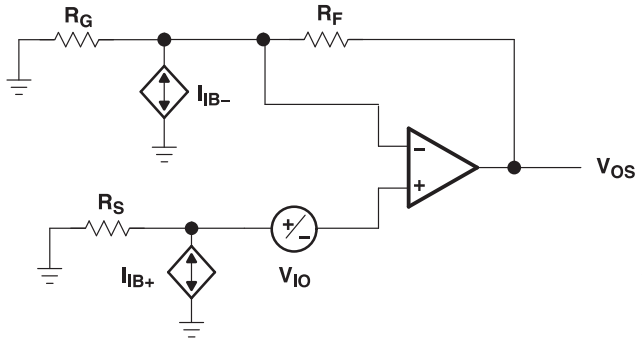
Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third-order harmonic distortion increases more than the second-order harmonic distortion.

Table 1. Recommended Resistor Values for Optimum Frequency Response

GAIN	R_F for V_{CC} = ±15 V	R_F for V_{CC} = ±5 V
1	1 kΩ	1 kΩ
2, -1	680 Ω	750 Ω
2	620 Ω	620 Ω
5	560 Ω	620 Ω

OFFSET VOLTAGE

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

Figure 48. Output Offset Voltage Model

NOISE CALCULATIONS

Noise can cause errors on small signals. This is especially true for amplifying small signals coming over a transmission line or an antenna. The noise model for current-feedback amplifiers (CFB) is the same as for voltage feedback amplifiers (VFB). The only difference between the two is that CFB amplifiers generally specify different current-noise parameters for each input, while VFB amplifiers usually only specify one noise-current parameter. The noise model is shown in Figure 49. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Nonverting current noise (pA/$\sqrt{Hz}$)
- IN- = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

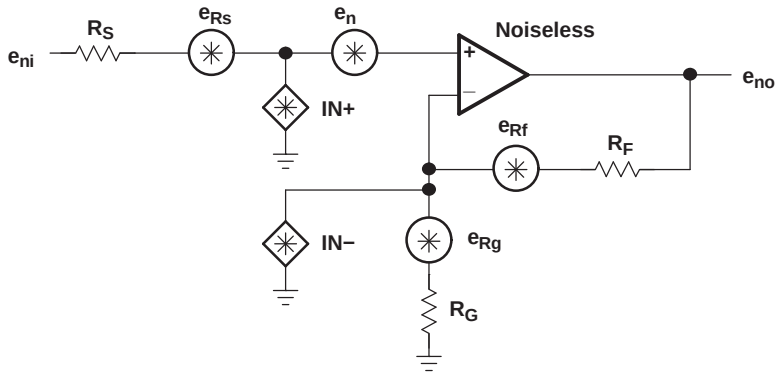


Figure 49. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
R_F || R_G = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier.

SLEW RATE

The slew rate performance of a current-feedback amplifier, like the THS3001, is affected by many different factors. Some of these factors are external to the device, such as amplifier configuration and PCB parasitics, and others are internal to the device, such as available currents and node capacitance. Understanding some of these factors should help the PCB designer arrive at a more optimum circuit with fewer problems.

Whether the THS3001 is used in an inverting amplifier configuration or a noninverting configuration can impact the output slew rate. As can be seen from the specification tables as well as some of the figures in this data sheet, slew-rate performance in the inverting configuration is faster than in the noninverting configuration. This is because in the inverting configuration the input terminals of the amplifier are at a virtual ground and do not significantly change voltage as the input changes. Consequently, the time to charge any capacitance on these input nodes is less than for the noninverting configuration, where the input nodes actually do change in voltage an amount equal to the size of the input step. In addition, any PCB parasitic capacitance on the input nodes degrades the slew rate further simply because there is more capacitance to charge. Also, if the supply voltage (V_{CC}) to the amplifier is reduced, slew rate decreases because there is less current available within the amplifier to charge the capacitance on the input nodes as well as other internal nodes.

Internally, the THS3001 has other factors that impact the slew rate. The amplifier's behavior during the slew-rate transition varies slightly depending upon the rise time of the input. This is because of the way the input stage handles faster and faster input edges. Slew rates (as measured at the amplifier output) of less than about 1500 V/µs are processed by the input stage in a linear fashion. Consequently, the output waveform smoothly transitions between initial and final voltage levels. This is shown in Figure 50. For slew rates greater than 1500 V/µs, additional slew-enhancing transistors present in the input stage begin to turn on to support these faster signals. The result is an amplifier with extremely fast slew-rate capabilities. Figure 50 and Figure 51 show waveforms for these faster slew rates. The additional aberrations present in the output waveform with these faster-slewing input signals are due to the brief saturation of the internal current mirrors. This phenomenon, which typically lasts less than 20 ns, is considered normal operation and is not detrimental to the device in any way. If for any reason this type of response is not desired, then increasing the feedback resistor or slowing down the input-signal slew rate reduces the effect.

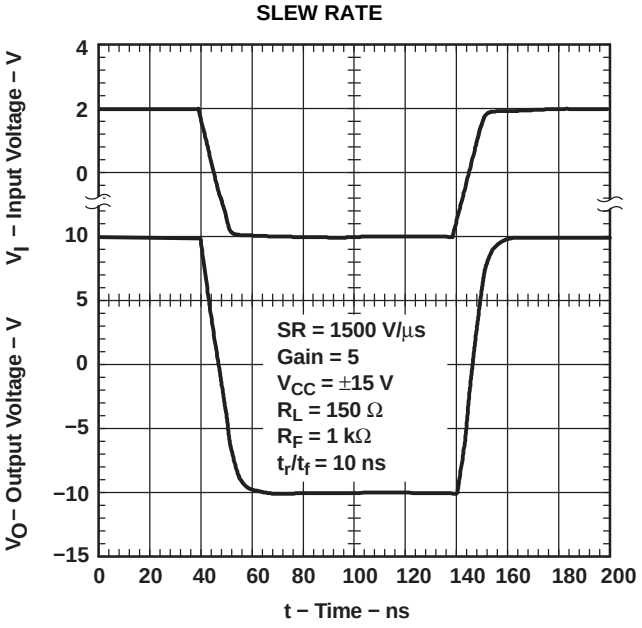


Figure 50.

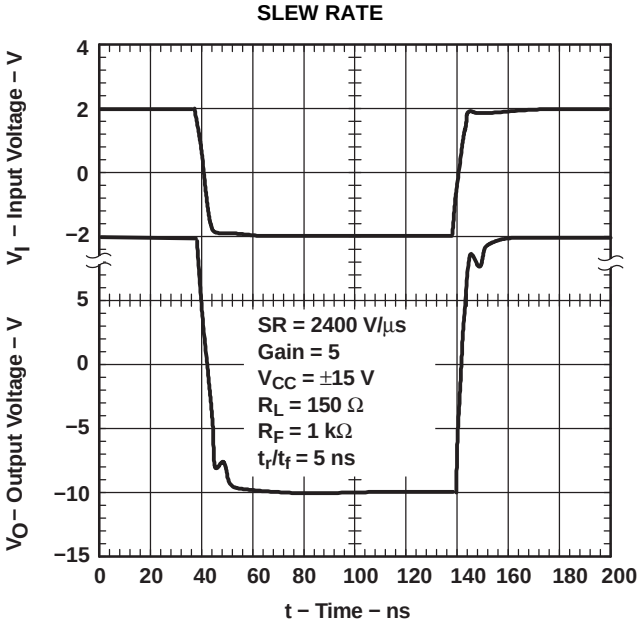


Figure 51.

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS3001 has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 52. A minimum value of 20Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

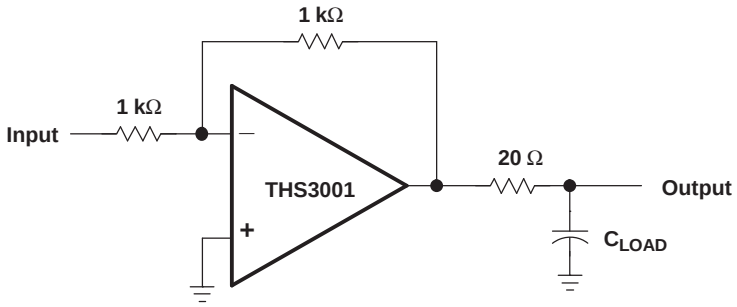


Figure 52. Driving a Capacitive Load

PCB DESIGN CONSIDERATIONS

Proper PCB design techniques in two areas are important to ensure proper operation of the THS3001. These areas are high-speed layout techniques and thermal-management techniques. Because the THS3001 is a high-speed part, the following guidelines are recommended.

- Ground plane - It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection, but should be removed from below the output and negative input pins as noted below.
- The DGN package option includes a thermal pad for increased thermal performance. When using this package, it is recommended to distribute the negative supply as a power plane, and tie the thermal pad to this supply with multiple vias for proper power dissipation. It is not recommended to tie the thermal pad to ground when using split supply (±V) as this will cause worse distortion performance than shown in this data sheet.
- Input stray capacitance - To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 53, which shows what happens when a 1-pF capacitor is added to the inverting input terminal. The bandwidth increases at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. Although, while the device is in the inverting mode, stray capacitance at the inverting input has a minimal effect. This is because the inverting node is at a *virtual ground* and the voltage does not fluctuate nearly as much as in the noninverting configuration. This can be seen in Figure 54, where a 10-pF capacitor adds only 0.35 dB of peaking. In general, as the gain of the system increases, the output peaking due to this capacitor decreases. While this can initially look like a faster and better system, overshoot and ringing are more likely to occur under fast transient conditions. So proper analysis of adding a capacitor to the inverting input node should be performed for stable operation.

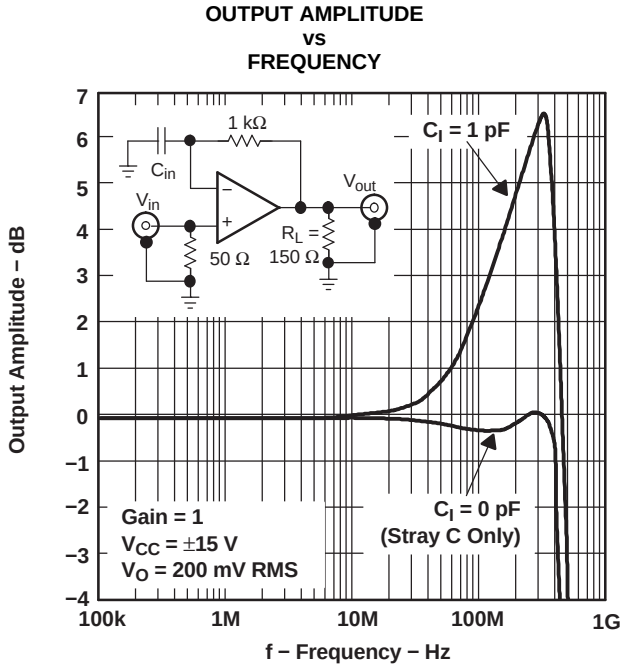


Figure 53.

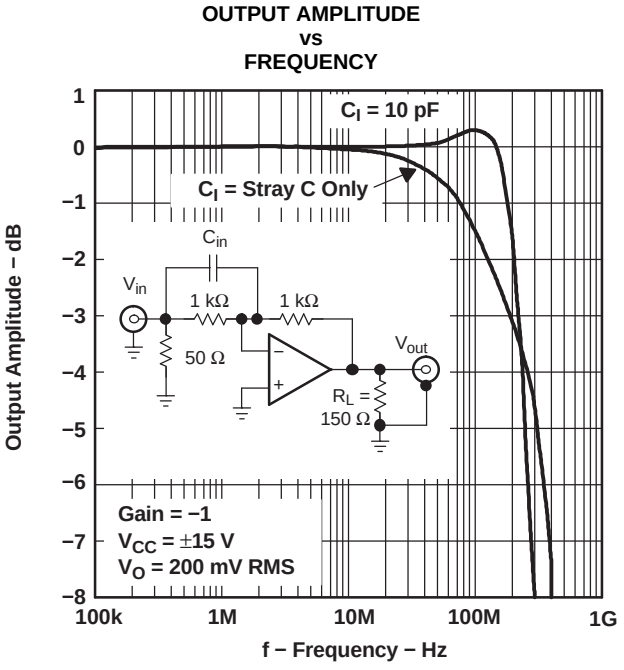


Figure 54.

- Proper power-supply decoupling - Use a minimum 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch between the device power terminal and the ceramic capacitors.

THERMAL INFORMATION

The THS3001 incorporates output-current-limiting protection. Should the output become shorted to ground, the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) is not recommended. Failure of the device is possible under this condition and should be avoided. But, the THS3001 does not incorporate thermal-shutdown protection. Because of this, special attention must be paid to the device's power dissipation or failure may result.

The thermal coefficient θ_{JA} is approximately 169°C/W for the SOIC 8-pin D package. For a given θ_{JA}, the maximum power dissipation, shown in Figure 55, is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS3001 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = Thermal coefficient from die junction to ambient air (°C/W)

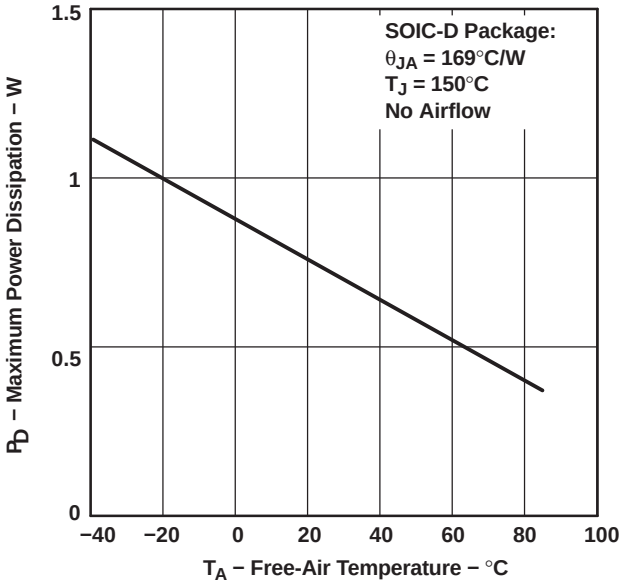
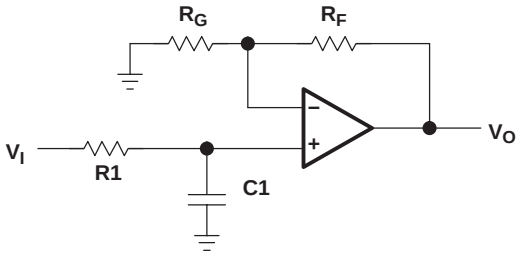


Figure 55. Maximum Power Dissipation vs Free-Air Temperature

GENERAL CONFIGURATIONS

A common error for the first-time CFB user is the creation of a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration will oscillate and is *not* recommended. The THS3001, like all CFB amplifiers, *must* have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 56).

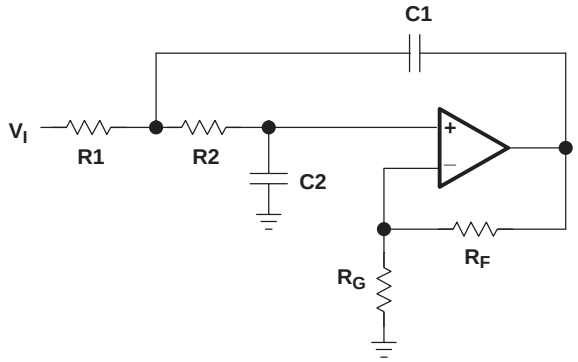


$$f_{-3\,dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 56. Single-Pole Low-Pass Filter

If a multiple-pole filter is required, the use of a Sallen-Key filter can work well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew rates and high bandwidths, CFB amplifiers can create accurate signals and help minimize distortion. An example is shown in Figure 57.



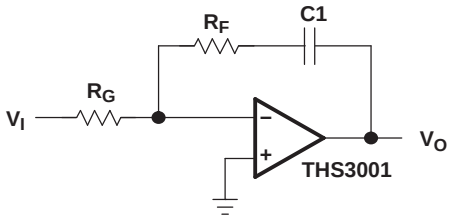
R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3\,dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 57. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first, shown in Figure 58, adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second, shown in Figure 59, uses positive feedback to create the integration. Caution is advised because oscillations can occur due to the positive feedback.



$$\frac{V_O}{V_I} = \left(\frac{R_F}{R_G}\right)\left[\frac{S + \frac{1}{R_F C1}}{S}\right]$$

Figure 58. Inverting CFB Integrator

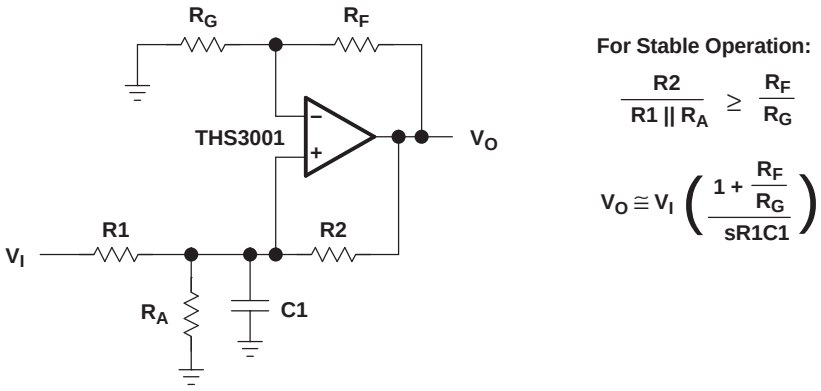


Figure 59. Noninverting CFB Integrator

The THS3001 may also be employed as a good video distribution amplifier. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases (see Figures 22 to 25 for more information). Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

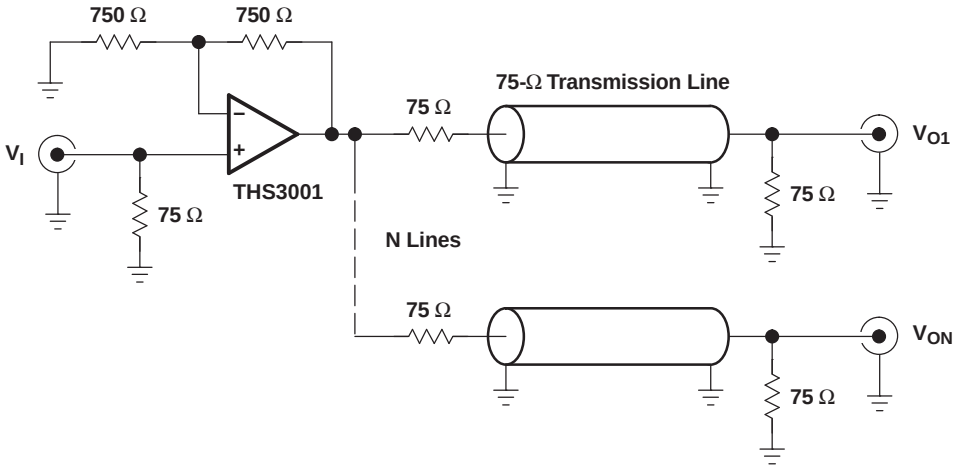


Figure 60. Video Distribution Amplifier Application

EVALUATION BOARD

An evaluation board is available for the THS3001 (THS3001EVM). The board has been configured for low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 61. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more detailed information, refer to the *THS3001 EVM User's Guide* (literature number SLOU021). The evaluation board can be ordered online through the TI web site, or through your local TI sales office or distributor.

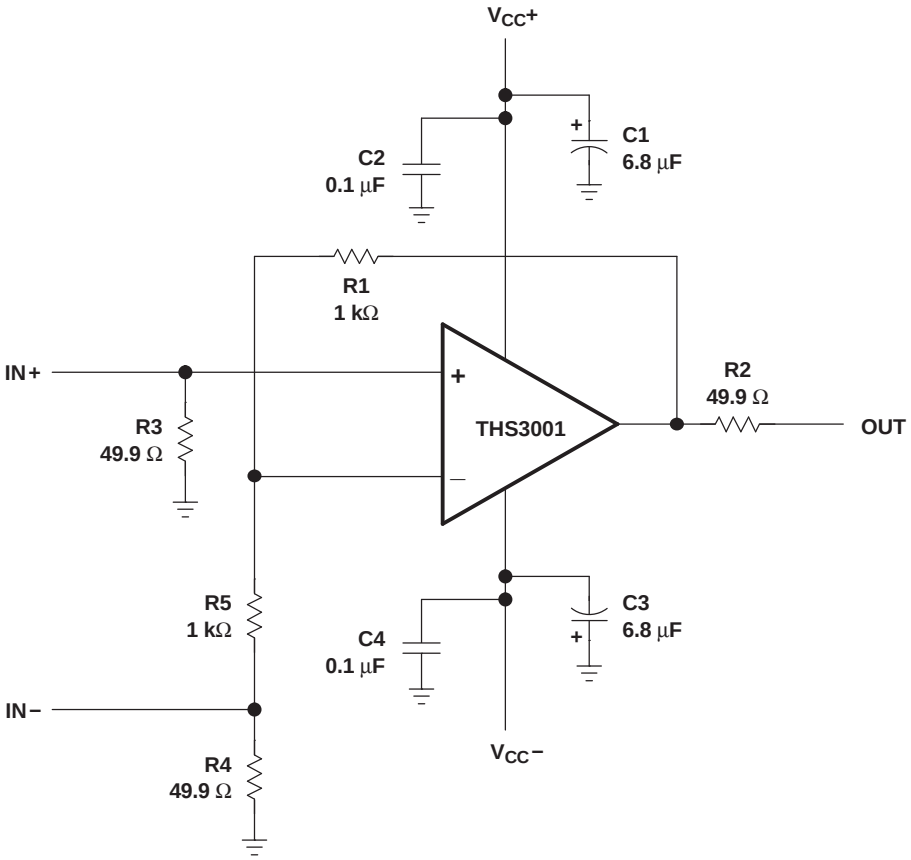


Figure 61. THS3001 Evaluation Board Schematic

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March, 2008) to Revision H	Page
• Updated document format to current standards	1
• Deleted references to HV version in SOIC package; this version is not available	2
• Updated information about THS3001EVM availability	27

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS3001CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3001C	
THS3001CDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3001C	
THS3001CDGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ADP	
THS3001HVCDGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BNK	
THS3001HVIDGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BNJ	
THS3001IDGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM		ADQ	
THS3001IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM		ADQ	Samples
THS3001IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		3001I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

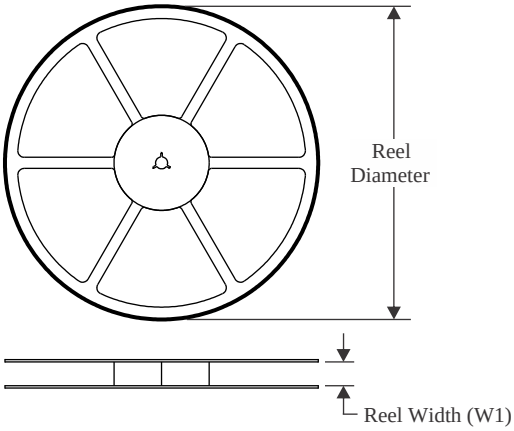
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

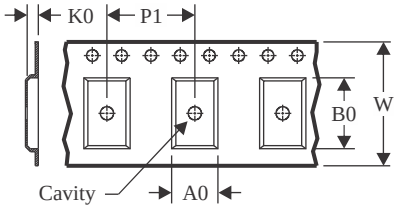
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

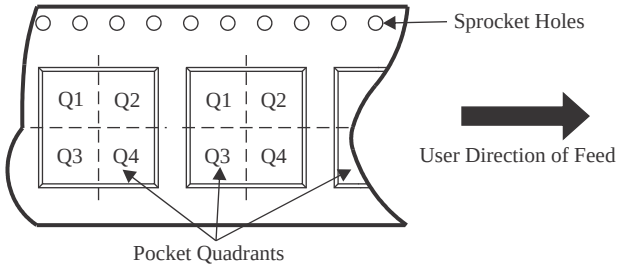


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

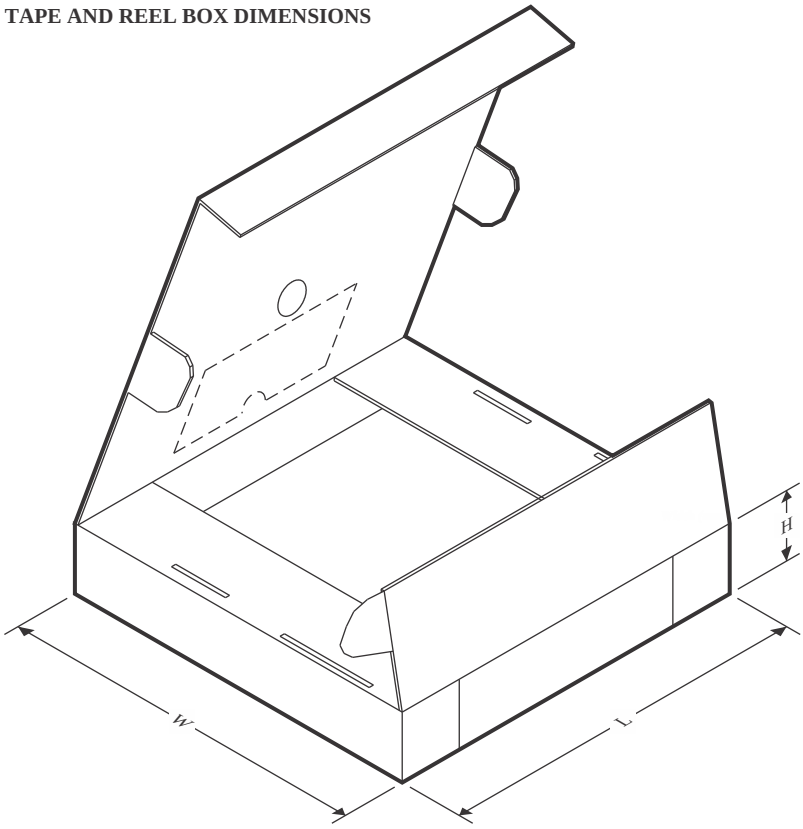
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3001IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS3001IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS3001IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

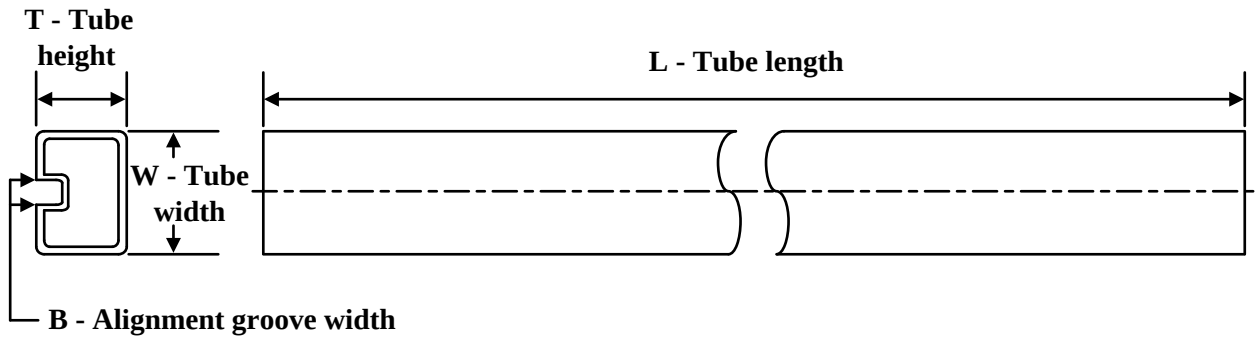
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3001IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS3001IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS3001IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS3001CD	D	SOIC	8	75	505.46	6.76	3810	4
THS3001CDG4	D	SOIC	8	75	505.46	6.76	3810	4
THS3001CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS3001HVIDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS3001IDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

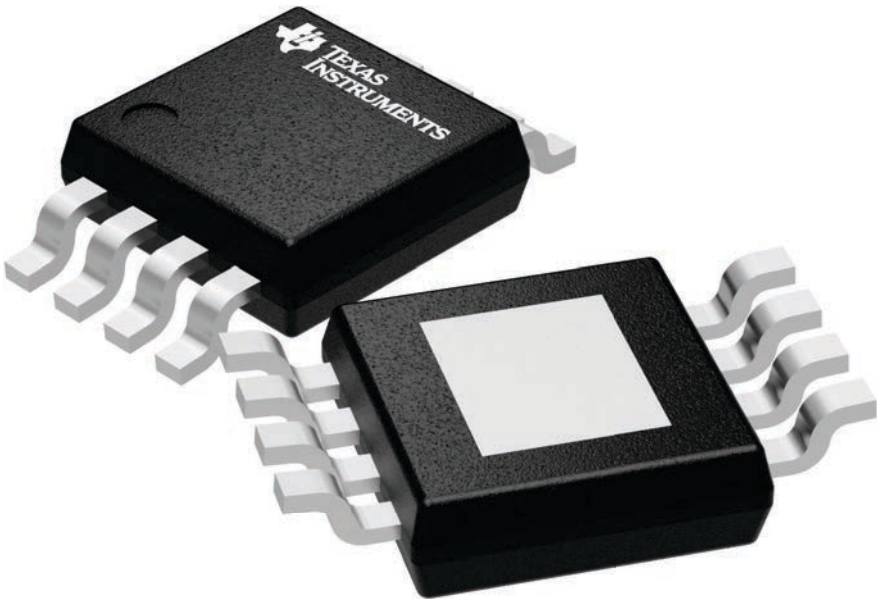
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

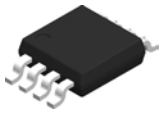
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

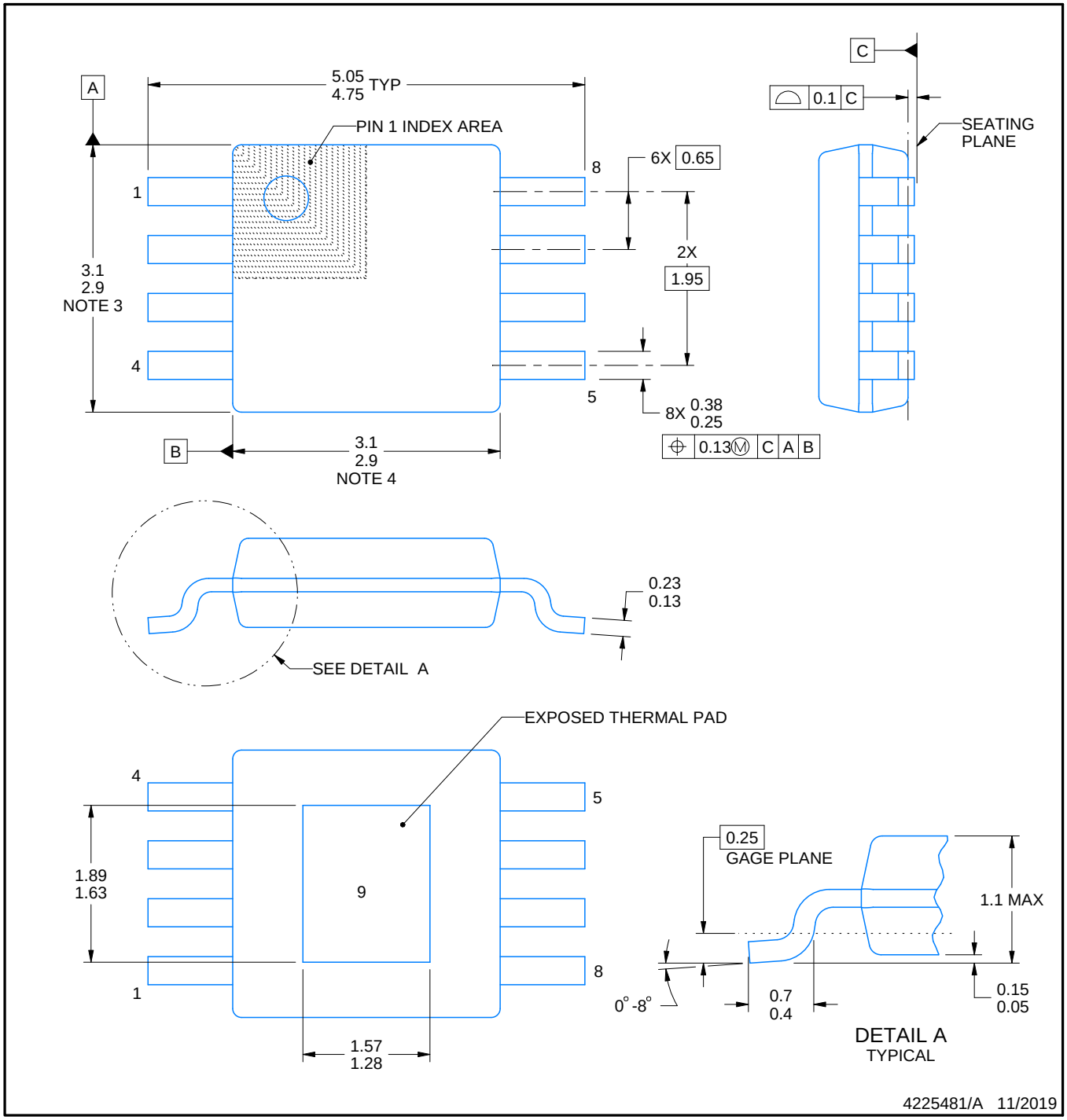
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

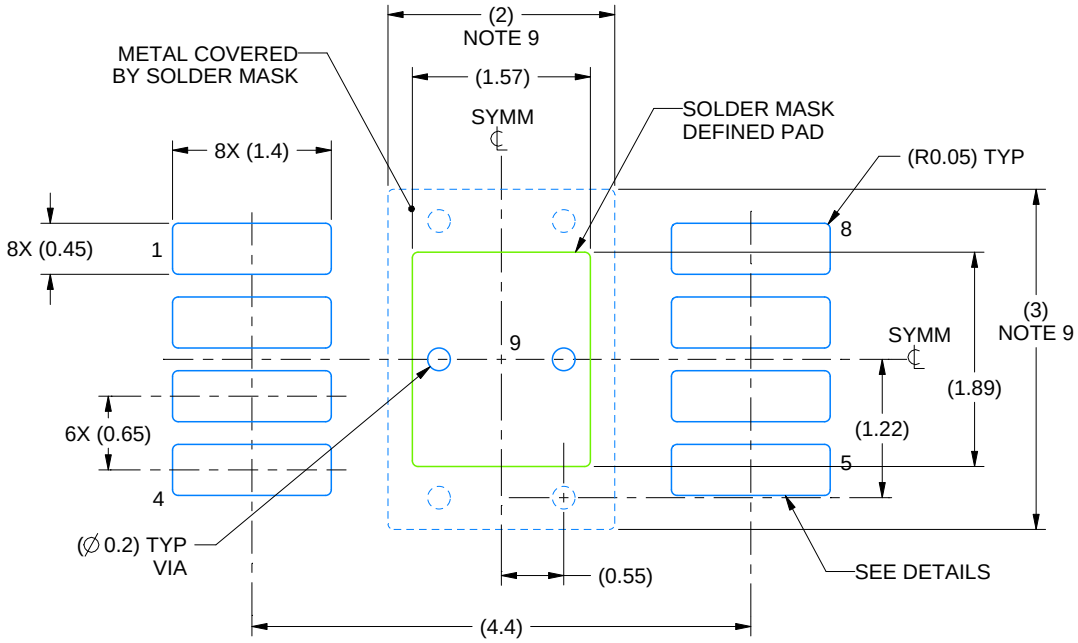
SMALL OUTLINE PACKAGE



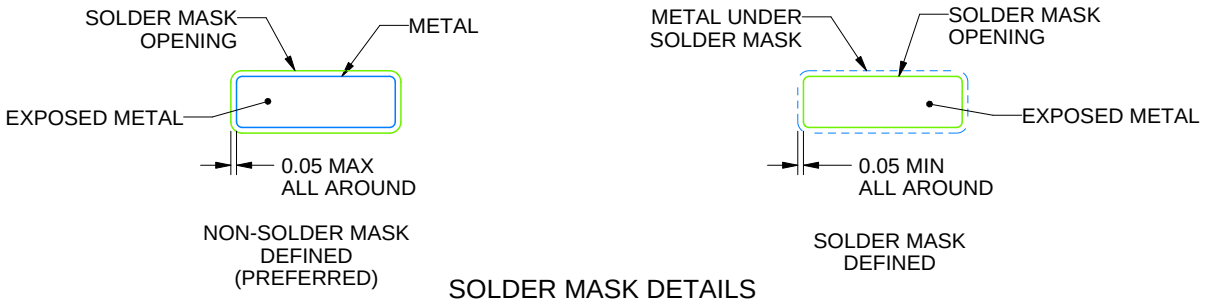
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

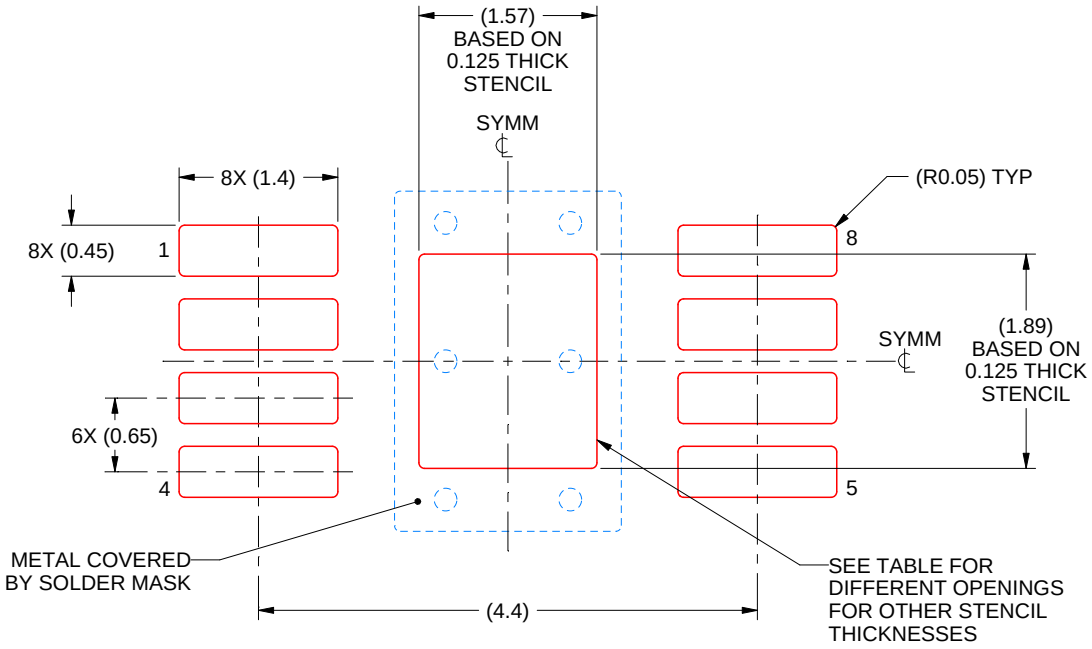


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

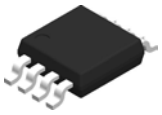
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

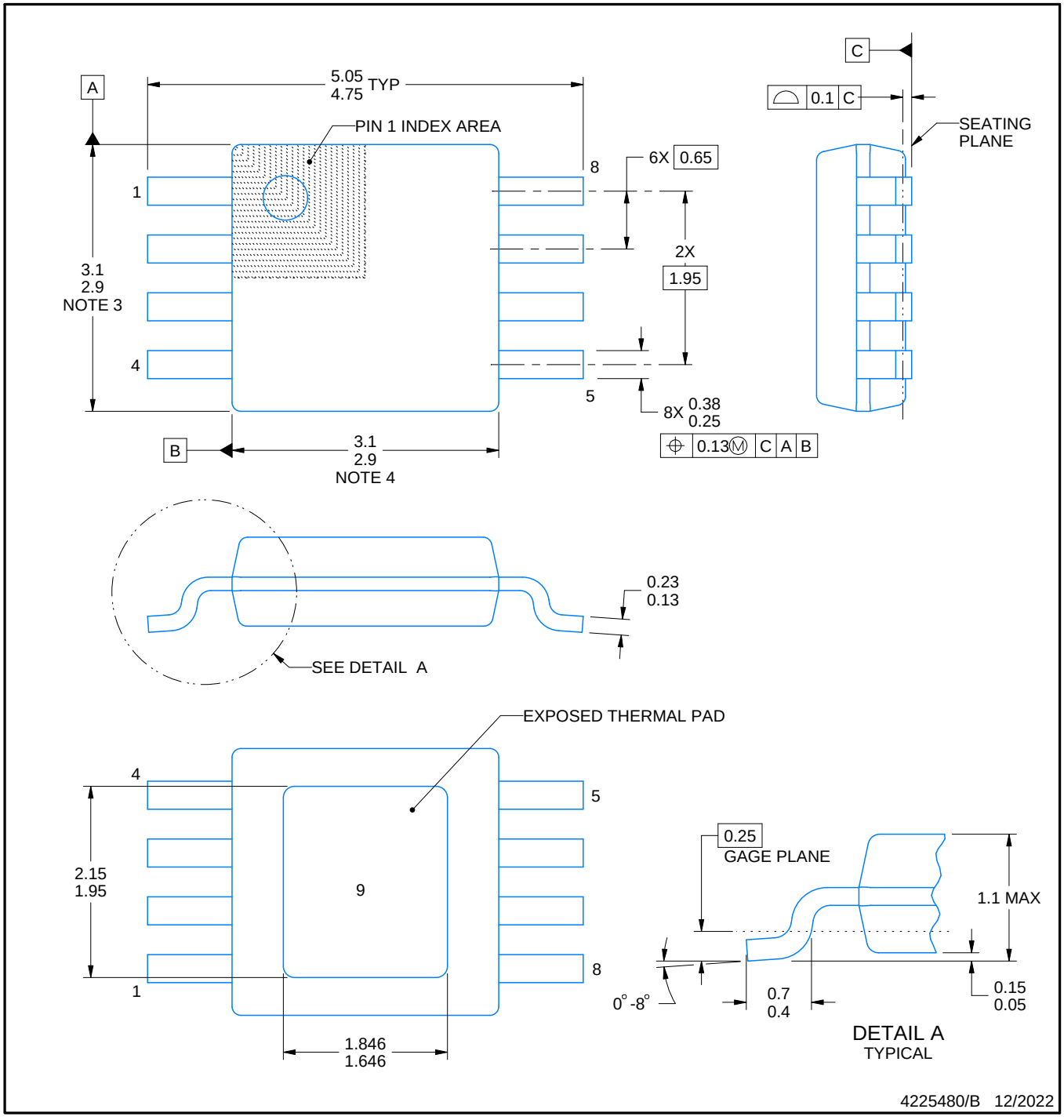
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

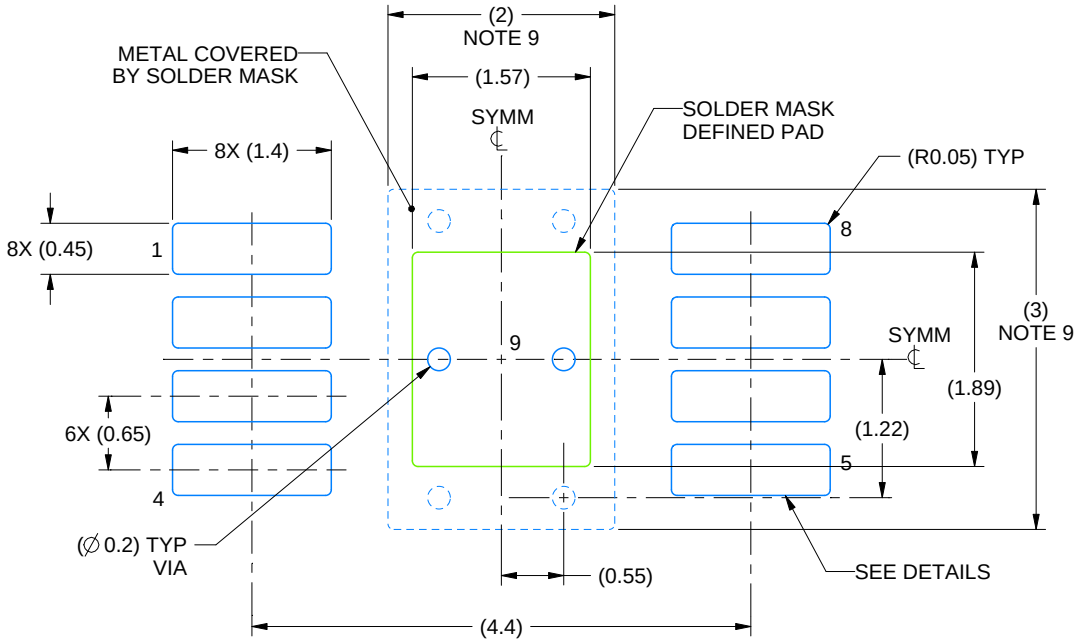
SMALL OUTLINE PACKAGE



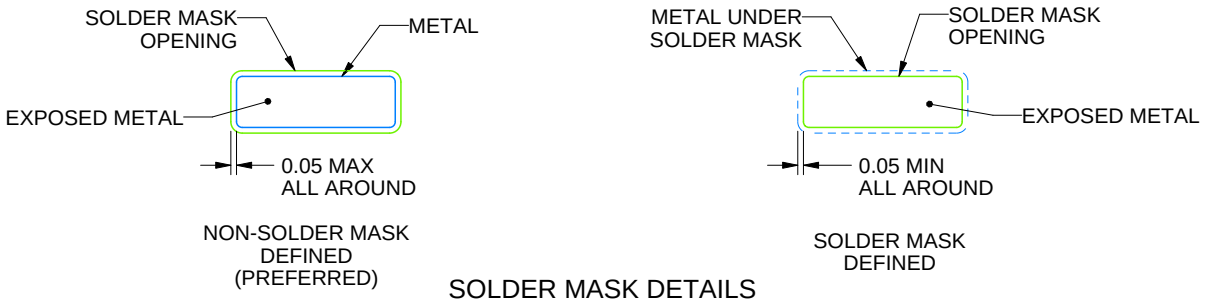
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

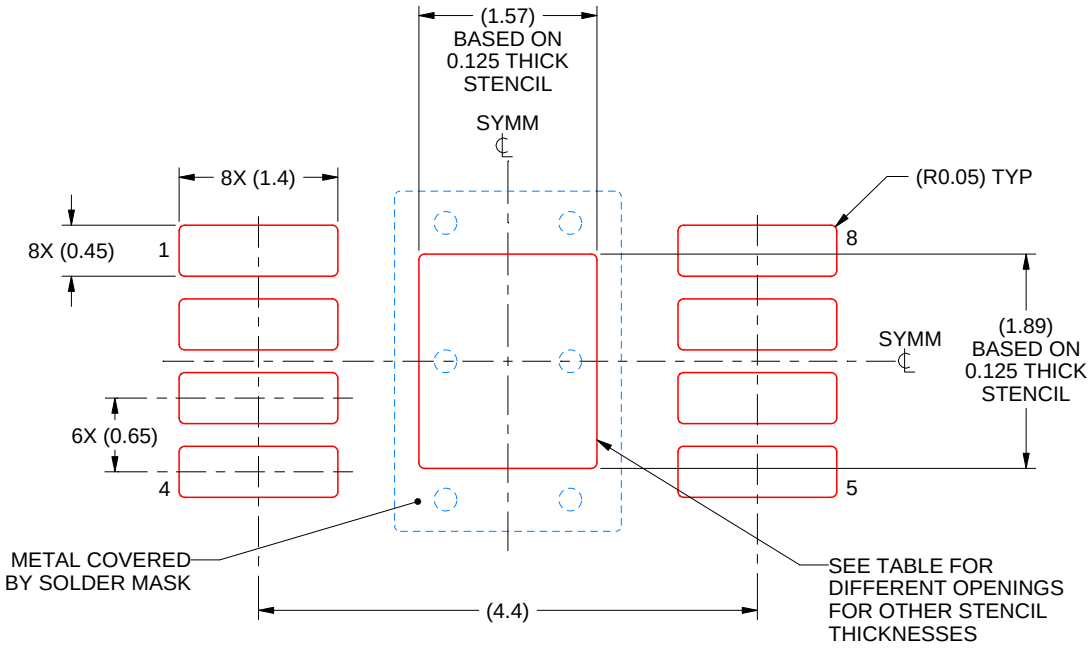


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



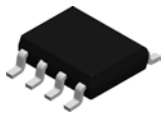
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

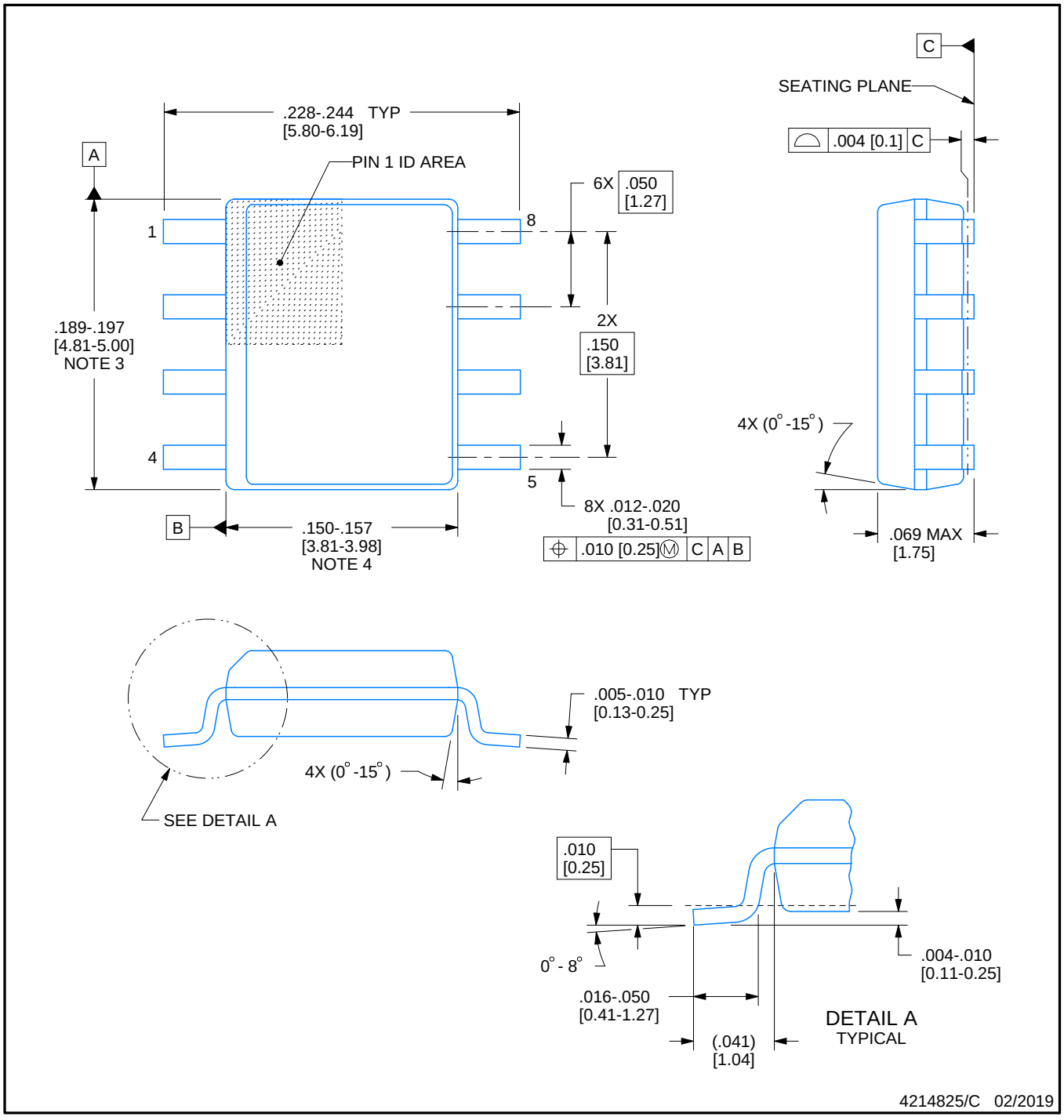


PACKAGE OUTLINE

D0008A

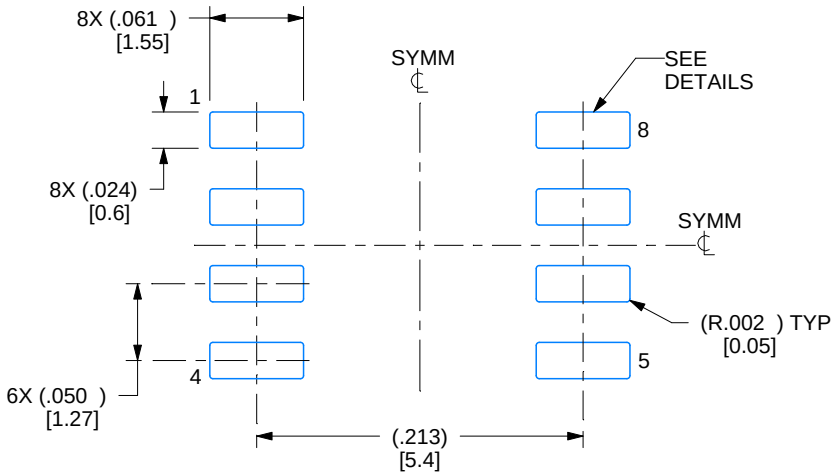
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

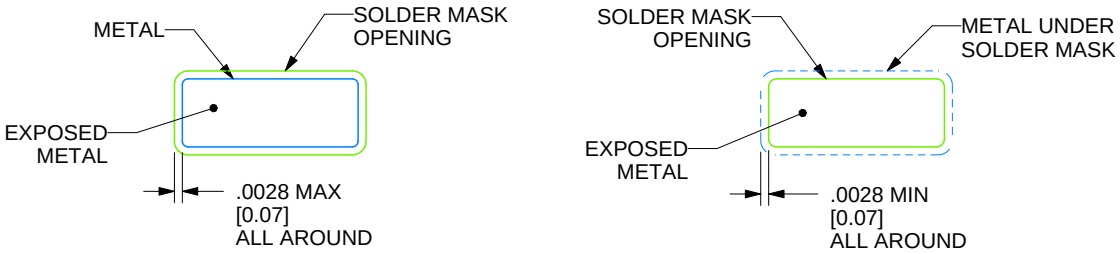


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

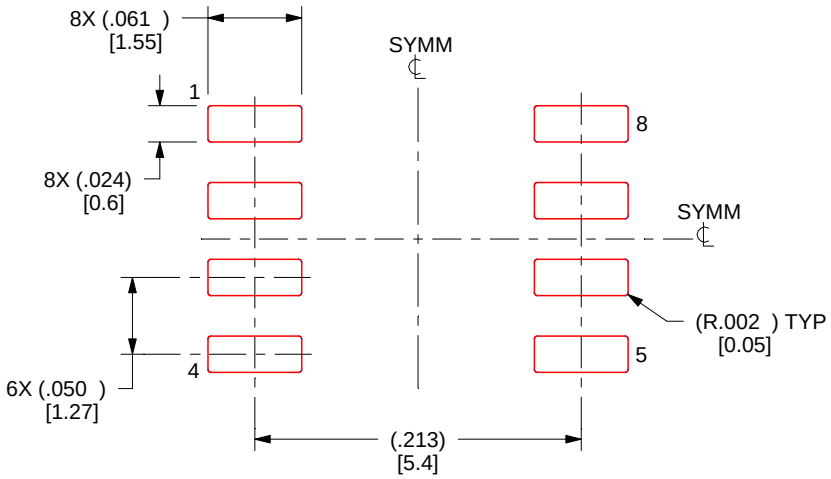
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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