

## TPS3809xxx-Q1 3-Pin Supply Voltage Supervisors

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- 3-Pin SOT-23 Package
- Supply Current of  $9\ \mu\text{A}$  (Typical)
- Precision-Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, 5 V
- Power-On Reset Generator With Fixed Delay Time of 200 ms
- Pin-For-Pin Compatible With MAX 809

### 2 Applications

- [Automotive Camera Systems](#)
- [Telematics](#)
- [Automotive Cluster](#)
- [Engine Controls](#)
- [Surround View Systems](#)

### 3 Description

The TPS3809 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems. The newer [TLV809E](#) device is an alternative with the same pins, functions and electrical parameters.

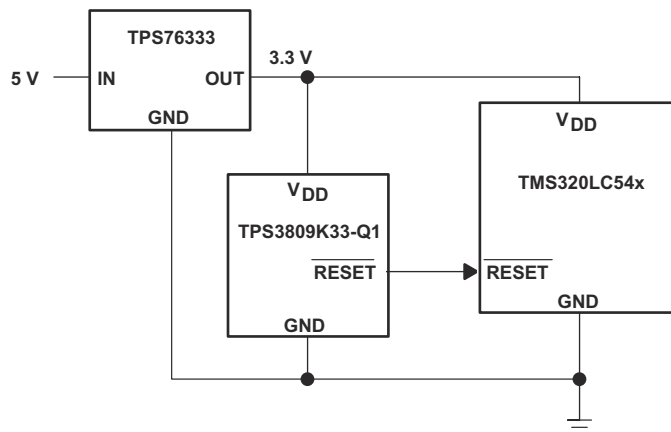
During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage  $V_{\text{DD}}$  becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors  $V_{\text{DD}}$  and keeps  $\overline{\text{RESET}}$  active as long as  $V_{\text{DD}}$  remains below the threshold voltage  $V_{\text{IT}}$ . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time,  $t_{\text{d(typ)}} = 200\ \text{ms}$ , starts after  $V_{\text{DD}}$  has risen above the threshold voltage  $V_{\text{IT}}$ . When the supply voltage drops below the threshold voltage  $V_{\text{IT}}$ , the output becomes active (low) again. No external components are required. All the devices of this family have a fixed sense-threshold voltage  $V_{\text{IT}}$  set by an internal voltage divider.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23. The TPS3809xxx-Q1 devices are characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , and are qualified in accordance with AEC-Q100 stress test qualification for integrated circuits.

#### Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3809xxx-Q1	SOT-23 (3)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Typical Application



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (March 2016) to Revision C (December 2020)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added new sentence regarding the new TLV809E to the <i>Description</i> section.....	1
• Renamed <i>Device Comparison</i> modified device option table and added comparison table .....	3
• Changed VDD from 7 to 6.5 in <i>Absolute Maximum Ratings</i> .....	4
• Changed V <sub>OL</sub> @ 500µA from 0.2 to 0.3 in <i>Electrical Characteristics</i> .....	5
• Changed t <sub>w</sub> pulse duration from 3 to 10µs in <i>Timing Requirements</i> .....	5
• Changed t <sub>PHL</sub> from 1 to 10µs in <i>Switching Characteristics</i> .....	5
• Deleted figure for Minimum Pulse Duration At V <sub>DD</sub> in Typical Characteristics.....	7

<b>Changes from Revision A (December 2002) to Revision B (February 2016)</b>	<b>Page</b>
• Added AEC-Q100 Qualified information in bullets .....	1
• Changed <i>Applications</i> list items .....	1
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Changed device part numbers by adding -Q1 to them throughout document .....	5

## 5 Device Comparison

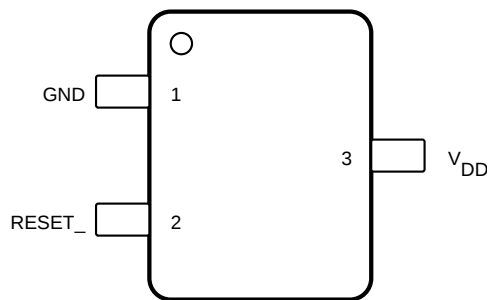
**Table 5-1. Device Threshold Options**

PRODUCT	THRESHOLD VOLTAGE
TPS3809J25QDBVRQ1	2.25 V
TPS3809L30QDBVRQ1	2.64 V
TPS3809K33QDBVRQ1	2.93 V
TPS3809I50QDBVRQ1	4.55 V

**Table 5-2. Device Family Comparison**

DEVICE	FUNCTION
<a href="#">TLV803</a>	Open-Drain, $\overline{\text{RESET}}$ Output
<a href="#">TLV809</a>	Push-Pull, $\overline{\text{RESET}}$ Output
<a href="#">TLV810</a>	Push-Pull, RESET Output

## 6 Pin Configuration and Functions



**Figure 6-1. DBV Package  
3-Pin SOT-23  
Top View**

### 6.1 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground
$\overline{\text{RESET}}$	2	O	Reset output
$V_{\text{DD}}$	3	I	Supply voltage and supervising input

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$ <sup>(2)</sup>		6.5	V
All other pins <sup>(2)</sup>	-0.3	6.5	V
Maximum low output current, $I_{OL}$		5	mA
Maximum high output current, $I_{OH}$		-5	mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )	-20	20	mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )	-20	20	mA
Continuous total power dissipation			
Operating free-air temperature range, $T_A$	-40	125	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 6.5 V for more than  $t = 1000$  h continuously.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD}$	Supply voltage	2		6	V
$T_A$	Operating free-air temperature	-40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS3809xxx-Q1	UNIT
		DBV (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	232.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	187.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	104.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	40.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	104.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = 2.5 V to 6 V, I <sub>OH</sub> = -500 μA	V <sub>DD</sub> - 0.2			V		
		V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = -2 μA	V <sub>DD</sub> - 0.4					
		V <sub>DD</sub> = 6 V, I <sub>OH</sub> = -4 mA	T <sub>A</sub> = -40°C to +25°C	V <sub>DD</sub> - 0.4				
			T <sub>A</sub> = 125°C	V <sub>DD</sub> - 0.5				
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 2 V to 6 V, I <sub>OL</sub> = 500 μA			0.3	V		
		V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 2 mA			0.4			
		V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 4 mA			0.4			
Power-up reset voltage <sup>(1)</sup>		V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 50 μA			0.2	V		
V <sub>IT-</sub>	Negative-going input threshold voltage <sup>(2)</sup>	TPS3809J25-Q1	T <sub>A</sub> = -40°C to +125°C	2.20	2.25	2.30	V	
		TPS3809L30-Q1		2.58	2.64	2.7		
		TPS3809K33-Q1		2.87	2.93	2.99		
		TPS3809I50-Q1		T <sub>A</sub> = -40°C to +85°C	4.45	4.55		4.65
				T <sub>A</sub> = -40°C to +125°C	4.4	4.55		4.65
V <sub>hys</sub>	Hysteresis	TPS3809J25-Q1		30		mV		
		TPS3809L30-Q1		35				
		TPS3809K33-Q1		40				
		TPS3809I50-Q1		60				
I <sub>DD</sub>	Supply current	V <sub>DD</sub> = 2 V, Output unconnected		9	15	μA		
		V <sub>DD</sub> = 6 V, Output unconnected		20	30			
C <sub>i</sub>	Input capacitance	V <sub>i</sub> = 0 V to V <sub>DD</sub>		5		pF		

(1) The lowest supply voltage at which RESET becomes active. t<sub>r</sub>, V<sub>DD</sub> ≥ 15 μs/V.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (0.1 μF, ceramic) should be placed near the supply terminals.

## 7.6 Timing Requirements

R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

			MIN	NOM	MAX	UNIT
t <sub>w</sub>	Pulse width at V <sub>DD</sub>	V <sub>DD</sub> = V <sub>IT-</sub> + 0.2 V, V <sub>DD</sub> = V <sub>IT-</sub> - 0.2 V	10			μs

## 7.7 Switching Characteristics

R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>d</sub>	Delay time	V <sub>DD</sub> ≥ V <sub>IT-</sub> + 0.2 V, See timing diagram, <a href="#">Section 7.8</a>	120	200	280	ms
t <sub>PHL</sub>	Propagation (delay) time, high-to-low-level output	V <sub>DD</sub> to RESET delay V <sub>IL</sub> = V <sub>IT-</sub> - 0.2 V, V <sub>IH</sub> = V <sub>IT-</sub> + 0.2 V		10		μs

## 7.8 Timing Diagrams

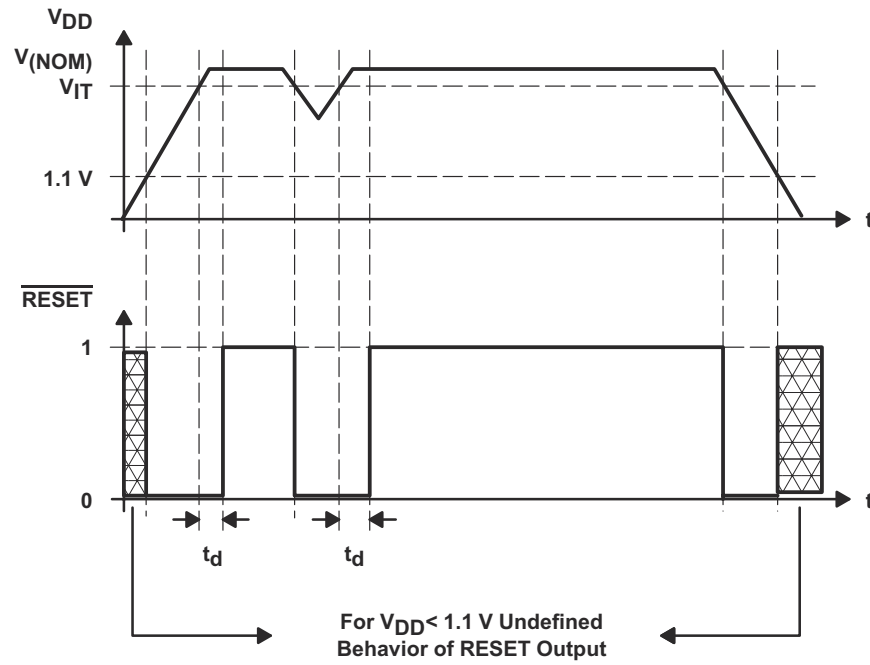
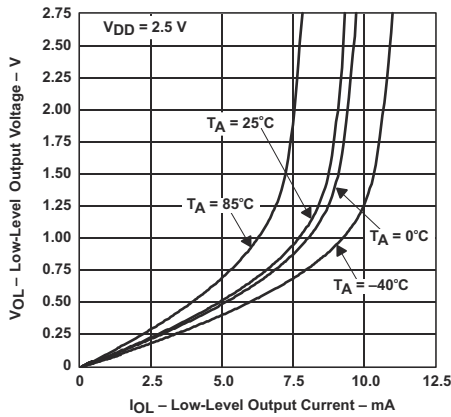
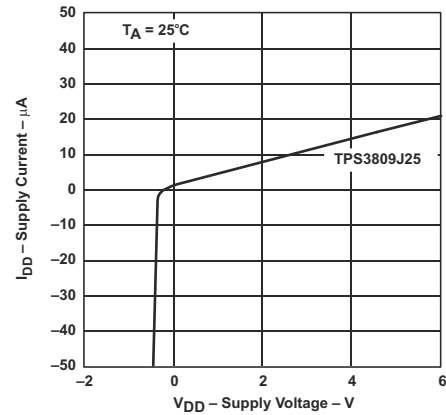


Figure 7-1. Timing Diagram

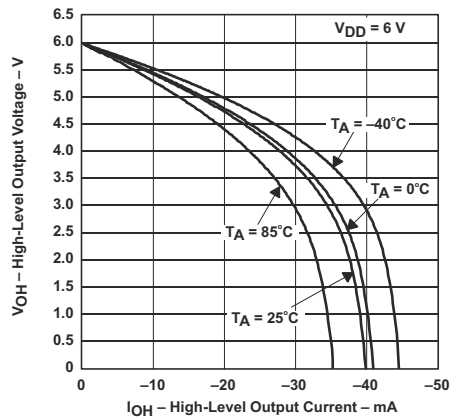
## 7.9 Typical Characteristics



**Figure 7-2. Low-Level Output Voltage vs Low-Level Output Current**

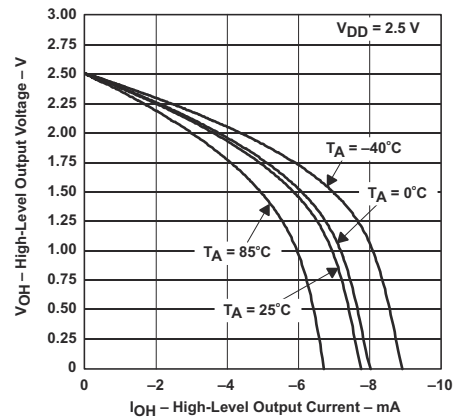


**Figure 7-3. Supply Current vs Supply Voltage**



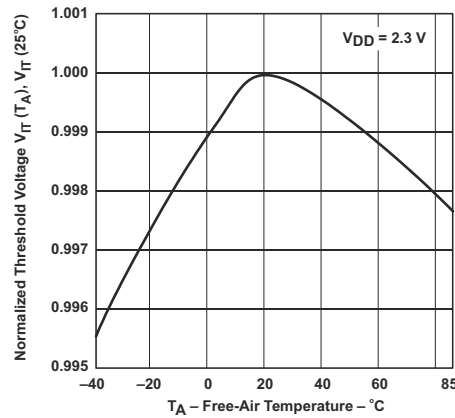
$V_{DD} = 6\text{ V}$

**Figure 7-4. High-Level Output Voltage vs High-Level Output Current**



$V_{DD} = 2.5\text{ V}$

**Figure 7-5. High-Level Output Voltage vs High-Level Output Current**



$V_{DD} = 2.3\text{ V}$

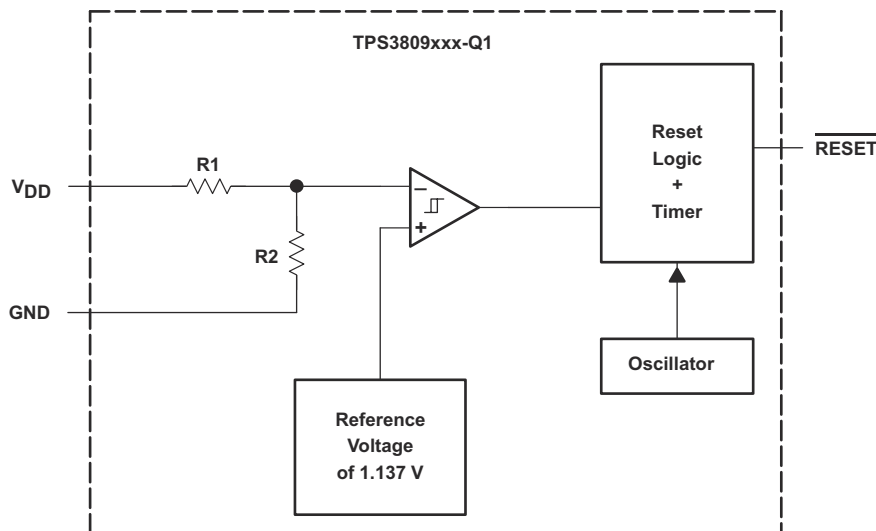
**Figure 7-6. Normalized Input Threshold Voltage vs Free-Air Temperature at  $V_{DD}$**

## 8 Detailed Description

### 8.1 Overview

The TPS3809xxx-Q1 device is a low-current supervisory circuit for monitoring system voltages above 2 V. The device asserts an active-low  $\overline{\text{RESET}}$  signal when VDD drops below a preset threshold. The  $\overline{\text{RESET}}$  output remains low until VDD returns above its threshold. The device design is also to be relatively immune to short negative transients on the VDD pin.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 V<sub>DD</sub> Monitoring

The V<sub>DD</sub> pin provides a terminal at which a system voltage can be monitored. If the voltage on this pin drops below V<sub>IT</sub>,  $\overline{\text{RESET}}$  is asserted low. The comparator has a built-in hysteresis to ensure smooth  $\overline{\text{RESET}}$  assertions and deassertions. Refer to [Section 5](#) to determine the V<sub>DD</sub> voltage threshold for each device.

#### 8.4 Device Functional Modes

TPS3809xxx-Q1 monitors one supply using the V<sub>DD</sub> pin. When V<sub>DD</sub> is above the V<sub>IT</sub> threshold for the device,  $\overline{\text{RESET}}$  will be high. When V<sub>DD</sub> is below the V<sub>IT</sub> threshold for the device,  $\overline{\text{RESET}}$  will be low.



## 9 Application and Implementation

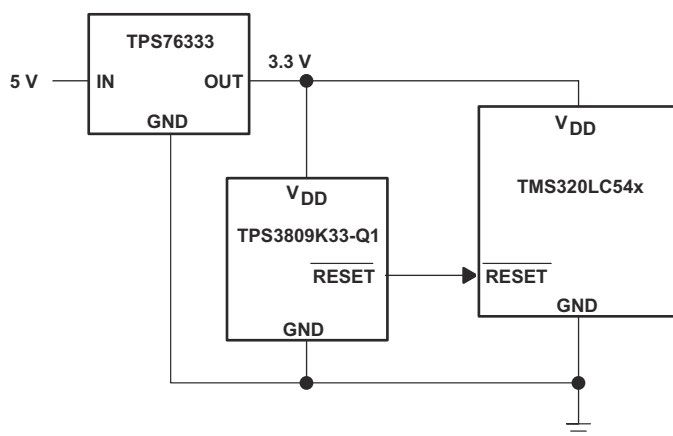
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS3809xxx-Q1 voltage supervisor device design asserts an active-low RESET signal when  $V_{DD}$  drops below a voltage threshold  $V_{IT}$ . The  $\overline{\text{RESET}}$  signal remains low until the voltage returns above its threshold. The typical application is with a processor or microcontroller, which needs to be reset when the supply rail drops below a specified tolerance.

### 9.2 Typical Application



**Figure 9-1. Typical Application Schematic**

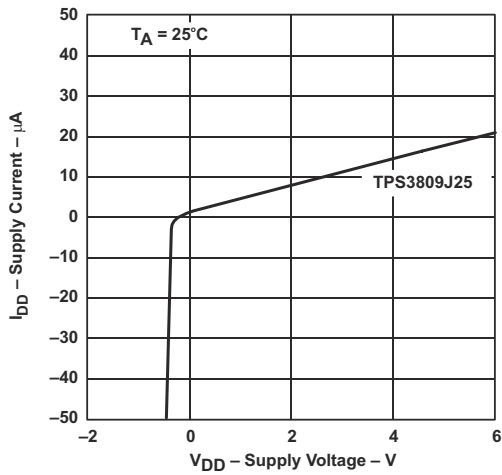
#### 9.2.1 Design Requirements

Each device has a fixed-voltage monitoring threshold, and the device should be chosen based on the voltage being monitored. Refer to [Section 5](#) to determine the  $V_{DD}$  voltage threshold for each device. In this example, a 3.3V supply rail to a microcontroller will be monitored.

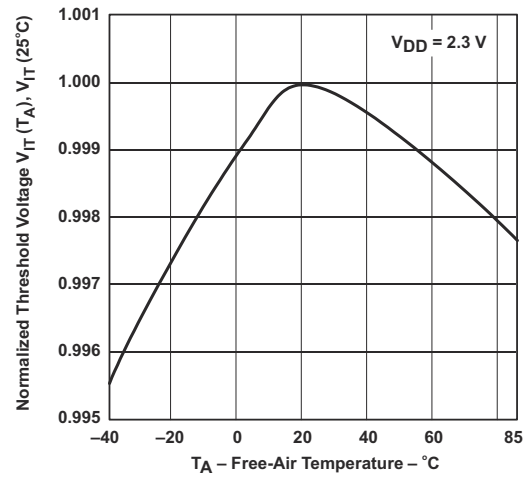
#### 9.2.2 Detailed Design Procedure

Because a 3.3-V supply rail needs to be monitored, TPS3809K33-Q1 should be used. This device has a 2.93-V threshold for reset. Connect the 3.3-V supply to the  $V_{DD}$  pin and the reset output of the supervisor to the reset pin of the microcontroller.

### 9.2.3 Application Curves



**Figure 9-2. Supply Current vs Supply Voltage**



**Figure 9-3. Normalized Input Threshold Voltage vs Free-Air Temperature at V<sub>DD</sub>**

## 10 Power Supply Recommendations

The TPS3809xxx-Q1 device design operates from an input supply from 2 V to 6 V. TI recommends placing a 0.1- $\mu$ F capacitor near the  $V_{DD}$  pin.

## 11 Layout

### 11.1 Layout Guidelines

TI recommends placing the 0.1- $\mu\text{F}$  decoupling capacitor close to the  $V_{\text{DD}}$  pin. The  $V_{\text{DD}}$  and GND traces should be able to carry 30  $\mu\text{A}$  without a significant drop in voltage.

### 11.2 Layout Example

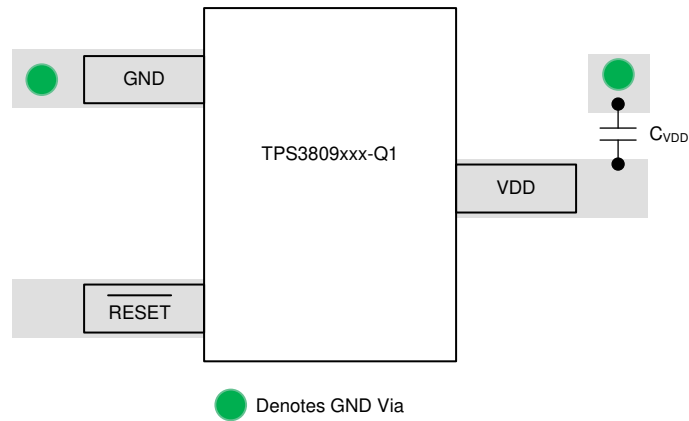


Figure 11-1. Layout Example

## 12 Device and Documentation Support

### 12.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
2T09I50QDBVRG4Q	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDCQ	<a href="#">Samples</a>
TPS3809I50QDBVRQ1	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDCQ	<a href="#">Samples</a>
TPS3809K33QDBVRQ1	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDBQ	<a href="#">Samples</a>
TPS3809L30QDBVRQ1	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDAQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS3809-Q1 :**

- Catalog: [TPS3809](#)
- Enhanced Product: [TPS3809-EP](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
2T09I50QDBVRG4Q	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3809I50QDBVRQ1	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3809K33QDBVRQ1	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3809L30QDBVRQ1	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
2T09I50QDBVRGB4Q	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809I50QDBVRQ1	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809K33QDBVRQ1	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809L30QDBVRQ1	SOT-23	DBV	3	3000	180.0	180.0	18.0

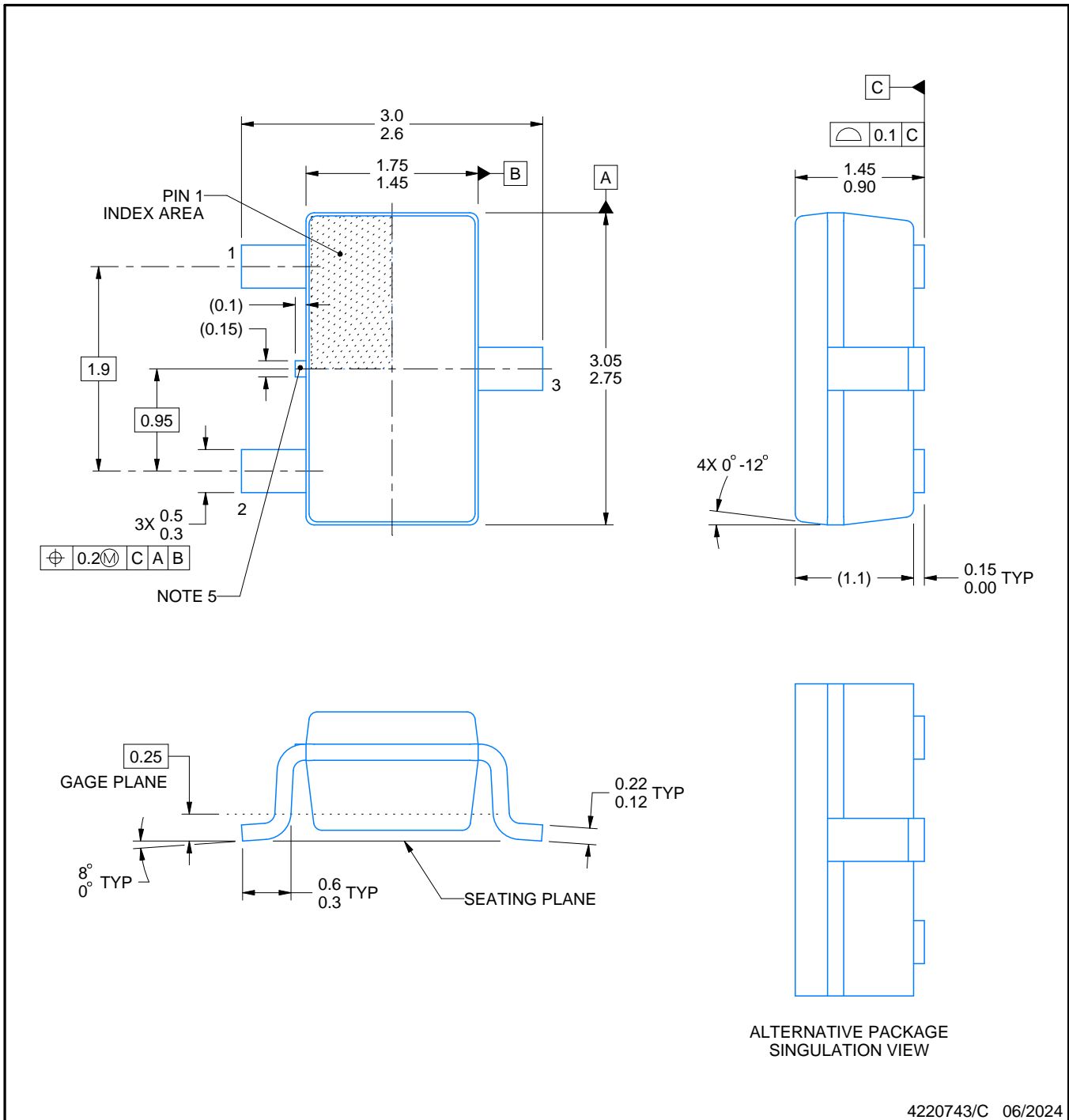
# DBV0003A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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**NOTES:**

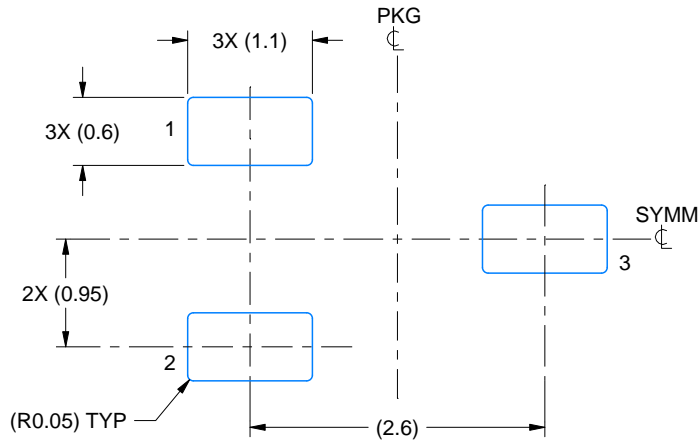
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

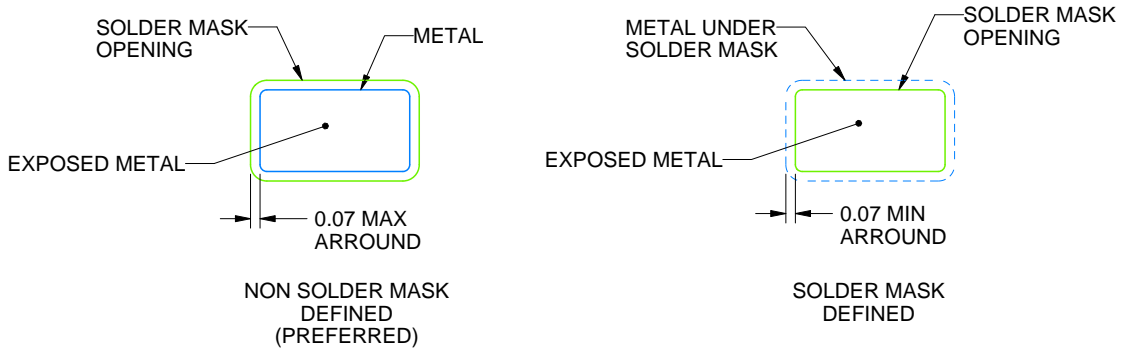
DBV0003A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

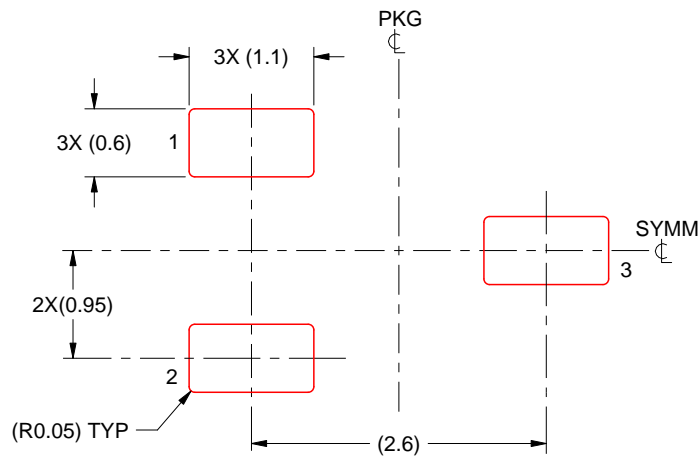
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0003A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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