DUAL D-CAP™ SYNCHRONOUS STEP-DOWN CONTROLLER FOR NOTEBOOK POWER RAILS

FEATURES

- **Fixed-Frequency Emulated On-Time Control; Frequency Selectable from Three Options**
- **D-CAP™ Mode Enables Fast Transient Response Less than 100 ns**
- **Advanced Ramp Compensation Allows Low Output Ripple with Minimal Jitter**
- **Selectable PWM-Only/OOA™/Auto-Skip Modes**
- **Wide Input Voltage Range: 5.5 V to 28 V**
- **Dual Fixed or Adjustable SMPS:**
  - **0.7 V to 5.9 V (Channel1)**
  - **0.5 V to 2.5 V (Channel2)**
- **Fixed 3.3-V/5-V, or Adjustable Output 0.7-V to 4.5-V LDO; Capable of Sourcing 100 mA**
- **Fixed 3.3-VREF Output Capable of Sourcing 10 mA**
- **Temperature Compensated Low-Side $R_{DS(on)}$ Current Sensing**
- **Adaptive Gate Drivers with Integrated Boost Switch**
- **Bootstrap Charge Auto Refresh**
- **Integrated Soft Start, Tracking Soft Stop**
- **Independent PGOOD and EN for Each Channel**
- **OOB Function Disabled. Refer to TPS51427 for OOB-Enabled Device**

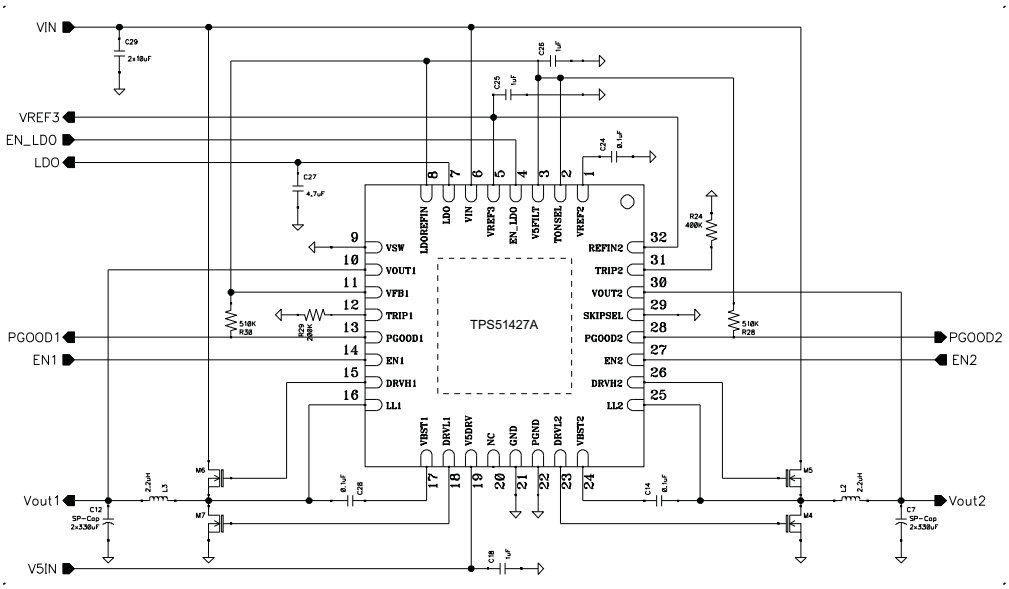
APPLICATIONS

- **Notebook I/O and System Bus Rails**
- **Graphics Application**
- **PDAs and Mobile Communication Devices**

DESCRIPTION

The TPS51427A is a dual synchronous step-down controller designed for notebook and mobile communications applications. This device is part of a low-cost suite of notebook power bus regulators that enables system designs with low external component counts. The TPS51427A includes two pulse-width-modulation (PWM) controllers, SMPS1 and SMPS2. The output of SMPS1 can be adjusted from 0.7 V to 5.9 V, while the output of SMPS2 can be adjusted from 0.5 V to 2.5 V. This device also features a low-dropout (LDO) regulator that provides a 5-V/3.3-V output, or adjustable from 0.7-V to 4.5-V output via LDOREFIN. The fixed-frequency emulated adaptive on-time control supports seamless operation between PWM mode under heavy load conditions and reduced frequency operation at light loads for high-efficiency down to the milliampere range. An integrated boost switch enhances the high-side MOSFET to further improve efficiency. The main control loop is the D-CAP™ mode that is optimized for low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP. Advanced ramp compensation minimizes jitter without degrading line and load regulation. $R_{DS(on)}$ current sensing methods offers maximum cost saving.

The TPS51427A supports supply input voltages that range from 5.5 V to 28 V. It is available in the 32-pin, 5-mm × 5-mm QFN package (Green, RoHs-compliant, and Pb-free). The device is specified from –40°C to +85°C.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NO.	TRANSPORT MEDIA	QUANTITY	ECO STATUS(2)
–40°C to +85°C	Plastic Quad Flatpack (32-pin QFN)	TPS51427ARHBT	Tape and Reel	250	Green (RoHs and No Sb/Br)
		TPS51427ARHBR		3000	

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) **Eco-Status information:** Additional details including specific material content can be accessed at www.ti.com/leadfree
GREEN: Ti defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight.
N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree.
Pb-FREE: Ti defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range; all voltages are with respect to GND (unless otherwise noted).

PARAMETER		VALUE	UNIT
5V voltage range	V5DRV, V5FILT	–0.3 to 7	V
Input voltage range(2)	VIN, ENLDO	–0.3 to 30	
	VBST1, VBST2	–0.3 to 37	
	VBST1, VBST2 (w.r.t. LLx)	–0.3 to 7	
	EN1, EN2, VOUT1, VOUT2, VFB1, REFIN2, TRIP1, TRIP2, SKIPSEL, TONSEL, VSW, LDOREFIN	–0.3 to 7	
	TRIP1, TRIP2	–0.3 to (V5FILT + 0.3)	
Output voltage range(2)	DRVH1, DRVH2	–2 to 37	V
	DRVH1, DRVH2 (w.r.t. LLx)	–0.3 to 7	
	LL1, LL2	–2 to 30	
	DRVL1, DRVL2, VREF2, PGOOD1, PGOOD2, LDO, VREF3	–0.3 to 7	
	PGND	–0.3 to 0.3	
T_{stg} Storage temperature range		–55 to +150	°C
T_J Junction temperature range		+150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS(1)

PACKAGE	T_A < +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +85°C POWER RATING
32Ld 5 × 5 QFN	2.320 W	23.2 mW/°C	0.93 W

(1) Dissipation ratings are calculated based on the usage of nine standard thermal vias and thermal pad soldered on the PCB. If thermal pad is not soldered to the PCB, the junction-to-ambient thermal resistance is 88.6°C/W.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

		MIN	TYP	MAX	UNIT
Supply input voltage range	V5DRV, V5FILT	4.5		5.5	V
Input voltage range	VBST1, VBST2	–0.1		34	
	VBST1, VBST2 (with regard to LLx)	–0.1		5.5	
	EN1, EN2, VOUT1, VFB1, REFIN2, TRIP1, TRIP2, SKIPSEL, TONSEL, ENLDO,VSW, LDOREFIN	–0.1		5.5	
	VOUT2	–0.1		3.7	
Output voltage range	DRVH1, DRVH2	–0.8		34	V
	DRVH1, DRVH2 (w.r.t. LLx)	–0.1		5.5	
	LL1, LL2	–0.8		28	
	DRVL1, DRVL2, VREF2, PGOOD1, PGOOD2, LDO, VREF3	–0.1		5.5	
	PGND	–0.1		0.1	
Operating free-air temperature, T_A		–40		+85	°C

ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range, V_{V5DRV} = 5 V, V_{VIN} = 12 V (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLIES					
VIN Input Voltage Range	LDO in regulation	5.5		28	V
VIN Operating Supply Current	LDO switched over to VSW, 4.5-V to 5.5-V SMPS		5	10	µA
VIN Standby Current	5.5 V ≤ V_{VIN} ≤ 28 V, T_A = +25°C, no load, EN_LDO = 5 V, EN1 = EN2 = VSW = 0 V		115	150	µA
VIN Shutdown Current	5.5 V ≤ V_{VIN} ≤ 28 V, T_A = +25°C, no load, EN_LDO = EN1 = EN2 = VSW = 0 V		12	20	µA
Quiescent Power Consumption	T_A = +25°C, no load, EN_LDO = EN1 = EN2 = REFIN2 = 5 V, VFB1 = SKIPSEL = 0 V, VOUT1 = VSW = 5.3 V, VOUT2 = 3.5 V		5	7	mW
PWM CONTROLLERS					
VOUT1 Output Voltage Accuracy	5-V Preset output: 5.5 V ≤ V_{VIN} ≤ 28 V, VFB1 = 0 V, SKIPSEL = 5 V	4.975 (–1.5%)	5.05	5.125 (+1.5%)	V
	1.5-V Preset output: 5.5 V ≤ V_{VIN} ≤ 28 V, VFB1 = 5V, SKIPSEL = 5V	1.482 (–1.2%)	1.50	1.518 (+1.2%)	
	Adjustable feedback output, 5.5 V ≤ V_{VIN} ≤ 28 V, SKIPSEL = 5 V	0.693 (–1%)	0.70	0.707 (+1%)	
VOUT1 Voltage Adjust Range		0.707		5.900	V
VFB1 Threshold Voltage	5-V Preset output			0.20	V
	1.5-V Preset output	3.90			V
VFB1 Input Current	VFB1 = 0.8 V	–0.20		0.20	µA
VOUT2 Output Voltage Accuracy	3.3-V Preset output: REFIN2 = 5 V, 5.5 V ≤ V_{VIN} ≤ 28 V, SKIPSEL = 5 V	3.285 (–1.4%)	3.33	3.375 (+1.4%)	V
	1.05-V Preset output: REFIN2 = 3.3 V, 5.5 V ≤ V_{VIN} ≤ 28 V, SKIPSEL= 5 V	1.038 (-1.2%)	1.05	1.062 (+1.2%)	
	Tracking output: REFIN2 = 1.0 V, 5.5 V ≤ V_{VIN} ≤ 28 V, SKIPSEL = 5 V	0.99 (-1%)	1.00	1.01 (+1%)	
REFIN2 Voltage Adjust Range		0.50		2.50	V
REFIN2 Input Current	0.5 V ≤ $V_{VREFIN2}$ ≤ 2.5 V	–0.2		0.2	µA
REFIN2 Threshold Voltage	1.05-V Preset output	3.00		3.45	V
	3.3-V Preset output	3.90			
DC Load Regulation	Either SMPS, SKIPSEL = 5 V, 0 A to 5 A(1)		–0.10%		
	Either SMPS, SKIPSEL = 2 V, 0 A to 5 A(1)		–2.20%		
	Either SMPS, SKIPSEL = GND, 0 A to 5 A(1)		–0.50%		
Line Regulation	Either SMPS, 5.5 V < VIN < 28 V(1)		0.005		%/V
Channel1 On-Time	TONSEL = 0 V, 2 V, or OPEN (400 kHz), VOUT1 = 5.05 V	895	1052	1209	ns
	TONSEL = 5 V (200 kHz), VOUT1 = 5.05 V	1895	2105	2315	
Channel2 On-Time	TONSEL = 0 V (500 kHz), VOUT2 = 3.33 V	475	555	635	ns
	TONSEL = 2 V, OPEN, or 5 V (300 kHz), VOUT2 = 3.33 V	833	925	1017	
Minimum Off-Time		300	400	500	ns
Soft Start Ramp Time	Zero to full limit		1.8		ms
VOUT1, VOUT2 Discharge On Resistance	EN1 = EN2 = 0 V, VOUT1 = VOUT2 = 0.5 V		17	35	Ω
OOA Operating Frequency	SKIPSEL = 2 V or OPEN	22	30		kHz

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended free-air temperature range, V_{V5DRV} = 5 V, V_{VIN} = 12 V (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LINEAR REGULATOR (LDO)					
LDO Output Voltage	LDOREFIN = VSW = 0 V, 0 < I_{LDO} < 10 0mA, 6 V< VIN< 28 V	4.94 (–1.7%)	5.025	5.11 (+1.7%)	V
	LDOREFIN = 5 V, VSW = 0 V, 0 < I_{LDO} < 100 mA, 5.5 V < VIN < 28 V	3.28 (–1.5%)	3.33	3.38 (+1.5%)	
	LDOREFIN = 0.5 V, VSW = 0 V, 0 < I_{LDO} < 50 mA, 5.5V < VIN < 28 V	0.98 (–2%)	1.00	1.02 (+2%)	
LDOREFIN Input Range	VLDO = 2 × VLDOREFIN	0.35		2.25	V
LDOREFIN Leakage Current	VLDOREFIN = 0 V or 5 V	–0.5		0.5	µA
LDOREFIN Threshold Voltage	Fixed LDO = 5 V			0.15	V
	Fixed LDO = 3.3 V	3.90			
LDO Output Current	VSW = GND , VIN = 5.5 V to 28 V			100	mA
LDO Output Current During Switchover to 5 V	VSW = 5 V , VIN = 5.5 V to 28 V, LDOREFIN = 0 V		340	500	mA
LDO Output Current During Switchover to 3.3 V	VSW = 3.3 V , VIN = 5.5 V to 28 V, LDOREFIN = 5 V		330	500	mA
LDO Short-Circuit Current	VSW = LDO = 0 V	140	180	220	mA
LDO 5-V Switchover Threshold	Rising edge of VSW, LDOREFIN = 0 V	4.63 (92.6%)	4.78 (95.6%)	4.93 (98.6%)	V
	Hysteresis		0.20		
LDO 3.3-V Switchover Threshold	Rising edge of VSW, LDOREFIN = 5 V	3.05 (92.5%)	3.15 (95.5%)	3.25 (98.5%)	V
	Hysteresis		0.150		
LDO Switchover Switch On Resistance	LDO to VSW, VSW = 5 V, ILDO = 100 mA		0.7	1.5	Ω
LDO Switchover Delay	Turning on		3.96		ms
LDO Undervoltage Lockout Threshold	Falling edge of V5FILT	3.80	3.93	4.10	V
	Rising edge of V5FILT	4.20	4.37	4.50	
VIN POR Threshold	Falling edge of VIN		1.8		V
	Rising edge of VIN		2.1		
Thermal-Shutdown Threshold	Hysteresis = +10°C (2)		+140		°C
3.3V ALWAYS-ON LINEAR REGULATOR (VREF3)					
VREF3 Output Voltage	No external load, V_{VSW} > 4.5 V	3.250 (–1.5%)	3.300	3.350 (+1.5%)	V
	No external load, V_{VSW} < 4.0 V	3.220 (–2.4%)	3.300	3.380 (+2.4%)	
VREF3 Load Regulation	0 mA < I_{LOAD} < 10 mA			60	mV
VREF3 Current Limit	VREF3 = GND		15	20	mA
VREF3 Undervoltage Lockout Threshold	Falling edge of VREF3		2.96		V
	Hysteresis		0.17		

(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended free-air temperature range, V_{V5DRV} = 5 V, V_{VIN} = 12 V (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE (REF)					
VREF2 Output Voltage	$\|I_{VREF2}\|$ = 0 µA	1.98 (–1%)	2.00	2.02 (+1%)	V
	$\|I_{VREF2}\|$ < 50 µA	1.975 (–1.25%)	2.00	2.025 (+1.25%)	
VREF2 Sink Current	VREF2 in regulation	50			µA
VREF2 Undervoltage Lockout Threshold	Falling edge of VREF2	1.575	1.700	1.825	V
	Hysteresis		0.1		
OUT1 FAULT DETECTION					
Overvoltage Trip Threshold	VFB1 with respect to nominal regulation point	+12.5%	+15%	+17.5%	
Overvoltage Fault Propagation Delay	VFB1 delay with 50-mV overdrive		10		µs
Undervoltage Trip Threshold	VFB1 with respect to nominal output voltage	–35%	–30%	–25%	
Undervoltage Fault Propagation Delay		0.8	1	1.2	ms
Undervoltage Fault Enable Delay	From ENx signal	10	20	30	ms
PGOOD1 Lower Trip Threshold	VFB1 with respect to nominal output, falling edge, typical hysteresis = 5%	–12.5%	–10%	–7.5%	
PGOOD1 Low Propagation Delay	Falling edge, 50-mV overdrive		10		µs
PGOOD1 High Propagation Delay	Rising edge, 50-mV overdrive	0.8	1.0	1.2	ms
PGOOD1 Output Low Voltage	PGOOD1 Low impedance, I_{SINK} = 4 mA		0.4	0.8	V
PGOOD1 Leakage Current	PGOOD1 High impedance, forced to 5.5 V			1	µA
OUT2 FAULT DETECTION					
Overvoltage Trip Threshold	REFIN2 with respect to nominal regulation point	+12.5%	+15.0%	+17.5%	
Overvoltage Fault Propagation Delay	REFIN2 delay with 50-mV overdrive		10		µs
Undervoltage Trip Threshold	REFIN2 with respect to nominal output voltage	–35%	–30%	–25%	
Undervoltage Fault Propagation Delay		0.8	1	1.2	ms
Undervoltage Fault Enable Delay	From ENx signal	10	20	30	ms
PGOOD2 Lower Trip Threshold	REFIN2 with respect to nominal output, falling edge, typical hysteresis = 5%	–12.5%	–10%	–7.5%	
PGOOD2 Low Propagation Delay	Falling edge, 50-mV overdrive		10		µs
PGOOD2 High Propagation Delay	Rising edge, 50-mV overdrive	0.8	1.0	1.2	ms
PGOOD2 Output Low Voltage	PGOOD2 Low impedance, I_{SINK} = 4 mA		0.4	0.8	V
PGOOD2 Leakage Current	PGOOD2 High impedance, forced to 5.5 V			1	µA

ELECTRICAL CHARACTERISTICS (continued)

Over recommended free-air temperature range, V_{V5DRV} = 5 V, V_{VIN} = 12 V (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT					
TRIPx Adjustment Range		0.2		2.0	V
TRIPx Source Current	0.2 V < V_{TRIPx} < 2 V, T_A = +25°C	4.75 (–5%)	5	5.25 (+5%)	µA
TRIPx Current Temperature	Coefficient on the basis of T_A = +25°C (3)		2900		ppm/°C
Current-Limit Threshold (Positive, Adjustable)	GND – LLx, V_{TRIPx} = 0.2 V	13 (–35%)	20	27 (+35%)	mV
	GND – LLx, V_{TRIPx} = 0.5 V	42.5 (–15%)	50	57.5 (+15%)	
	GND – LLx, V_{TRIPx} = 1 V	93 (–7%)	100	107 (+7%)	
	GND – LLx, V_{TRIPx} = 2 V	190 (–5%)	200	210 (+5%)	
Current-Limit Threshold (Positive, Default)	V_{TRIPx} = 5.0 V, GND – LLx (no temperature compensation)	93 (–7%)	100	107 (+7%)	mV
Fixed 100-mV OCL TRIPx Threshold Voltage	High threshold	3.0	3.2	3.3	V
	Hysteresis	40	70	100	mV
Current Limit Threshold (Negative)	With respect to valley current limit threshold, SKIPSEL = 5 V		–100%		
Zero-Crossing Current Limit Threshold	SKIPSEL = 0 V, 2 V, or OPEN, GND – LLx	–3.5	0	3.5	mV
GATE DRIVERS					
DRVHx Gate-Driver On-Resistance	Source, VBSTx-DRVHx = 0.1 V		1.0	3.6	Ω
	Sink, DRVHx-LLx = 0.1 V		0.8	2.6	
DRVLx Gate-Driver On-Resistance	Source, V5DRV-DRVLx = 0.1 V		1.2	4.0	Ω
	Sink, DRVLx-PGND = 0.1 V		0.6	1.5	
DRVHx Gate-Driver Source Current	VBSTx-LLx = 5 V, DRVHx = 2.0 V(3)		1.8		A
DRVHx Gate-Driver Sink Current	VBSTx-LLx = 5 V, DRVHx = 2.0 V(3)		1.6		A
DRVLx Gate-Driver Source Current	V5DRV-PGND = 5 V, DRVLx = 2.0 V(3)		1.4		A
DRVLx Gate-Driver Sink Current	V5DRV-PGND = 5 V, DRVLx = 2.0 V(3)		2.6		A
Dead Time	DRVHx low (DRVHx = 1 V) to DRVLx high (DRVLx = 4 V), LLx = –0.05 V	20	30	50	ns
	DRVLx low (DRVLx = 1 V) to DRVHx high (DRVHx = 4 V), LLx = –0.05 V	25	40	60	ns
Internal BST_ Switch On-Resistance	I_{VBSTx} = 10 mA, V5DRV = 5 V, T_A = +25°C		10		Ω
VBSTx Leakage Current	V_{VBSTx} = 35 V, LLx = 28 V		0.01	2.0	µA

(3) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended free-air temperature range, V_{V5DRV} = 5 V, V_{VIN} = 12 V (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUTS AND OUTPUTS					
TONSEL Input Logic Levels	High level	2.9			V
	Float level	1.85		2.25	
	Low level			0.45	
SKIPSEL Input Logic Levels	High threshold (PWM Only)	2.9			V
	Float level (OOA)	1.85		2.25	
	Low level (Auto Skip)			0.45	
SKIPSEL, TONSEL Input Current	SKIPSEL = TONSEL = 0 V	2.5	4.0	5.5	µA
EN1, EN2 Input Logic Levels	SMPS On level	2.9			V
	Delay start level	1.85		2.25	
	SMPS Off level			0.45	
EN1, EN2 Leakage Current	EN1 = EN2 = 0 V	–0.1		0.1	µA
EN_LDO Input Logic Levels	Rising edge	1.3	1.65	1.9	V
	Hysteresis		0.6		
EN_LDO Input Current	EN_LDO = 0 V	0.7	1.0	1.3	µA
	EN_LDO = 30 V	–0.1	0	0.1	

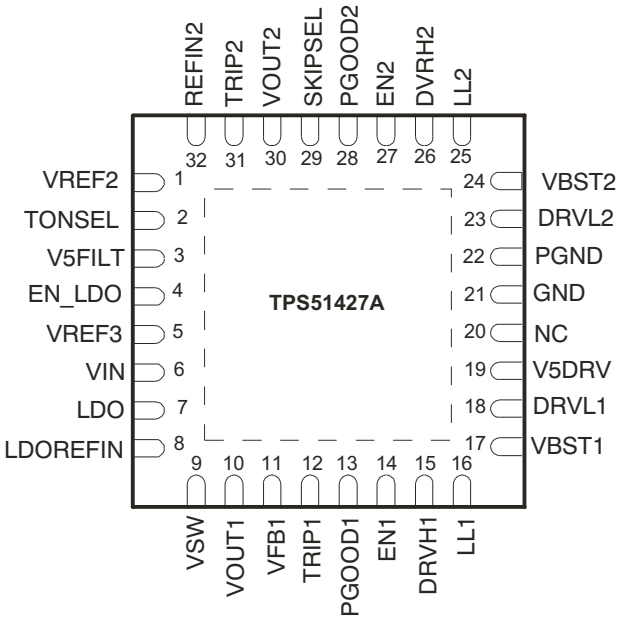
DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DRVH1	15	O	High-side N-Channel FET driver outputs. LL referenced floating drivers. The gate drive voltage is defined by the voltage across VBST to LL node bootstrap capacitor.
DRVH2	26		
DRVL1	18	O	Synchronous low-side MOSFET driver outputs. Ground referenced drivers. The gate drive voltage is defined by V5DRV voltage.
DRVL2	23		
EN1	14	I	Channel enable pins. If EN1 is connected to VREF2, Channel1 starts after Channel2 reaches regulation (delay start). If EN2 is connected to VREF2, Channel2 starts after Chanel1 reaches regulation.
EN2	27		
EN_LDO	4	I	LDO Enable Input. The LDO is enabled if EN_LDO is within logic high level and disabled if EN_LDO is less than the logic low level.
GND	21	I	Analog ground for both channels and LDO.
LL1	16	I/O	Phase node connections for high-side drivers. These connections also serve as inputs to current comparators for $R_{DS(on)}$ sensing and input voltage monitor for on-time control circuitry.
LL2	25		
LDO	7	O	Linear regulator output. The LDO regulator can provide a total of 100-mA external loads. The LDO regulates at 5 V If LDOREFIN is connected to GND. When the LDO is set at 5 V and VSW is within a 5-V switchover threshold, the internal regulator shuts down and the LDO output pin connects to VSW through a 0.7-Ω switch. The LDO regulates at 3.3 V if LDOREFIN is connected to V5FILT. When the LDO is set at 3.3 V and VSW is within a 3.3-V switchover threshold, the internal regulator shuts down and the LDO output pin connects to VSW through a 0.7-Ω switch. Bypass the LDO output with a minimum of 4.7-µF ceramic capacitance.
LDOREFIN	8	I	LDO Reference Input. Connect LDOREFIN to GND for fixed 5-V operation. Connect LDOREFIN to V5FILT for fixed 3.3-V operation. LDOREFIN can be used to program LDO output voltage from 0.7 V to 4.5 V. LDO output is twice the voltage of LDOREFIN. There is no switchover in adjustable mode.
PGND	22	I	Ground pin for drivers and LS synchronous FET source terminals. This pin is also the input to zero crossing comparator and overcurrent comparator.
PGOOD1	13	O	Channel1/Channel2 power-good open-drain output. PGOOD1/PGOOD2 is low when the Channel1/Channel2 output voltage is 10% less than the normal regulation point, at onset of OVP events, or during soft start. PGOOD1/PGOOD2 is high impedance when the output is in regulation and the soft-start circuit has terminated. PGOOD1/PGOOD2 is low in shutdown.
PGOOD2	28		
REFIN2	32	I	Output voltage control for Channel2. Connect REFIN2 to V5FILT for fixed 3.3-V operation. Connect REFIN2 to VREF3 for fixed 1.05-V operation. REFIN2 can be used to program Channel2 output voltage from 0.5 V to 2.5 V.
NC	20	-	
SKIPSEL	29	I	Low-noise mode control. Connect SKIPSEL to GND for Auto Skip mode operation or to V5FILT for PWM mode (fixed frequency). Connect to VREF2 or leave floating for OOA™ mode operation.
TONSEL	2	I	Frequency select input. Connect to GND for 400-kHz/500-kHz operation. Connect to VREF2 (or leave open) for 400-kHz/300-kHz operation. Connect to V5FILT for 200-kHz/300-kHz operation (5-V/3.3-V SMPS switching frequencies, respectively).
TRIP1	12	I	Overcurrent trip point set input. Sourcing current is 5 µA at RT with 2900 ppm/°C temperature coefficient.
TRIP2	31		
V5DRV	19	I	Supply voltage for the low-side MOSFET driver DRVL1/DRVL2. Connect a 5-V power source to the V5DRV pin (bypass with 4.7-µF MLCC capacitor to PGND if necessary).
V5FILT	3	I	5-V analog supply input.
VFB1	11	I	Channel1 feedback input. Connect VFB1 to GND for fixed 5-V operation. Connect VFB1 to V5FILT for fixed 1.5-V operation. Connect VFB1 to a resistive voltage divider from OUT1 to GND to adjust the output from 0.7 V to 5.9 V.
VBST1	17	I	Supply input for high-side MOSFET driver (bootstrap terminal). Connect a capacitor from this pin to the respective LL terminals.
VBST2	24		
VIN	6	I	Power supply input. VIN supplies power to the linear regulators. The linear regulators are powered by Channel1 if VOUT1 is set greater than 5 V and VSW is tied to VOUT1.
VOUT1	10	O	Output connections to SMPS. These terminals serve two functions: on-time adjustment and output discharge.
VOUT2	30		
VREF2	1	O	2-V reference output. Bypass to GND with a 0.1-µF capacitor. VREF2 can source up to 50 µA for external loads.
VREF3	5	O	3.3-V reference output. VREF3 can source up to 10 mA for external loads. Bypass to GND with a 1-µF capacitor.
VSW	9	I	VSW is the switchover source voltage for the LDO when LDOREFIN is connected to GND or V5FILT. Connect VSW to 5 V if LDOREFIN is tied GND. Connect VSW to 3.3 V if LDOREFIN is tied to V5FILT.

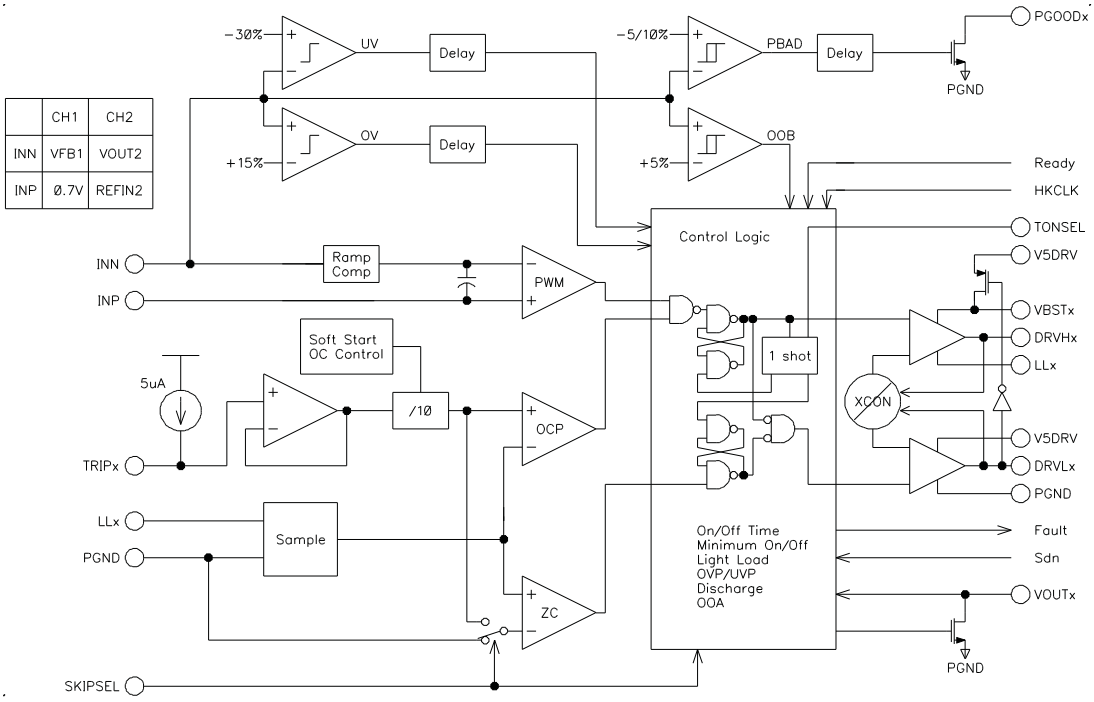
QFN-32, 5-mm × 5-mm
(TOP VIEW)

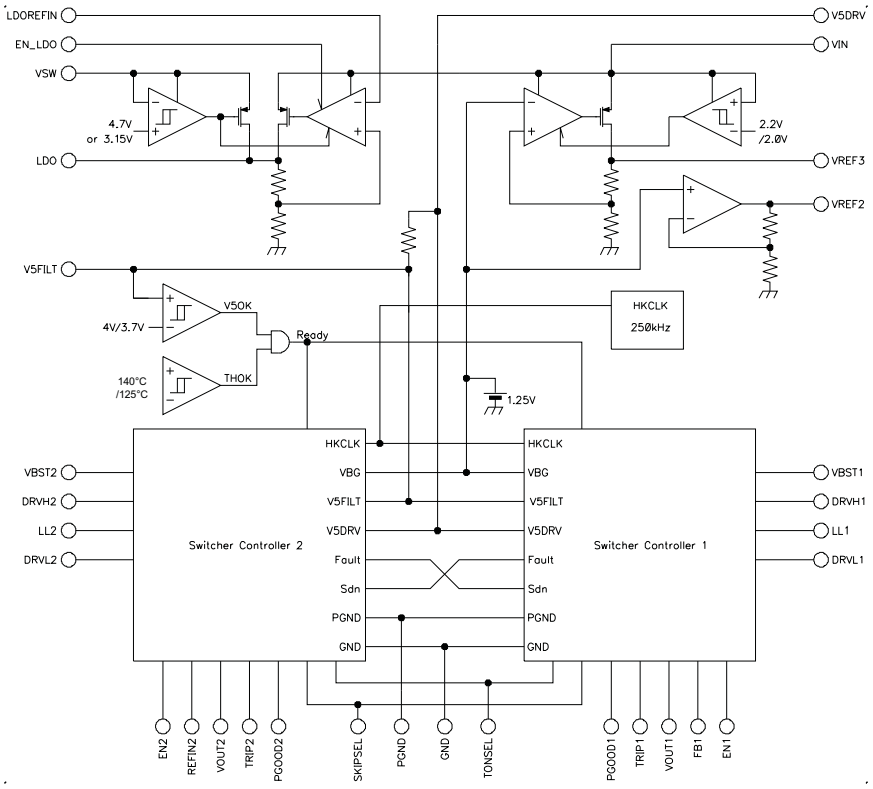
RHB PACKAGE
(TOP VIEW)



NC = No connection.

FUNCTIONAL BLOCK DIAGRAMS





DETAILED DESCRIPTION

BASIC PWM OPERATION

The main control loop of the TPS51427A is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports a proprietary D-CAP™ mode that uses internal compensation circuitry and is suitable for a minimal external component count configuration when an appropriate amount of ESR at the output capacitor(s) is allowed. D-CAP mode can also enable stable operation when using capacitors with low ESR, such as specialty polymer capacitors.

The basic operation of D-CAP mode can be described in this way: At the beginning of each cycle, the synchronous high-side MOSFET turns on or goes to an *ON* state. This MOSFET turns off, or returns to an *OFF* state, after an internal one-shot timer expires. The one-shot timer is determined by VIN and VOUT and keeps the frequency fairly constant over the input voltage range under steady-state conditions; it is an adaptive on-time control or *fixed-frequency emulated* on-time control. The MOSFET turns on again when the following two conditions occur:

- Feedback information, monitored at the VFB1/VOUT2 voltage, indicates insufficient output voltage; and
- the inductor current information indicates that current is below the overcurrent limit.

Operating in this manner, the controller regulates the output voltage. The synchronous low-side or the *rectifying* MOSFET is turned on each OFF state to keep the conduction loss minimum.

LIGHT LOAD CONDITIONS

The TPS51427A supports three selectable operating modes: PWM-only, Out-Of-Audio (OOA™), and Auto-Skip.

If the SKIPSEL pin is connected to GND, Auto-Skip mode is selected. This mode enables a seamless transition to the reduced frequency operation under light load conditions so that high efficiency is maintained over a wide range of load current. This frequency reduction is achieved smoothly and without an increase in V_{OUT} ripple or load regulation.

Auto-Skip operation can be described in this way: As the output current decreases from a heavy load condition, the inductor current is also reduced. Eventually, the inductor current reaches the point that its *valley* equals zero current; that is, the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET turns off when this zero inductor current is detected. Because the output voltage remains higher than the reference voltage at this point, both high-side and low-side MOSFETs are turned off and wait for the next cycle. As the load current decreases further, the converter runs in discontinuous conduction mode and takes longer to discharge the output capacitor below the reference voltage. Note that the *ON* time remains the same as that in the heavy load condition. On the other hand, when the output current increases from a light load to a heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction limit. The transition load point to the light load operation $I_{OUT(LL)}$ (that is, the threshold between continuous conduction and discontinuous conduction mode) can be calculated as shown in Equation 1:

$$I_{OUT(LL)} = \left(\frac{1}{2 \times L \times f_{SW}} \right) \times \left(\frac{(V_{VIN} - V_{VOUT}) \times V_{VOUT}}{V_{VIN}} \right) \quad (1)$$

Where f_{SW} is the PWM switching frequency. Switching frequency versus output current under a light load condition is a function of L, f_{SW}, V_{IN}, and V_{OUT}, but decreases at a near-proportional rate to the output current from the $I_{OUT(LL)}$ threshold. For example, the frequency is approximately 60 kHz at $I_{OUT(LL)}/5$ if the PWM switching frequency is 300 kHz.

PWM-only mode is selected if the SKIPSEL pin is connected to 5 V. The rectifying MOSFET does not turn off when the inductor current reaches zero. The converter runs in forced continuous conduction mode over the entire load range. System designers may want to use this mode to avoid certain frequencies under light load conditions but do so at the cost of lower efficiency. However, keep in mind that the output has the capability to both source and sink current in this mode. If the output terminal is connected to a voltage source that is higher than the regulator target value, the converter sinks current from the output and boosts the charge into the input capacitors. This operation may cause an unexpected high voltage at VIN and may damage the power FETs.

If SKIPSEL pin is connected to VREF2 or left floating, OOA mode operation is selected.

Table 1. SKIPSEL Operating Modes

SKIPSEL	GND	FLOAT/VREF2	V5IN
Operating Mode	Auto Skip	OOA™	PWM Only

OUT-OF-AUDIO (OOA™) OPERATION

If out-of-audio (OOA) operation is enabled, the switching frequency of the channel remains higher than the audible frequency under any load condition, at a minimum of 22 kHz to minimize the audible noise in the system. The TPS51427A automatically reduces switching frequencies under light load conditions. The OOA control circuit monitors the switching period and forces the high-side MOSFET to turn on if the switching frequency goes below the 22-kHz threshold.

The high-side MOSFET turns on even if the output voltage is higher than the target value; therefore, the output voltage tends to be higher when operating in OOA mode. The OOA control circuit detects the overvoltage condition and prevents the voltage from rising by re-modulating the device on time. The overvoltage condition is detected by the VFB1/VOUT2 voltages.

The inductor current ripple (peak-to-peak) should be less than two-thirds of the OCL setting for the OOA circuit to work properly at a 0-A load. To keep the OOA mode loop stable, the output voltage ripple cannot be too large. If OOA mode operation is desired, the recommended output ripple voltage cannot be more than 1% of the target dc voltage.

RAMP COMPENSATION

The TPS51427A employs an advanced ramp compensation technique in D-CAP mode to optimize jitter performance. An internal ramp signal is added to the reference voltage to virtually increase the slope of the VFB1/VOUT2 down ramp, which the PWM comparator uses to determine the turn-on timing.

LOW-SIDE DRIVER

The low-side driver is designed to drive high-current, low $R_{DS(on)}$, N-channel MOSFET(s). The drive capability is represented by its internal resistance: 1.2 Ω for V5DRV to DRVLx and 0.6 Ω for DRVLx to PGND. A dead time to prevent shoot-through is generated internally between the two transistors, with the top MOSFET off and bottom MOSFET on, and then with the bottom MOSFET off and the top MOSFET on. A 5-V bias voltage is delivered from the V5DRV supply. The instantaneous drive current is supplied by an input capacitor connected between V5DRV and GND. The average drive current is equal to the gate charge at V_{GS} = 5 V times the switching frequency.

HIGH-SIDE DRIVER

The high-side driver is also designed to drive high-current, low $R_{DS(on)}$, N-channel MOSFET(s). When configured as a floating driver, a 5-V bias voltage is delivered from the V5DRV supply. The average drive current is also calculated by the gate charge at V_{GS} = 5 V times the switching frequency. The instantaneous drive current is supplied by the floating capacitor between the VBSTx and LLx pins. The drive capability is represented by its internal resistance: 1.0 Ω for VBSTx to DRVHx and 0.8 Ω for DRVHx to LLx.

BOOSTRAP CHARGE AUTO REFRESH

Boost undervoltage protection is activated during the device *ON* time when the voltage difference between DRVH and LL becomes less than 1.8 V. Upon detection of the undervoltage condition, the high-side gate driver immediately turns off and the low-side gate driver turns on after the deadtime expires for the minimum off time in an attempt to recharge the boost capacitor.

PWM FREQUENCY AND ADAPTIVE ON-TIME CONTROL

The TPS51427A employs an adaptive on-time control scheme and does not have a dedicated onboard oscillator. However, the device runs with pseudo-constant frequency by feed-forwarding the input voltage and output voltage into the on-time one-shot timer. The frequencies are set by the TONSEL terminal connection as Table 2 shows. The on-time is controlled: it is inversely proportional to the input voltage and proportional to the output voltage, so that the duty ratio maintains technically as VOUT/VIN with the same cycle time. Although the TPS51427A does not use VIN directly, the input voltage is monitored at the LLx pin during the *ON* state.

Table 2. TONSEL Terminal Connection Options

TONSEL	GND	VREF2 or Float	V5FILT
Channel1 Frequency	400 kHz	400 kHz	200 kHz
Channel2 Frequency	500 kHz	300 kHz	300 kHz

ENABLE AND SOFT START

TPS51427A has an internal digital soft-start timer that begins to ramp up to the maximum allowed current limit during device startup. The soft-start ramp occurs in five steps of positive current limit; step sizes are 20%, 40%, 60%, 80%, and 100%. Smooth control of the output voltage during device startup is maintained. In addition, if tracking discharge is required, the ENx pin can be used to control the output voltage discharge smoothly. At the beginning of the soft-start period, the rectifying MOSFET maintains an off state until the top MOSFET turns on at least once. This architecture prevents a high negative current from flowing back from the output capacitor in the event of an output capacitor pre-charged condition.

If EN1 is connected to VREF2, Channel1 starts up after the Channel2 reaches regulation (delay start). If EN2 is connected to VREF2, Channel2 starts up after the Channel1 reaches regulation (delay start).

When both ENx are low and ENLDO is low, the TPS51427A enters a shutdown state and consumes less than 15 μA.

POWER-GOOD

The TPS51427A has a power-good output (PGOODx) for each switching channel. The power-good function activates after the soft start finishes. If the output voltage reaches within ±95% of the target value, internal comparators detect a power-good state and the power-good signal goes high after a 1-ms internal delay. If the output voltage falls below 90% of the target value, the power-good signal goes low after a 10-μs internal delay.

OUTPUT SHUTDOWN AND DISCHARGE CONTROL

The TPS51427A discharges the output when ENx is low, or when the controller is shut down by the circuit protection functions (OVP, UVP, UVLO, and thermal shutdown). The TPS51427A discharges the outputs using an internal, 17-Ω MOSFET that is connected to VOUTx and PGND. The external low-side MOSFET does not turn on during the output discharge operation to avoid the possibility of causing a negative voltage at the output. The output discharge time constant is a function of the output capacitance and the resistance of the internal discharge MOSFET. This discharge ensures that on device restart, the regulated voltage always starts from 0 V. If an SMPS restarts before the discharge completes, the discharge action is terminated and switching resumes after the reference level (ramped up by an internal digital-to-analog converter, or DAC) returns to the remaining output voltage. When shutdown mode activates, the 3.3-V VREF3 remains on.

2-V REFERENCE (VREF2)

The 2-V reference is useful for generating auxiliary voltages. The tolerance for this reference voltage is ±1.25% over a 50-μA load and –40°C to +85°C ambient temperature range. This reference is enabled when ENLDO goes high, and shuts down after both switching channels are turned off and ENLDO is shut down. If this output is forcibly tied to ground, both SMPSs are turned off without a latch. Bypass the VREF2 pin to GND with a minimum 0.1-μF ceramic capacitor.

3-V REFERENCE (VREF3)

The 3.3-V reference (VREF3) is accurate to ±1.5% over temperature, making VREF3 useful as a precision system reference for the real-time clock (RTC) circuit in many notebook applications. VREF3 can supply up to 10 mA for external loads. Bypass VREF3 to GND with a 1-μF capacitor. VREF3 is activated when VIN rises above 2.1 V, and remains on even when the SMPS and LDO are both shut down. VREF3 is deactivated if VIN falls below 1.8 V. In thermal shutdown conditions, VREF3 remains activate.

LDO

When the LDOREFIN pin is connected to GND, the TPS51427A internal linear regulator produces a fixed 5-V LDO output; when LDOREFIN is connected to V5FILT, the linear regulator produces a fixed 3.3-V LDO output. The LDO regulator can supply up to 100 mA for external loads. Bypass the LDO with a minimum 4.7-µF ceramic capacitor. When the LDO is fixed at 5 V, and VSW voltage is equal to or greater than 4.7 V, the 5 V LDO switches off after a 3.8-ms delay, and the 5V rail is bootstrapped to the VSW output, thereby improving the efficiency of the converter. A glitch-free switchover is also accomplished. The switchover impedance from the VSW pin to the LDO pin is typically 0.7 Ω. In the same way, when the LDO is fixed at 3.3-V and the VSW voltage is equal to or greater than 3.15 V, the 3.3-V LDO switches off after a delay of 4 ms, and the 3.3-V rail is bootstrapped to the VSW output.

In adjustable mode, the LDO output can be set from 0.7 V to 4.5 V. The LDO output voltage is equal to two times the LDOREFIN voltage. There is no switchover action in adjustable mode.

For the 5-V LDO output, a 4.7-µF ceramic capacitor (minimum) is required from the LDO to GND. For the 3.3-V LDO output, a 10-µF ceramic capacitor (minimum) is required from the LDO to GND. If a lower voltage LDO output is desired, scale the output capacitance of the LDO according to Equation 2.

$$C_{LDO(min)} = \frac{5\,V}{V_{LDO}} \times 4.7\,\mu F \tag{2}$$

For example, if V_{LDO} = 1 V, $C_{LDO(min)}$ = 23.5 µF. Use the standard capacitance value to choose 27 µF for the 1-V LDO output.

CURRENT SENSING AND OVERCURRENT PROTECTION

In order to provide the most cost-effective solution, the TPS51427A supports low-side MOSFET $R_{DS(on)}$ sensing for overcurrent protection. In any setting, the output signal of the current amplifier becomes 100 mV at the overcurrent limit (OCL) set point. This configuration means that the current sensing amplifier normalizes the current information signal based on the OCL setting.

The TPS51427A supports cycle-by-cycle OCL control. The controller does not allow the next *ON* cycle while the current level is above the trip threshold. The overcurrent trip threshold voltage is determined by the TRIPx pin as Table 3 shows. The TRIPx terminal sources 5-µA current with a 2900ppm/°C temperature slope, with respect to its +25°C value, to compensate the temperature dependency of the MOS $R_{DS(on)}$. The trip level is set to the voltage across R_{TRIPx} when TRIPx is between 200 mV and 2 V at room temperature. When the TRIPx pin is tied to 5 V directly, the controller defaults to 100 mV fixed OCL setting. With this option, temperature compensation is not obtained.

Table 3. Overcurrent Trip Threshold Voltage

TRIPx	0.2 V to 2 V	5 V
OCL threshold in $R_{DS(on)}$ sensing	20 mV to 200 mV	100 mV
Temperature Coefficient (ppm/°C)	2900	None

The overcurrent condition is detected during the *OFF* state; therefore, I_{TRIP} sets the valley level of the inductor current. Thus, the load current at overcurrent threshold, I_{OCP}, can be calculated in Equation 3.

$$I_{OCP} = I_{TRIP} + \left(\frac{I_{RIPPLE}}{2}\right) = I_{TRIP} + \left(\frac{1}{2 \times L \times f}\right) \times \left(\frac{(V_{VIN} - V_{VOUT}) \times V_{VOUT}}{V_{VIN}}\right) \tag{3}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor. As a result, the output voltage tends to drop, and ends up crossing the undervoltage protection threshold, and the device shuts down.

The TPS51427A also supports a cycle-by-cycle negative overcurrent limit in PWM-only mode. The negative overcurrent limit is set to be negative, but at the same absolute value as the positive overcurrent limit. If the output voltage continues to rise, the bottom MOSFET is always on; the inductor current reduces and reverse direction after it reaches zero. When there is too much negative current in the inductor, the bottom MOSFET turns off and a new on-time period is initiated; that is, the top MOSEFET turns on to allow current to flow into VIN. After the on-time expires, the bottom MOSFET turns on again. This protection ensures a maximum allowable discharge capability when the output voltage continues to rise, effectively reducing the possibility of the overvoltage protection (OVP) circuitry.

OVERVOLTAGE/UNDERVOLTAGE PROTECTION

The TPS51427A monitors the feedback voltage for Channel1 and output voltage for Channel2 to detect both over- and undervoltage conditions. When the output voltage becomes 15% higher than the target value, the OVP comparator output goes high after a 10-µs propagation delay; the circuit then latches the top MOSFET driver off and the bottom MOSFET driver on, until the negative OCL limit is reached. At that time, the bottom MOSFET turns off and the top MOSFET turns on for the minimum on-time. Once the minimum on-time expires, the bottom MOSFET turns on again. This process repeats until the valley current of the inductor is above the negative overcurrent limit. Once the inductor valley current is greater than the OCL, the bottom MOSFET remains on until it is reset. Upon OVP activation, both PGOODx outputs are pulled low.

When the voltage becomes lower than 70% of the target voltage, the undervoltage protection (UVP) comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the TPS51427A latches both top and bottom MOSFETs off and shuts off the other channel as well. This function is enabled after the device soft start completes.

UNDERVOLTATGE LOCKOUT (UVLO) PROTECTION

The TPS51427A has V5FILT undervoltage lockout (UVLO) protection. When the V5FILT voltage is lower than the UVLO threshold voltage, the TPS51427A shuts off. This feature is a non-latched protection circuit.

THERMAL SHUTDOWN

The TPS51427A monitors the temperature of the die itself. If the temperature exceeds the threshold value (typically +140°C), the TPS51427A shuts down. This feature is a non-latched protection circuit.

TYPICAL CHARACTERISTICS

SYSTEM DUAL RAILS

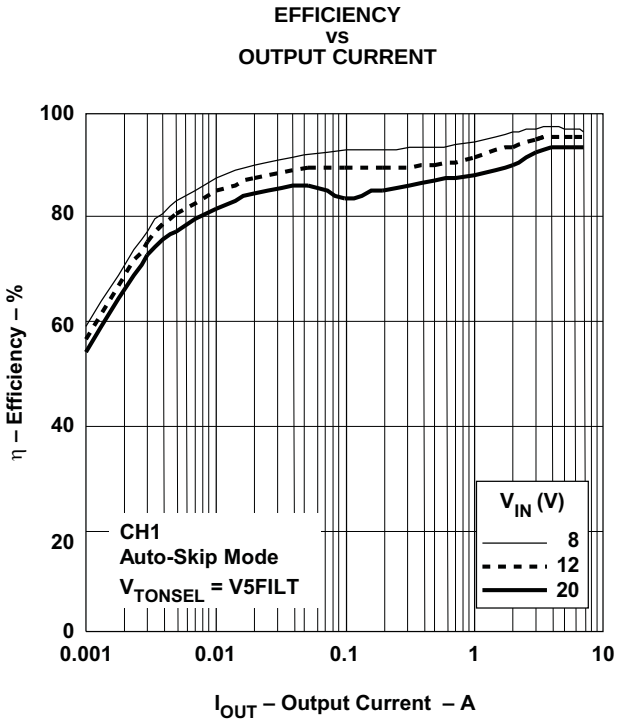


Figure 1. 5-V Efficiency in Auto-Skip Mode

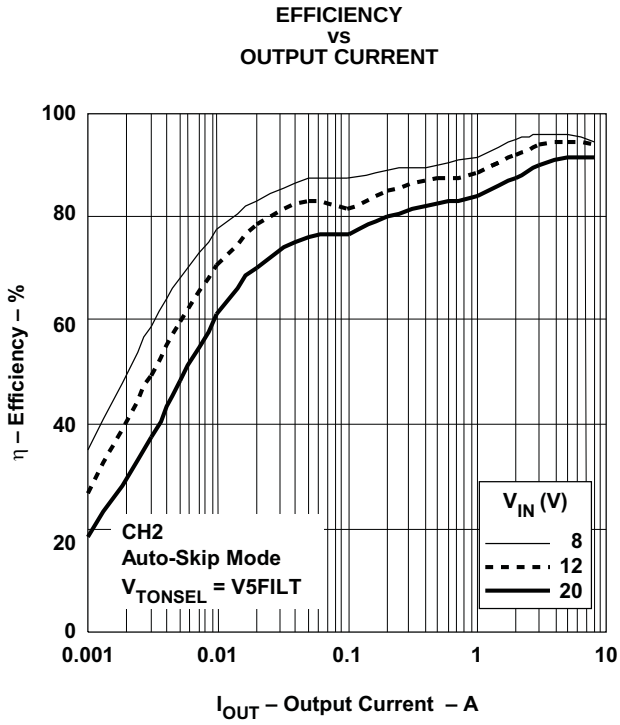


Figure 2. 3.3-V Efficiency in Auto-Skip Mode

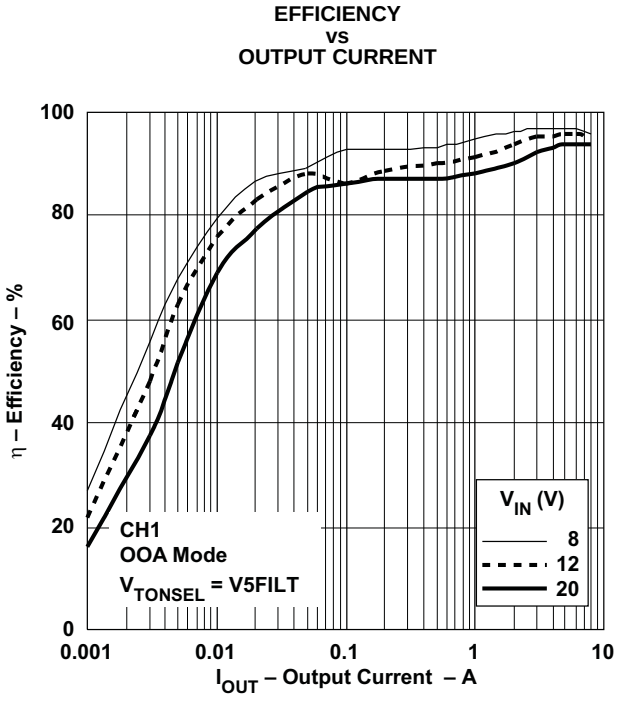


Figure 3. 5-V Efficiency in OOA Mode

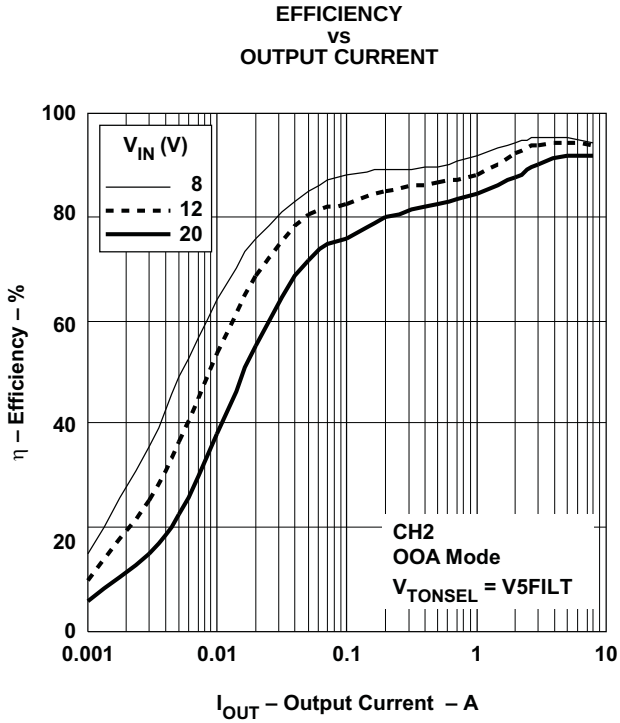


Figure 4. 3.3-V Efficiency in OOA Mode

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY
vs
OUTPUT CURRENT

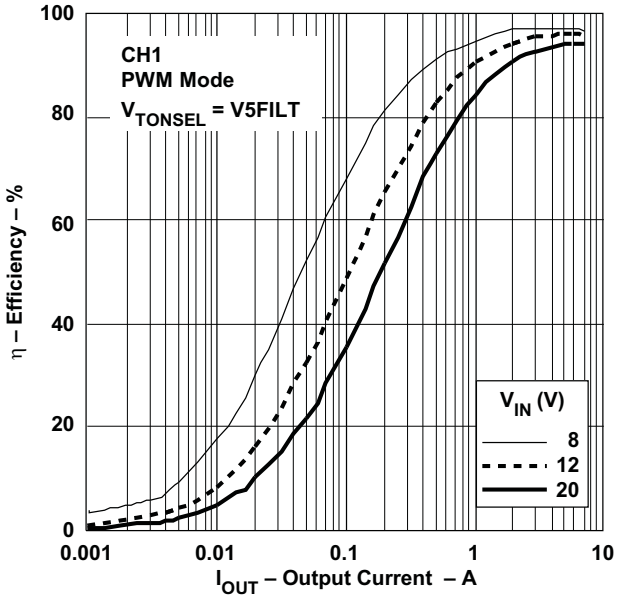


Figure 5. 5-V Efficiency in PWM Mode

EFFICIENCY
vs
OUTPUT CURRENT

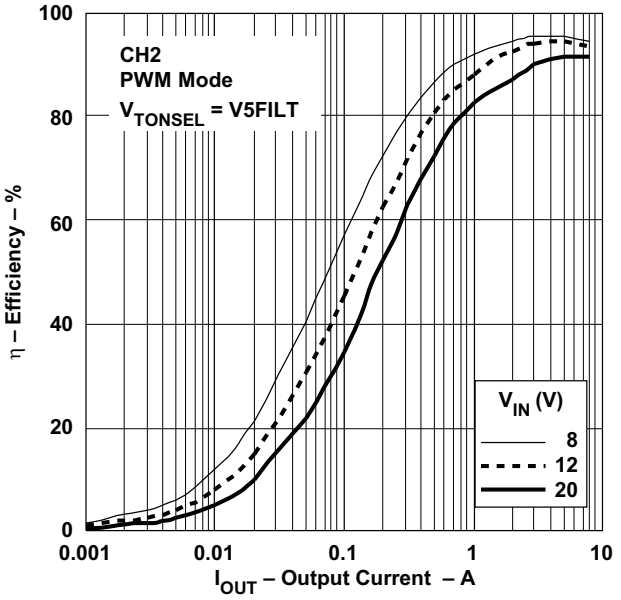


Figure 6. 3.3-V Efficiency in PWM Mode

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

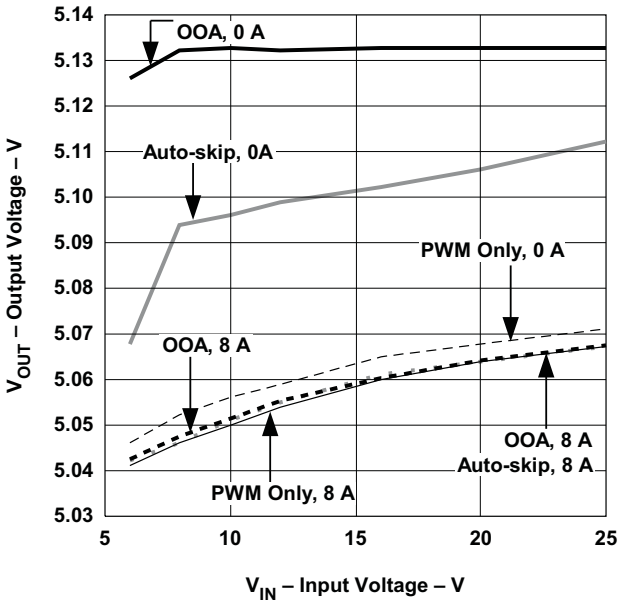


Figure 7. 5-V Line Regulation

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

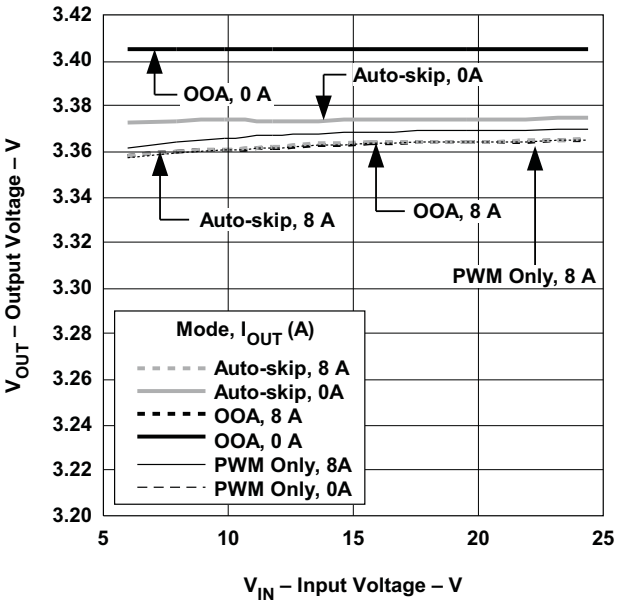


Figure 8. 3.3-V Line Regulation

TYPICAL CHARACTERISTICS (continued)

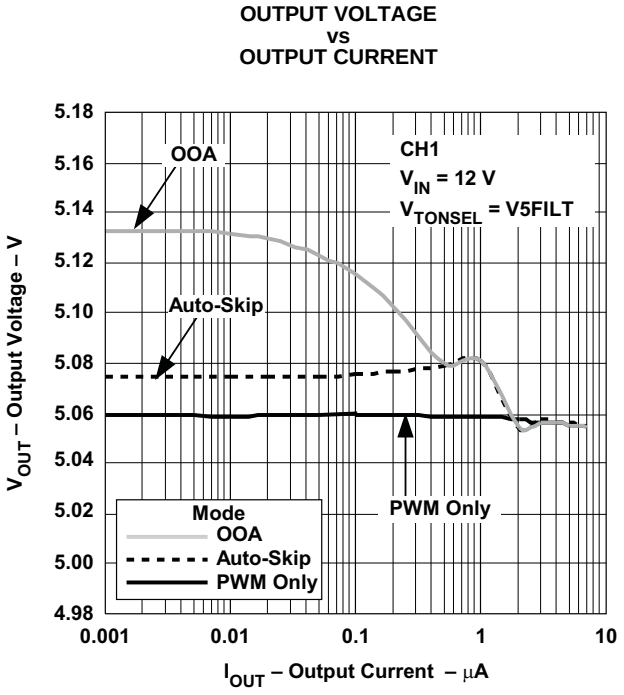


Figure 9. 5-V Load Regulation

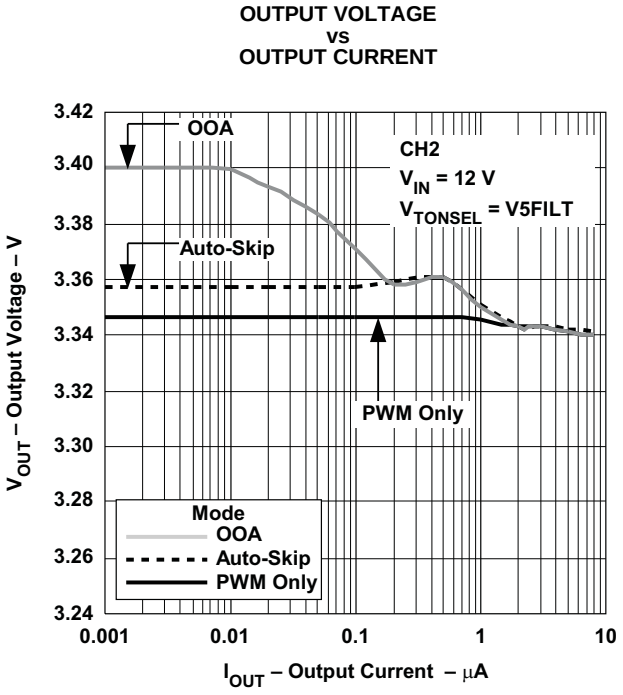


Figure 10. 3.3-V Load Regulation

LOW VOLTAGE DUAL RAILS

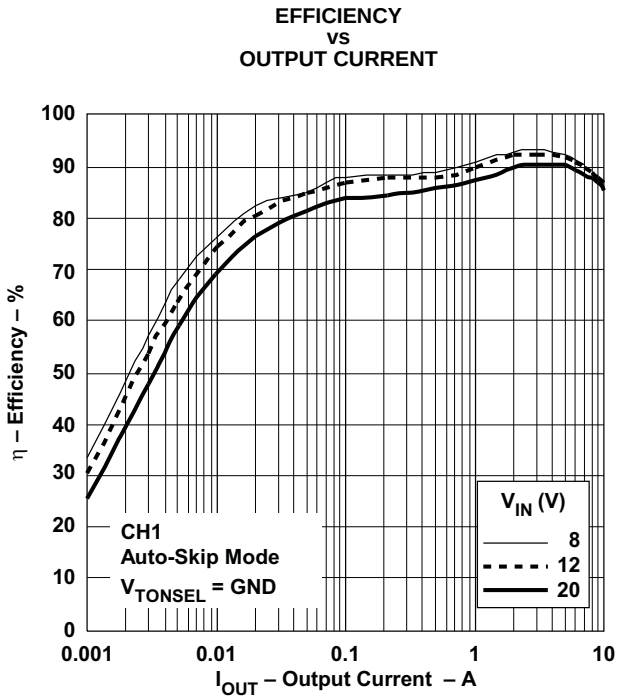


Figure 11. 1.5-V Efficiency in Auto-Skip mode

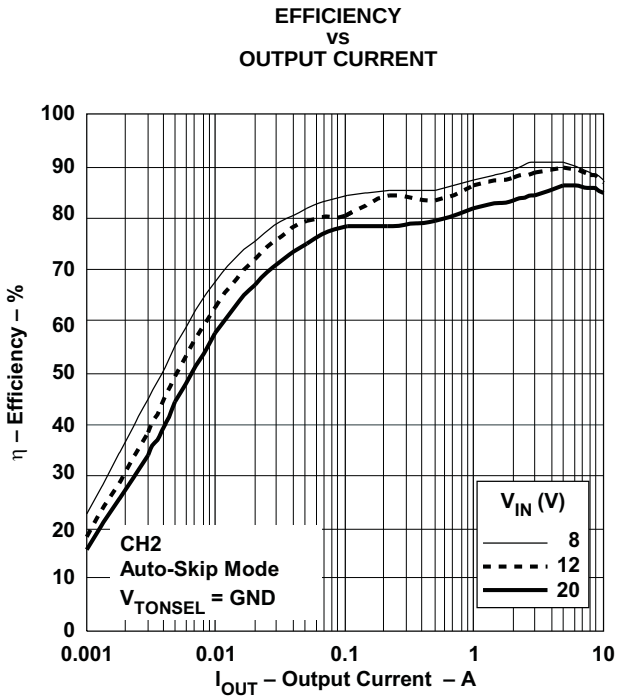


Figure 12. 1.05-V Efficiency in Auto-Skip Mode

TYPICAL CHARACTERISTICS (continued)

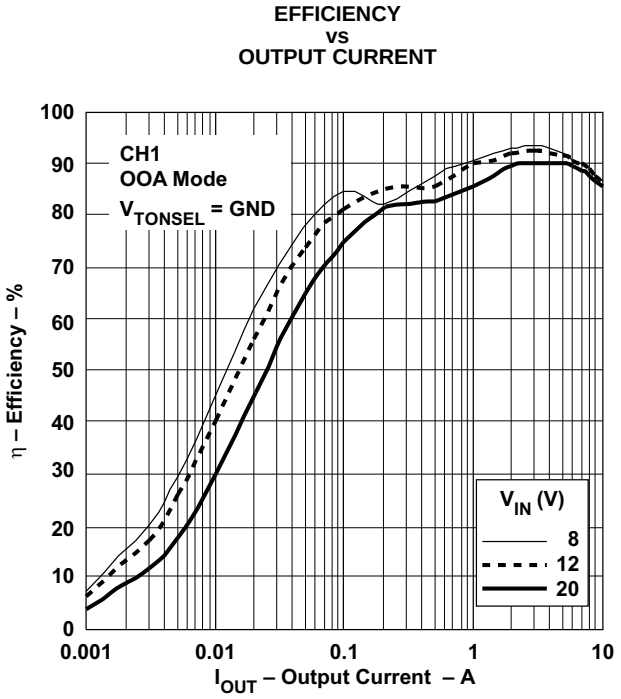


Figure 13. 1.5-V Efficiency in OOA mode

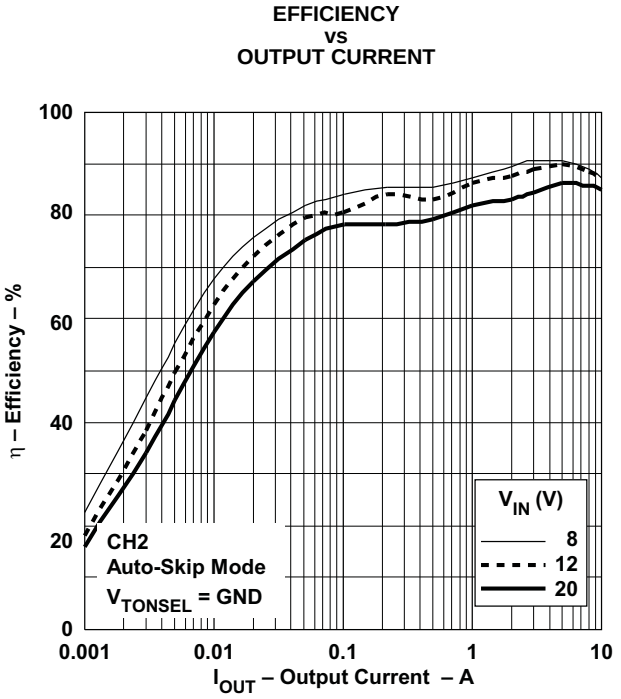


Figure 14. 1.05-V Efficiency in OOA mode

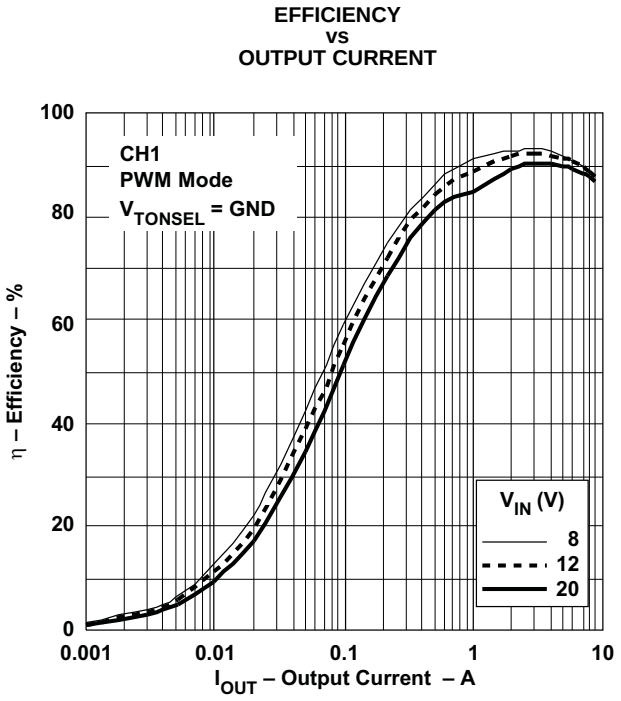


Figure 15. 1.5-V Efficiency in PWM mode

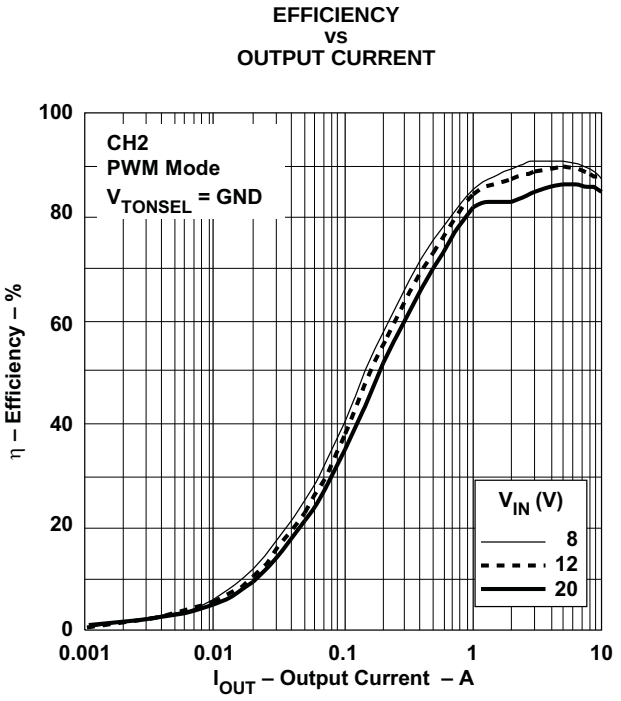


Figure 16. 1.05-V Efficiency in PWM mode

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

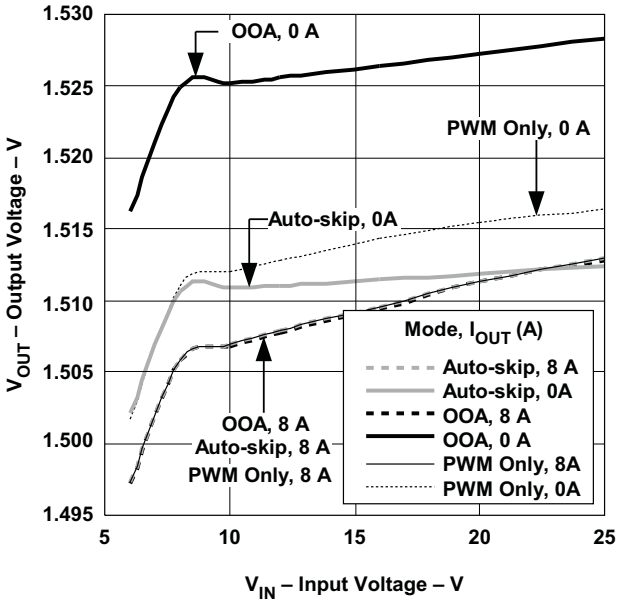


Figure 17. 1.5-V Line Regulation

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

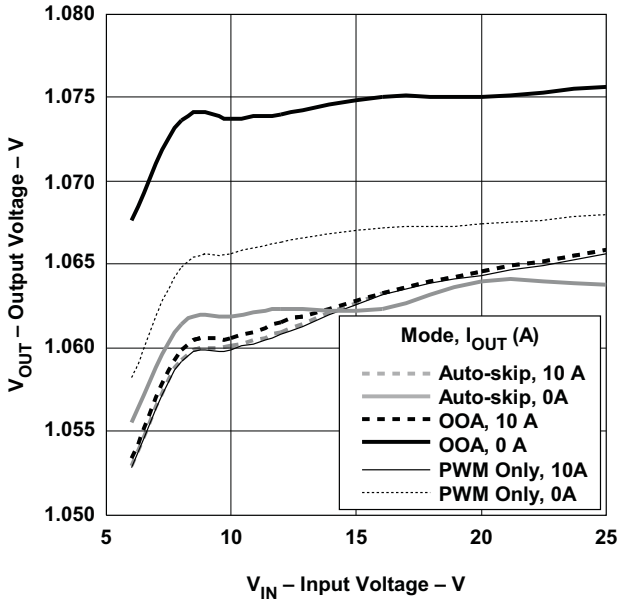


Figure 18. 1.05-V Line Regulation

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

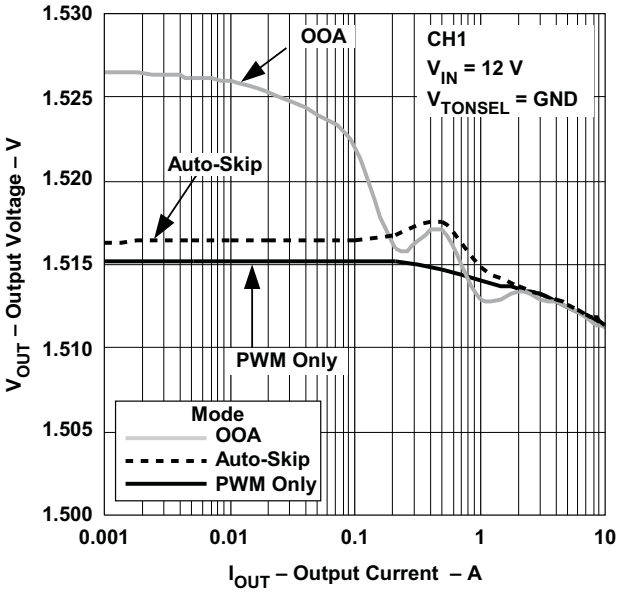


Figure 19. 1.5-V Load Regulation

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

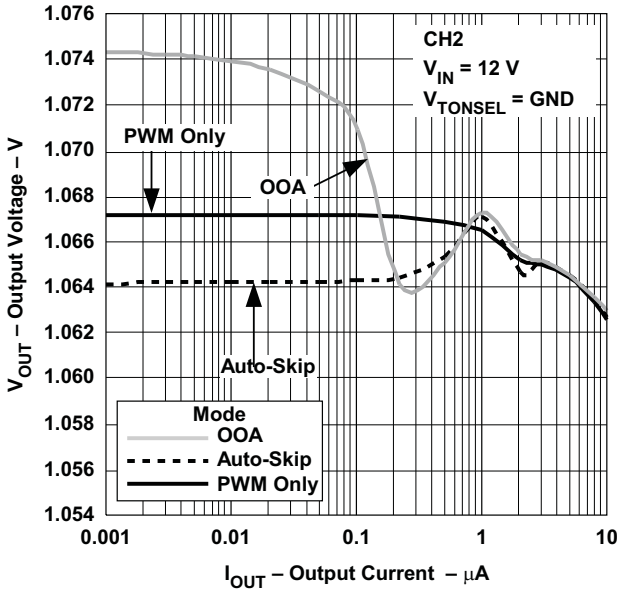


Figure 20. 1.05-V Load Regulation

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

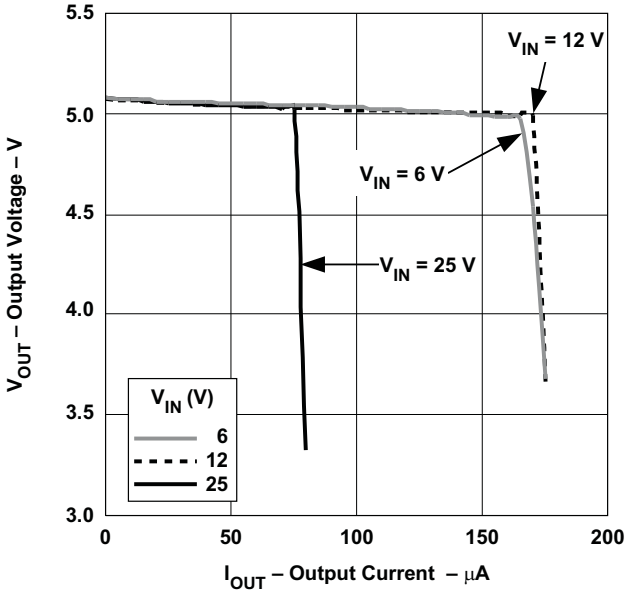


Figure 21. 5-V LDO Load Regulation

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

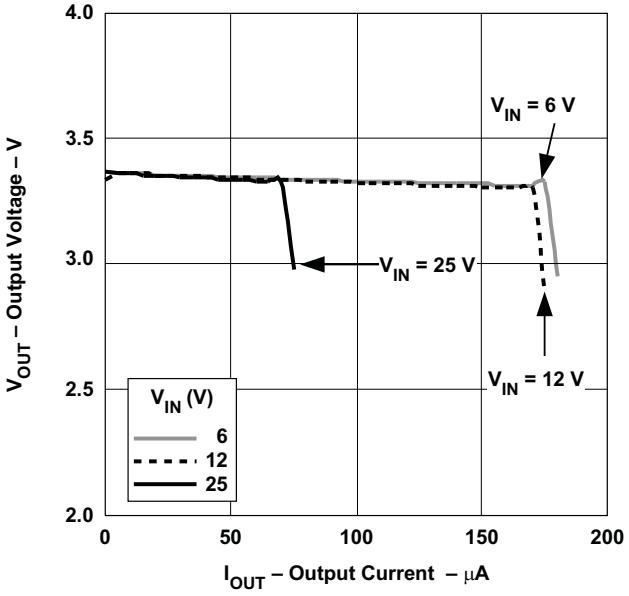


Figure 22. 3.3-V LDO Load Regulation

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

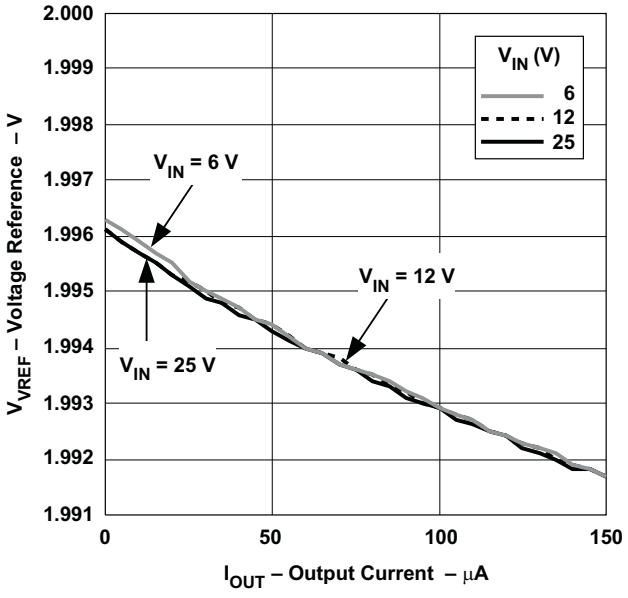


Figure 23. 2-V Reference Load Regulation

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

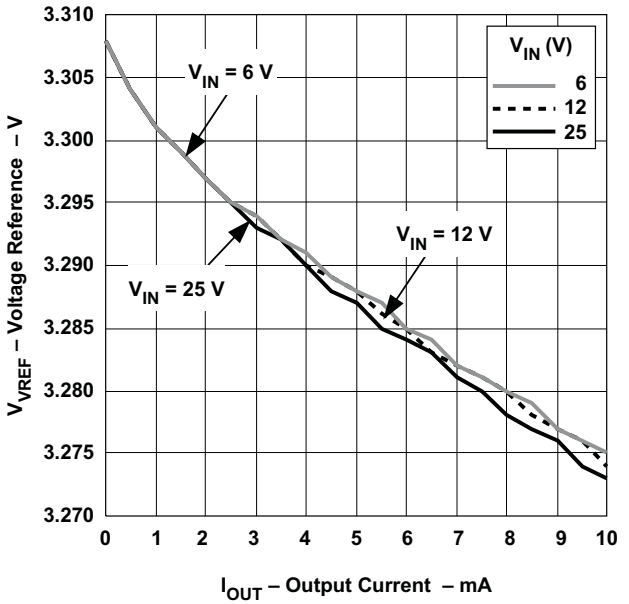


Figure 24. 3.3-V Reference Load Regulation

TYPICAL CHARACTERISTICS (continued)

FREQUENCY
vs
INPUT VOLTAGE

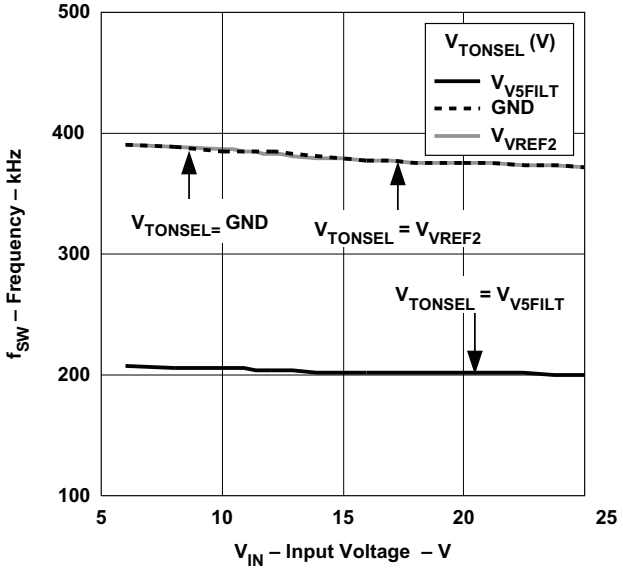


Figure 25. Channel 1 (5-V Setting)

FREQUENCY
vs
INPUT VOLTAGE

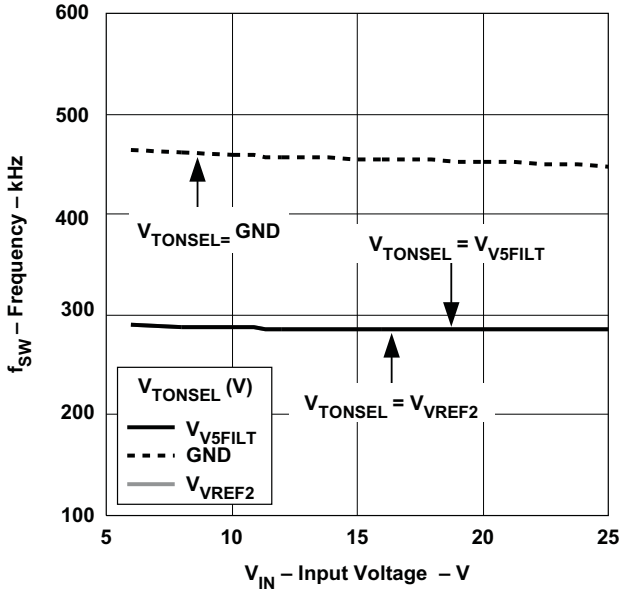


Figure 26. Channel 2 (3.3-V Setting)

FREQUENCY
vs
OUTPUT CURRENT

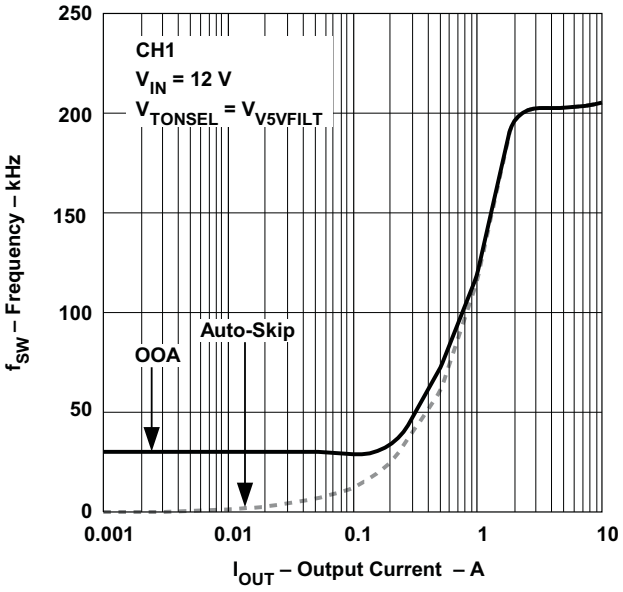


Figure 27. Load Current (5-V Setting)

FREQUENCY
vs
OUTPUT CURRENT

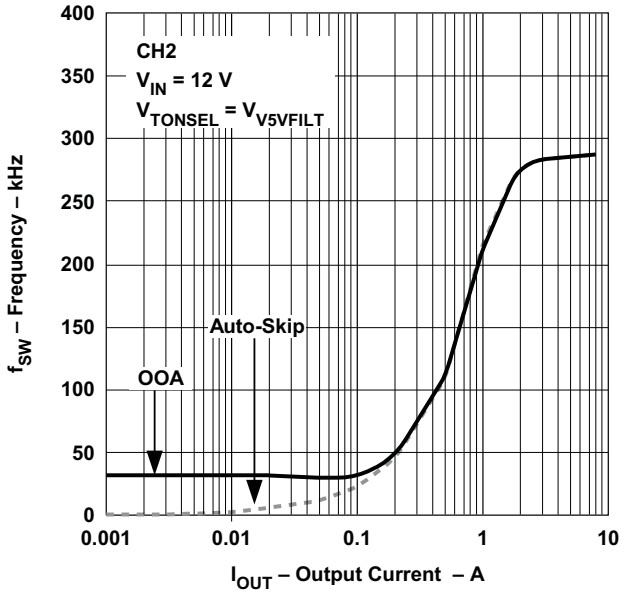


Figure 28. Load Current (3.3-V Setting)

TYPICAL CHARACTERISTICS (continued)

FREQUENCY
vs
INPUT VOLTAGE

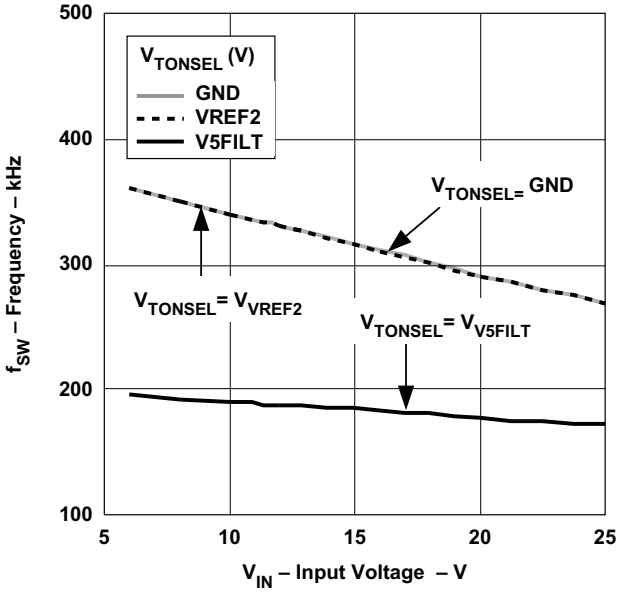


Figure 29. Channel 1 (1.5-V Setting)

FREQUENCY
vs
INPUT VOLTAGE

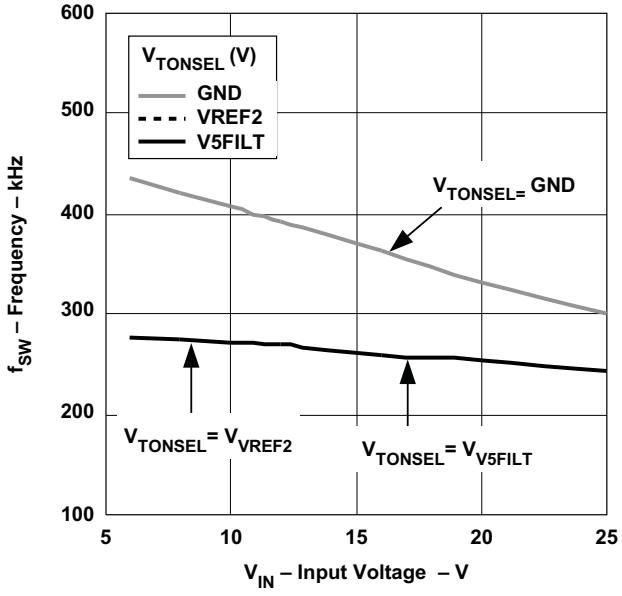


Figure 30. Channel 2 (1.05-V Setting)

FREQUENCY
vs
OUTPUT CURRENT

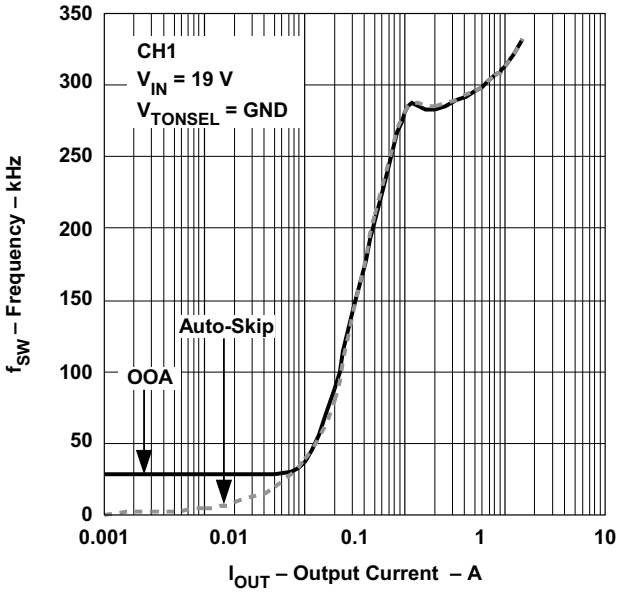


Figure 31. Load Current (5-V Setting)

FREQUENCY
vs
OUTPUT CURRENT

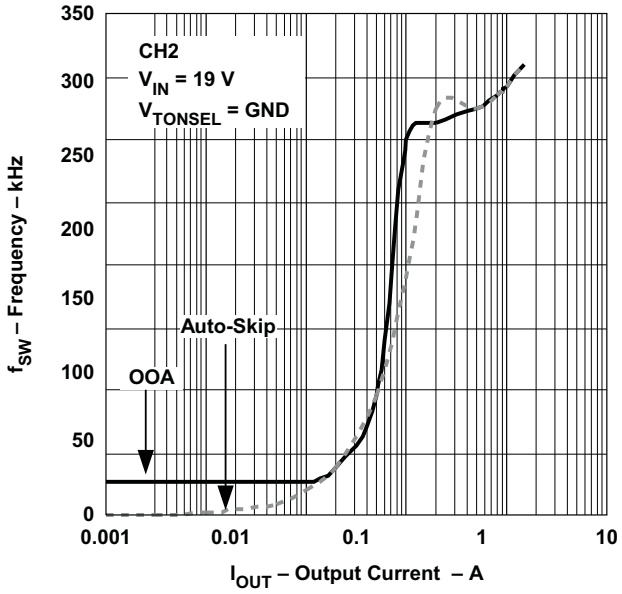


Figure 32. Load Current (3.3-V Setting)

TYPICAL CHARACTERISTICS (continued)

FREQUENCY
vs
OUTPUT VOLTAGE

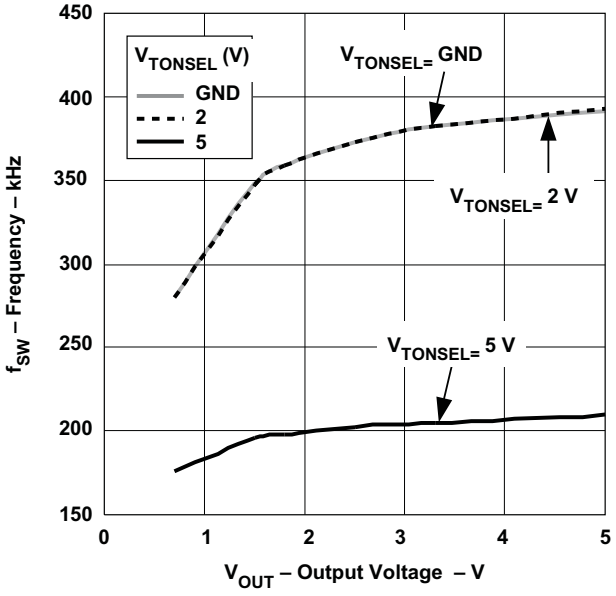


Figure 33. Channel 1 Setting

FREQUENCY
vs
OUTPUT VOLTAGE

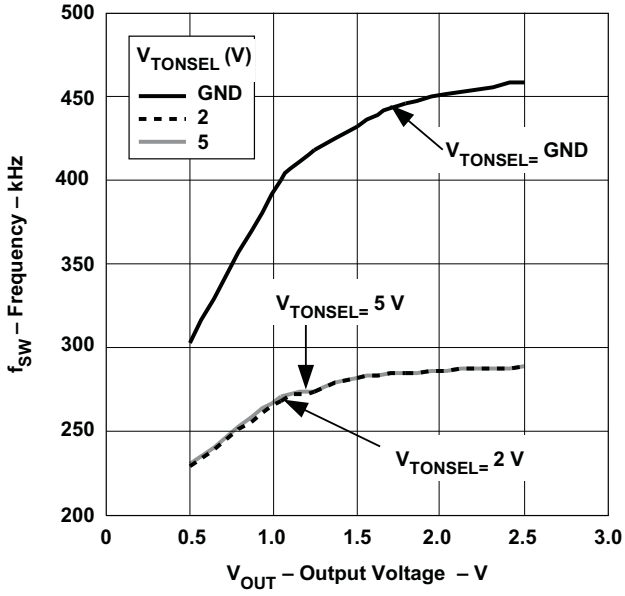


Figure 34. Channel 2 Setting

TYPICAL CHARACTERISTICS (continued)

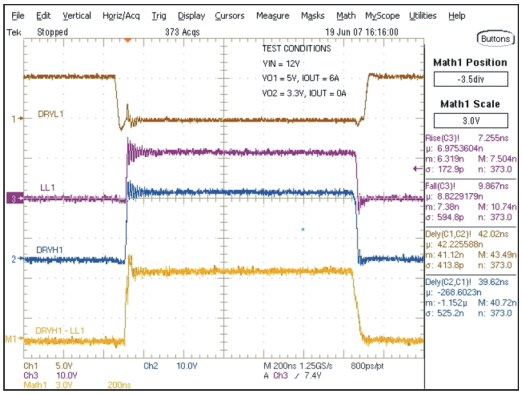


Figure 35. Channel 1 Gate Driver Performance

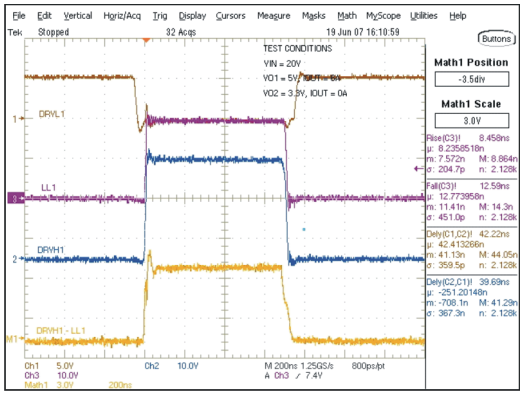


Figure 36. Channel 2 Gate Driver Performance

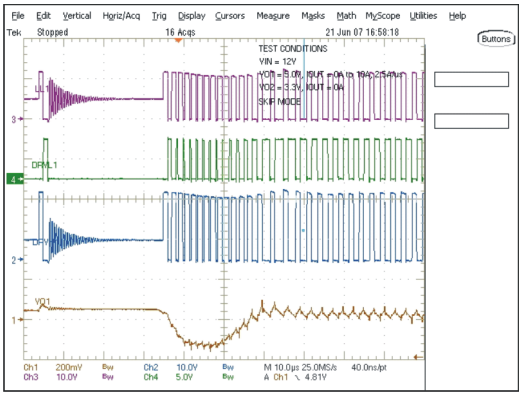


Figure 37. Channel 1 Load Step

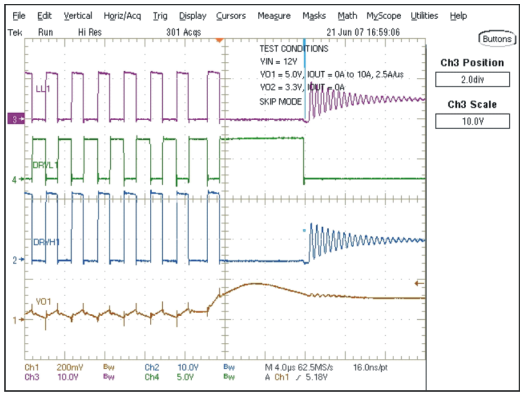


Figure 38. Channel 1 Load Release

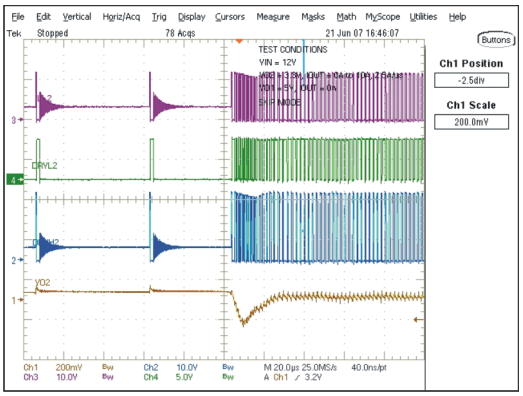


Figure 39. Channel 2 Load Step

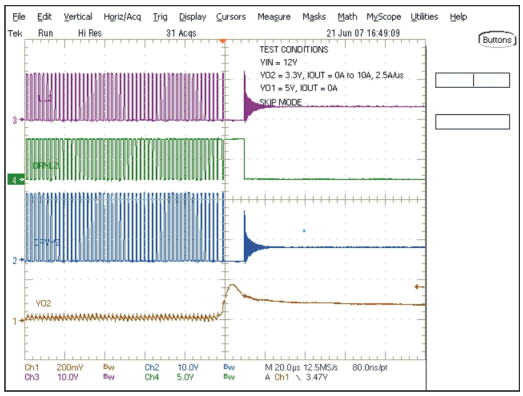


Figure 40. Channel 2 Load Release

APPLICATION INFORMATION

Table 4. List of Materials

COMPONENTS	CONFIGURATION NO. 1	CONFIGURATION NO. 2	CONFIGURATION NO. 3
	400 kHz/300 kHz Channel1: 5 V/8 A (fixed) Channel2: 3.3 V/10 A (fixed)	400 kHz/500 kHz Channel1: 1.5V/10A (fixed) Channel2: 1.05 V/15 A(fixed)	400kHz/500kHz Channel1: 1.8V/10A (adj) Channel2: 1.1V/15A (adj)
Input voltage	8 V ≤ V_{IN} ≤ 22 V		
Input MLCC capacitors	4 x 10 µF, 25 V Murata GRM31CR61E106KA12L	4 x 10 µF, 25 V Murata GRM31CR61E106KA12L	4 x 10 µ F, 25 V Murata GRM31CR61E106KA12L
Channel1			
Output capacitor	1 x 330 µF, 6 V, 25 mΩ, Sanyo, 6TPE330ML	2 x 330 µF, 2.5 V, 12 mΩ, Sanyo, 2R5TPE330MC	2 x 330 µF, 2.5 V, 12 mΩ, Sanyo, 2R5TPE330MC
Output inductor	Sumida, 4.3 µH, CEP125NP-4R3M-U, 11.4 mΩ	Sumida, 2.2 µH, CEP125NP-2R2M-U, 5.4 mΩ	Sumida, 2.2 µH, CEP125NP-2R2M-U, 5.4 mΩ
High-side MOSFET	International Rectifier, IRF7807V, 30 V, 8.3 A, 0.017 Ω	International Rectifier, IRF7807V, 30V, 8.3A, 0.017Ω	International Rectifier, IRF7807V, 30V, 8.3A, 0.017Ω
Low-side MOSFET	International Rectifier, IRF7811AV, 30 V, 10.8 A, 0.011 Ω	International Rectifier, IRF7832, 30V, 20A, 0.004Ω	International Rectifier, IRF7832, 30V, 20A, 0.004Ω
R_{OCL}	267 kΩ for OCL of 10 A to 14 A	110 kΩ for OCL of 12 A to 18 A	110 kΩ for OCL of 12 A to 18 A
R_{UPPER_DIV}	Tie VFB1 to GND	Tie VFB1 to V5FILT	39.2 kΩ, 1%
R_{LOWER_DIV}			24.9 kΩ, 1%
Channel2			
Output capacitor	1 x 330 µF, 4 V, 18 mΩ Sanyo, 4TPE330MI	2 x 470µF, 2.5 V, 9 mΩ, Sanyo, 2R5TPE470M9	2 x 470 µF, 2.5 V, 9 mΩ, Sanyo, 2R5TPE470M9
Output inductor	Sumida, 3.2 µH, 8.0 mΩ, CEP125NP-3R2M-U	Vishay, 1 µH, 3 mΩ, IHLP5050CE	Vishay, 1 µH, 3 mΩ, IHLP5050CE
High-side MOSFET	International Rectifier, IRF7807V, 30 V, 8.3 A, 0.017 Ω	International Rectifier, IRF7821, 30 V, 13 A, 0.009 Ω	International Rectifier, IRF7821, 30 V, 13 A, 0.009 Ω
Low-side MOSFET	International Rectifier, IRF7832, 30 V, 20 A, 0.004 Ω	International Rectifier, IRF7832, 30 V, 20 A, 0.004 Ω	International Rectifier, IRF7832, 30 V, 20 A, 0.004 Ω
R_{OCL}	110 kΩ for OCL of 12 A to 18 A	169 kΩ for OCL of 18 A to 26 A	169 kΩ for OCL of 18 A to 26 A
R_{UPPER_DIV}	Tie REFIN2 to V5FILT	Tie REFIN2 to VREF3	44.2 kΩ, 1%
R_{LOWER_DIV}			54.9 kΩ

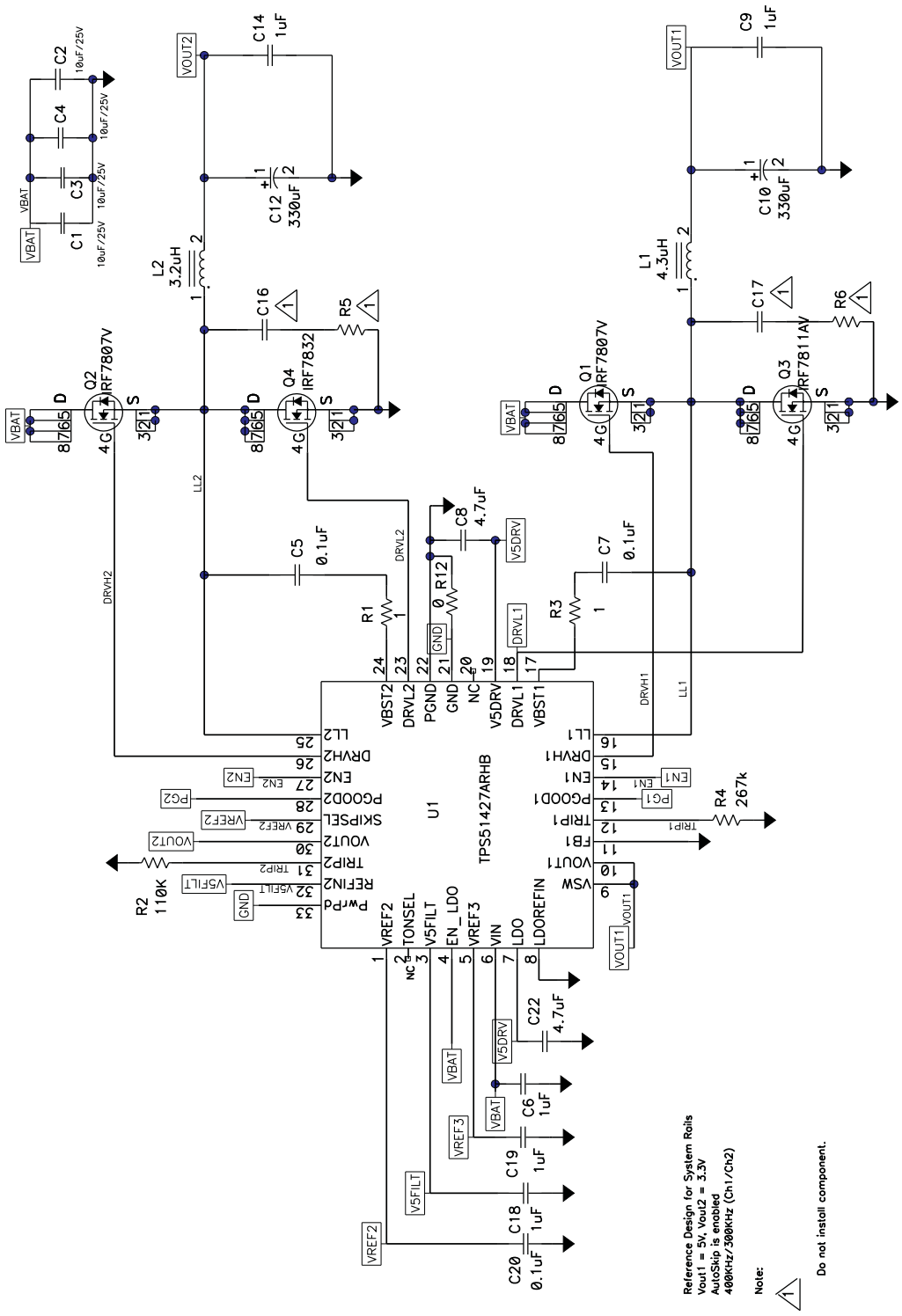


Figure 41. Configuration 1: System Rail

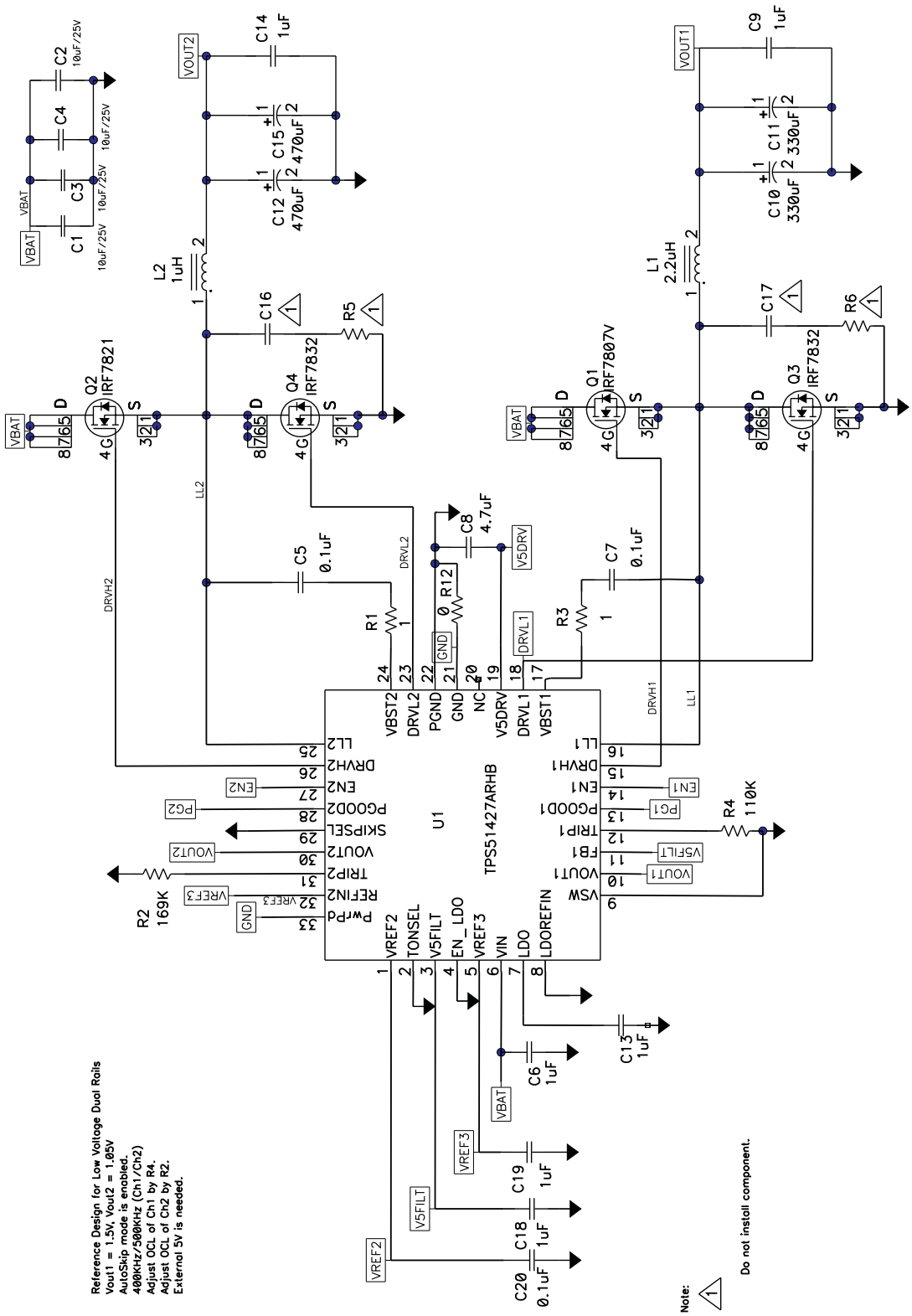


Figure 42. Configuration 2: Low Voltage Rail (Fixed Voltage Settings)

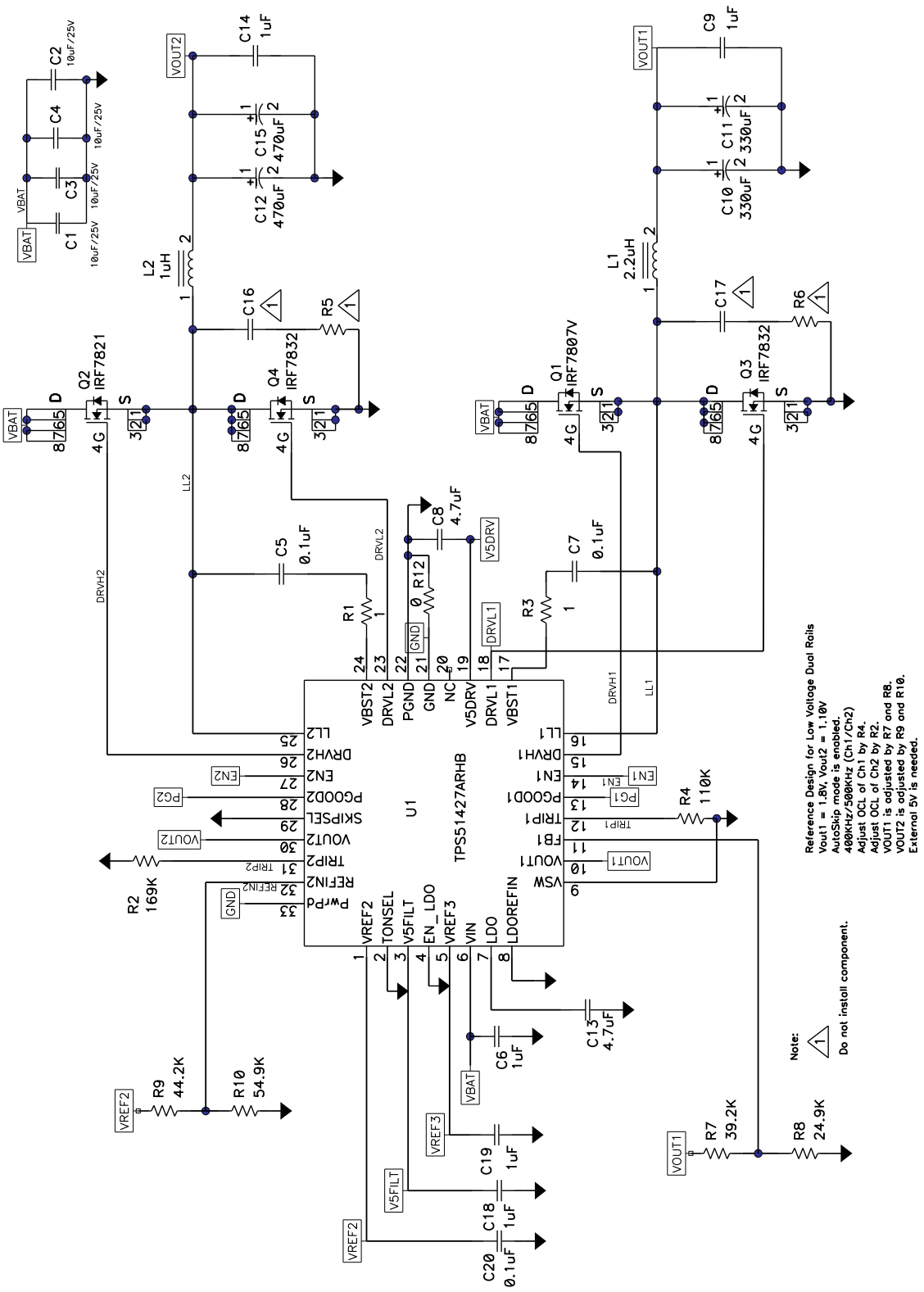


Figure 43. Configuration 3: Low-Voltage Dual Rail (Adjustable Voltage Settings)

Loop Compensation and External Part Selection

A simplified buck converter system using D-CAP mode is shown below in Figure 44.

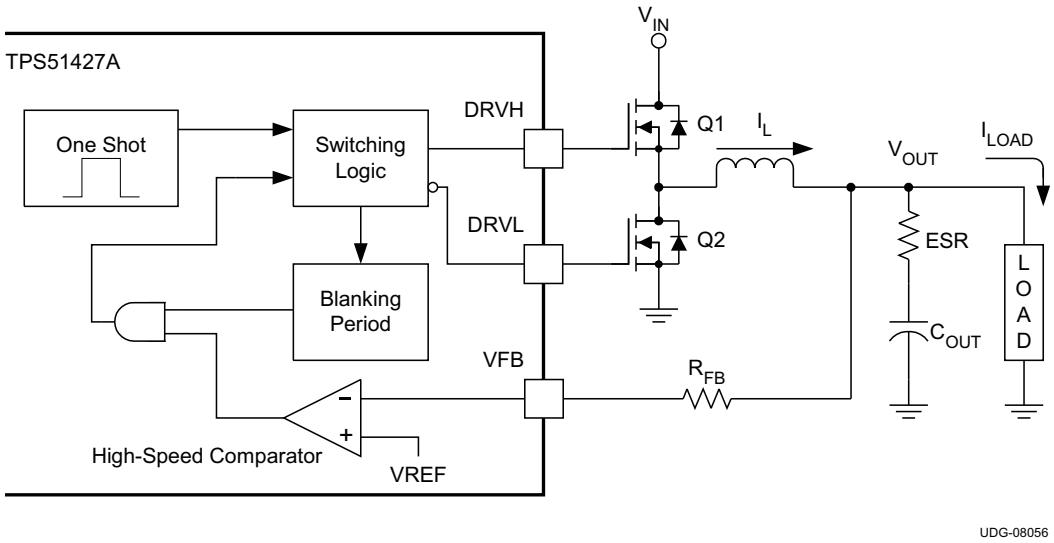


Figure 44. D-CAP Mode Operation Schematic

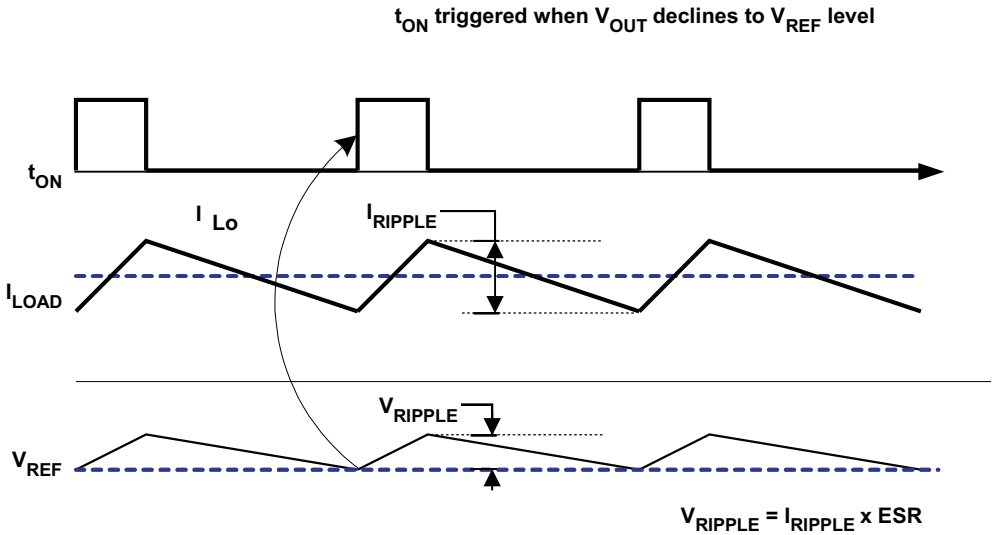


Figure 45. D-CAP Mode Operation Waveforms

The output voltage is compared with an internal reference voltage through scaling. The PWM comparator determines the timing to turn on the high side MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The DC output voltage changes when the input voltage changes due to the fact that voltage regulation is maintained at the valley point. Therefore, as the output ripple amplitude increases when the input voltage increases, the DC output voltage increases as well.

For loop stability, the 0-dB frequency, f_0, defined in Equation 4 must be lower than of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \le \frac{f_{SW}}{4} \quad (4)$$

As f_0 is determined solely by the output capacitor's characteristics, loop stability of D-CAP mode is determined by the capacitor's chemistry. For example, the output capacitance of specialty polymer capacitors (SP-CAP) is on the order of several hundred microfarads and an ESR of approximately 10 mΩ. These values yield a 0-dB frequency of 100 kHz or less and the loop is stable. However, ceramic capacitors yield a f_0 at more than 700 kHz which is not suitable for this operational mode.

Although D-CAP mode provides many advantages such as ease-of-use, minimum external components, and extremely fast transient response, a sufficient amount of feedback signal needs to be provided to reduce the jitter level. In a TPS51427A design, it is generally recommended to optimize the output voltage ripple at around 1.5% of the targeted DC voltage in both Auto-skip and PWM mode operations. For example, if V_{VOUT1} = 1.5 V, the desired output ripple should be at least 1.5 V x 1.5% = 22.5 mV. This can be achieved by taking advantage of the output bulk capacitor ESR.

The external component selection is much simpler in D-CAP mode. Below is a simplified design procedure targeting to the customers that are very familiar with SMPS design.

1. Determine the output voltage setting.

   For the fixed 5 V/3.3 V option, tie VFB1 pin to GND and REFIN2 to V5FILT. For the fixed 1.5 V/1.05 V configuration, tie VFB1 to V5FILT and REFIN2 to VREF3. TPS51427A also supports adjustable voltage options for both channels. The adjustable range for Channel1 is between 0.7 V and 5.9 V and for Channel2 is between 0.5 V and 2.5 V. Figure 46 shows how to configure the adjustable voltage option for Channel1 and Figure 47 shows the configuration for Channel2. Also, equations are provided in Table 5 to aid the design process.

2. Choose the output inductor.

   Output inductance is a function of V_{IN}, V_{OUT}, f_{SW} and the desired ripple current. For available switching frequency settings with TPS51427A, refer to Table 2. The process of choosing the right output inductance is an iterative one; many considerations need to be taken, such as the desired transient response, efficiency over the entire load range, load/line regulation, component availability and cost. Base the initial output inductance value upon where the ripple current is 25% to 50% of the maximum loading current. For transient optimized design, ripple factor can be higher; and for efficiency and load/line regulation optimized design, the ripple factor can be lower.

$$L = \frac{1}{I_{IND(ripple)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (5)$$

3. Choose the output capacitor(s).

   Organic semiconductor capacitors or specialty polymer capacitor(s) are recommended. Determine ESR to meet the required ripple voltage indicated previous.

$$ESR = V_{OUT} \times \frac{1.5\%}{I_{RIPPLE}} \quad (6)$$

Table 5. Design Assistance

	Channel1		Channel2	
FIXED VOLTAGE OPTIONS	5 V by shorting VFB1 to GND	1.5 V by shorting VFB1 to V5FILT	3.3 V by shorting REFIN2 to V5FILT	1.05 V by shorting REFIN2 to VREF3
ADJUSTABLE VOLTAGE OPTIONS	VOUT1 is set by R_{UPPER_DIV}, R_{LOWER_DIV}, and VFB1 Figure 46 $V_{VOUT1} = V_{VFB1} \times \left(\frac{R_{UPPER\_DIV} + R_{LOWER\_DIV}}{R_{LOWER\_DIV}} \right)$ (7) where • V_{VFB1} = 0.7 V		VOUT2 is set by R_{UPPER_DIV}, R_{LOWER_DIV}, and VFB1 Figure 47 $V_{REFIN2} = \left(\frac{(R_{LOWER\_DIV} \times V_{VREF2})}{(R_{UPPER\_DIV} + R_{LOWER\_DIV})} \right)$ (8) where • V_{VREF} = 2 V • $V_{VOUT2} = V_{REFIN2}$	

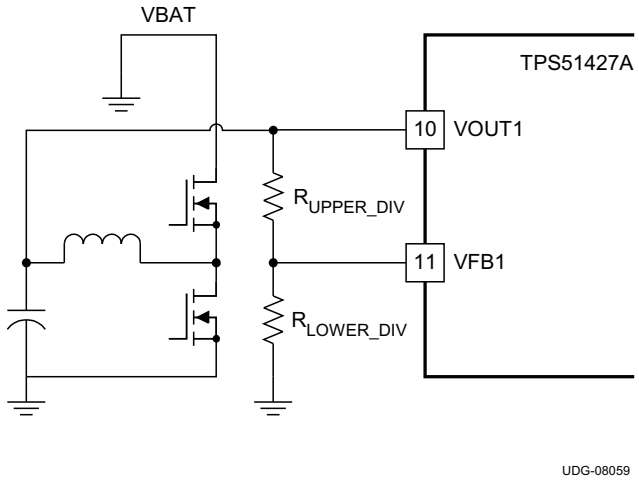


Figure 46. Channel1 Adjustable Voltage Configuration

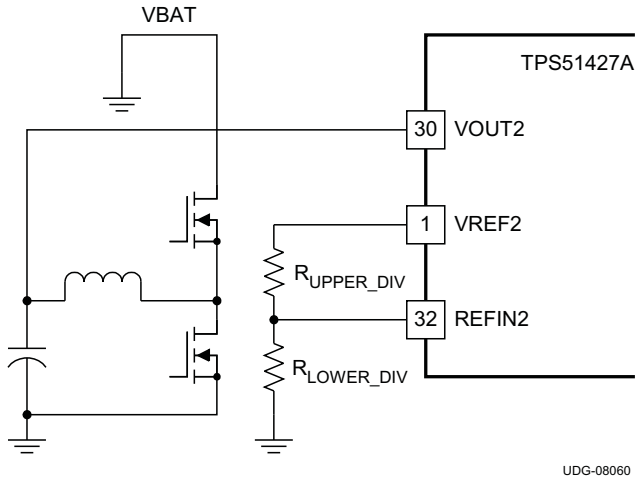


Figure 47. Channel2 Adjustable Voltage Configuration

Ripple Requirement in PWM Mode, Skip Mode and OOA Mode

Since TPS51427A is a constant on time based controller, minimum ripple requirement at the output is necessary to keep the main voltage loop stable. For loop stability, the ESR zero frequency, f_0 must be lower than 1/4 of the switching frequency. This requirement can be easily fulfilled by using either POSCAP or SPCAP, due to their similar characteristics. In order for a constant on time topology to work properly in a real world environment, there should not be any substantial phase delay contributed by the parasitic model of the output capacitors. Such delay would create distortion to the essential feedback signal necessary for the device to process.

In a TPS51427A design, it is generally recommended to optimize the output voltage ripple at around 1.5% of the targeted DC voltage in both auto-skip and PWM mode operations. Higher ripple is better in terms of jitter performance, however, lower ripple improves the line regulation and efficiency performance. It is a common practice as an attainable goal to optimize the converter design in terms of regulation and efficiency.

There is an additional voltage loop in the TPS51427A design that needs to be considered. OOA (out-of-audio) mode is designed to keep the minimum switching frequency at least 22 kHz in the light load/no load operation in order to minimize the audible noise in the notebook system design during standby mode. Both main voltage loop and OOA loop require certain output ripple in order for the device to function properly. If the ripple is too low, the main loop is unstable. If OOA mode operation is desired, the recommended ripple cannot be more than 1% of the target DC voltage.

Current Limit Design Considerations

The current limit of Channel1 can be set using the TRIP1 pin via an external small resistor to GND. Channel2 current limit can be set via the TRIP2 pin. The sourcing current for both Channel1 and Channel2 is 5 µA at room temperature with 2900 ppm/°C built-in temperature coefficient (to compensate for the temperature dependency of the $R_{DS(on)}$ of the low-side MOSFET). To take advantage of this feature, a good thermal coupling between the TPS51427A and the low-side MOSFET has to be obtained.

The current limit adjustment range (VTRIPx) is between 0.2 V and 2 V. If 5 V is applied to the pin (TRIP1 and/or TRIP2) directly (V_{TRIPx} > 3.1 V), TPS51427A assumes a default of a 100-mV current limit without temperature compensation.

Once the minimum OCL level is determined, translate the minimum OCL point (DC) into minimum valley current by subtracting of the peak-to-peak inductor current. Then convert the current information into the voltage level for the TPS51427A to process.

$$V_{OCLx} = R_{DS(on)max} \times I_{(MIN)OCLvalley} \quad (9)$$

where

- the low-side MOSFET at T_J = 25°C

The external resistor can be set using Equation 10.

$$R_{OCLx} = 10 \times \left(\frac{V_{OCLx} + 5mV}{I_{TRIP}} \right) \quad (10)$$

where

- I_{TRIP} = 5 µA and the tolerance is ±5%

Once R_{OCLx} is obtained, calculate the maximum V_{TRIPx} voltage to make sure the maximum voltage on the TRIP1 pin and/or the TRIP2 pin is less than 3.1 V for the entire operating temperature range.

The TRIPx voltage (V_{TRIPx}) can be calculated by Equation 11.

$$V_{TRIPx} = I_{TRIP} \times R_{OCLx} \quad (11)$$

And maximum VTRIPx voltage can be calculated by Equation 12.

$$V_{TRIPx(max)} = I_{TRIP} \times R_{OCLx} \times (1 + TOL) \times \left(1 + 2900ppm/°C \times (T_J - 25°C)\right) \quad (12)$$

where

- I_{TRIP} = 5 µA
- TOL = 5%
- T_J is assumed to be 125°C for the worst case junction temperature

Shutdown and Standby Control Logic

Shutdown and Standby Control Logic Table

ENLDO	LDO	VREF2	VREF3	EN1	EN2	Channel1	Channel1
Low	Off	Low	On (if V_{IN} > 2.2 V) Off (if V_{IN} < 2 V)	Low	Low	Off	Off
High	On	On		Low	Low	Off	Off
High	On	On		High	High	On	On
High	On	On		High	Low	On	Off
High	On	On		Low	High	Off	On
High	On	On		High		On	On (after Channel1 is up)
High	On	On			High	On (after Channel2 is up)	On

Layout Guidelines

1. Place one or two 10-µF ceramic capacitor(s) for V_{IN} between two channels. Add 1000-pF ceramic capacitor between drain of the high-side MOSFET and source of the low-side MOSFET of each channel.
2. Place V_{IN} capacitors, VOUT1/VOUT2 capacitors and MOSFETs on the same side of the board. Positive terminal of V_{IN} capacitor and drain of the high-side MOSFET should be as close as possible (within 10 mm if possible). Also place negative terminals of both V_{IN} capacitor and V_{OUT} capacitor, and source of the low-side MOSFET as close as possible.
3. GND terminal of the device (signal GND) and PGND terminal (power GND) should be connected with the lowest impedance near the device.
4. Trace of the switching node which is connected between the source of the high-side MOSFET, drain of the low-side MOSFET and the upstream of the output inductor should be as short and thick as possible. Use 40 mil of width (LL1 and LL2) for every ampere of load current.
5. LL1 and LL2 serve the phase node connections for the high-side drivers. Also, they are served as input to the current comparators for $R_{DS(on)}$ sensing and input voltage monitor for the on time control circuitry. Route the return of these two traces to device pins as wide and short as possible to eliminate the parasitic inductance effect to the accuracy of the measurement.
6. Place a low-pass filter MLCC capacitor with a value of 1-µF from V5FILT to GND, as close as possible.
7. The output of LDO if configured as 5VLDO, requires at least 4.7-µF of MLCC to GND. If it is configured as 3.3 VLDO, 10 µF of MLCC is recommended. For optimized stability and transient response, use a value of 27 µF if the output of LDO is configured as 1VLDO. VREF2 requires 0.1-µF ceramic bypass capacitor to GND which should be placed as close to the device as possible. For VREF3, it generally requires a 1-µF ceramic by pass capacitor to GND which also should be placed as close to the device as possible.
8. Connect the overcurrent setting resistors from TRIP1/TRIP2 to GND. The traces from TRIP1/TRIP2 should be routed as far as possible from the switching nodes.
9. 9. In the case of adjustable output voltage with external resistor dividers, the discharge path (VOx) can share the trace to the output capacitor with the feedback trace (VFB1/REFIN2). Please place the voltage setting resistors as close to the device as possible. Route the VOx and feedback traces as far from the high speed switching nodes as possible to avoid noise coupling.
10. Connections from the drivers to the respective gate of the high-side or the low-side MOSFETs should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace.
11. All sensitive analog traces and components such as VO1/VO2, VFB1/REFIN2, VREF2, VREF3, EN1/EN2, GND, VSW, PGOOD1/PGOOD2, TRIP1/TRIP2, ENLDO, LDOREFIN, V5FILT, TONSEL and SKIPSEL should be placed away from high-voltage switching nodes such as LLx, DRVLx or DRVHx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback traces from power traces and components.
12. In order to effectively remove heat from the package, prepare thermal land and solder to the package's thermal pad. 3 × 3 or more vias with a 0.33-mm (13mils) diameter connected from the thermal land to the internal ground plane should be used to help dissipation. Connect GND to the thermal land directly.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51427ARHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51427A	Samples
TPS51427ARHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51427A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

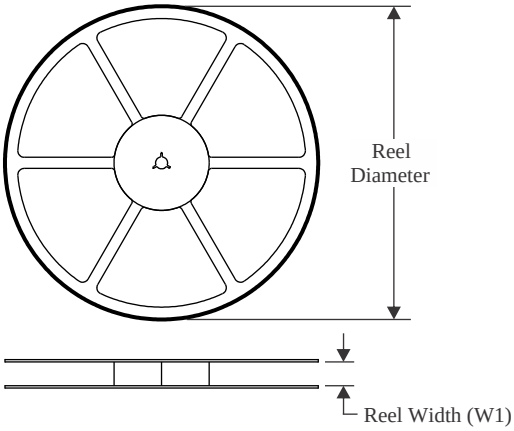
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

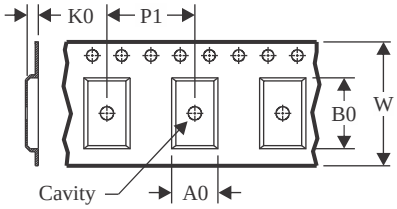
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

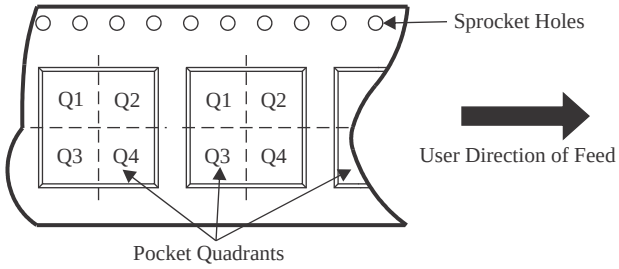


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

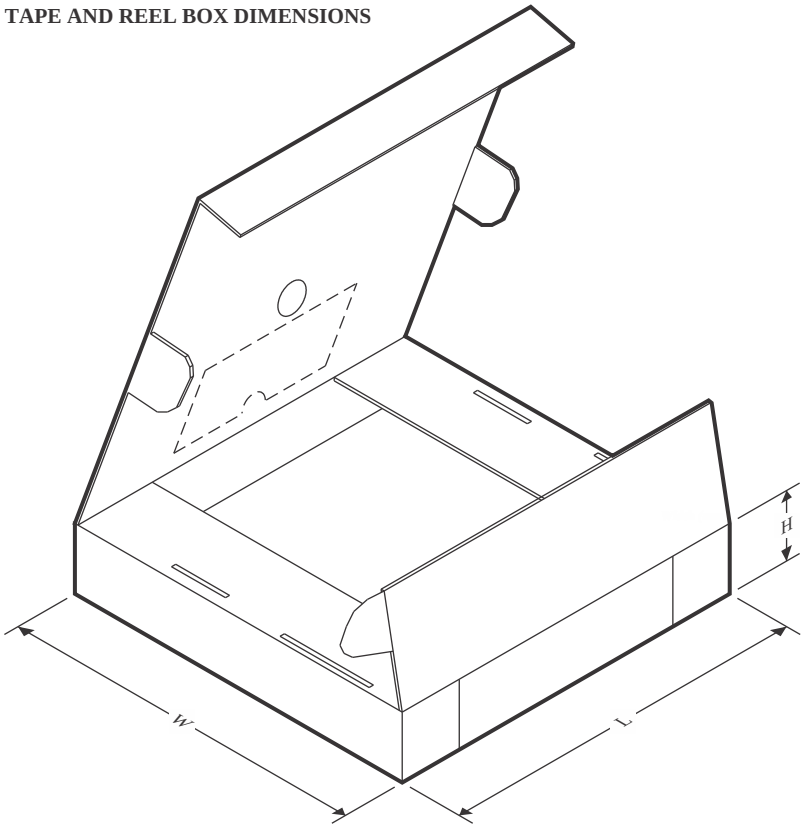
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51427ARHBR	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS51427ARHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS51427ARHBT	VQFN	RHB	32	250	180.0	12.5	5.25	5.25	1.1	8.0	12.0	Q2
TPS51427ARHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51427ARHBR	VQFN	RHB	32	3000	338.0	355.0	50.0
TPS51427ARHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
TPS51427ARHBT	VQFN	RHB	32	250	205.0	200.0	33.0
TPS51427ARHBT	VQFN	RHB	32	250	210.0	185.0	35.0

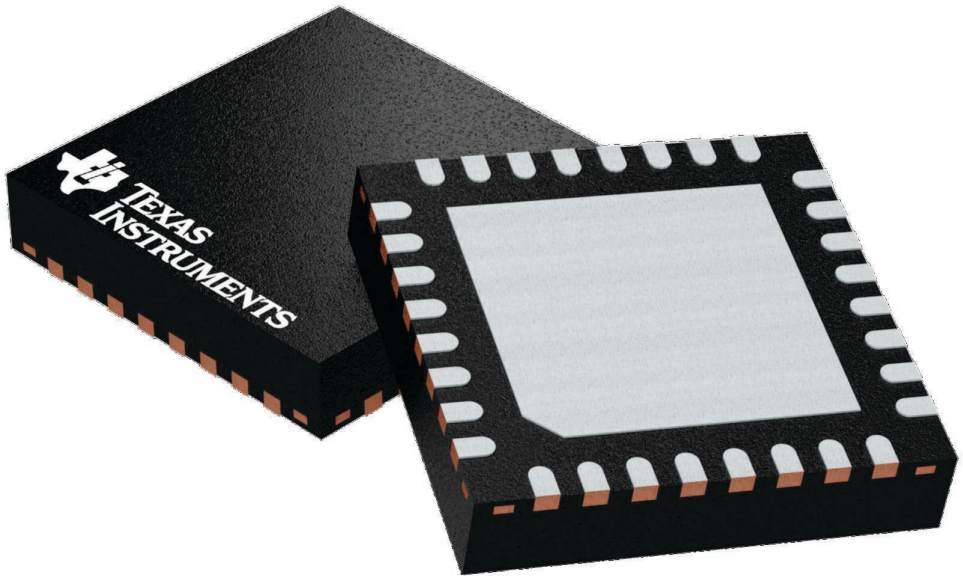
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

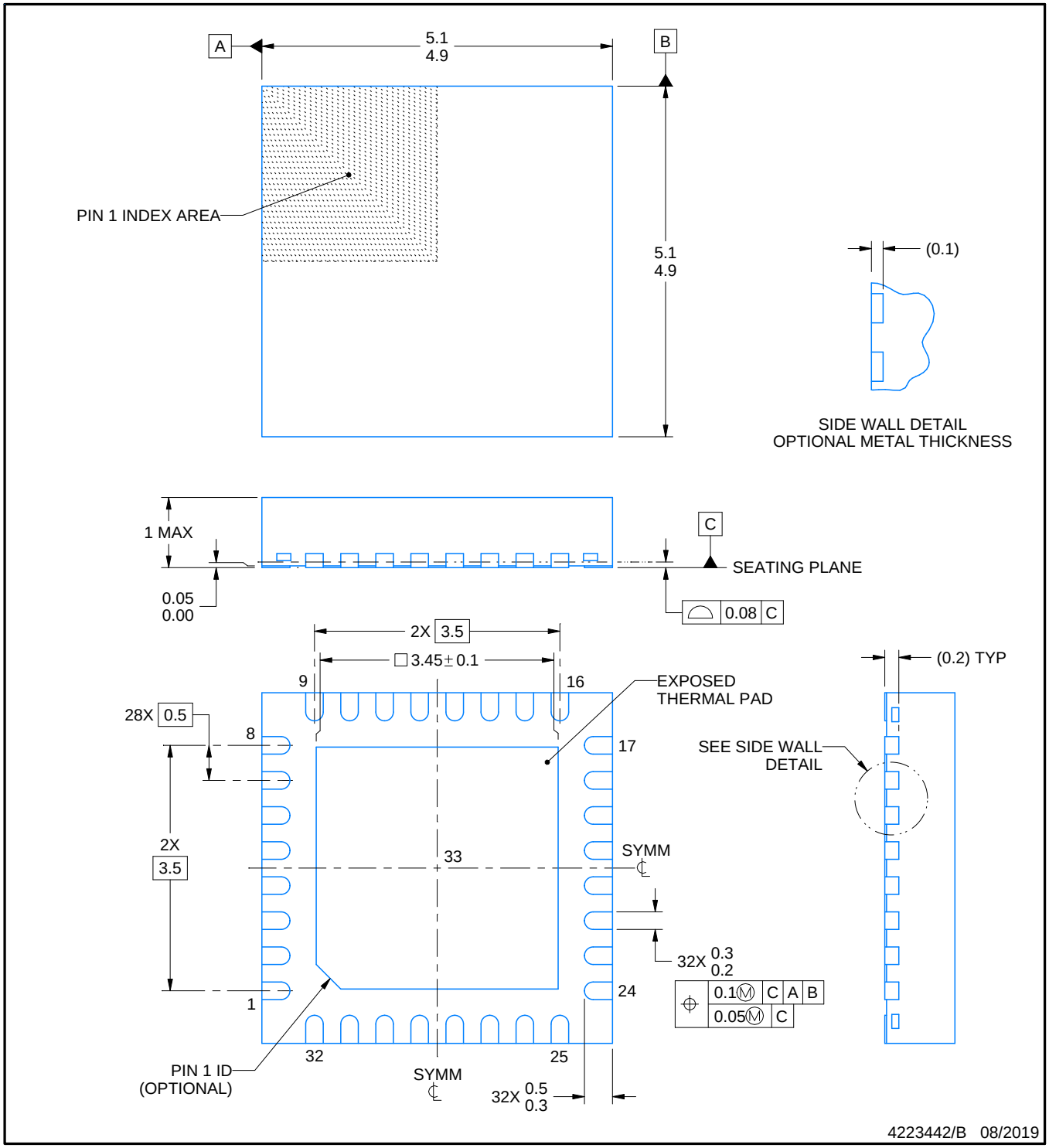
4224745/A

RHB0032E

PACKAGE OUTLINE

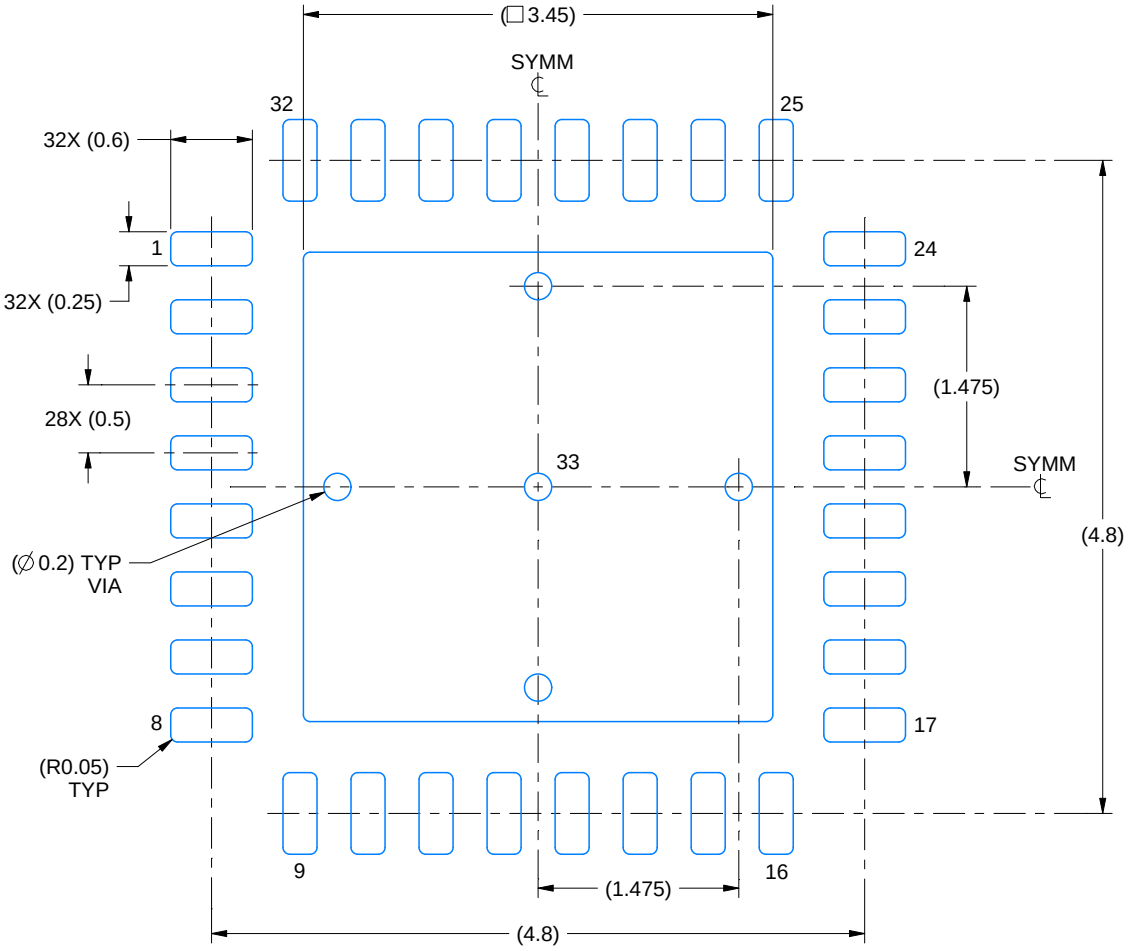
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

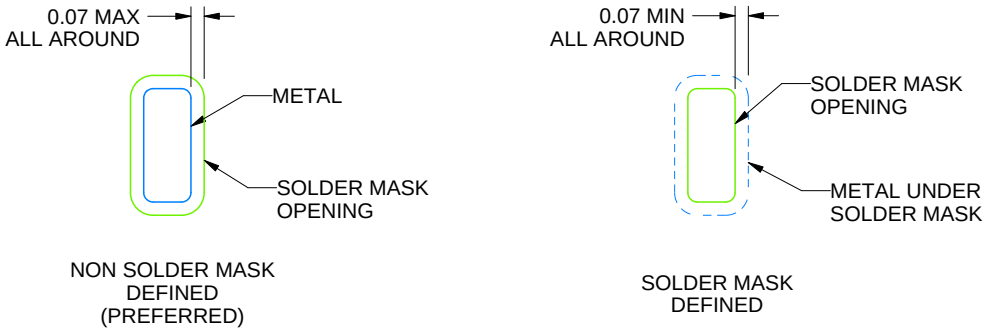


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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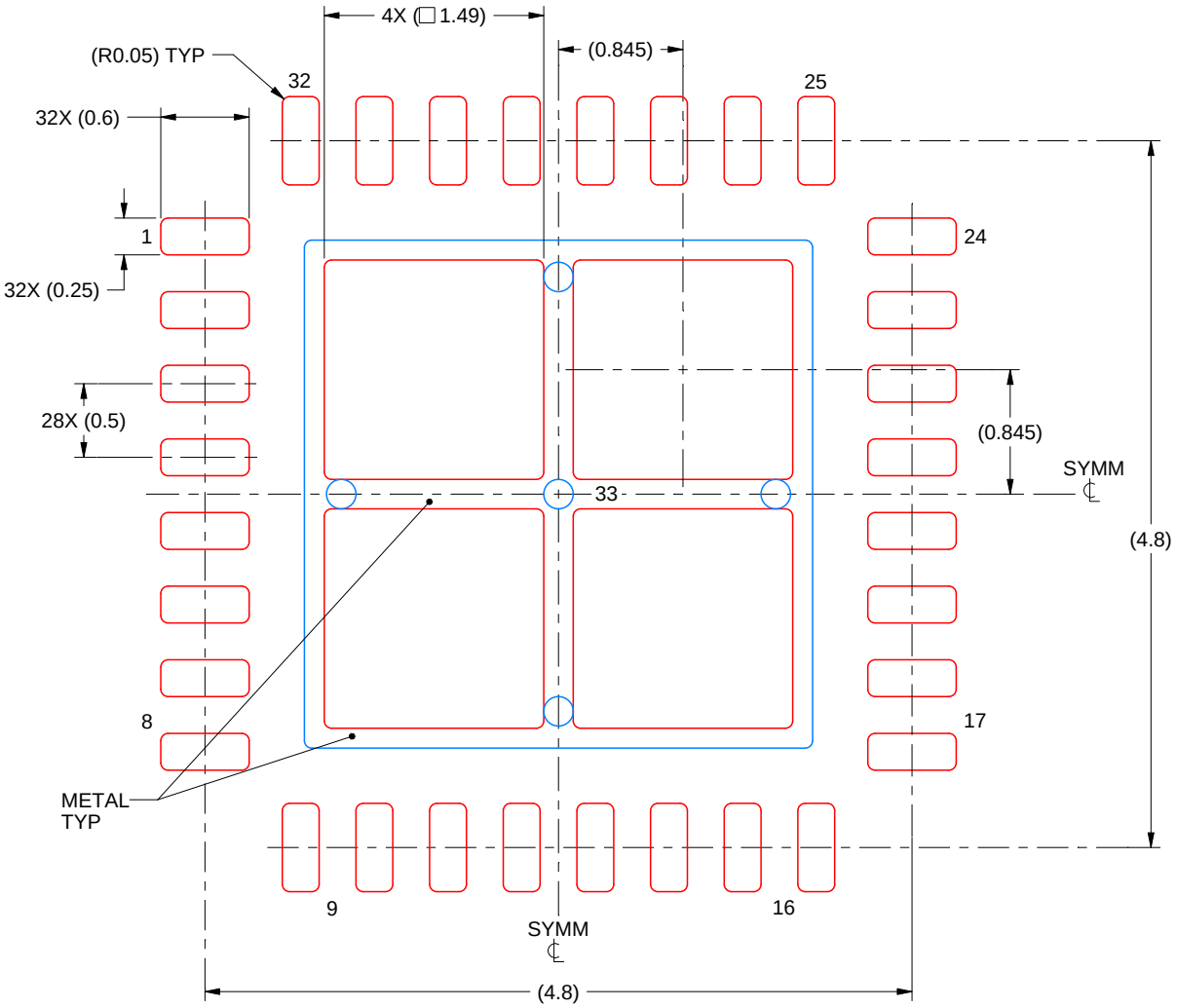
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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