ULTRA LOW-POWER, 10 mA, LDO LINEAR REGULATORS WITH POWER GOOD OUTPUT

FEATURES

- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree**[1]
- **10 mA Low-Dropout Regulator**
- **Ultralow 1.2 μA Quiescent Current at 10 mA**
- **5-Pin SC70/SOT-323 (DCK) Package**
- **Integrated Power Good Output**
- **Stable With Any Capacitor (> 0.47 μF)**
- **Dropout Voltage Typically 105 mV at 10 mA (TPS79733)**
- **Overcurrent Limitation**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **Battery-Powered Microcontrollers and Microprocessors**

DESCRIPTION/ORDERING INFORMATION

The TPS797xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage and ultralow-power operation. The device is stable with any capacitor (> 0.47 μF). Therefore, implementations of this device require little board space due to the miniaturized packaging and potentially small output capacitor. In addition, the family includes an integrated open drain active-high power good (PG) output. Intended for use in microcontroller based, battery-powered applications, the TPS797xx family's low dropout and ultralow-powered operation results in a significant increase in system battery operating life. The small packaging minimizes consumption of board space.

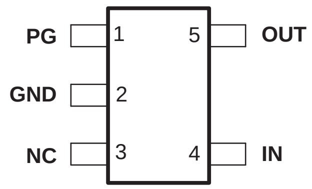
The device is enabled when the applied voltage exceeds the minimum input voltage. The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is low, 125 mV (typ) at 10 mA of load current and is directly proportional to the load current. The quiescent current is ultralow (1.2 μA typ) and is stable over the entire range of output load current (0 mA to 10 mA). When properly configured with a pullup resistor, the PG output can be used to implement a power-on reset or low battery indicator. The TPS797xx is offered in 1.8 V, 3 V, and 3.3 V fixed options.

ORDERING INFORMATION[1]

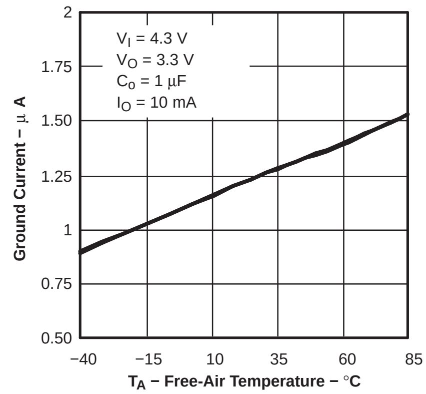
T_A	VOLTAGE	PACKAGE[2]	PART NUMBER	SYMBOL
–55°C to 125°C	1.8 V	SC70/SOT-323 (DCK)	TPS79718MDCKREP	CKW
	3 V		TPS79730MDCKREP	BUA
	3.3 V		TPS79733MDCKREP[3]	TBD

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Product Preview. Parameters in electrical characteristics are subject to change.

DCK PACKAGE
(TOP VIEW)

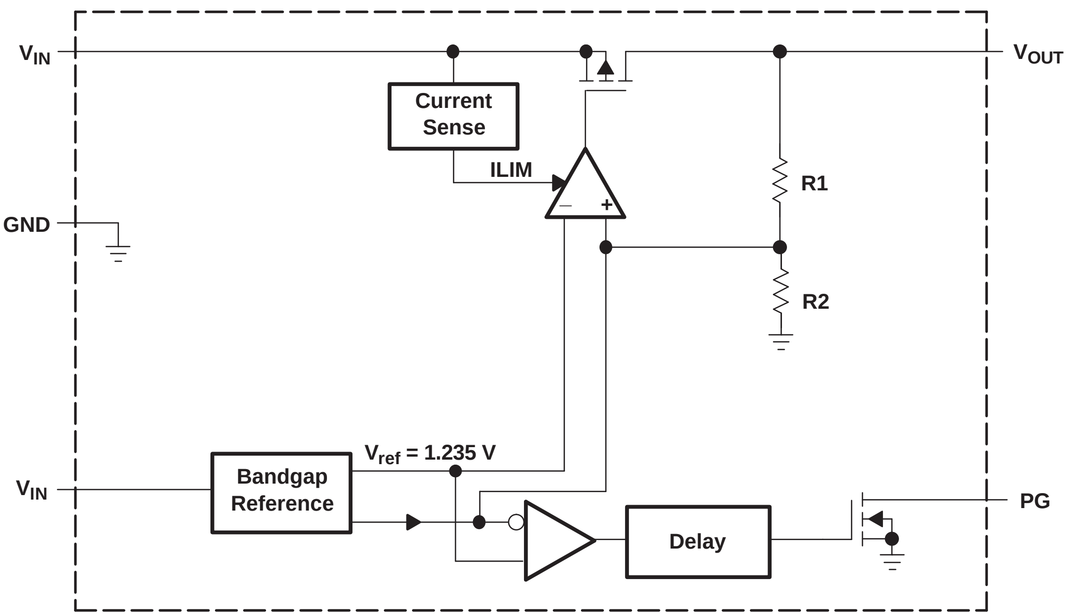


GROUND CURRENT
vs
FREE-AIR TEMPERATURE



DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
IN	4	I	The IN terminal is the power supply input to the device.
GND	2		Ground
NC	3		No connection
OUT	5	O	The OUT terminal provides the regulated output voltage of the device.
PG	1	O	The PG terminal for the fixed voltage option devices is an open-drain active-high output that indicates the status of V_O (output of the LDO). When V_O exceeds approximately 90% of the regulated voltage, PG goes to a high impedance state. It goes to a low-impedance state when V_O falls below approximately 90% (i.e. overload condition) of the regulated voltage. The open drain output of the PG terminal requires a pullup resistor.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Input voltage range(2)	0.3 to 6	V
	Maximum dc output voltage	4.9	V
	Peak output current	Internally limited	
	ESD rating, HBM	3	kV
	ESD rating, CDM	1	kV
	Continuous total power dissipation	See Dissipation Rating Table	
T_J	Operating junction temperature range	–55 to 145	°C
T_A	Operating ambient temperature range	–55 to 125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)	DERATING FACTOR ABOVE T_A = 25°C	$T_A \geq$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
Low K	DCK	165.39	396.24	2.52 mW/°C	252 mW	139 mW	101 mW	0 W
High K	DCK	165.39	314.74	3.18 mW/°C	318 mW	175 mW	127 mW	127 mW

TEXAS INSTRUMENTS
www.ti.com

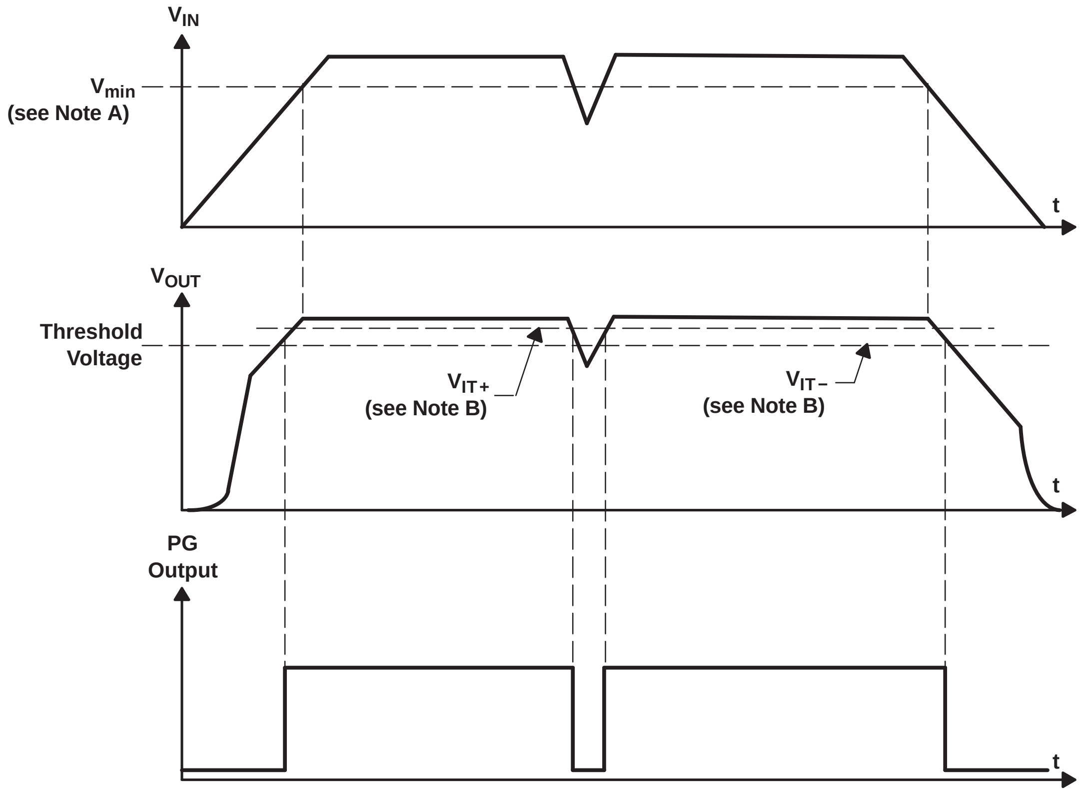
ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage (1)		I_O = 3 mA	1.8		5.5	V
			I_O = 10 mA	2		5.5	V
I_O	Continuous output current (2)			0		10	mA
T_A	Operating ambient temperature			–55		125	°C
	Output voltage (1mA to 10mA load) (3)	TPS79718	T_A = 25°C, 2.8 V < V_I < 5.5 V		1.8		V
			T_J = –55°C to 125°C, 2.8 V < V_I < 5.5 V	1.705		1.895	
		TPS79730	T_A = 25°C, 4 V < V_I < 5.5 V		3		V
			T_J = –55°C to 125°C, 4 V < V_I < 5.5 V	2.88		3.12	
		TPS79733	T_A = 25°C, 4.3 V < V_I < 5.5 V		3.3		V
			T_J = –55°C to 125°C, 4.3 V < V_I < 5.5 V	3.168		3.432	
	Quiescent current (GND current) (3)		T_A = 25°C, 0 mA < I_O < 10 mA		1.2		µA
			T_J = –55°C to 125°C, I_O = 10 mA			5	
	Load regulation		T_A = 25°C, I_O = 1 mA to 10 mA		17		mV
	Output voltage line regulation (ΔVout/ΔVin) (3)		V_O + 1 V < V_I ≤ 5.5 V, T_A = 25°C		0.15		%/V
			V_O + 1 V < V_I ≤ 5.5 V, T_J = –55°C to 125°C			0.8	
	Output noise voltage (TPS79718)		BW = 200 Hz to 100 kHz, C_O = 10 mF, I_O = 10 mA, T_A = 25°C		600		μV_{RMS}
	Output current limit		V_O = 0 V, See Note 4		190	300	mA
	Power supply ripple rejection (TPS79718)		f = 100 Hz, C_O = 10 mF, I_O = 10 mA, T_A = 25°C		50		dB
	Dropout voltage (4)	TPS79730	I_O = 10 mA, T_A = 25°C		125		mV
			I_O = 10 mA, T_A = –55°C to 125°C			400	
		TPS79733	I_O = 10 mA, T_A = 25°C		105		
			I_O = 10 mA, T_A = –55°C to 125°C			400	
	Minimum input voltage for valid PG		$I_{(PG)}$ = 100 uA, $V_{(PG)}$ ≥ 0.8 V		1.2		V
	PG trip threshold voltage		V_O decreasing		90		$\%V_O$
	PG output low voltage		V_I = 1.4 V, $I_{(PG)}$ = 100 uA		0.14	0.4	V
	PG leakage current		$V_{(PG)}$ = 5 V	0.1			nA

(1) To calculate the minimum input voltage for your maximum output current, use the following formula: V_I(min) = V_O(max) + V_{DO} (max load)
(2) Continuous output current is limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.
(3) The minimum IN operating voltage is 1.8 V or V_O (typ) + 1 V, whichever is greater. The maximum IN voltage is 5.5 V. There is no minimum output current requirement and the maximum output current is 10 mA.
(4) IN voltage equals V_O(typ) – 100 mV; The TPS79730 input voltage is set to 2.9 V and the TPS79733 input voltage is set to 3.2 V. The TPS79718 dropout voltage is limited by input voltage range limitations.

TPS797xx PG TIMING DIAGRAM



A. $V_{min} = V_{OUT} + V_{DO}$

B. The PG trip voltage is typically 10% lower than the output voltage (90%V_O). V_{IT-} to V_{IT+} is the hysteresis voltage.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT CURRENT

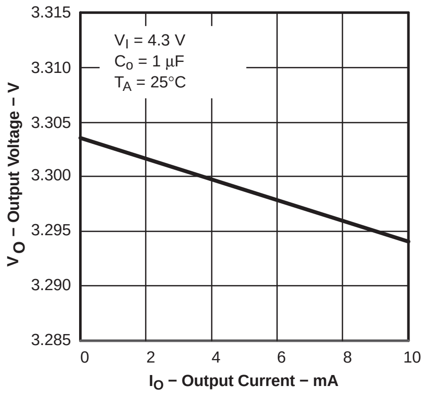


Figure 1.

OUTPUT VOLTAGE vs OUTPUT CURRENT

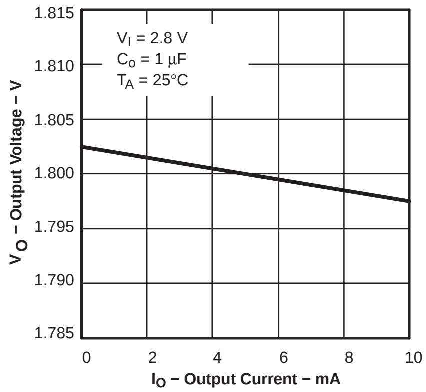


Figure 2.

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

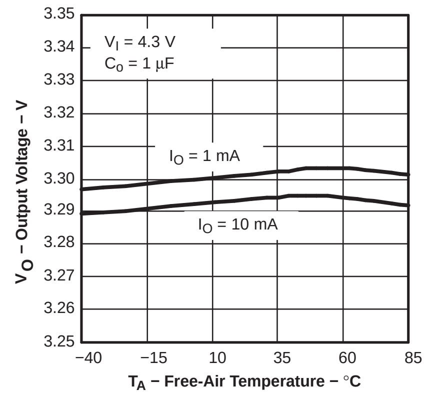


Figure 3.

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

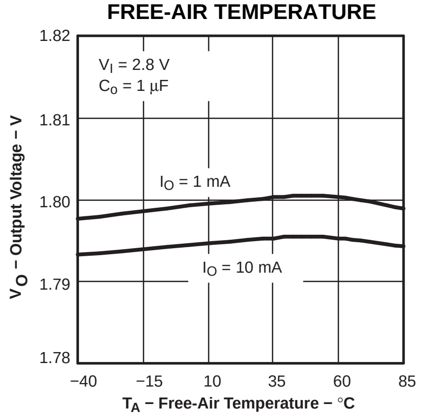


Figure 4.

GROUND CURRENT vs FREE-AIR TEMPERATURE

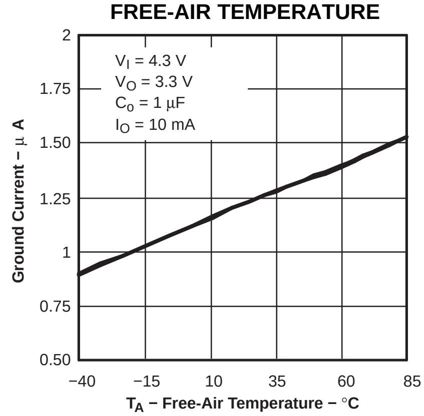


Figure 5.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

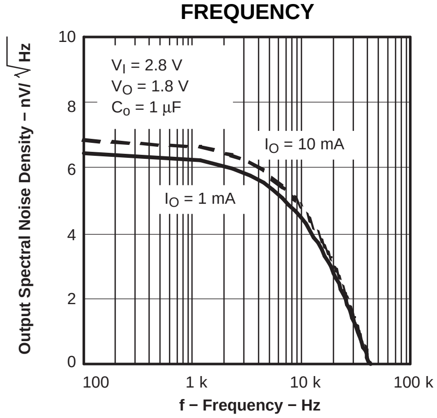


Figure 6.

OUTPUT IMPEDANCE vs FREQUENCY

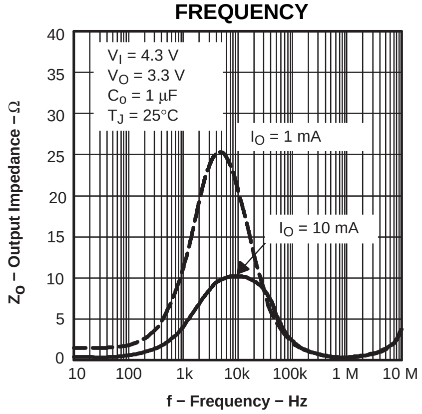


Figure 7.

DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

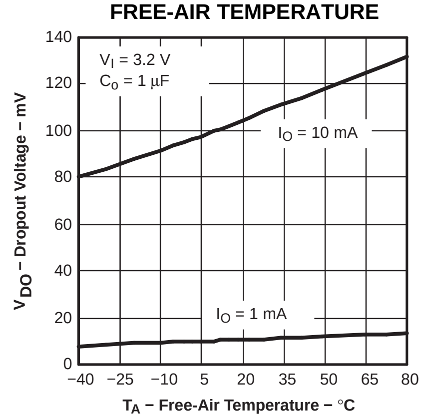


Figure 8.

vs POWER UP / POWER DOWN

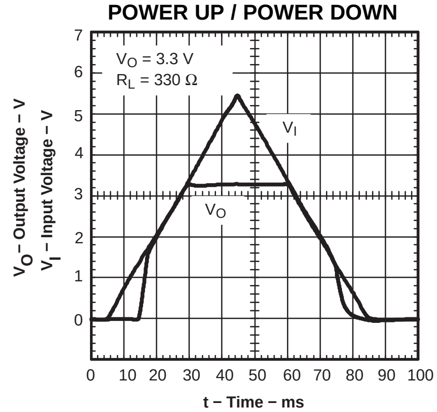


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TPS79718
LINE TRANSIENT RESPONSE

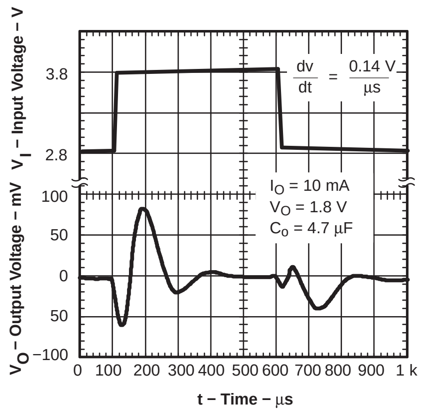


Figure 10.

TPS79718
LOAD TRANSIENT RESPONSE

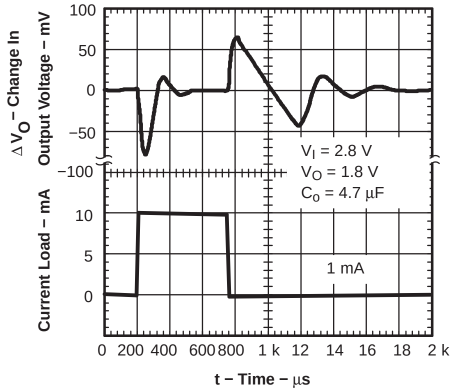


Figure 11.

TPS79733
LINE TRANSIENT RESPONSE

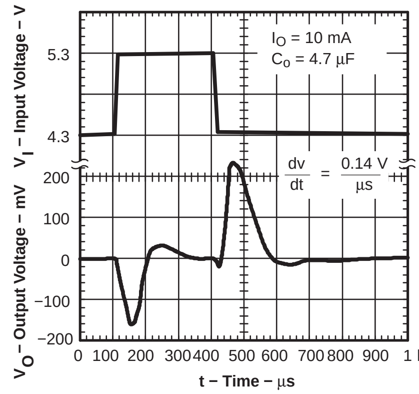


Figure 12.

TPS79733
LOAD TRANSIENT RESPONSE

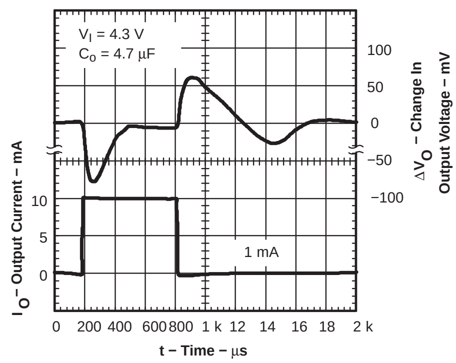


Figure 13.

APPLICATION INFORMATION

The TPS797xx family of low-dropout (LDO) regulators haS been optimized for use in micropower applications. The devices feature extremely low dropout voltages and ultralow quiescent current (1.2 μA typ).

A typical application circuit is shown in Figure 14.

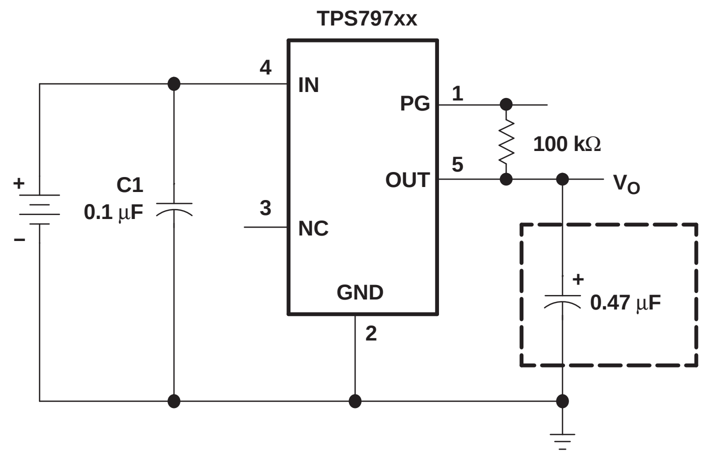


Figure 14. Typical Application Circuit

External Capacitor Requirements

Although not required, a 0.1 μF or larger input bypass capacitor, connected between IN and GND and located close to the TPS797xx, is recommended, especially when a highly resistive power supply is powering the LDO in addition to other devices.

Like all low-dropout regulators, the TPS797xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 0.47 μF. Any 0.47 μF capacitor is suitable. Capacitor values larger than 0.47 μF are acceptable.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; restrict the maximum junction temperature to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation: $P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$

Where:

$T_J$max is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the Power Dissipation Rating Table).

TA is the ambient temperature.

The regulator dissipation is calculated using:

$P_D = (V_I - V_O) \times I_O$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Regulator Protection

The TPS797xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS797xx features internal current limiting. During normal operation, the TPS797xx limits output current to approximately 190 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

Microcontroller Application

One application for which this device is particularly suited is providing a regulated input voltage and power good (PG) supervisory signal to low-power devices such as mixed-signal microcontrollers. The quiescent or ground current of the TPS797xx family is typically 1.2 µA even at full load; therefore, the reduction in battery life by including the TPS797xx in the system is negligible. The primary benefits of using the TPS797xx to power low power digital devices include:

- Regulated output voltage that protects the device from battery droop and noise on the line (e.g., switch bounce)
- Smooth, monotonic power up
- PG signal for controlled device RESET
- Potential to use an existing 5-V power rail to power a 3.3 V or lower device
- Potential to provide separate digital and analog power and ground supplies for a system with only one power source

Figure 15 shows an application in which the TPS79718 is used to power Texas Instruments MSP430 mixed signal microcontroller.

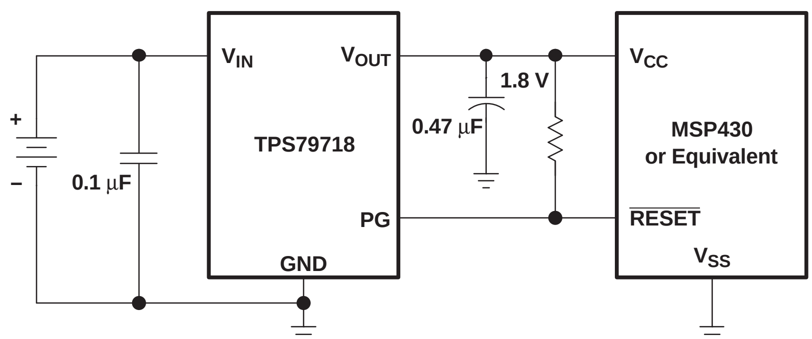


Figure 15. MSP430 Microcontroller Powered by the TPS79718 Regulator

Minimal board space is needed to accommodate the DCK (SC70/SOT-323) packaged TPS79718, the 0.1 µF output capacitor, the 0.47 µF input capacitor, and the pullup resistor on the PG pin.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79718MDCKREP	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	CKW	Samples
TPS79730MDCKREP	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	BUA	Samples
V62/06673-01XE	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	CKW	Samples
V62/06673-02XE	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	BUA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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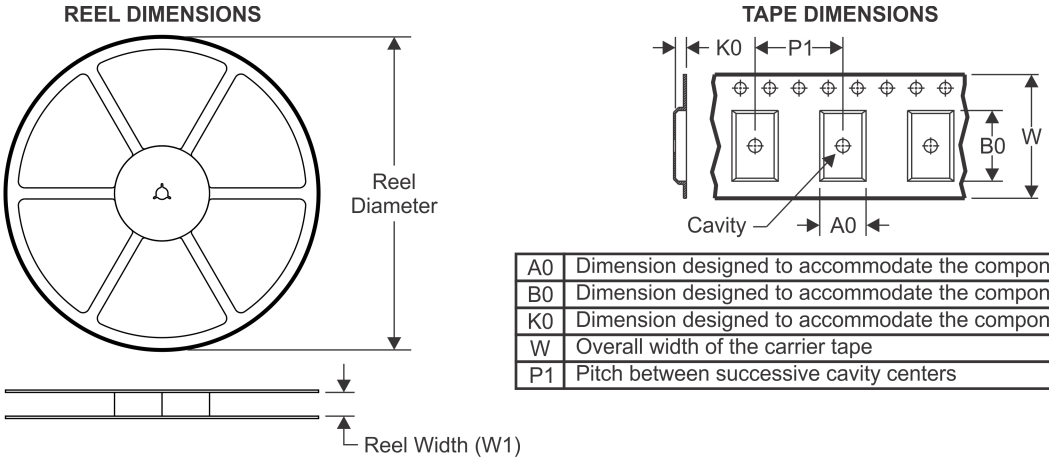
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

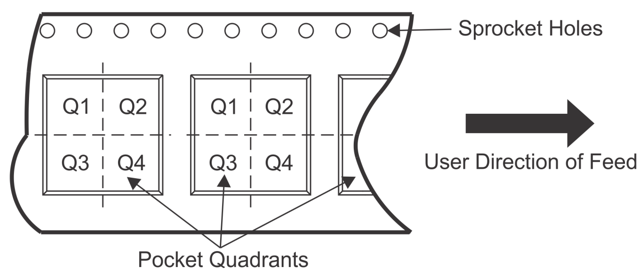
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

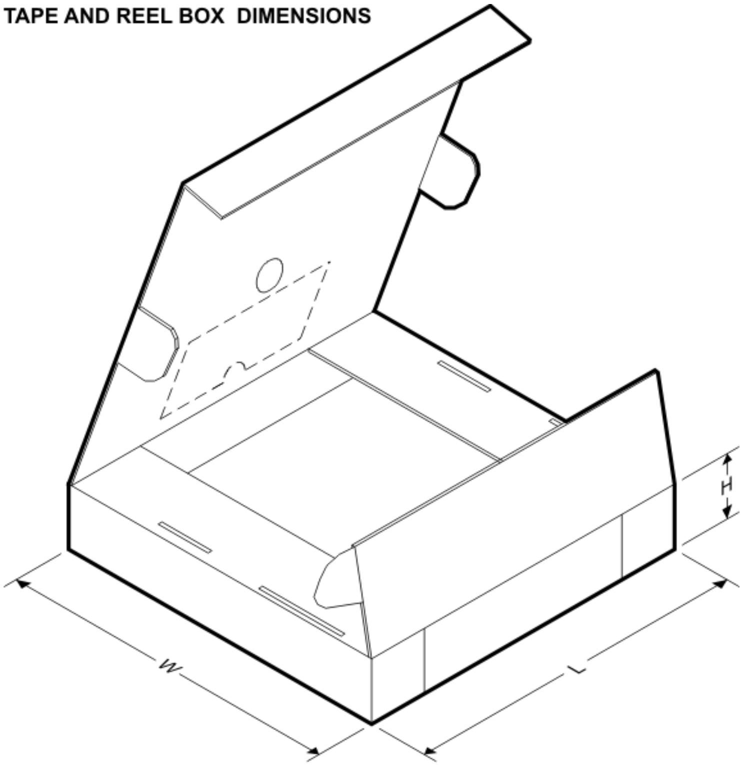
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

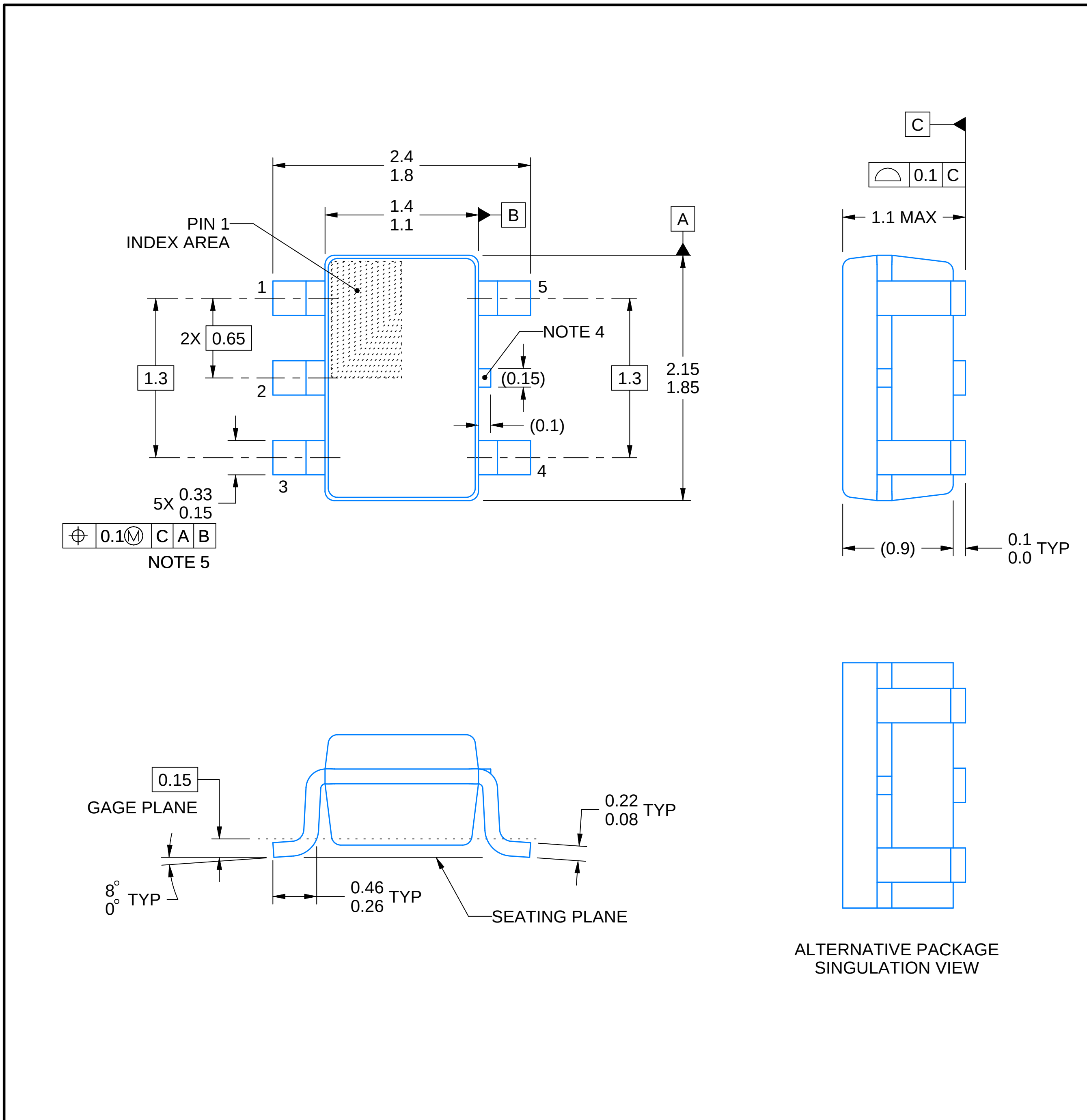
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79718MDCKREP	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS79730MDCKREP	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79718MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0
TPS79730MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0



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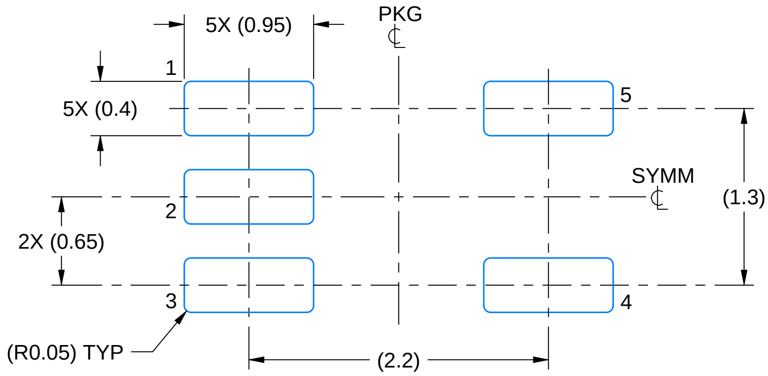
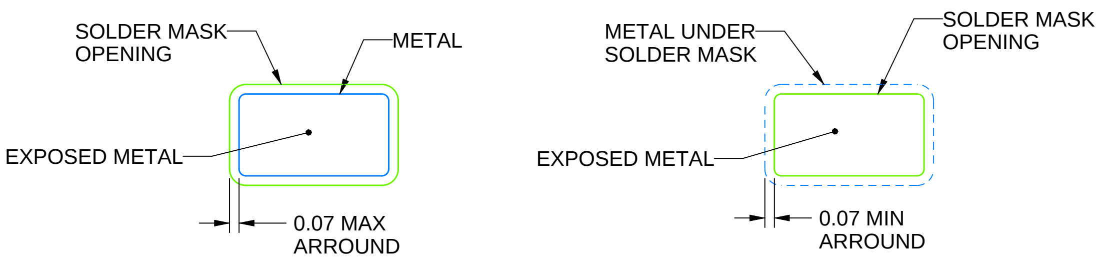
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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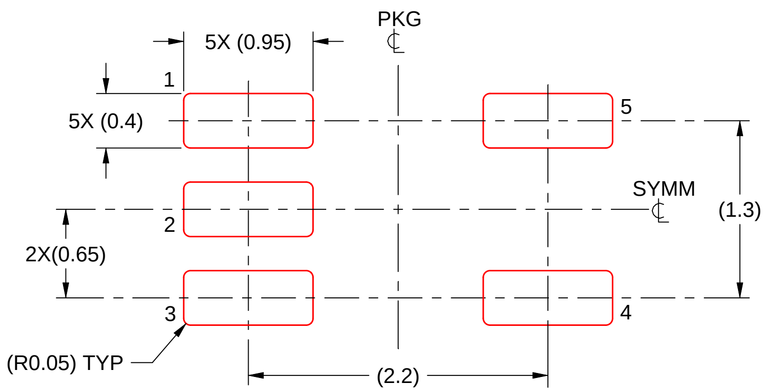
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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