TS3USB221A ESD Protected, High-Speed USB 2.0 (480Mbps) 1:2 Multiplexer and Demultiplexer Switch With Single Enable

1 Features

- V_{CC} operation at 2.5V to 3.3V
- $V_{I/O}$ accepts signals up to 5.5V
- 1.8V compatible control-pin inputs
- Low-power mode when $\overline{OE}$ is disabled (1µA)
- R_{ON} = 6ω maximum
- δR_{ON} = 0.2ω typical
- $C_{IO(ON)}$ = 6pf typical
- Low power consumption (30µA maximum)
- High bandwidth (900MHz typical)
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD performance tested per JEDEC JS-001
  - 7000V human-body model
  - 1000V charged-device model (JEDEC JS-002)
- ESD performance I/O to GND
  - 12kV human-body model

2 Applications

- Routes signals for USB 1.0, 1.1, and 2.0
- Mobile phones
- Cameras
- Notebooks
- USB I/O expansion

3 Description

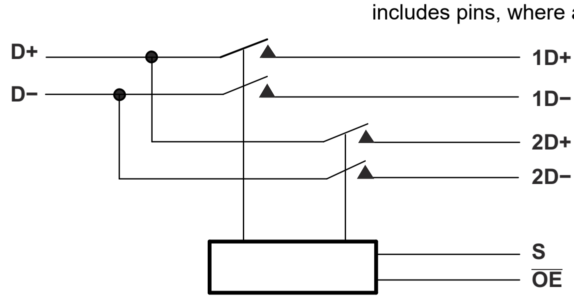
The TS3USB221A device is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that can reduce the power consumption to 1µA for portable applications with a battery or limited power budget. The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480Mbps).

The TS3USB221A device integrates ESD protection cells on all pins, is available in a tiny µQFN package (2mm × 1.5mm) and is characterized over the free air temperature range from –40°C to 85°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TS3USB221A	RSE (UQFN, 10)	2mm × 1.5mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



EN is the internal enable signal applied to the switch.

Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

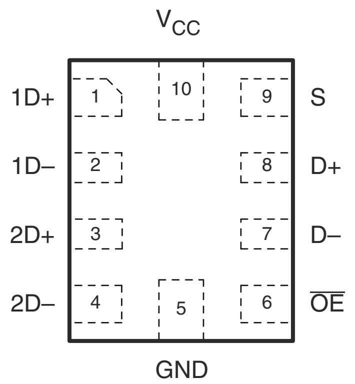


Figure 4-1. RSE Package, 10-Pin µQFN (Top View)

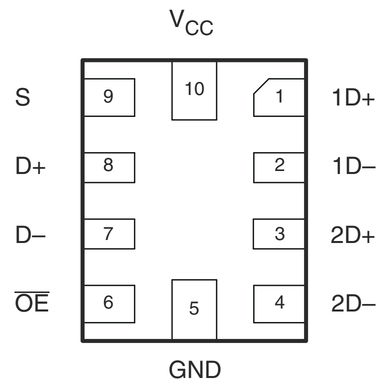


Figure 4-2. RSE Package, 10-Pin µQFN (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1D+	1	I/O	USB port 1
1D–	2	I/O	
2D+	3	I/O	USB port 2
2D–	4	I/O	
GND	5	—	Ground
$\overline{OE}$	6	I	Bus-switch enable
D+	8	I/O	Common USB port
D—	7	I/O	
S	9	I	Select input
V_{CC}	10	—	Supply voltage

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	4.6	V
Control input voltage, V_S, $V_{\overline{OE}}$ [(2)] [(3)]		–0.5	7	V
Switch I/O voltage, $V_{I/O}$ [(2)] [(3)] [(4)]		–0.5	7	V
Control input clamp current, I_{IK}	$V_{IN} < 0$		–50	mA
I/O port clamp current, $I_{I/OK}$	$V_{I/O} < 0$		–50	mA
ON-state switch current, $I_{I/O}$ [(5)]			±120	mA
Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	All pins except I/O to GND	±7000	V
			I/O to GND	±12000	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	All pins	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_S, $V_{\overline{OE}}$	High-level control input voltage	V_{CC} = 2.3V to 2.7V	0.46 × V_{CC}	V_{CC}	V
		V_{CC} = 2.7V to 3.6V	0.46 × V_{CC}	V_{CC}	
	Low-level control input voltage	V_{CC} = 2.3V to 2.7V	0	0.25 × V_{CC}	V
		V_{CC} = 2.7V to 3.6V	0	0.25 × V_{CC}	
$V_{I/O}$	Data input/output voltage[(1)]		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) The I/O pins are 5.5V tolerant and functional for the entire range. However, for $V_{I/O}$ > 3.6V, channel RON will be high (up to 100Ω).

5.4 Thermal Information

THERMAL METRIC[1]		RSE (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	118.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	121.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	121.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{IK}	Input-Source Clamp Voltage	V_{CC} = 3.6V, 2.7V, I_I = –18 mA		–1.8			V
I_{IN}	Input leakage current, control inputs	V_{CC} = 3.6V, 2.7V, 0V, V_{IN} = 0V to 3.6V				±1	µA
I_{OZ} [3]	Off-state leakage current	V_{CC} = 3.6V, 2.7V, V_O = 0V to 5.25V, V_I = 0V, V_{IN} = V_{CC} or GND, Switch OFF				±1	µA
$I_{(OFF)}$	Power-off leakage current	V_{CC} = 0V	$V_{I/O}$ = 0V to 5.25V			±2	µA
			$V_{I/O}$ = 0V to 3.6V			±2	
			$V_{I/O}$ = 0V to 2.7V			±1	
I_{CC}	Supply Current	V_{CC} = 3.6V, 2.7V, V_{IN} = V_{CC} or GND, $I_{I/O}$ = 0V, Switch ON or OFF				30	µA
I_{CC}	Supply Current (low power mode)	V_{CC} = 3.6V, 2.7V, V_{IN} = V_{CC} or GND, Switch disabled, $\overline{OE}$ in high state				1	µA
ΔI_{CC} [4]	Supply-current change, control inputs	One input at 1.8V, Other inputs at V_{CC} or GND	V_{CC} = 3.6V			20	µA
			V_{CC} = 2.7V			0.5	
C_{in}	Input capacitance, control inputs	V_{CC} = 3.3V, 2.5V, V_{IN} = V_{CC} or 0V			1.5	2.5	pF
$C_{io(OFF)}$	OFF capacitance	V_{CC} = 3.3V, 2.5V, $V_{I/O}$ = V_{CC} or 0V, Switch OFF			3.5	5	pF
$C_{io(ON)}$	ON capacitance	V_{CC} = 3.3V, 2.5V, $V_{I/O}$ = V_{CC} or 0V, Switch ON			6	7.5	pF
R_{ON} [5]	ON-state resistance	V_{CC} = 3V, 2.3V	V_I = 0V, I_O = 30mA		3	6	Ω
			V_I = 2.4V, I_O = –15mA		3.4	6	
ΔR_{ON}	ON-state resistance match between channels	V_{CC} = 3V, 2.3V	V_I = 0V, I_O = 30mA		0.2		Ω
			V_I = 1.7, I_O = –15mA		0.2		
$R_{ON(flat)}$	ON-state resistance flatness	V_{CC} = 3V, 2.3V	V_I = 0V, I_O = 30mA		1		Ω
			V_I = 1.7, I_O = –15mA		1		

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

5.6 Dynamic Electrical Characteristics, V_{CC} = 3.3V ±10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3V ±10%, GND = 0V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250MHz		–40		dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250MHz		–41		dB
BW	Bandwidth (–3 dB)	R_L = 50		0.9		GHz

5.7 Dynamic Electrical Characteristics, V_{CC} = 2.5V ±10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5V ±10%, GND = 0V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250MHz		–39		dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250MHz		-40		dB
BW	Bandwidth (3 dB)	R_L = 50		0.9		GHz

5.8 Switching Characteristics, V_{CC} = 3.3V ±10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3V ±10%, GND = 0V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			30	ns
		$\overline{OE}$ to D, nD			17	
t_{OFF}	Line disable time	S to D, nD			12	ns
		$\overline{OE}$ to D, nD			10	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL}– t_{PLH})(2)			0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. This time constant is much smaller than the rise/fall times of typical driving signals, therefore the time adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and the switch interactions with the load on the driven side.

5.9 Switching Characteristics, V_{CC} = 2.5V ±10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5V ±10%, GND = 0V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			50	ns
		$\overline{OE}$ to D, nD			32	
t_{OFF}	Line disable time	S to D, nD			23	ns
		$\overline{OE}$ to D, nD			12	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL}– t_{PLH})(2)			0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. This time constant is much smaller than the rise/fall times of typical driving signals, therefore the time adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and the switch interactions with the load on the driven side.

5.10 Typical Characteristics

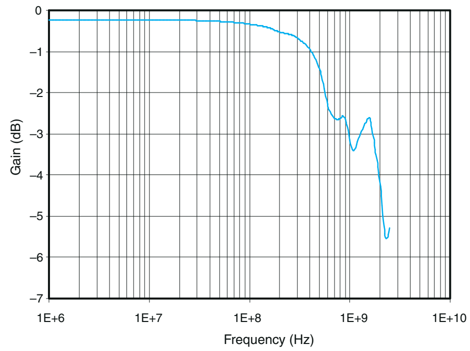


Figure 5-1. Gain vs Frequency

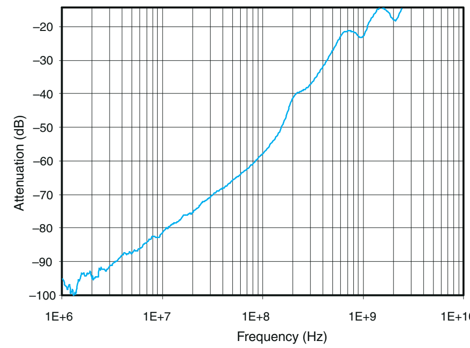


Figure 5-2. OFF Isolation vs Frequency

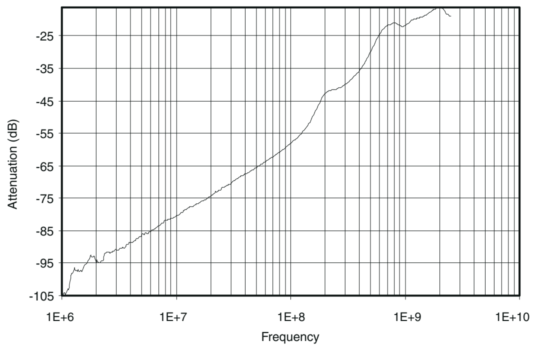


Figure 5-3. Crosstalk vs Frequency

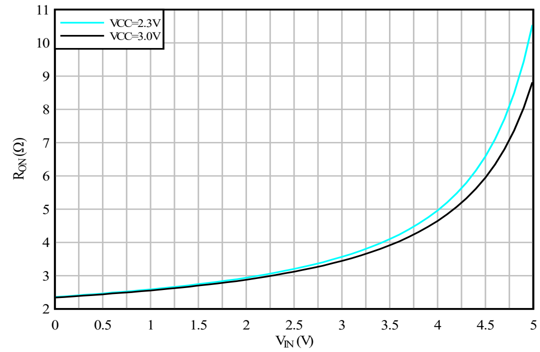
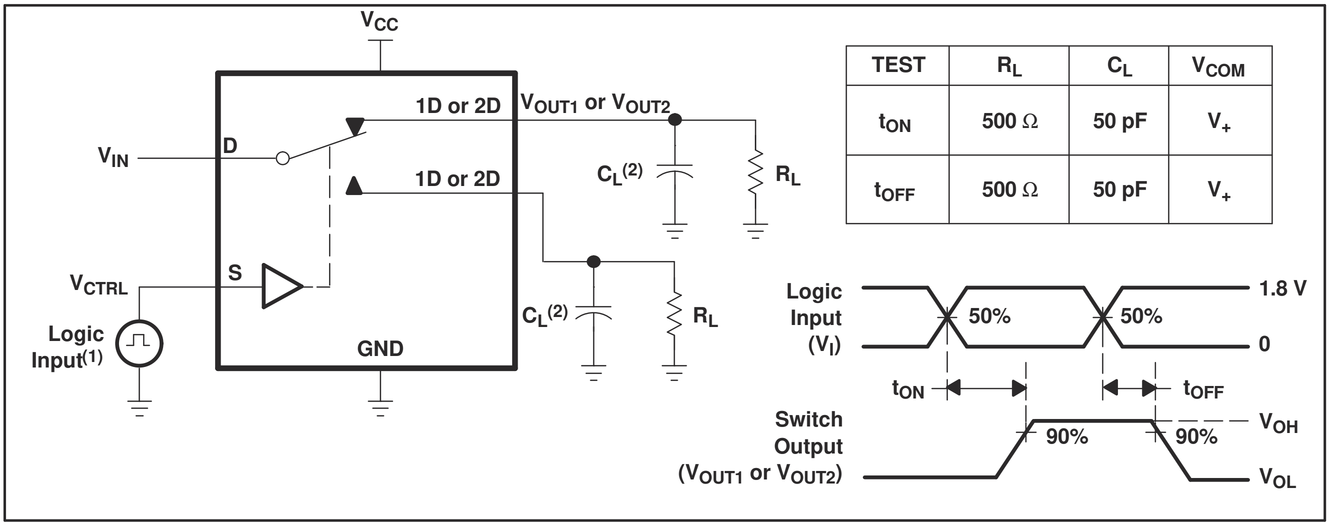


Figure 5-4. R_{on} vs V_{IN} (I_{OUT} = –30 mA)

6 Parameter Measurement Information



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 6-1. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

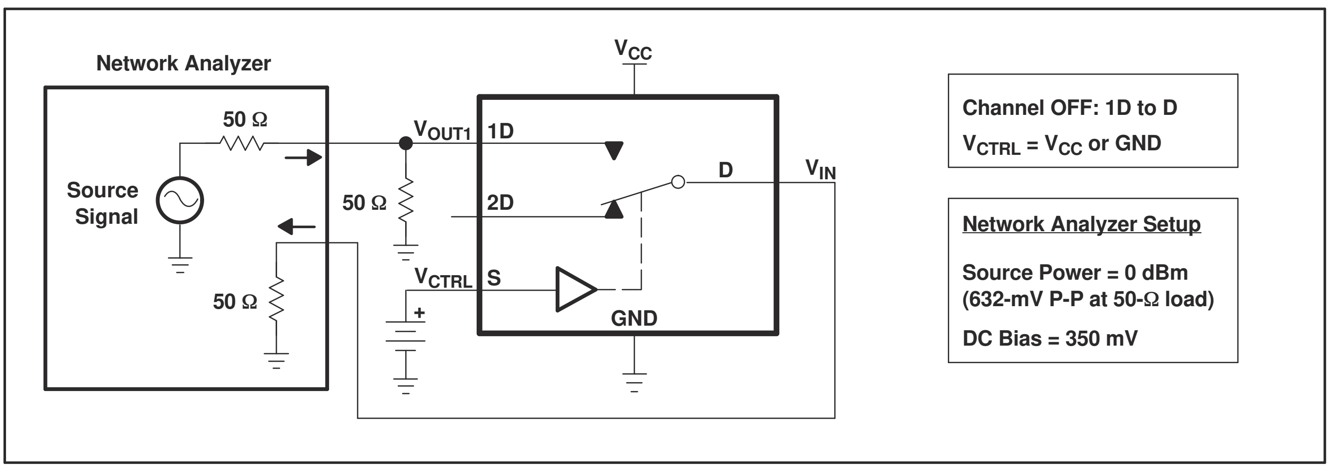


Figure 6-2. OFF Isolation (O_{ISO})

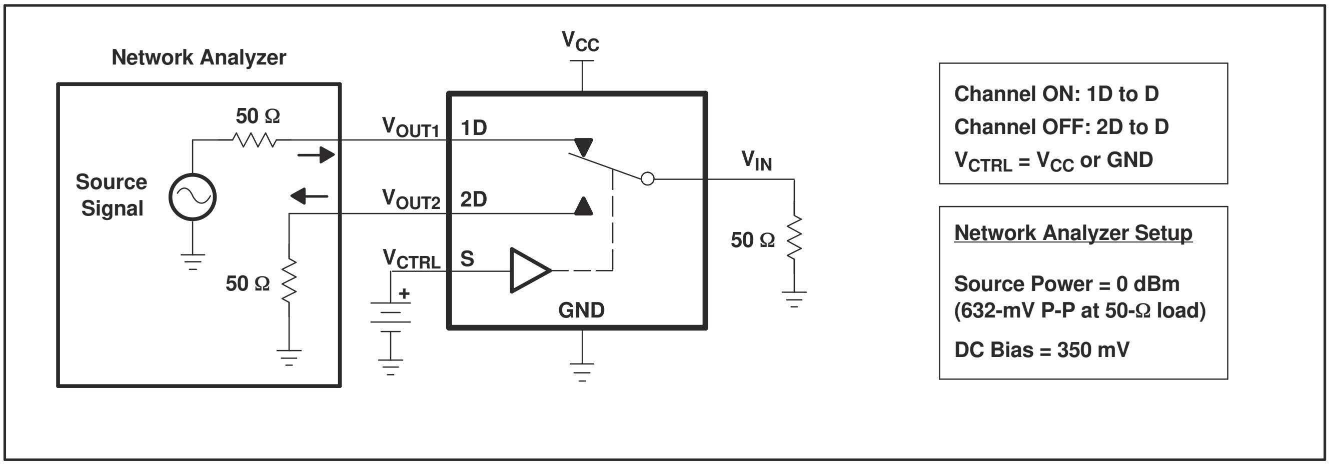


Figure 6-3. Crosstalk (X_{TALK})

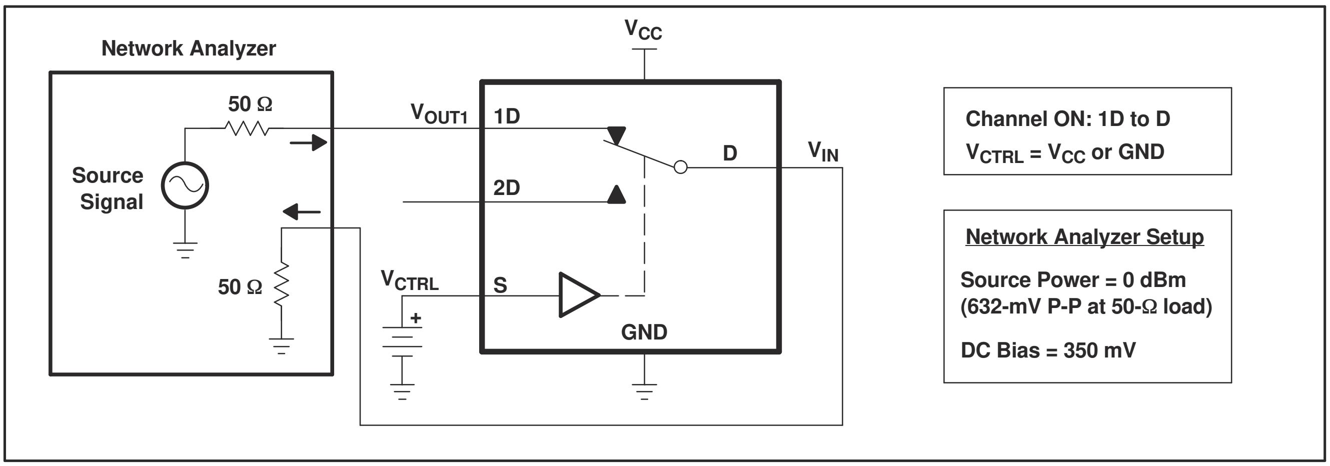


Figure 6-4. Bandwidth (BW)

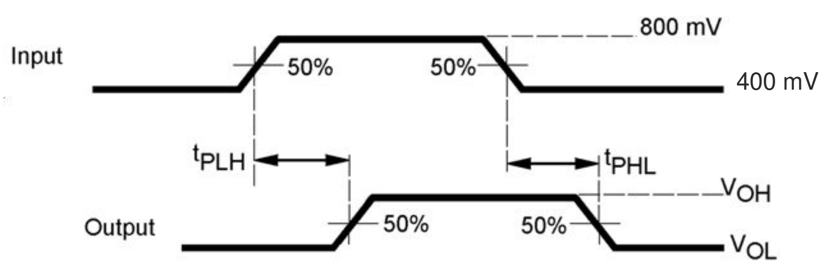


Figure 6-5. Propagation Delay

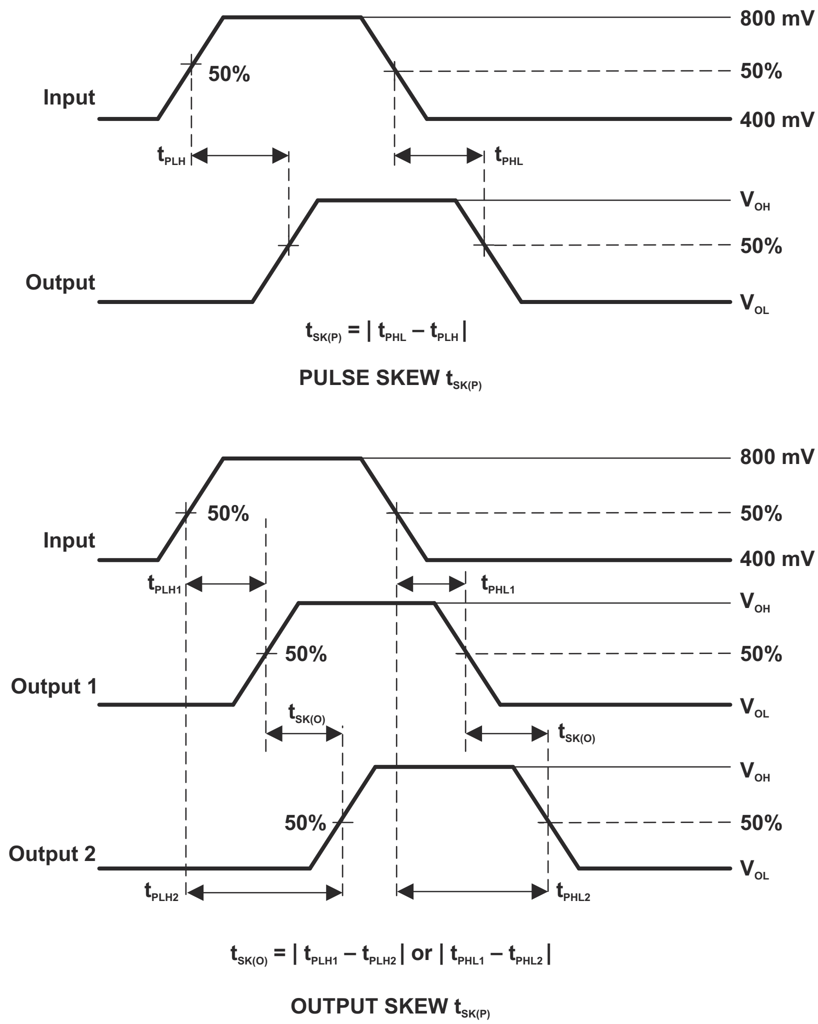


Figure 6-6. Skew Test

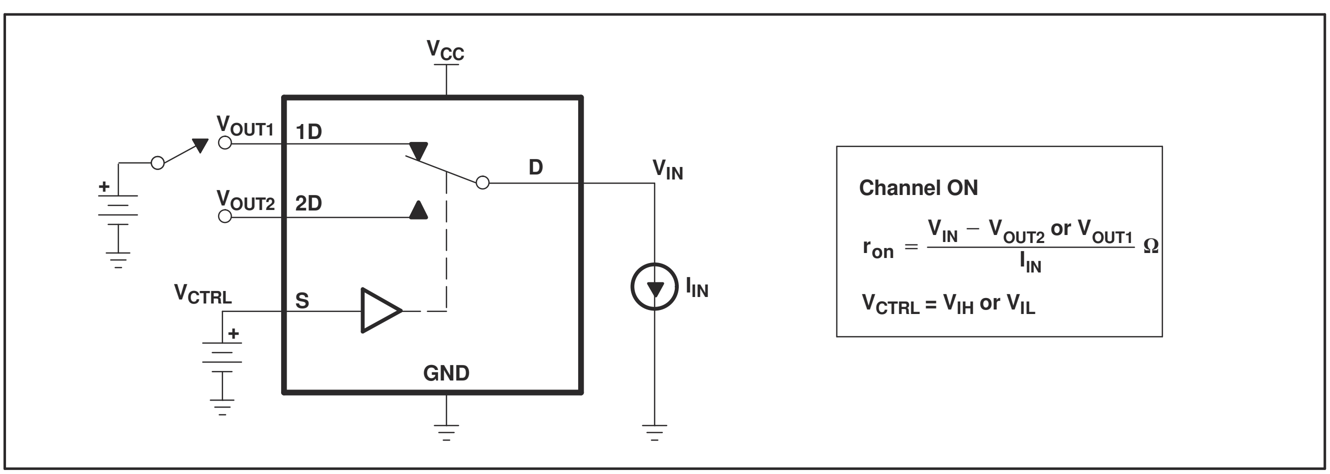


Figure 6-7. ON-State Resistance (r_{on})

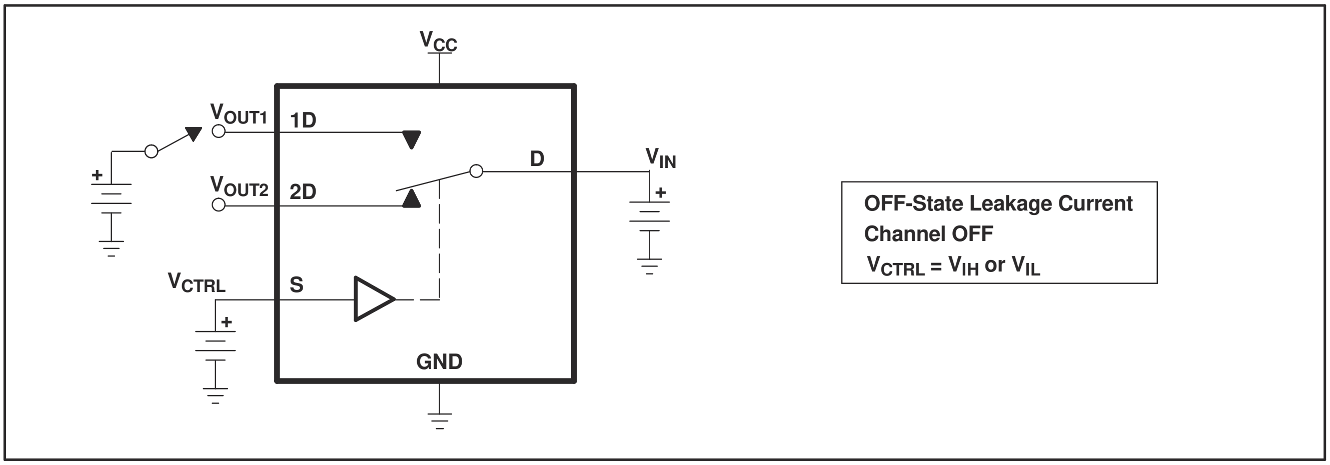


Figure 6-8. OFF-State Leakage Current

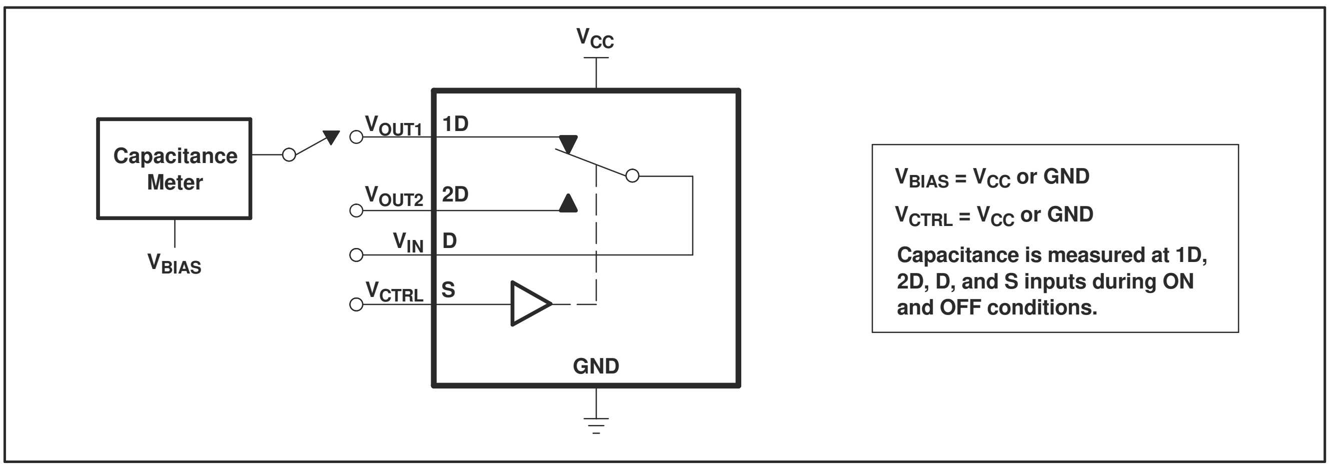


Figure 6-9. Capacitance

7 Detailed Description

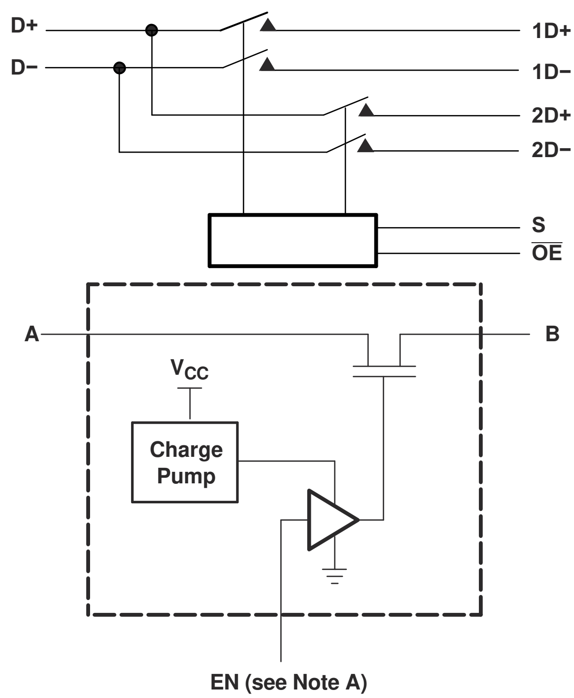
7.1 Overview

The TS3USB221A device is a 2-channel SPDT switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that can reduce the power consumption to 1µA for portable applications with a battery or limited power budget.

The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480Mbps).

The TS3USB221A device integrates ESD protection cells on all pins, is available in a tiny µQFN package (2mm × 1.5mm) and is characterized over the free air temperature range from –40°C to 85°C.

7.2 Functional Block Diagram



A. EN is the internal enable signal applied to the switch.

Figure 7-1. Simplified Schematic of Each FET Switch (SW)

7.3 Feature Description

7.3.1 Low Power Mode

The TS3USB221A has a low power mode that reduces the power consumption to 1 μA while the devices is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin $\overline{OE}$ must be supplied with a logic "High" signal.

7.4 Device Functional Modes

Table 7-1. Truth Table

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB221A can effectively expand the limited USB I/Os by switching between multiple USB buses and interface with the buses on a single USB hub or controller.

8.2 Typical Application

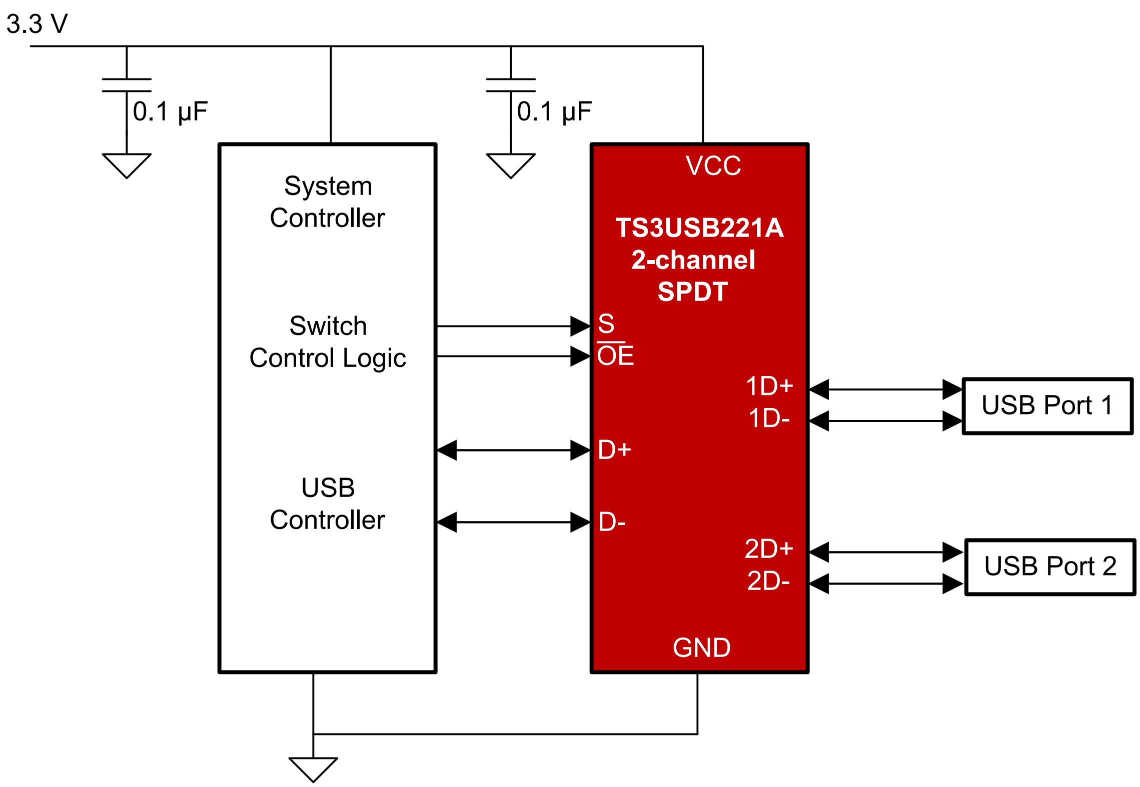


Figure 8-1. Application Schematic

8.2.1 Design Requirements

Follow the design requirements of the USB 1.0,1.1, and 2.0 standards.

TI recommends that the digital control pins S and $\overline{OE}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that can result from the floating pin.

8.2.2 Detailed Design Procedure

The TS3USB221A can operate properly without any external components. However, TI recommends to connect unused pins to ground through a 50Ω resistor to prevent signal reflections back into the device.

8.2.3 Application Curves

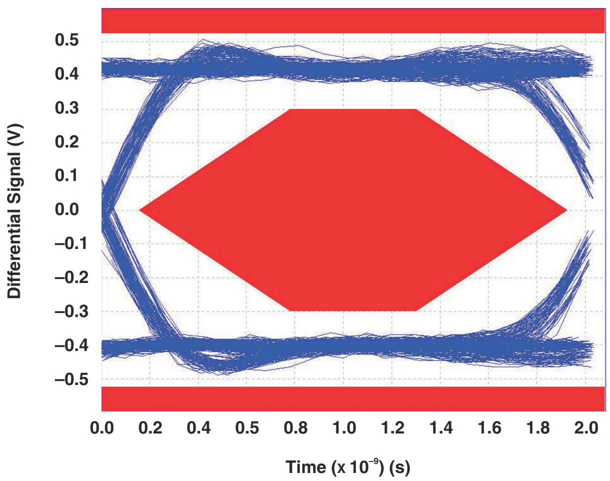


Figure 8-2. Eye Pattern: 480Mbps USB Signal With No Switch (Through Path)

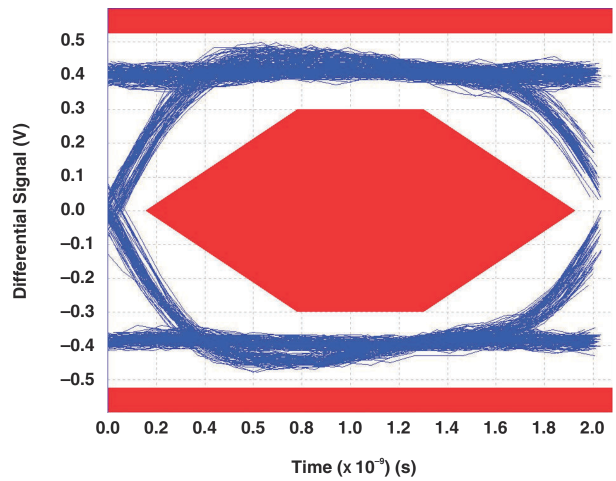


Figure 8-3. Eye Pattern: 480Mbps USB Signal With Switch NC Path

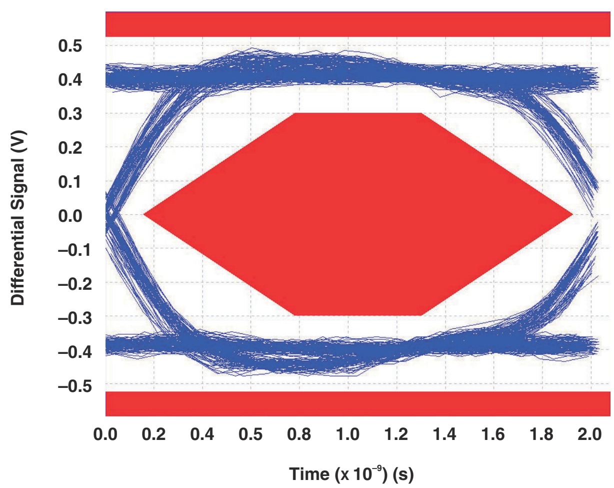


Figure 8-4. Eye Pattern: 480Mbps USB Signal With Switch NO Path

8.3 Power Supply Recommendations

Make sure the power to the device is supplied through the VCC pin and follows the USB 1.0, 1.1, and 2.0 standards. A bypass capacitor is recommended to be placed as close to the supply pin VCC to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

8.4 Layout

8.4.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D+/D– traces.

Make sure the high speed D+/D– trace lengths match and are no more than 4 inches; otherwise, the eye diagram performance can degrade. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, make sure the impedance of D+ and D– traces match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners to reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around the via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because stubs cause signal reflections. If a stub is unavoidable, keep the stub less than 200mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 8-5.

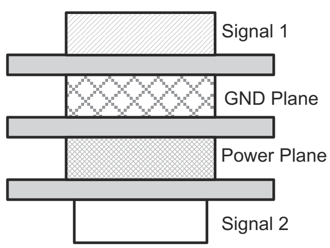


Figure 8-5. Four-Layer Board Stack-Up

Make sure the majority of signal traces run on a single layer, preferably Signal 1. Make sure the GND plane, which is solid with no cuts, is immediately next to this layer. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

8.4.2 Layout Example

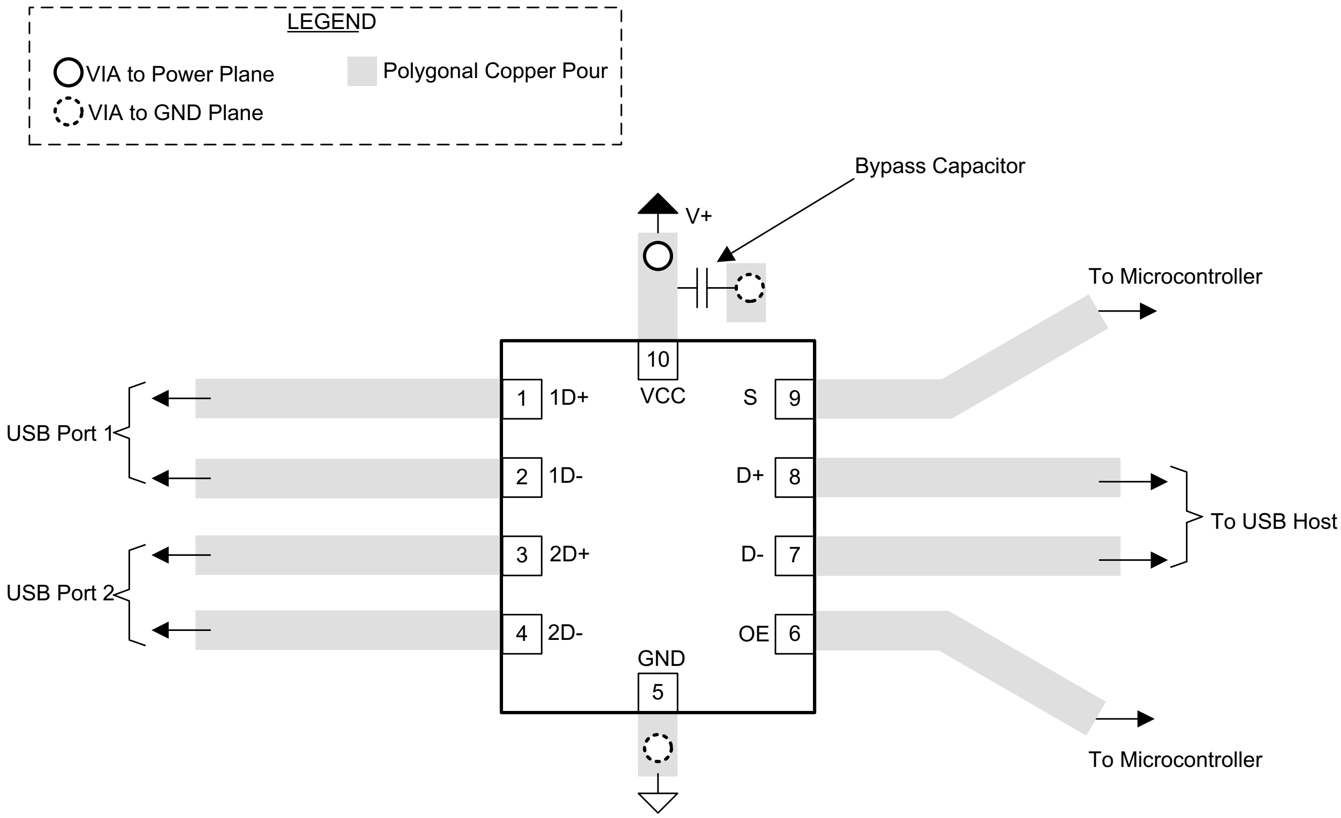


Figure 8-6. Package Layout Diagram

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2015) to Revision B (July 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Updated the ESD performance test conditions in the *Features* section... 1
- Changed CDM test conditions in the ESD Ratings table from: per JEDEC specification JESD22-C101 to: per ANSI/ESDA/JEDEC JS-002.. 4
- Added footnote to the $V_{I/O}$ parameter in the *Recommended Operating Conditions* table................................4
- Changed RSE (UQFN) junction-to-ambient thermal resistance value from: 179.7°C/W to: 204.8°C/W............ 5
- Changed RSE (UQFN) junction-to-case (top) thermal resistance value from: 107.9°C/W to: 118.1°C/W......... 5
- Changed RSE (UQFN) junction-to-board thermal resistance value from: 100.7°C/W to: 121.5°C/W................5
- Changed RSE (UQFN) junction-to-top characterization parameter value from: 7.1°C/W to: 13.9°C/W.............5
- Changed RSE (UQFN) junction-to-board characterization parameter value from: 100.0°C/W to: 121.2°C/W...5
- Changed the V_{IK} value in the *Electrical Characteristics* table from: –1.8V maximum to: –1.8V minimum......... 5
- Changed the *Typical Characteristics* section..7

Changes from Revision * (November 2008) to Revision A (February 2015) **Page**

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. 1
- Deleted the *Ordering Information* table from the data sheet. See the *Mechanical, Packaging, and Orderable Information* section for the ordering information.. 1
- Update the document to the new TI data sheet standard 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB221ARSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LH7, LHR, LHV)	Samples
TS3USB221ARSERG4	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LH7, LHR, LHV)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TS3USB221A :

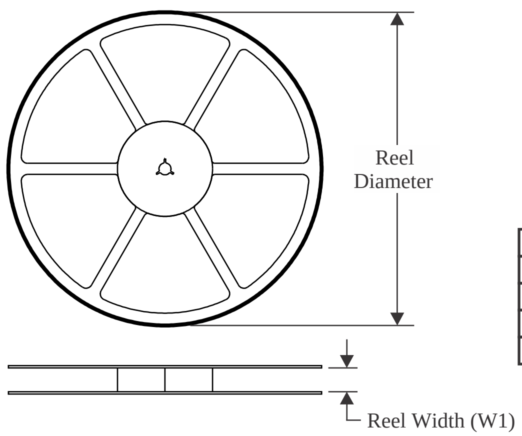
- Automotive : TS3USB221A-Q1

NOTE: Qualified Version Definitions:

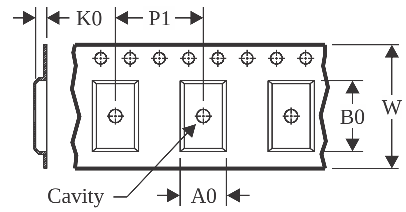
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

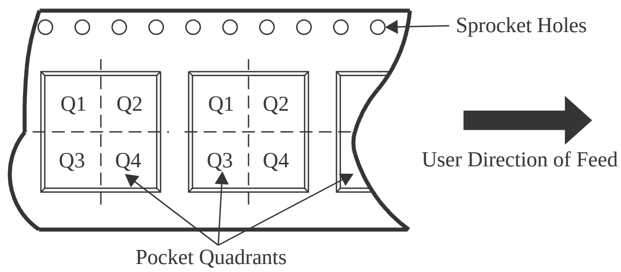


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

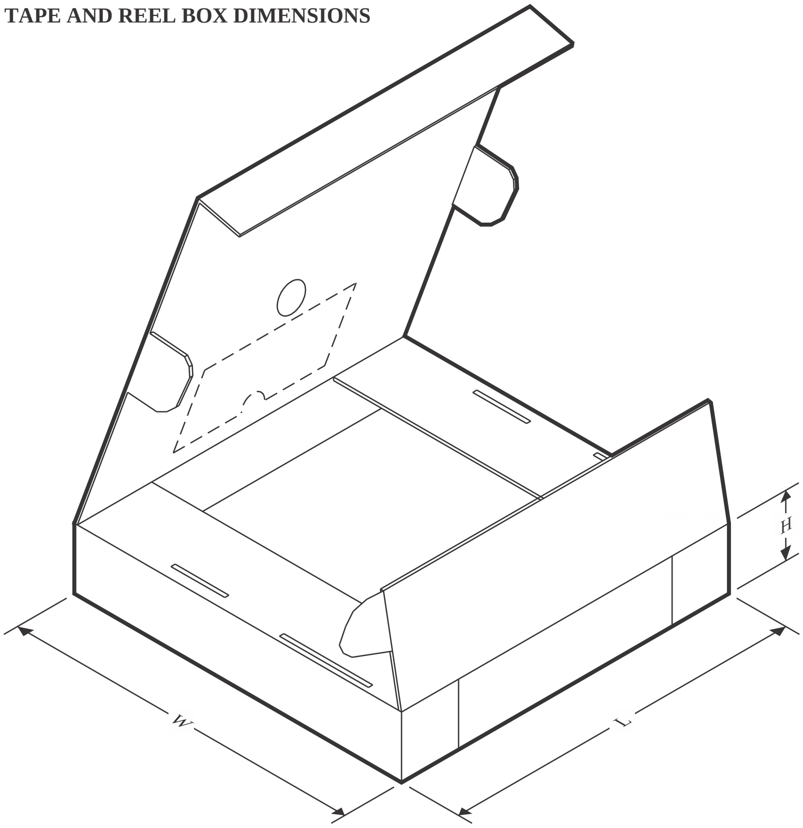
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

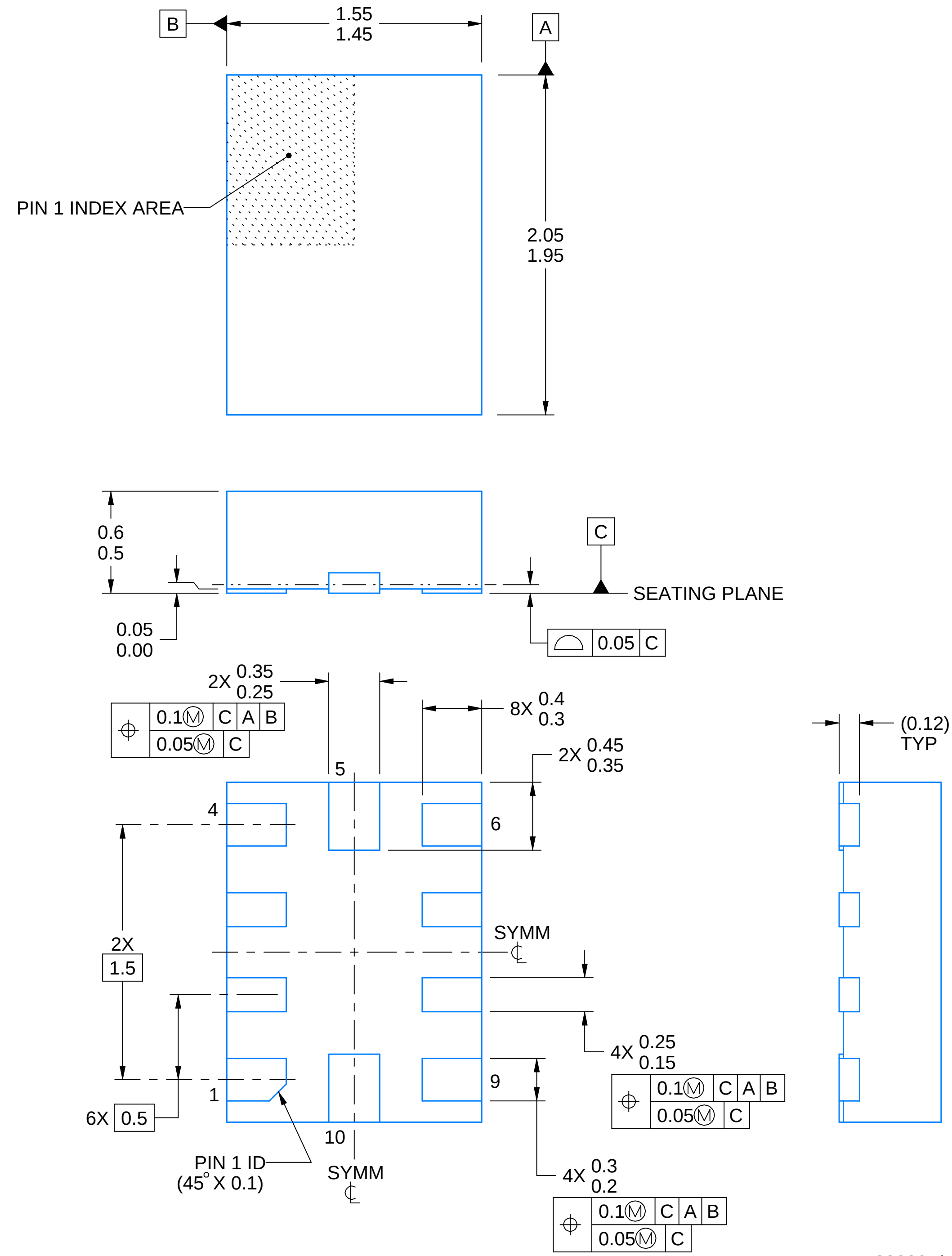
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB221ARSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.3	0.75	4.0	8.0	Q1
TS3USB221ARSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

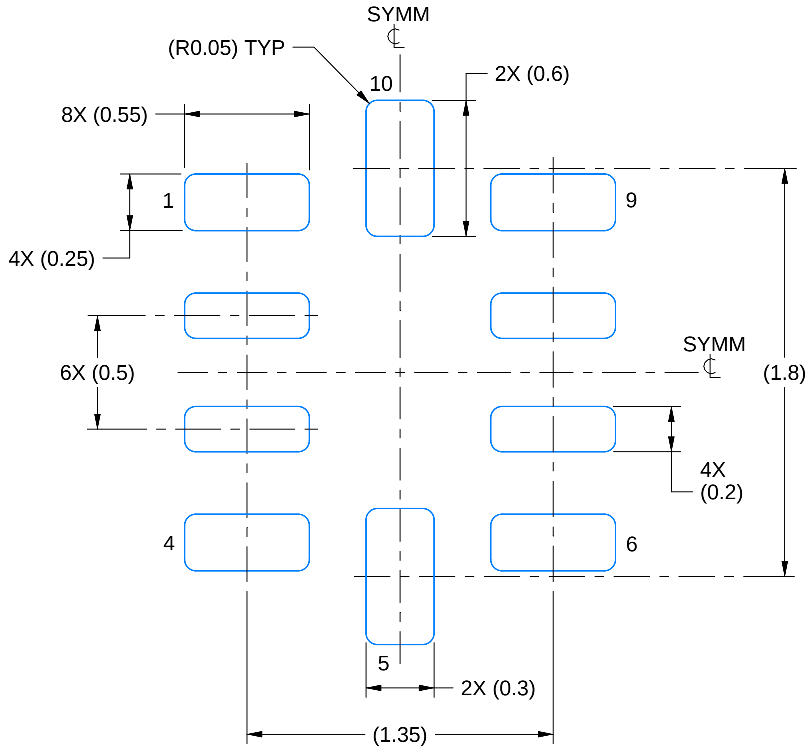
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB221ARSER	UQFN	RSE	10	3000	184.0	184.0	19.0
TS3USB221ARSER	UQFN	RSE	10	3000	189.0	185.0	36.0



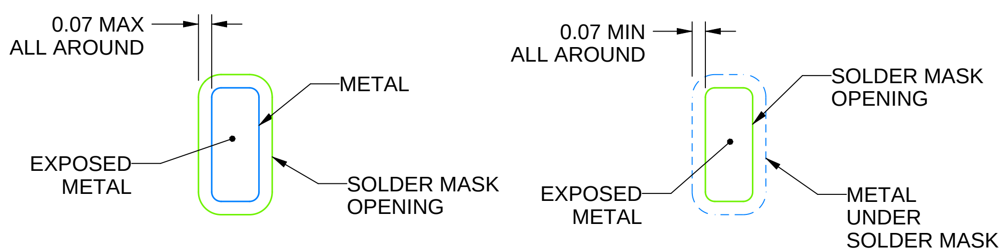
4220307/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



NON SOLDER MASK DEFINED (PREFERRED)

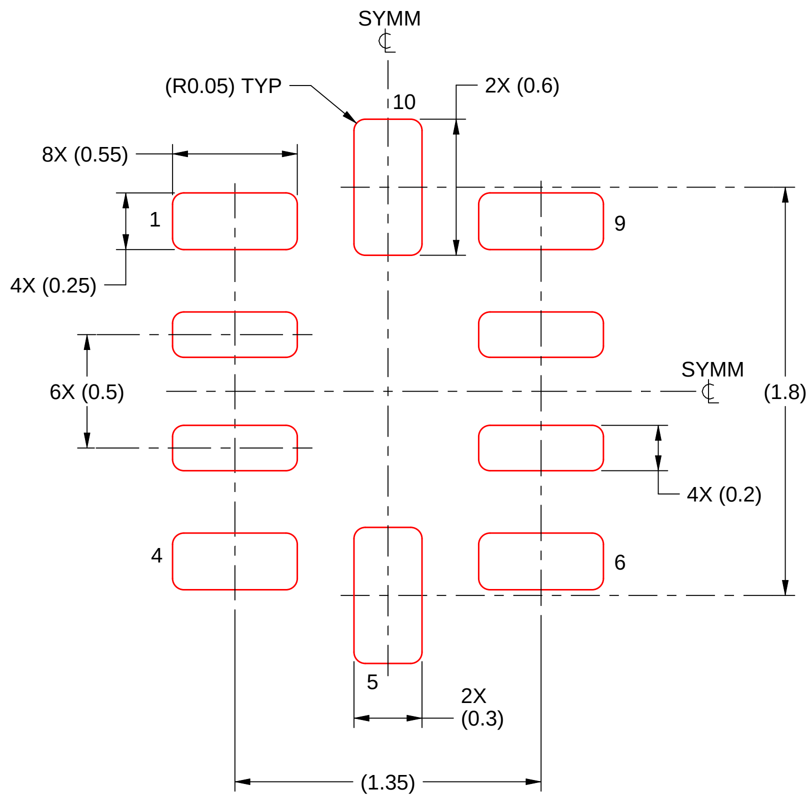
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER