TEXAS INSTRUMENTS
2N7001T-Q1
JAJSIK8A – FEBRUARY 2020 – REVISED JULY 2020

2N7001T-Q1 1 ビット、デュアル電源のバッファ付き電圧信号コンバータ

1 特長

- 1.65V～3.6V の昇圧および降圧変換
- AEC-Q100 車載認証済み
- 動作温度グレード 1：–40℃～+125℃
- 最大静止電流 (I_{CCA} + I_{CCB})：14μA (最大 125℃)
- 電源電圧の全範囲にわたって最高 100Mbps をサポート
- V_{CC} 絶縁機能
  - いずれかの V_{CC} 入力が 100mV より低下した場合、出力は高インピーダンスに変化
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JEDEC JS-001 を超える ESD 保護
  - 2000V、人体モデル
  - デバイス帯電モデルで 1000V

2 アプリケーション

- MCU / FPGA / プロセッサの GPIO 変換
- 通信モジュールからプロセッサへの変換
- プッシュプル I/O のバッファ

3 概要

AEC-Q100 認定済みの 2N7001T-Q1 デバイスは、互いに独立して構成可能な 2 つの電源レールを使用して、単方向信号を昇圧変換または降圧変換する 1 ビットのバッファ付き電圧信号コンバータです。このデバイスは、V_{CCA} と V_{CCB} 電源の両方が最低 1.65V、最高 3.60V の範囲で動作します。V_{CCA} は、A 入力の入力スレッショルド電圧を定義します。V_{CCB} は、B 出力の出力駆動電圧を定義します。

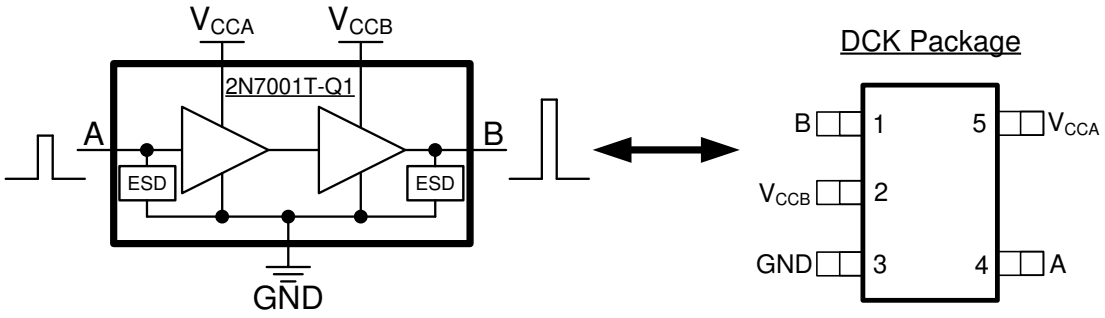
このデバイスは、I_{off} 電流を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off} 保護回路により、電源切断時に入力、出力、複合 I/O は指定の電圧にバイアスされ、それらとの間に過剰な電流が流れることはありません。

V_{CC} 絶縁機能により、V_{CCA} と V_{CCB} のいずれかが 100mV よりも低下した場合、出力ポート (B) は高インピーダンス状態に移行します。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
2N7001TDCKRQ1	SC70 (5)	2.00mm × 1.25mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ブロック図とピン配置

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2020) to Revision A (July 2020)	Page
• デバイス・ステータスを「事前情報」から「量産データ」に変更	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1

5 Pin Configuration and Functions

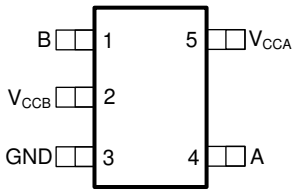


図 5-1. DCK Package 5-Pin SC70 Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DCK		
B	1	O	Data Output. This pin is referenced to V_{CCB}.
V_{CCB}	2	—	Output Supply voltage. 1.65V ≤ V_{CCB} ≤ 3.6 V.
GND	3	—	Ground
A	4	I	Data Input. This pin is referenced to V_{CCA}.
V_{CCA}	5	—	Input Supply voltage. 1.65V ≤ V_{CCA} ≤ 3.6 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		–0.5	4.2	V
V_{CCB}			–0.5	4.2	V
V_I	Input voltage(2)		–0.5	4.2	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.2	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		–0.5	V_{CCB} + 0.2	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current		–50	50	mA
I_{CC}	Continuous output current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2V maximum if the output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		1.65	3.6	V
V_{CCB}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CCA} = 1.65 V - 1.95V	V_{CCA} x 0.65		
		V_{CCA} = 2.30 V - 2.70V	1.6		
		V_{CCA} = 3.00 V - 3.60V	2.0		
V_{IL}	Low-level input voltage	V_{CCA} = 1.65 V - 1.95V		V_{CCA} x 0.35	
		V_{CCA} = 2.30 V - 2.70V		0.7	
		V_{CCA} = 3.00 V - 3.60V		0.8	
V_I	Input voltage		0	3.6	V
V_O	Output voltage	Active State	0	V_{CCB}	V
		Tri-State	0	3.6	
Δt/Δv	Input transition rise and fall rate			100	ns/V
T_A	Operating free-air temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		2N7001T-Q1 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	253.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	162.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	140.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	69.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	139.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		VCCA	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OH}	High Level Output Voltage	$V_I = V_{IH}$	I_{OH} = -100 µA	1.65 V - 3.6 V	1.65 V - 3.6 V	V_{CCB}-0.1			V
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			
			I_{OH} = -9 mA	2.30 V	2.30 V	1.75			
			I_{OH} = -12 mA	3.00 V	3.00 V	2.3			
V_{OL}	Low Level Output Voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	1.65 V - 3.6 V	1.65 V - 3.6 V			0.1	V
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45	
			I_{OL} = 9 mA	2.30 V	2.30 V			0.55	
			I_{OL} = 12 mA	3.00 V	3.00 V			0.7	
I_{off}	Partial power down current	V_I or V_O = 0 V - 3.6 V		0 V	0 V - 3.6 V	–8		8	µA
		V_I or V_O = 0 V - 3.6 V		0 V - 3.6 V	0 V	–8		8	
I_{CCA}	V_{CCA} Supply Current	$V_I = V_{CCA}$ or GND; I_o = 0 mA		1.65 V - 3.6 V	1.65 V - 3.6 V			8	µA
				0 V	3.60 V	–8			
				3.60 V	0 V			8	
I_{CCB}	V_{CCB} Supply Current	$V_I = V_{CCA}$ or GND; I_o = 0 mA		1.65 V - 3.6 V	1.65 V - 3.6 V			8	µA
				0 V	3.60 V			8	
				3.60 V	0 V	–8			
I_{CCA} + I_{CCB}	Combined Supply Current	$V_I = V_{CCA}$ or GND; I_o = 0 mA		1.65 V - 3.6 V	1.65 V - 3.6 V			14	µA
C_I	Input Capacitance	V_I = 1.65V DC + 1 MHz, -16 dBm sine wave		3.30V	0V		2		pF
C_O	Output Capacitance	V_O = 1.65V DC + 1 MHz, -16 dBm sine wave		0V	3.30V		4		pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VCCA	VCCB	MIN	MAX	UNIT
t_{pd}	Propagation delay	1.65 V - 1.95 V	1.65 V - 1.95 V	0.5	20	ns
			2.30 V - 2.70 V	0.5	17	ns
			3.00 V - 3.60 V	0.5	14	ns
		2.30 V - 2.70 V	1.65 V - 1.95 V	0.5	18	ns
			2.30 V - 2.70 V	0.5	15	ns
			3.00 V - 3.60 V	0.5	12	ns
		3.00 V - 3.60 V	1.65 V - 1.95 V	0.5	16	ns
			2.30 V - 2.70 V	0.5	13	ns
			3.00 V - 3.60 V	0.5	10	ns

6.7 Operating Characteritics: T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance - Port A	I_O = 0 mA, C_L = 0 pF, f = 1 MHz $t_r = t_f$ = 1 ns	$V_{CCA} = V_{CCB}$ = 1.8 V		1		pF
			$V_{CCA} = V_{CCB}$ = 2.5 V		1.3		
			$V_{CCA} = V_{CCB}$ = 3.3 V		1.8		

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdB}	Power Dissipation Capacitance - Port B	I_O = 0 mA, C_L = 0 pF, f = 1 MHz $t_r = t_f$ = 1 ns	$V_{CCA} = V_{CCB}$ = 1.8 V		12		pF
			$V_{CCA} = V_{CCB}$ = 2.5 V		15		
			$V_{CCA} = V_{CCB}$ = 3.3 V		18		

6.8 Typical Characteristics

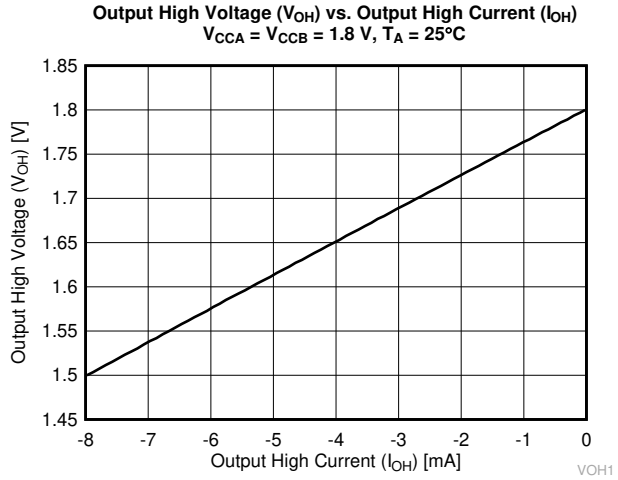


図 6-1. V_{OH} vs I_{OH}, 1.8 V

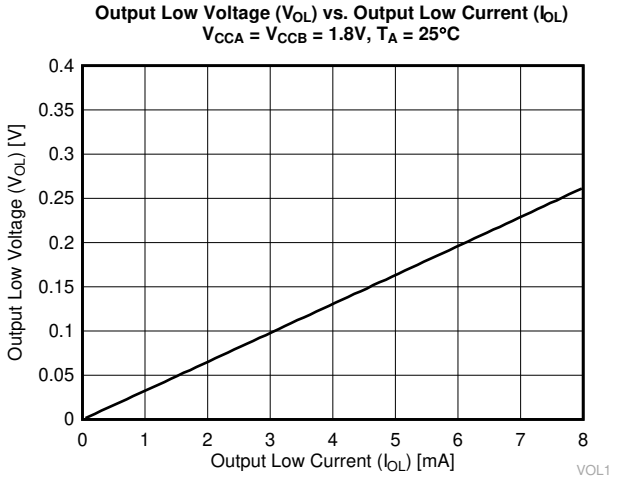


図 6-2. V_{OL} vs I_{OL}, 1.8 V

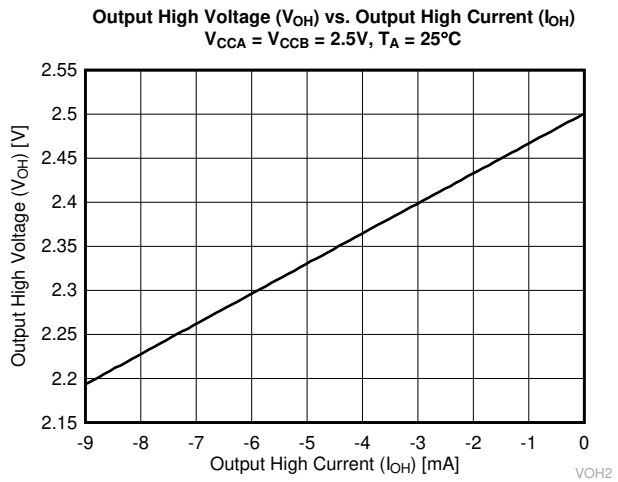


図 6-3. V_{OH} vs I_{OH}, 2.5 V

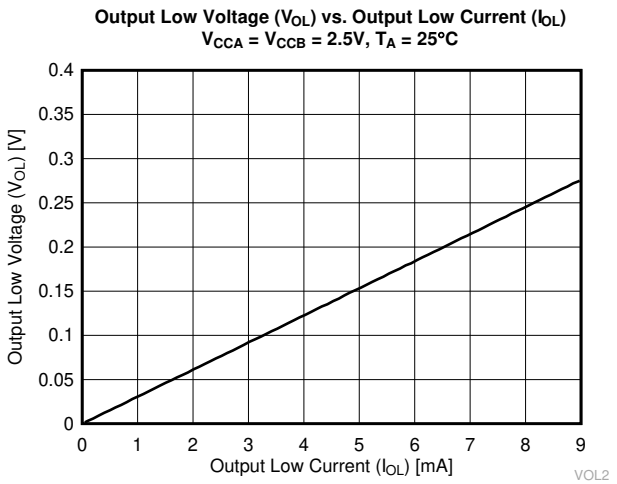


図 6-4. V_{OL} vs I_{OL}, 2.5 V

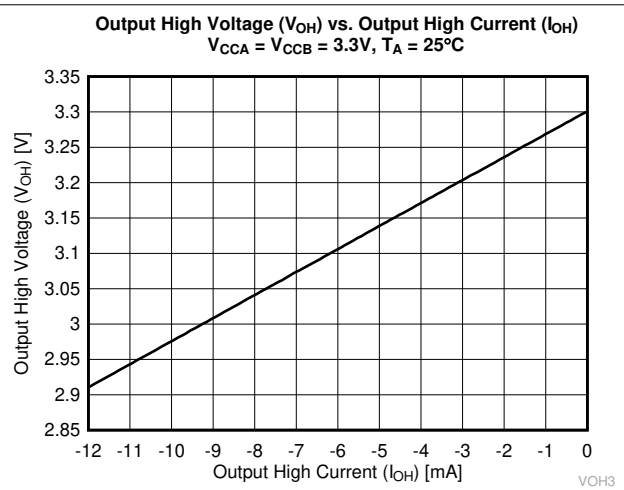


図 6-5. V_{OH} vs I_{OH}, 3.3 V

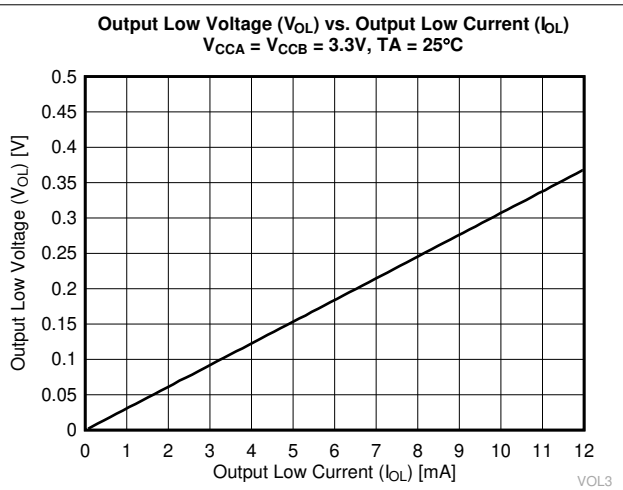


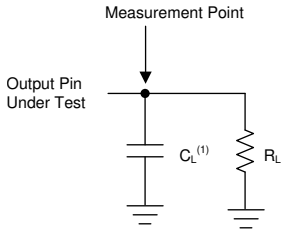
図 6-6. V_{OL} vs I_{OL}, 3.3 V

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- dv/dt ≤ 1 ns/V

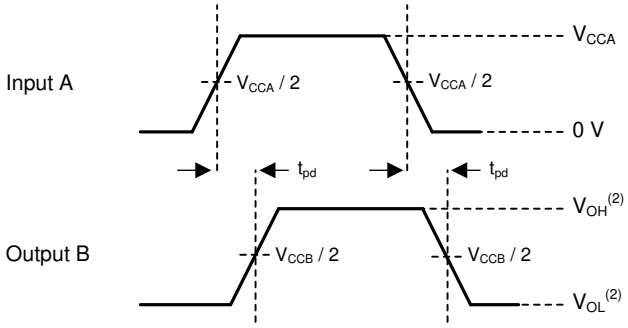


A. C_L includes probe and jig capacitance.

図 7-1. Load Circuit

表 7-1. Load Circuit Conditions

Parameter		V_{CC}	R_L	C_L
t_{pd}	Propagation (delay) time	1.65 V – 3.6 V	2 kΩ	15 pF



A. V_{CCI} is the supply pin associated with the input port.

B. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L and C_L.

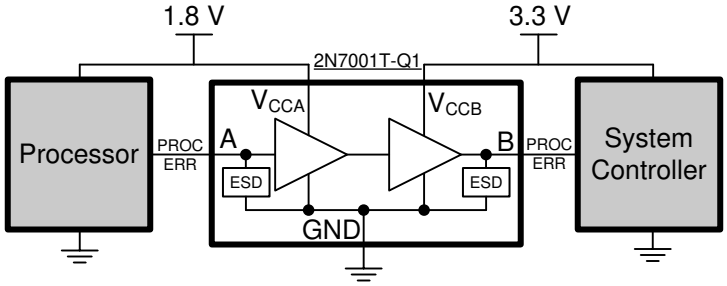
図 7-2. Propagation Delay

8 Detailed Description

8.1 Overview

The 2N7001T-Q1 is an automotive AEC-Q100 qualified single-bit dual-supply buffered voltage signal converter that can be used to up or down-translate a single unidirectional signal. The device is operational with both V_{CCA} and V_{CCB} supplies down to 1.65 V and up to 3.60 V. V_{CCA} defines the input threshold voltage on the A input while V_{CCB} defines the output voltage on the B output.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Up-Translation or Down-Translation from 1.65 V to 3.60 V

The V_{CCA} and V_{CCB} pins can both be supplied by a voltage range from 1.65 V to 3.6 V. This voltage range makes the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, and 3.3 V).

8.3.2 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Raings* must be followed at all times.

8.3.3 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance shown in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, shown in the *Absolute Maximum Ratings*, and the maximum input leakage current, shown in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.4 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in 図 8-1.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

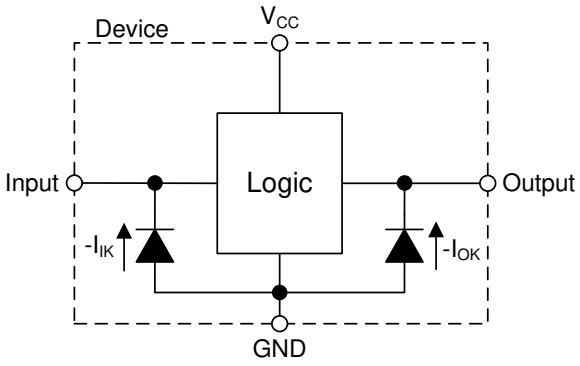


図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.5 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input pin or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.6 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the input supply voltage (V_{CCA}), as long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the 2N7001T-Q1 device.

表 8-1. Function Table

INPUT	OUTPUT
L (Referenced to V_{CCA})	L (Referenced to V_{CCB})
H (Referenced to V_{CCA})	H (Referenced to V_{CCB})

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The 2N7001T-Q1 device can be used in level-translation applications for interfacing between devices or systems that are operating at different interface voltages.

9.2 Typical Applications

9.2.1 Processor Error Up Translation

図 9-1 shows an example of the 2N7001T-Q1 being used in a unidirectional logic level-shifting application.

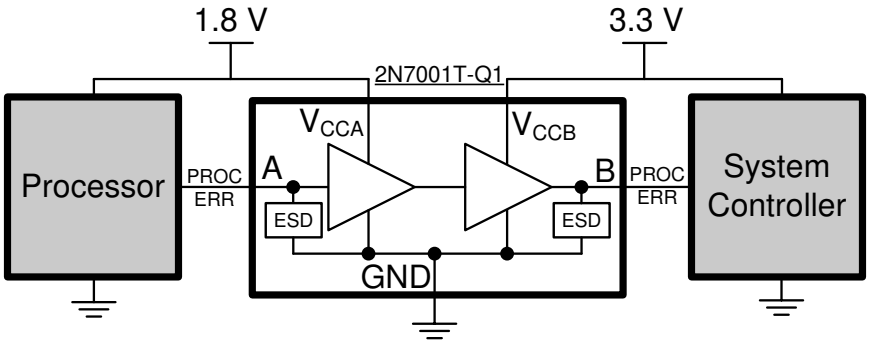


図 9-1. Processor Error Up Translation Application

9.2.1.1 Design Requirements

For this design example, use the parameters shown in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage supply	1.8 V
Output voltage supply	3.3 V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - The supply voltage of the upstream device (device that is driving input pin A) will determine the appropriate input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - The supply voltage of the downstream device (device that output pin B is driving) will determine the appropriate output voltage range.

9.2.1.3 Application Curve

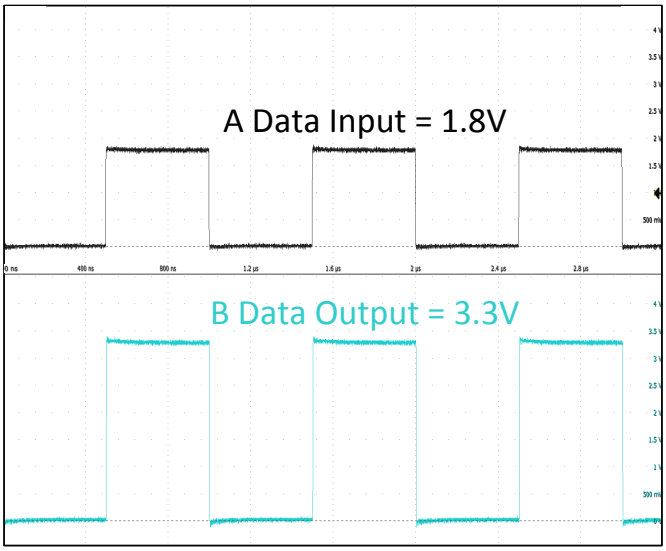


図 9-2. Up Translation (1.8 V to 3.3 V) at 1 MHz

9.2.2 Discrete FET Translation Replacement

The 2N7001T-Q1 device is an excellent option for replacing discrete translators, as shown in 図 9-3, and has the following benefits regarding discrete translation implementations:

- A single device vs a four component solution
- Minimized implementation size
- Lower power consumption
- V_{CC} isolation feature
- Higher data rates
- Integrated ESD protection
- Improved glitch performance

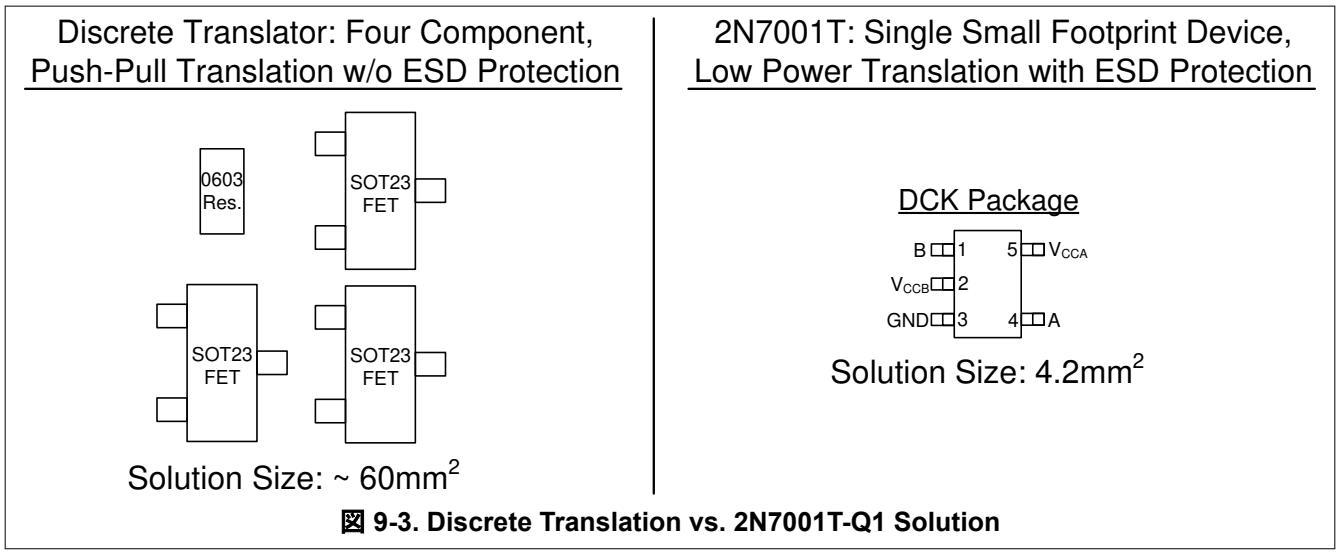


図 9-3. Discrete Translation vs. 2N7001T-Q1 Solution

10 Power Supply Recommendations

The 2N7001T-Q1 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. The V_{CCA} and V_{CCB} power-supply rails accept any supply voltage that range from 1.65 V to 3.6 V. The A input and B output are referenced to V_{CCA} and V_{CCB} respectively allowing up or down translation among the 1.8-V, 2.5-V, and 3.3-V voltage nodes. A 0.1 µF bypass capacitor is recommended on all V_{CC} pins.

Always apply a ground reference to the GND pin first. However, there are no additional requirement for power supply sequencing.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 µF capacitor is recommended, but transient performance can be improved by having both 1 µF and 0.1 µF capacitors in parallel as bypass capacitors.
- Use short trace lengths to avoid excessive loading.

11.2 Layout Example

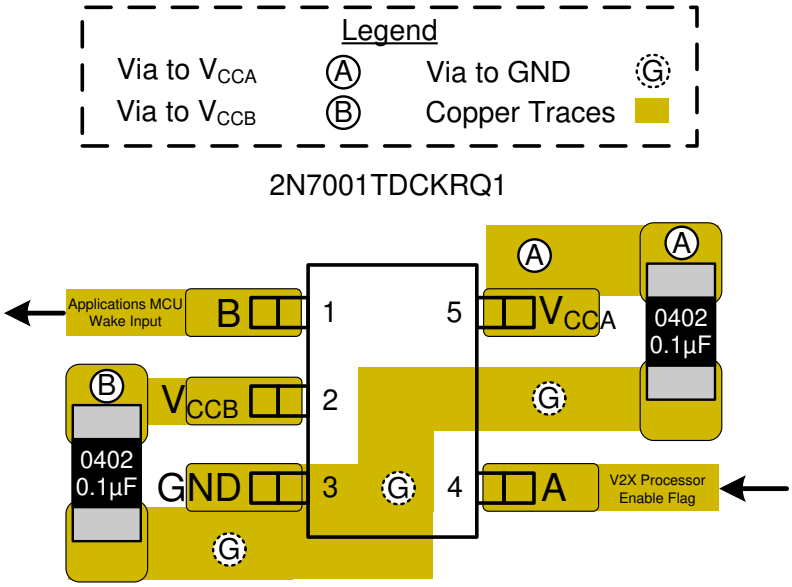


図 11-1. DCK Package Example Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Common Risks with FET Translation and Advantages of 2N7001T application report
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application report
- Texas Instruments, Designing and Manufacturing with TI's X2SON Packages application report

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報の 1 週間分のダイジェストを受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、検証済みの迅速な回答と設計支援をエンジニアがエキスパートから直接得るための頼れる情報源です。既存の回答を検索し、または新たに質問することで、必要とする設計支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
2N7001TQDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	W9	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

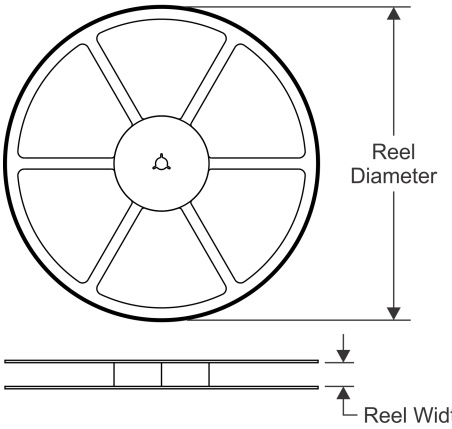
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

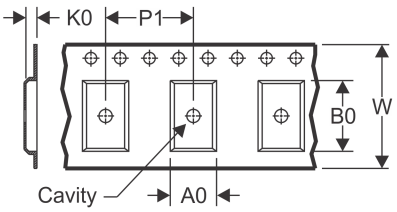
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

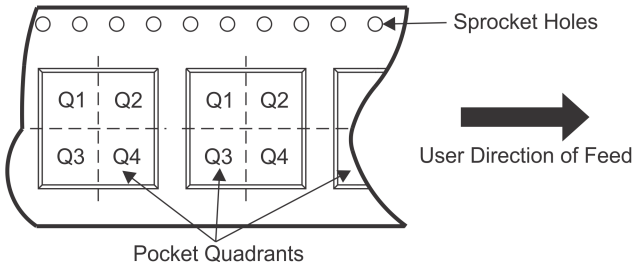


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

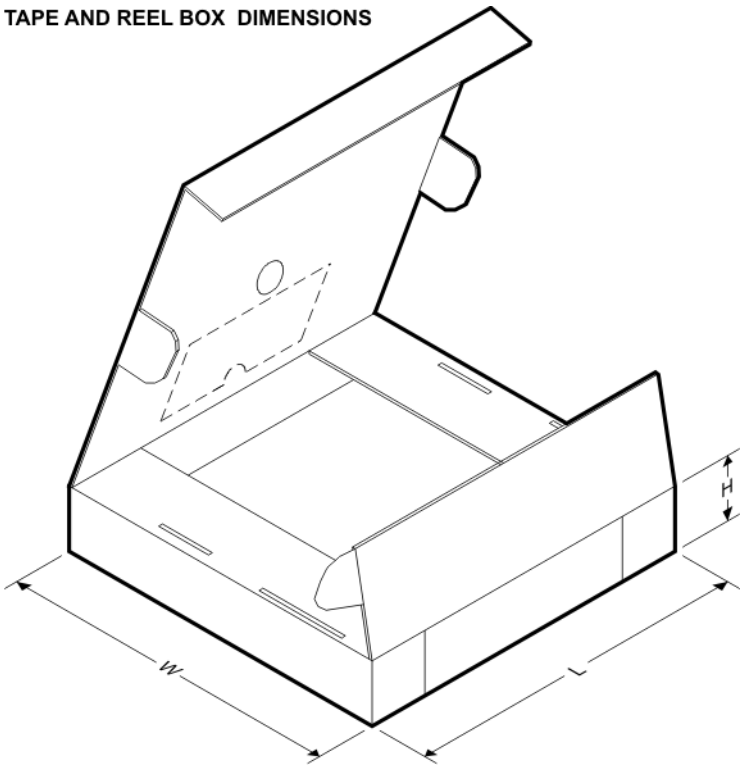
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
2N7001TQDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

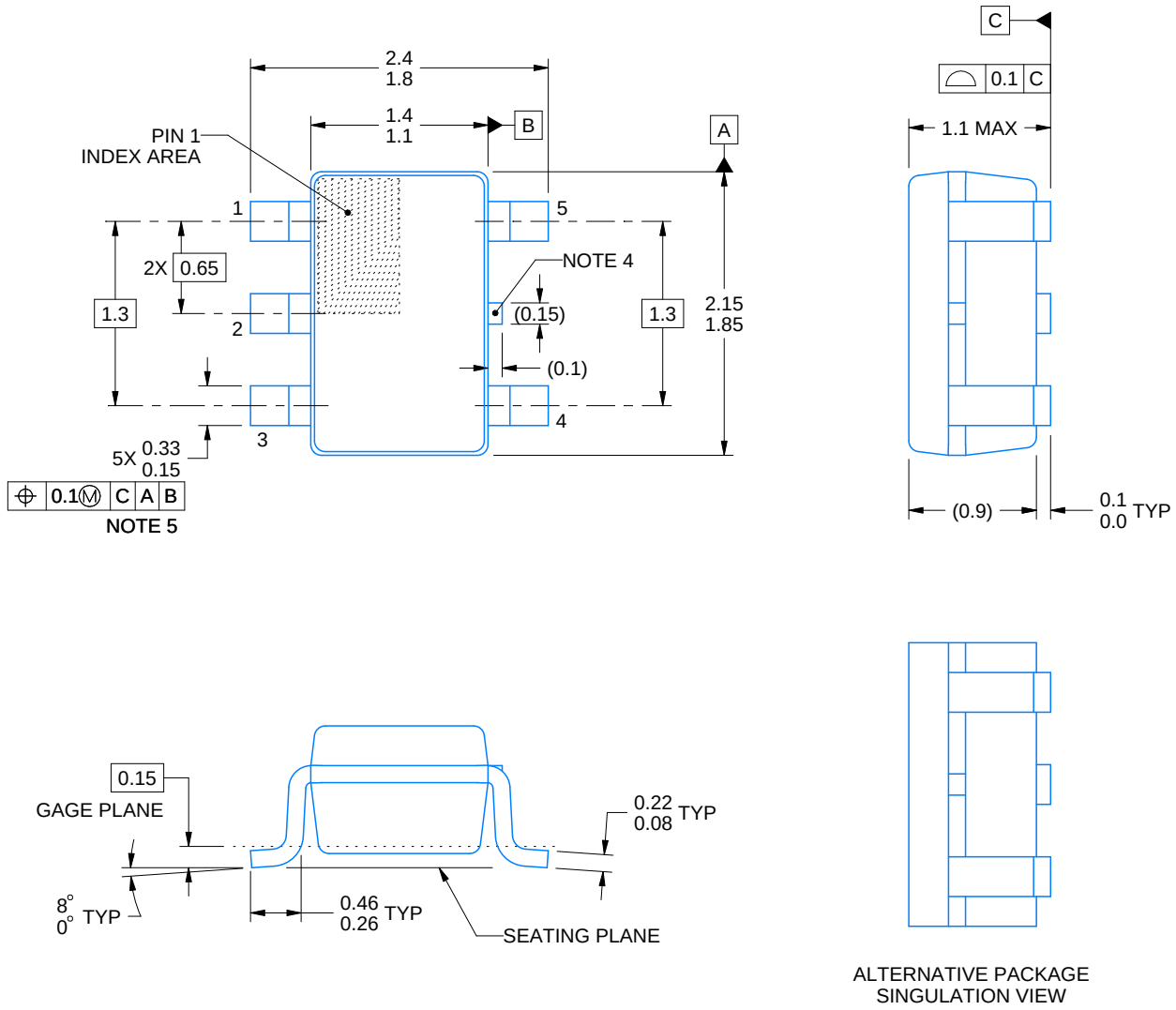
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
2N7001TQDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

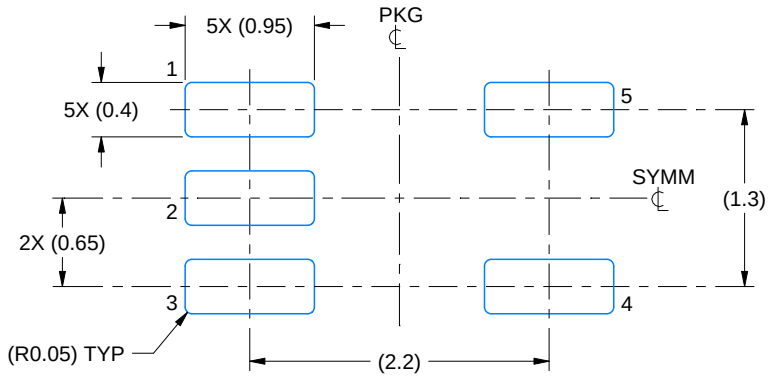
SMALL OUTLINE TRANSISTOR



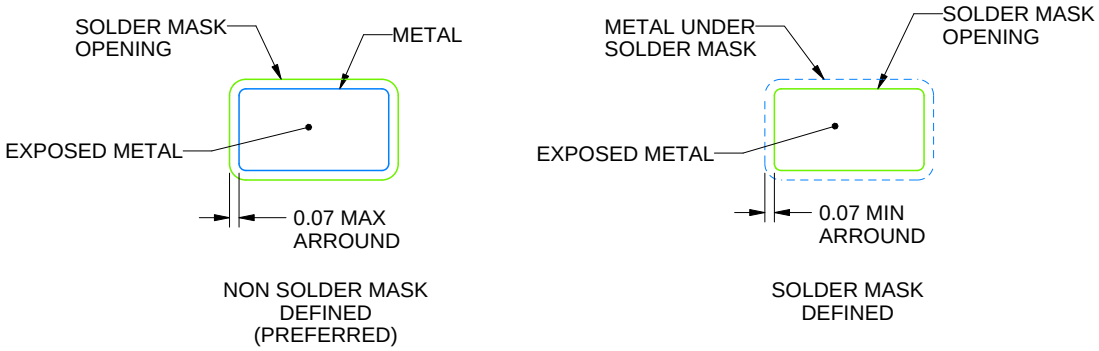
4214834/E 06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

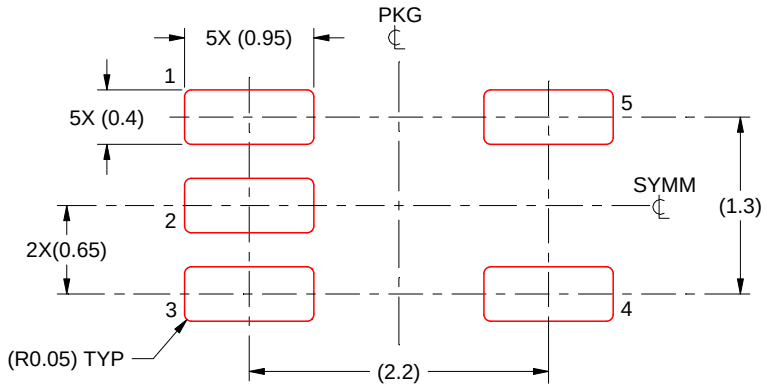


SOLDER MASK DETAILS

4214834/E 06/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/E 06/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265