TEXAS INSTRUMENTS
AM26LS32AC, AM26LS32AI, AM26LS32AM
AM26LS33AC, AM26LS33AM
JAJSQX4G – OCTOBER 1980 – REVISED AUGUST 2023

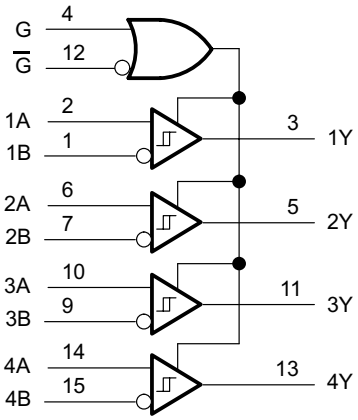
AM26LS32Ax、AM26LS33Ax クワッド差動ライン・レシーバ

1 特長

- AM26LS32A デバイスは、ANSI TIA/EIA-422-B、TIA/EIA-423-B、ITU 勧告 V.10 および V.11 の要件を満たす、または上回ります
- AM26LS32A デバイスは同相範囲が ±7V で、感度が ±200mV です
- AM26LS33A デバイスは同相範囲が ±15V で、感度が ± 500mV です
- 入力ヒステリシス:50mV (標準値)
- 単一の 5V 電源で動作
- 低消費電力ショットキー回路
- 3 ステート出力
- 相補出力のイネーブル入力
- 入力インピーダンス:12kΩ (最小値)
- オープン入力フェイルセーフ

2 アプリケーション

- 高信頼性車載用アプリケーション
- ファクトリ・オートメーション
- ATM およびキャッシュ・カウンタ
- スマート・グリッド
- AC およびサーボ・モータ・ドライブ



ピン番号は D、N、NS、PW パッケージのみのものです。

論理図 (正論理)

3 概要

AM26LS32Ax および AM26LS33Ax デバイスは、平衡および不平衡のデジタル・データ転送用のクワッド差動ライン・レシーバです。イネーブル機能は 4 つのレシーバすべてに共通で、アクティブ High またはアクティブ Low の入力から選択できます。3 ステート出力により、バス構成システムに直接接続できます。入力がオープンのとき、フェイルセーフ設計により出力が常に High であることが保証されます。

AM26LS32 や AM26LS33 と比較すると、AM26LS32A と AM26LS33A には感度を向上させるため追加の増幅段が組み込まれています。入力インピーダンスが増加し、その結果、バス・ラインの負荷が減少します。段を追加すると伝搬遅延が長くなりますが、ほとんどのアプリケーションでは交換可能性には影響しません。

AM26LS32AC および AM26LS33AC は 0℃～70℃での動作が規定されています。AM26LS32AI は -40℃～85℃での動作が規定されています。AM26LS32AM および AM26LS33AM は防衛用温度範囲 –55℃～125℃での動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
AM26LS3xAC AM26LS32AI	PDIP (16)	19.3mm × 9.4mm
	SOIC (16)	9.9mm × 6mm
AM26LS32AC	SO (16)	10.2mm × 7.8mm
	TSSOP (16)	5mm × 6.4mm
AM26LS3xAM	CDIP (16)	19.56mm × 6.92mm
	LCCC (20)	8.9mm × 8.9mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (August 2016) to Revision G (August 2023) — **Page**

- 「製品情報」表を「パッケージ情報」表に変更 ... 1
- Changed the *Thermal Information* table ... 5
- Changed the *Typical Characteristics* ... 8

Changes from Revision E (October 2007) to Revision F (August 2016) — **Page**

- 「アプリケーション」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1
- Changed $R_{\theta JA}$ values in the *Thermal Information* table: 73 to 75.7 for (D), 67 to 45.3 (N), 64 to 75.8 (NS), and 108 to 102.7 (PW) ... 5

5 Pin Configuration and Functions

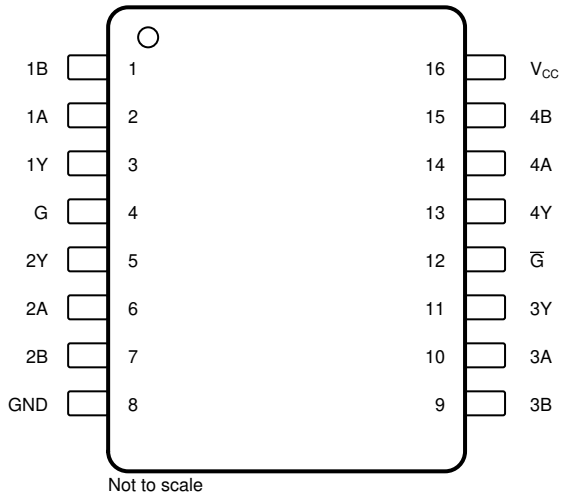
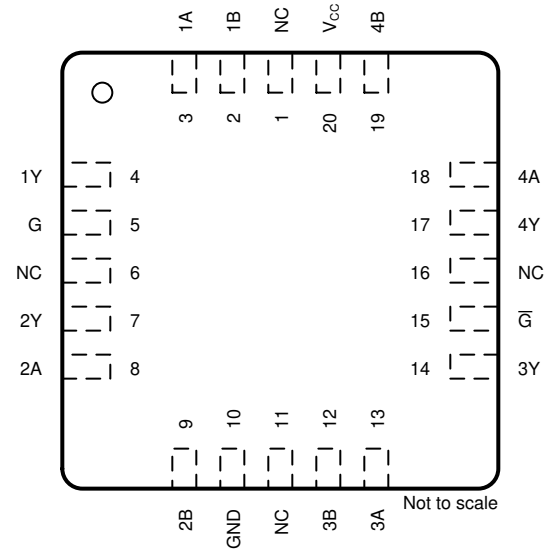


図 5-1. D, J, N, NS, and PW Package 16-Pin SOIC, CDIP, PDIP, SO, and TSSOP (Top View)



NC - No internal connection

図 5-2. FK Package, 20-Pin LCCC (Top View)

PIN			TYPE	DESCRIPTION
NAME	SOIC, CDIP, PDIP, SO, TSSOP	LCCC		
1A	2	3	I	RS422/RS485 differential input (noninverting)
1B	1	2	I	RS422/RS485 differential input (inverting)
1Y	3	4	O	Logic level output
2A	6	8	I	RS422/RS485 differential input (noninverting)
2B	7	9	I	RS422/RS485 differential input (inverting)
2Y	5	7	O	Logic level output
3A	10	13	I	RS422/RS485 differential input (noninverting)
3B	9	12	I	RS422/RS485 differential input (inverting)
3Y	11	14	O	Logic level output
4A	14	18	I	RS422/RS485 differential input (noninverting)
4B	15	19	I	RS422/RS485 differential input (inverting)
4Y	13	17	O	Logic level output
$\overline{G}$	12	15	I	Active-Low select
G	4	5	I	Active-High select
GND	8	10	—	Ground
NC	—	1, 6, 11, 16	—	No internal connection
V_{CC}	16	20	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (2)			7	V
Input voltage, V_I	Any differential input		±25	V
	Other inputs		7	
Differential input voltage, V_{ID} (3)			±25	V
Continuous total power dissipation			See セクション 6.7	
Case temperature, T_C, FK package (60 s)			260	°C
Lead temperature(4)	D or N package (10 s)		260	°C
	J package (60 s)		300	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground terminal.
(3) Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.
(4) 1.6 mm (1/16 inch) from case

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	AM26LS32AC, AM26LS32AI, AM26LS33AC	4.75	5	5.25	V
		AM26LS32AM, AM26LS33AM	4.5	5	5.5	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Common-mode input voltage	AM26LS32A			±7	V
		AM26LS33A			±15	
I_{OH}	High-level output current				–440	µA
I_{OL}	Low-level output current				8	mA
T_A	Operating free-air temperature	AM26LS32AC, AM26LS33AC	0		70	°C
		AM26LS32AI	–40		85	
		AM26LS32AM, AM26LS33AM	–55		125	

6.4 Thermal Information

THERMAL METRIC[1]		AM26LS3xAC, AM26LS32AI				AM26LS32AC				UNIT
		D (SOIC)	DR (SOIC-Reel)	N (PDIP)	NR (PDIP-Reel)	NS (SO)	NSR (SO-Reel)	PW (TSSOP)	PWR (TSSOP-Reel)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.7	84.6	45.3	60.6	75.8	88.5	102.7	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35	43.5	32.7	48.1	32.9	46.2	37.8	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	43.2	25.3	40.6	36.6	50.7	47.7	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	10.4	17.8	27.5	6	13.5	3	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	42.8	25.1	40.3	36.3	50.3	47.1	53.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = V_{OH}min, I_{OH} = –440 µA	AM26LS32A			0.2	V
			AM26LS33A			0.5	
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.45 V , I_{OL} = 8 mA	AM26LS32A	–0.2(2)			V
			AM26LS33A	–0.5(2)			
V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)				50		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN, I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{ID} = 1 V, $V_{I(G)}$ = 0.8 V, I_{OH} = –440 µA	AM26LS32AC, AM26LS33AC	2.7			V
			AM26LS32AM, AM26LS32AI, AM26LS33AM	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = –1 V, $V_{I(G)}$ = 0.8 V	I_{OL}= 4 mA			0.4	V
			I_{OL}= 8 mA			0.45	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = MAX	V_O = 2.4 V			20	µA
			V_O = 0.4 V			–20	
I_I	Line input current	V_I = 15 V, other input at –10 V to 15 V				1.2	mA
		V_I = –15 V, other input at –15 V to 10 V				–1.7	
$I_{I(EN)}$	Enable input current	V_I = 5.5 V				100	µA
I_H	High-level enable current	V_I = 2.7 V				20	µA
I_L	Low-level enable current	V_I = 0.4 V				–0.36	mA
r_i	Input resistance	V_{IC} = –15 V to 15 V, one input to ac ground		12	15		kΩ
I_{OS}	Short-circuit output current(3)	V_{CC} = MAX		–15		–85	mA
I_{CC}	Supply current	V_{CC} = MAX, all outputs disabled			52	70	mA

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
(3) Not more than one output must be shorted to ground at a time, and duration of the short circuit must not exceed one second.

6.6 Switching Characteristics

C_L = 15 pF, V_{CC} = 5 V, and T_A = 25°C (see セクション 7; unless otherwise noted)

PARAMETER		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output		22	35	ns
t_{PZH}	Output enable time to high level		17	22	ns
t_{PZL}	Output enable time to low level		20	25	ns
t_{PHZ}	Output disable time from high level		21	30	ns
t_{PLZ}	Output disable time from low level		30	40	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

6.7 Dissipation Ratings

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATION FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
FK	1375 mW	11 mW/°C	880 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	275 mW

6.8 Typical Characteristics

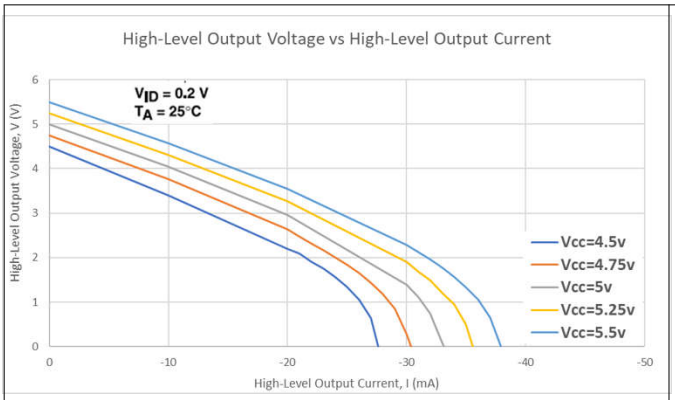


図 6-1. High-Level Output Voltage vs High-Level Output Current

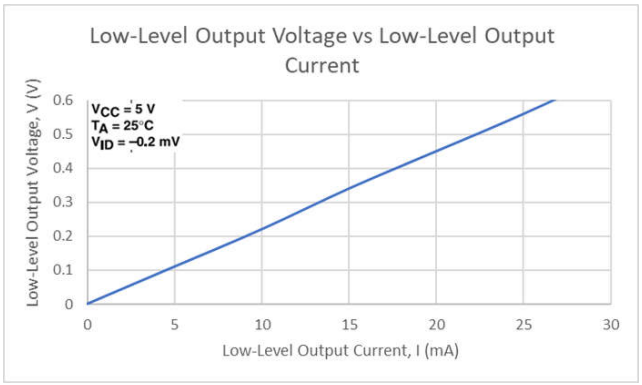


図 6-2. Low-Level Output Voltage vs Low-Level Output Current

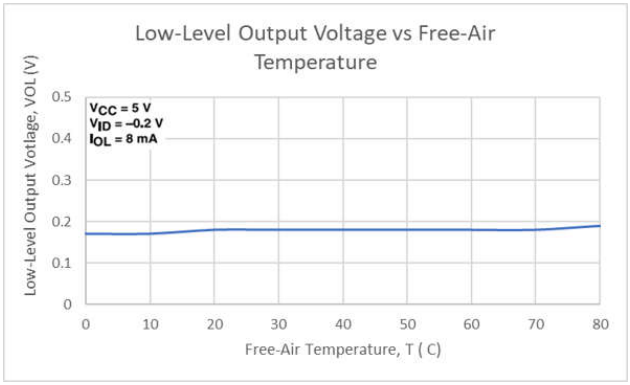


図 6-3. Low-Level Output Voltage vs Free-Air Temperature

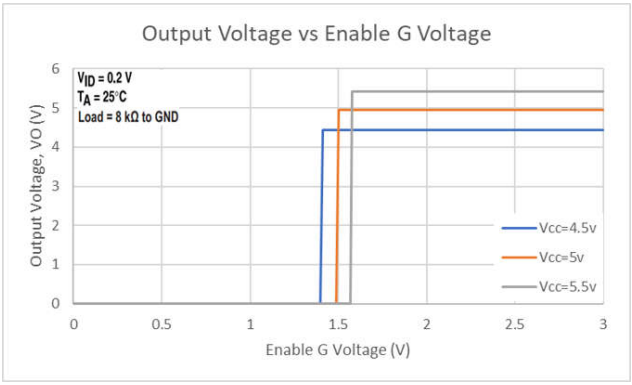


図 6-4. Output Voltage vs Enable G Voltage

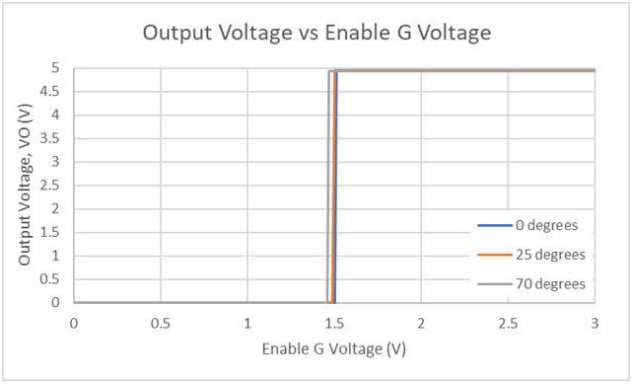


図 6-5. Output Voltage vs Enable G Voltage

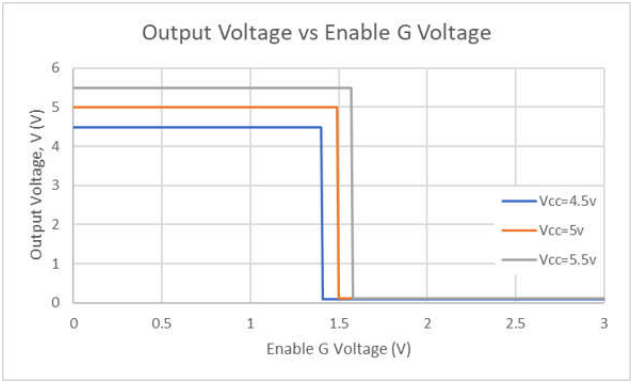


図 6-6. Output Voltage vs Enable G Voltage

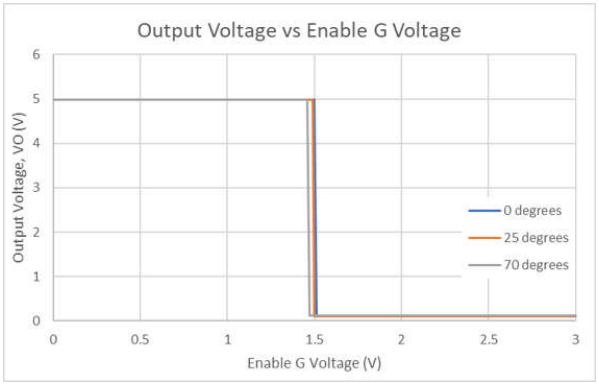


図 6-7. Output Voltage vs Enable G Voltage

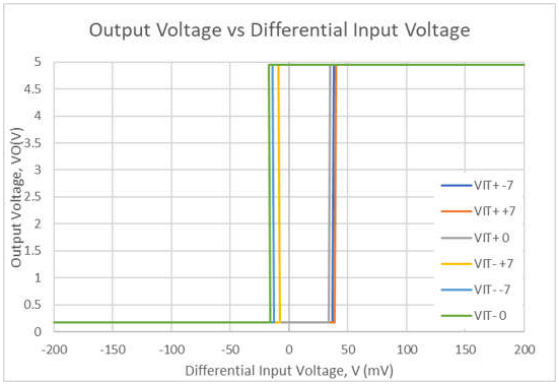


図 6-8. AM26LS32A Output Voltage vs Differential Input Voltage

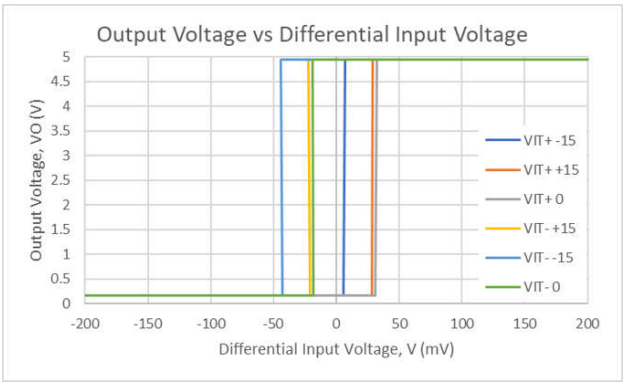
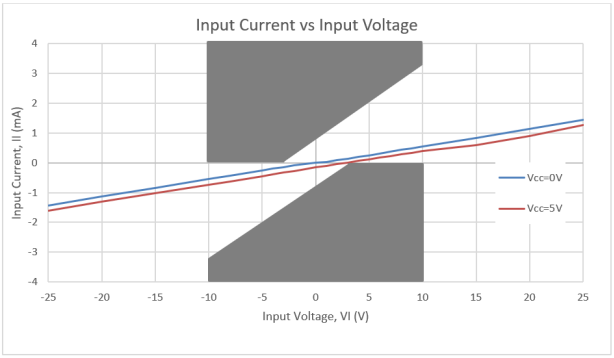


図 6-9. AM26LS33A Output Voltage vs Differential Input Voltage



The unshaded area shows requirements of paragraph 4.2.1 of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B.

図 6-10. Input Current vs Input Voltage

7 Parameter Measurement Information

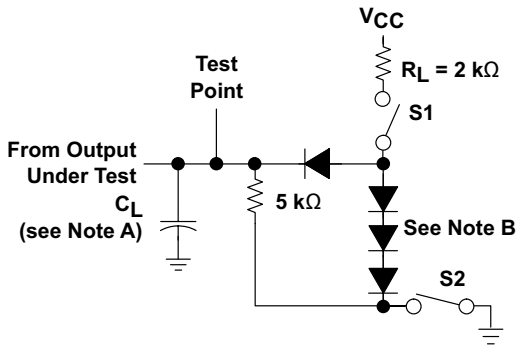


図 7-1. Test Circuit

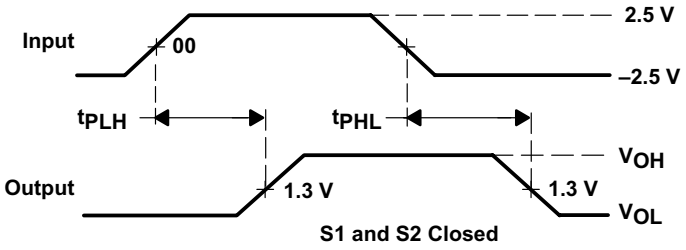


図 7-2. Voltage Waveforms For t_{PLH}, t_{PHL}

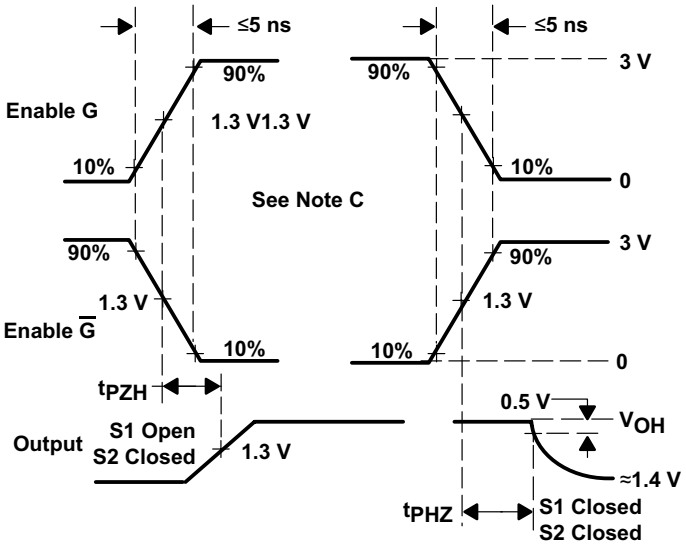
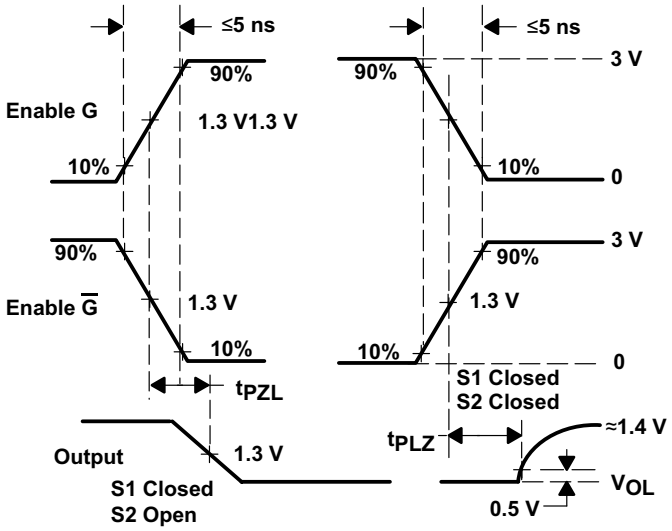


図 7-3. Voltage Waveforms For t_{PHZ}, t_{PZH}



A. CL includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high, $\overline{G}$ is tested with G low.

図 7-4. Voltage Waveforms For t_{PLZ}, t_{PZL}

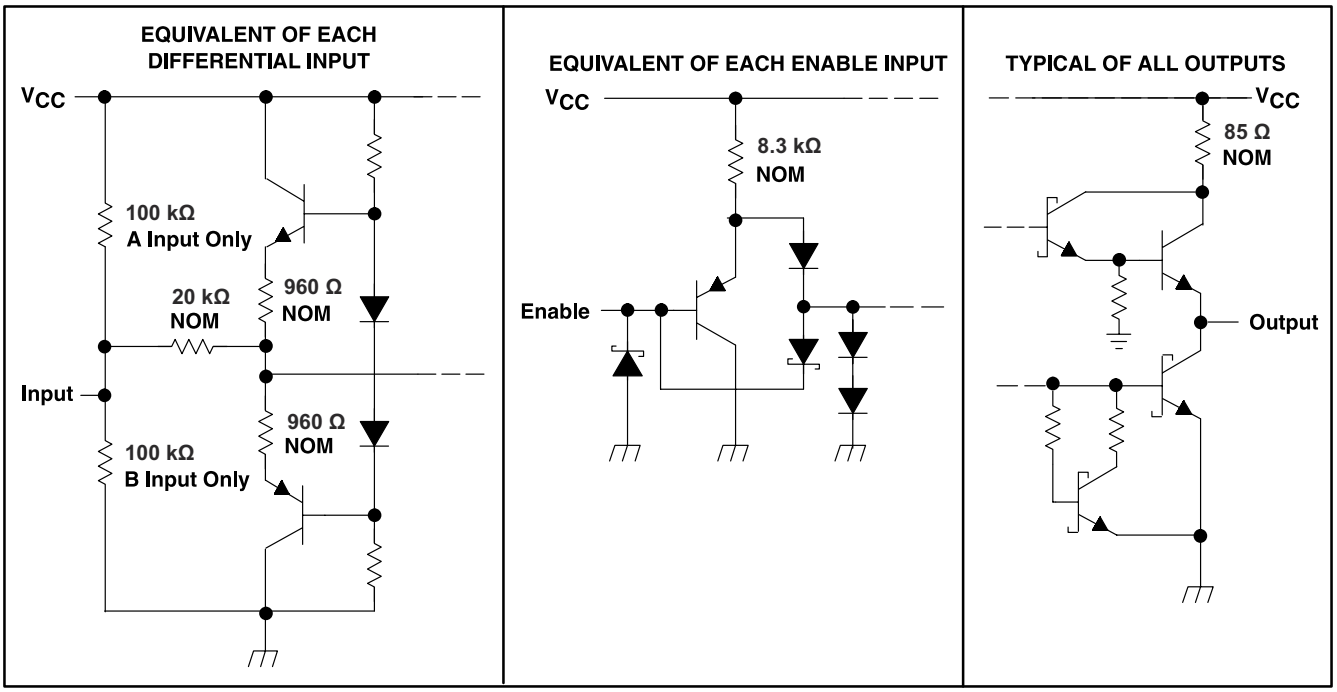


図 7-5. Schematics of Inputs and Outputs

8 Detailed Description

8.1 Overview

The AM26LS32 is a quadruple-differential line receiver that meets the necessary requirements for NSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11. This device allows a low-power or low-voltage MCU to interface with heavy machinery, subsystems, and other devices through long wires of up to 1000 m, giving any design a reliable and easy-to-use connection. As any RS422 interface, the AM26LS32 works in a differential voltage range, which enables very good signal integrity.

8.2 Functional Block Diagram

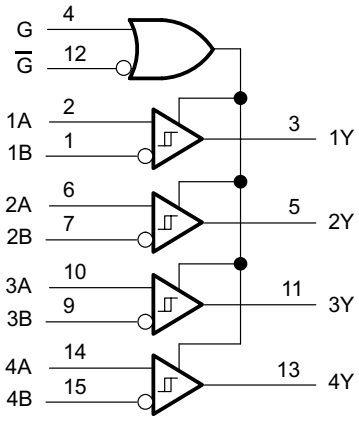


図 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The device can be configured using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin allows the device to operate on an active-high, and having a low voltage or logic 0 on the G enables active low operation. These are simple ways to configure the logic to match that of the receiving or transmitting controller or microprocessor.

8.4 Device Functional Modes

The receivers implemented in these RS422 devices can be configured using the G and $\overline{G}$ logic pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

表 8-1. Function Table, Each Receiver

DIFFERENTIAL A–B	ENABLES(1)		OUTPUT(1) Y
	G	$\overline{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

(1) H = High level, L = Low level, X = Irrelevant, Z = High impedance (off), ? = Indeterminate

9 Application and Implementation

注

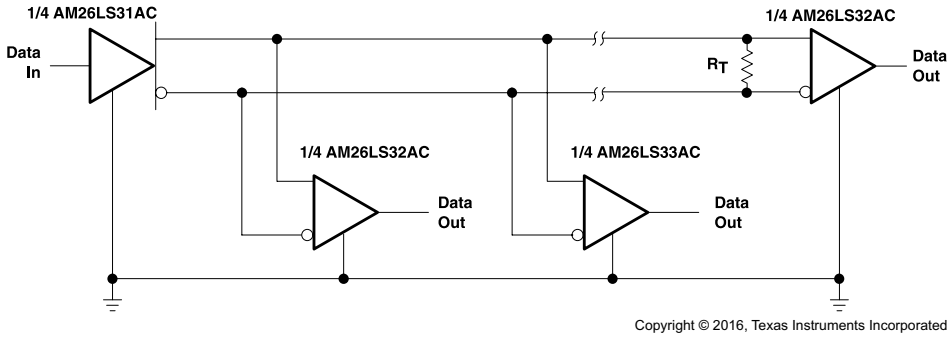
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

When using AM26LS32A as a receiver, the AM26LS31AC can allow multiple AM26LS32As to be used causing an increase in the amount of outputs.

9.2 Typical Application

図 9-1 shows a configuration with no termination. Although reflections are present at the receiver inputs at a data signaling rate of 200 kbps with no termination, the RS-422-compliant receiver reads only the input differential voltage and produces a clean signal at the output.



†R_T equals the characteristic impedance of the line.

図 9-1. Application Diagram

9.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, R_T, must be within 20% of the characteristic impedance, Z_O, of the cable and can vary from about 80 Ω to 120 Ω.

9.2.2 Detailed Design Procedure

Add a V_{CC} bypass capacitor (0.1 µF or more). Either enable (G pin) input can turn on the receivers, so connect the desired enable to a compatible logic line output. The other enable input must be tied to the inactive state supply rail. If the receivers must always be active, then connect both enables to the supply rail such that at least one is set to an active-state rail. V_{CC} must be 5 V within 10% and logic inputs must provide TTL-compatible voltage levels A & B Inputs can lead to an external connector or can be left unconnected. The last receiver on a cable requires termination, either on-board or use as an external resistor. Unused Y outputs can be left unconnected.

9.2.3 Application Curve

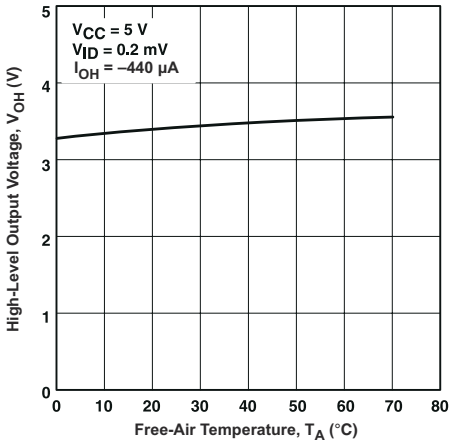


図 9-2. High-Level Output Voltage vs Free-Air Temperature

9.3 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

9.4.2 Layout Example

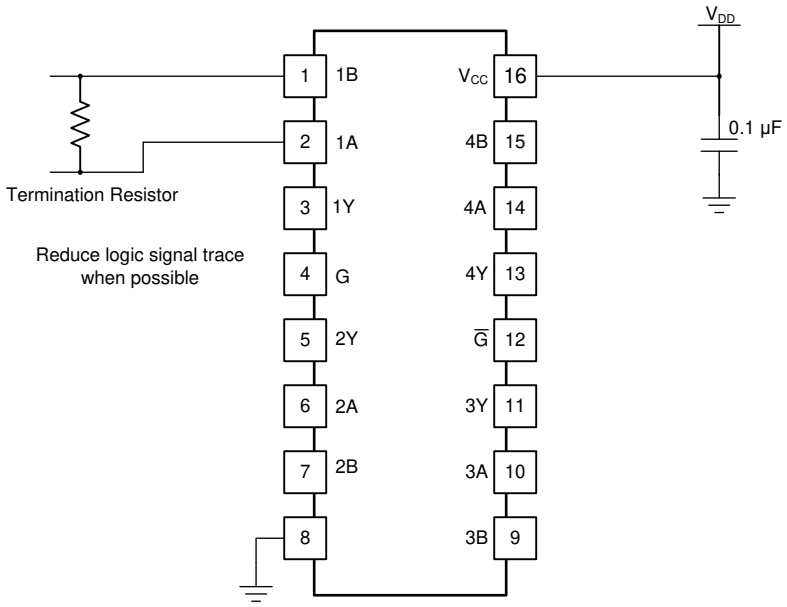


図 9-3. Layout with PCB Recommendations

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7802003M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802003M2A AM26LS 32AMFKB	Samples
5962-7802003MEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802003MEA AM26LS32AMJB	Samples
5962-7802003MFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802003MFA AM26LS32AMWB	Samples
5962-7802004M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802004M2A AM26LS 33AMFKB	Samples
5962-7802004MEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802004MEA AM26LS33AMJB	Samples
5962-7802004MFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802004MFA AM26LS33AMWB	Samples
AM26LS32ACD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	26LS32AC	
AM26LS32ACDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LS32AC	Samples
AM26LS32ACDRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LS32AC	Samples
AM26LS32ACDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LS32AC	Samples
AM26LS32ACN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	AM26LS32ACN	Samples
AM26LS32ACNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LS32A	Samples
AM26LS32ACNSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LS32A	Samples
AM26LS32ACPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	SA32A	
AM26LS32ACPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SA32A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LS32ACPWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SA32A	Samples
AM26LS32AID	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	26LS32AI	
AM26LS32AIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LS32AI	Samples
AM26LS32AIDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LS32AI	Samples
AM26LS32AIN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	AM26LS32AIN	Samples
AM26LS32AMFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802003M2A AM26LS 32AMFKB	Samples
AM26LS32AMJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	AM26LS32AMJ	Samples
AM26LS32AMJB	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802003ME A AM26LS32AMJB	Samples
AM26LS32AMWB	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802003MF A AM26LS32AMWB	Samples
AM26LS33ACD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	26LS33AC	
AM26LS33ACDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LS33AC	Samples
AM26LS33ACN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	AM26LS33ACN	Samples
AM26LS33AMFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802004M2A AM26LS 33AMFKB	Samples
AM26LS33AMJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	AM26LS33AMJ	Samples
AM26LS33AMJB	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802004ME A AM26LS33AMJB	Samples
AM26LS33AMWB	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7802004MF A AM26LS33AMWB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF AM26LS32A, AM26LS32AM, AM26LS33A, AM26LS33AM :

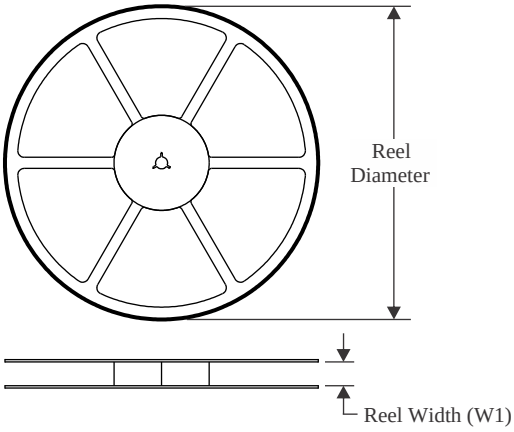
- Catalog : AM26LS32A, AM26LS33A
- Military : AM26LS32AM, AM26LS33AM
- Space : AM26LS33A-SP, AM26LS33A-SP

NOTE: Qualified Version Definitions:

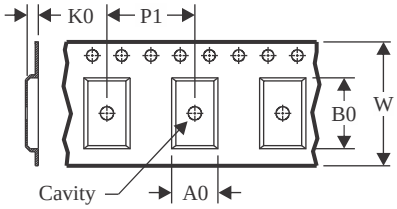
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

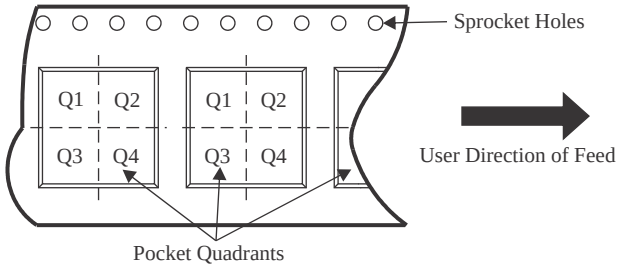


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

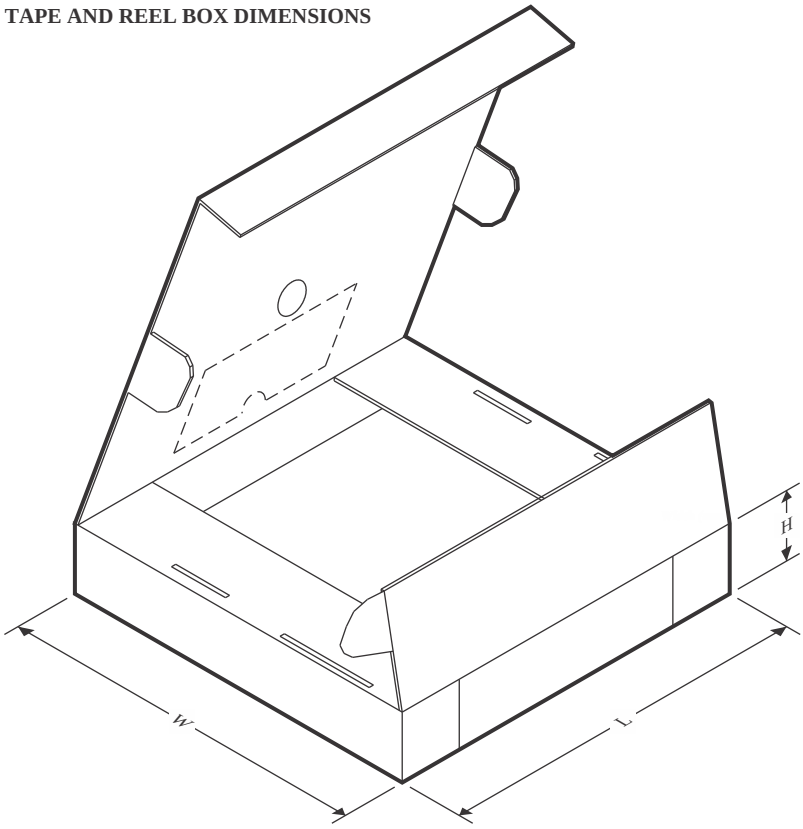
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LS32ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS32ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS32ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS32ACNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LS32ACNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LS32ACPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LS32ACPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LS32AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LS33ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

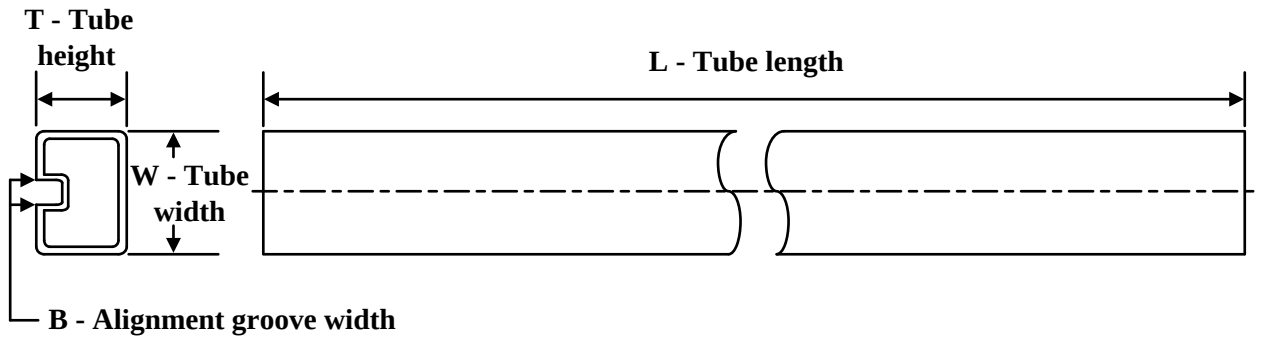
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

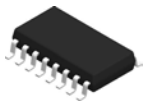
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LS32ACDR	SOIC	D	16	2500	356.0	356.0	35.0
AM26LS32ACDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26LS32ACDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26LS32ACNSR	SO	NS	16	2000	367.0	367.0	38.0
AM26LS32ACNSR	SO	NS	16	2000	353.0	353.0	32.0
AM26LS32ACPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
AM26LS32ACPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26LS32AIDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26LS33ACDR	SOIC	D	16	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-7802003M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-7802003MFA	W	CFP	16	25	506.98	26.16	6220	NA
5962-7802004M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-7802004MFA	W	CFP	16	25	506.98	26.16	6220	NA
AM26LS32ACN	N	PDIP	16	25	506	13.97	11230	4.32
AM26LS32AIN	N	PDIP	16	25	506	13.97	11230	4.32
AM26LS32AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
AM26LS32AMWB	W	CFP	16	25	506.98	26.16	6220	NA
AM26LS33ACN	N	PDIP	16	25	506	13.97	11230	4.32
AM26LS33AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
AM26LS33AMWB	W	CFP	16	25	506.98	26.16	6220	NA

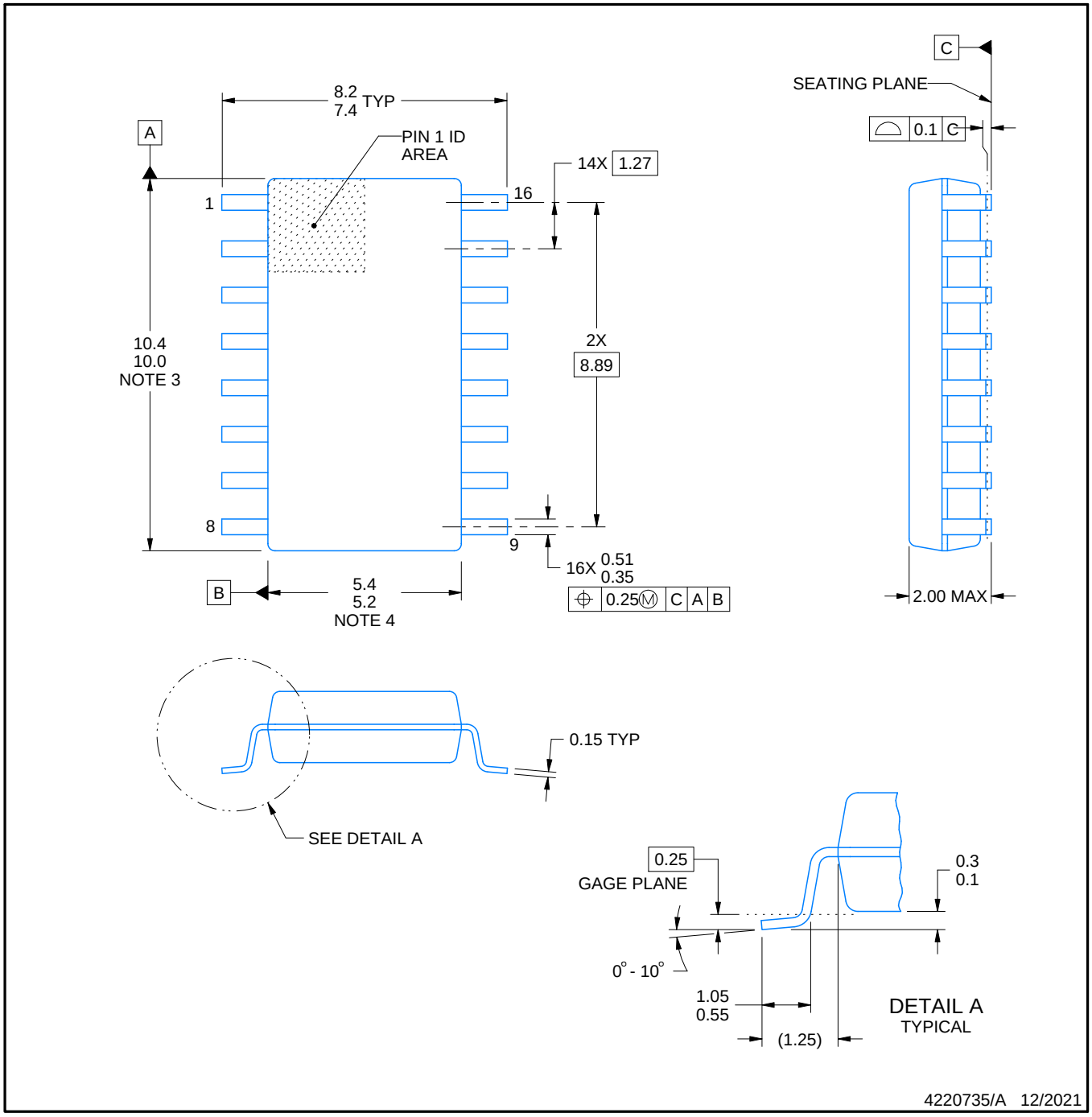


PACKAGE OUTLINE

NS0016A

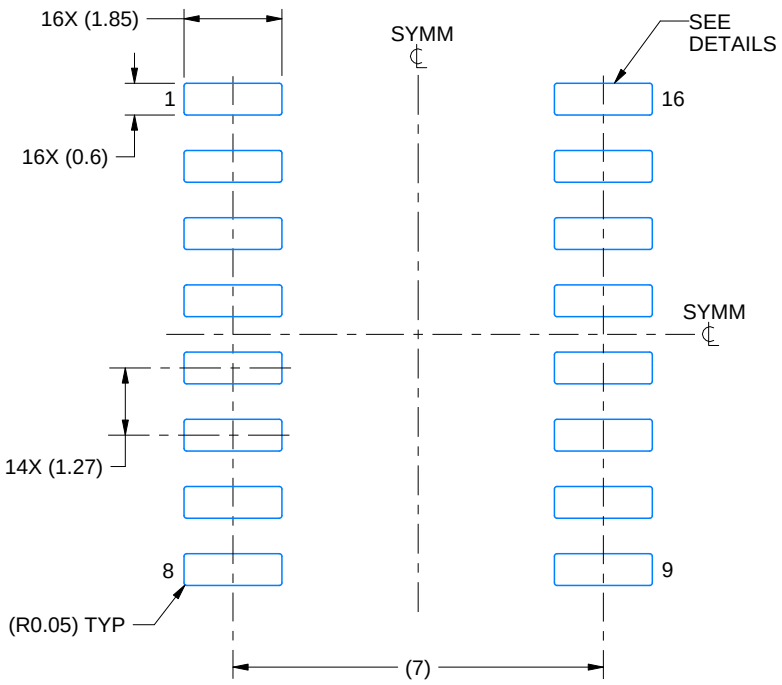
SOP - 2.00 mm max height

SOP

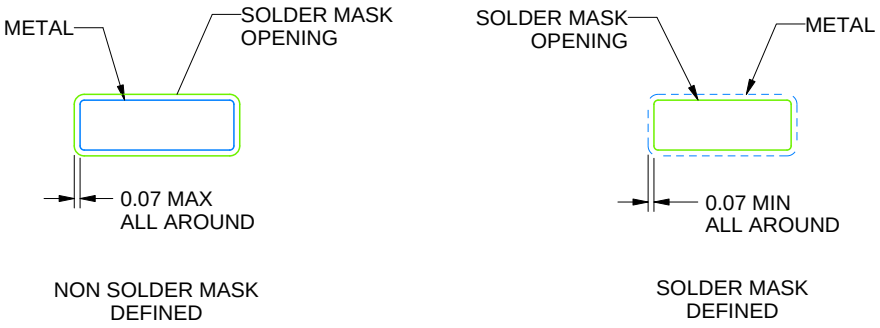


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

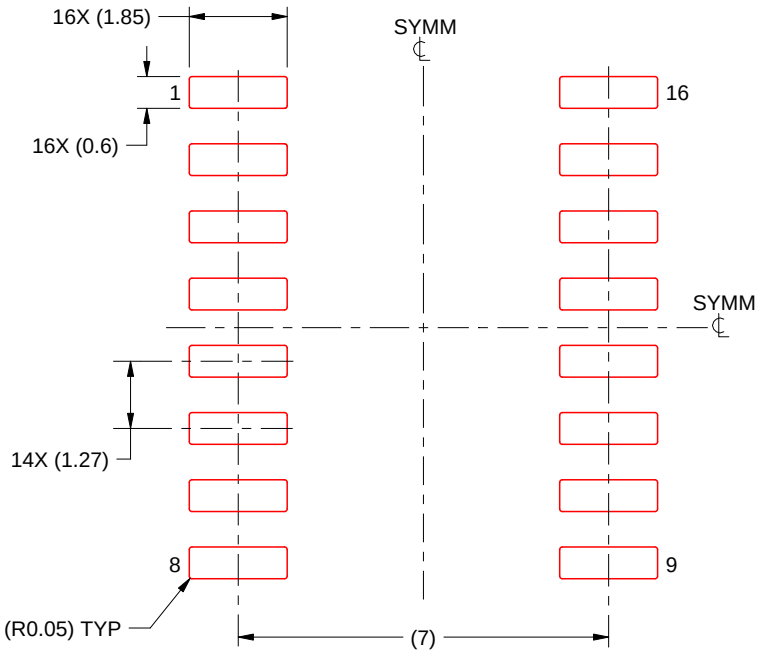
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



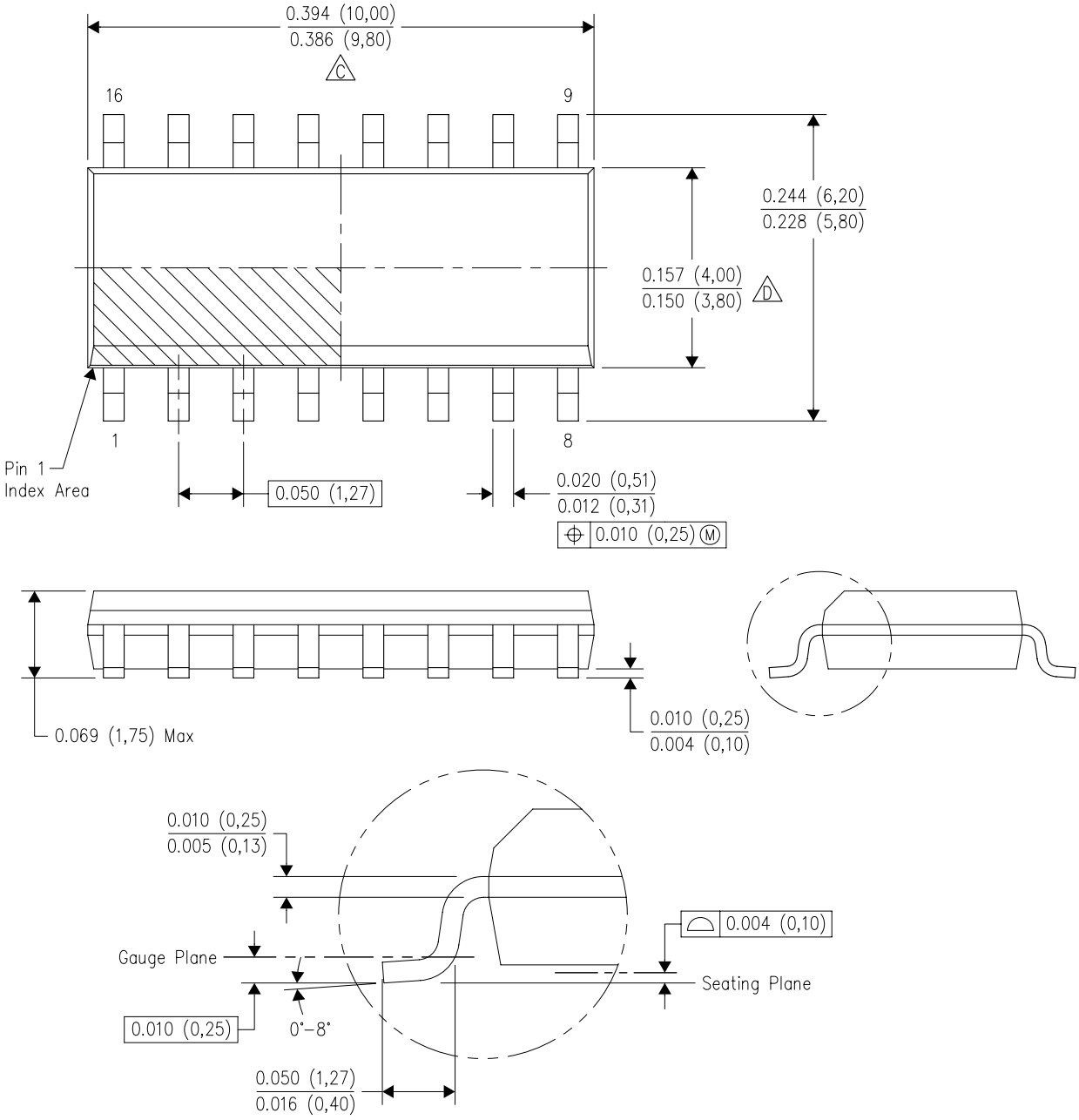
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



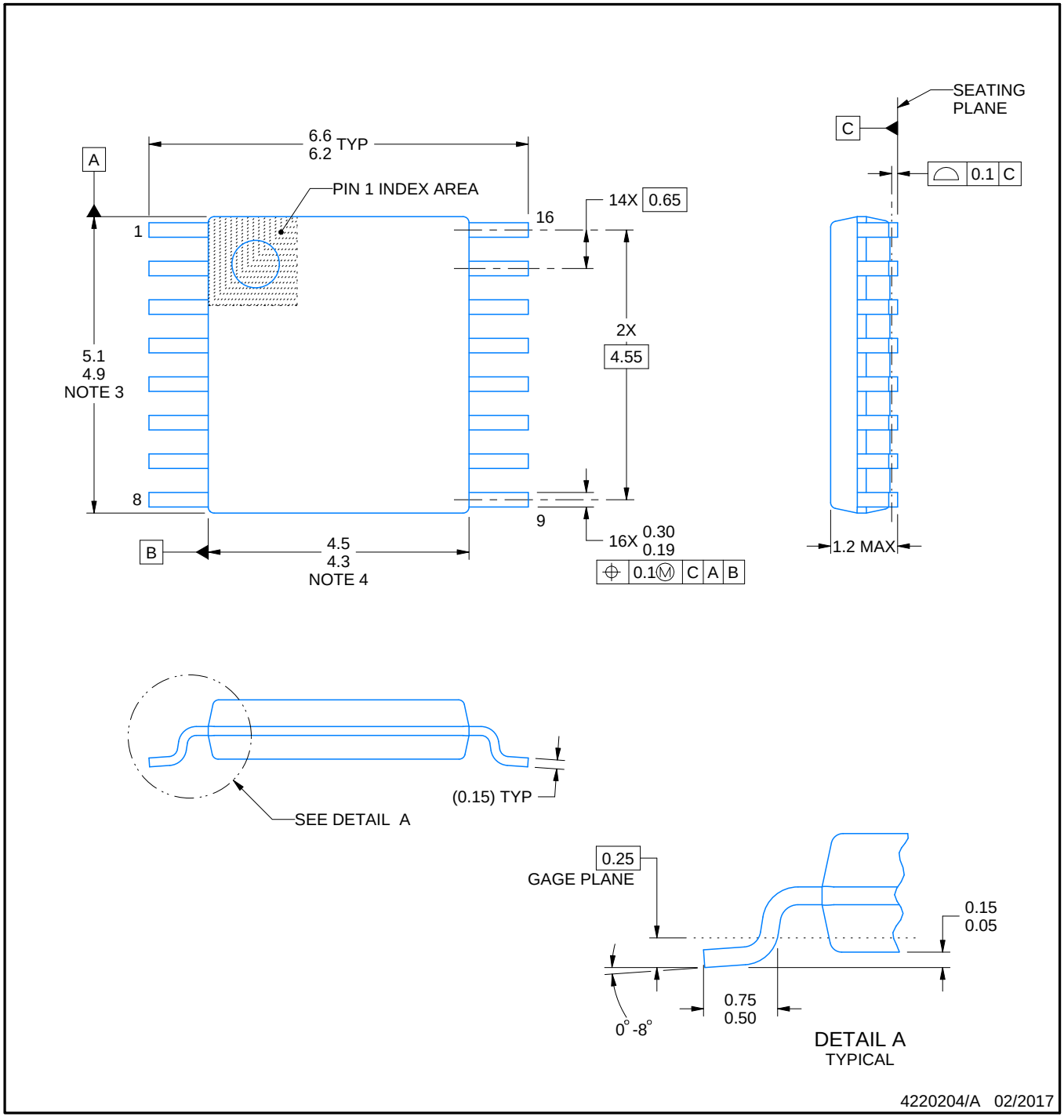
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

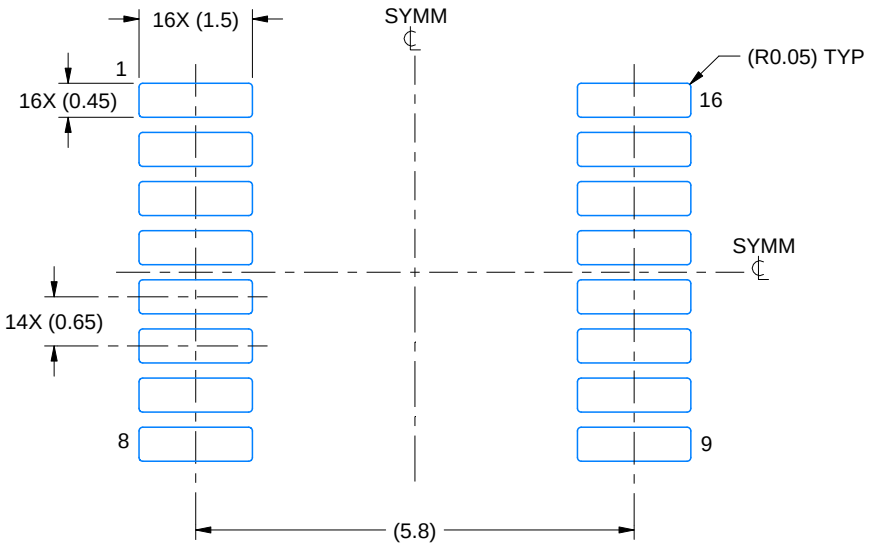
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

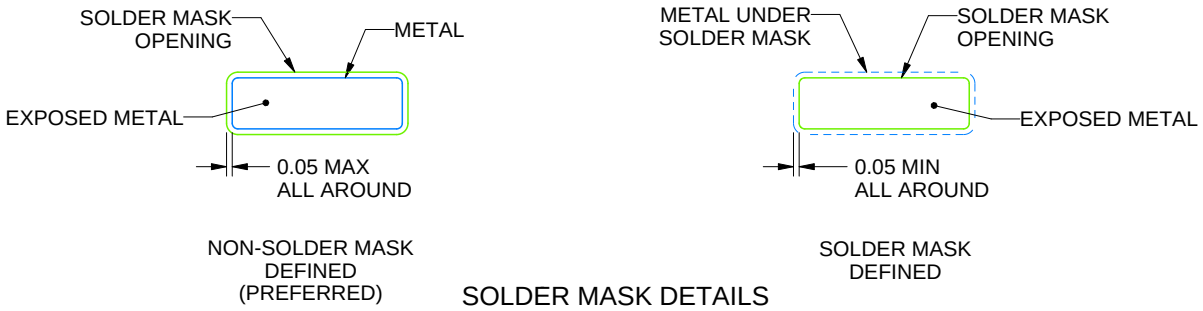


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

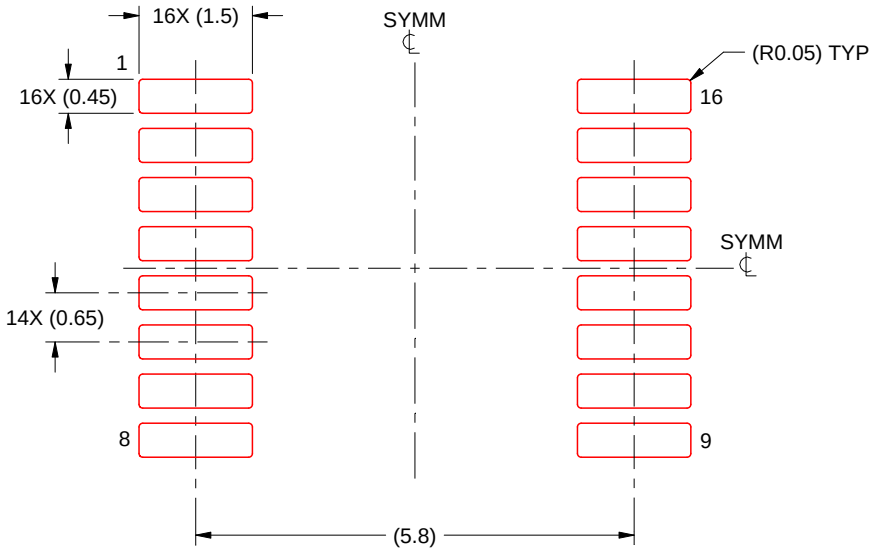


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

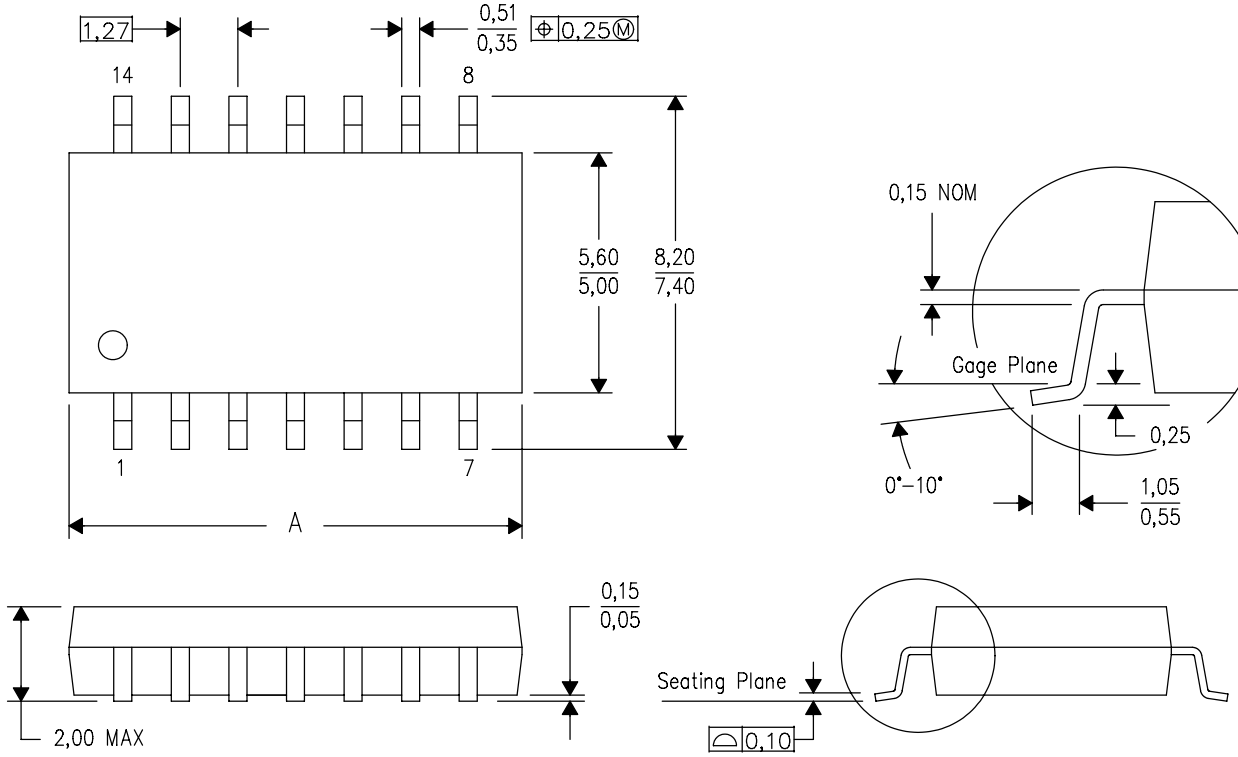
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

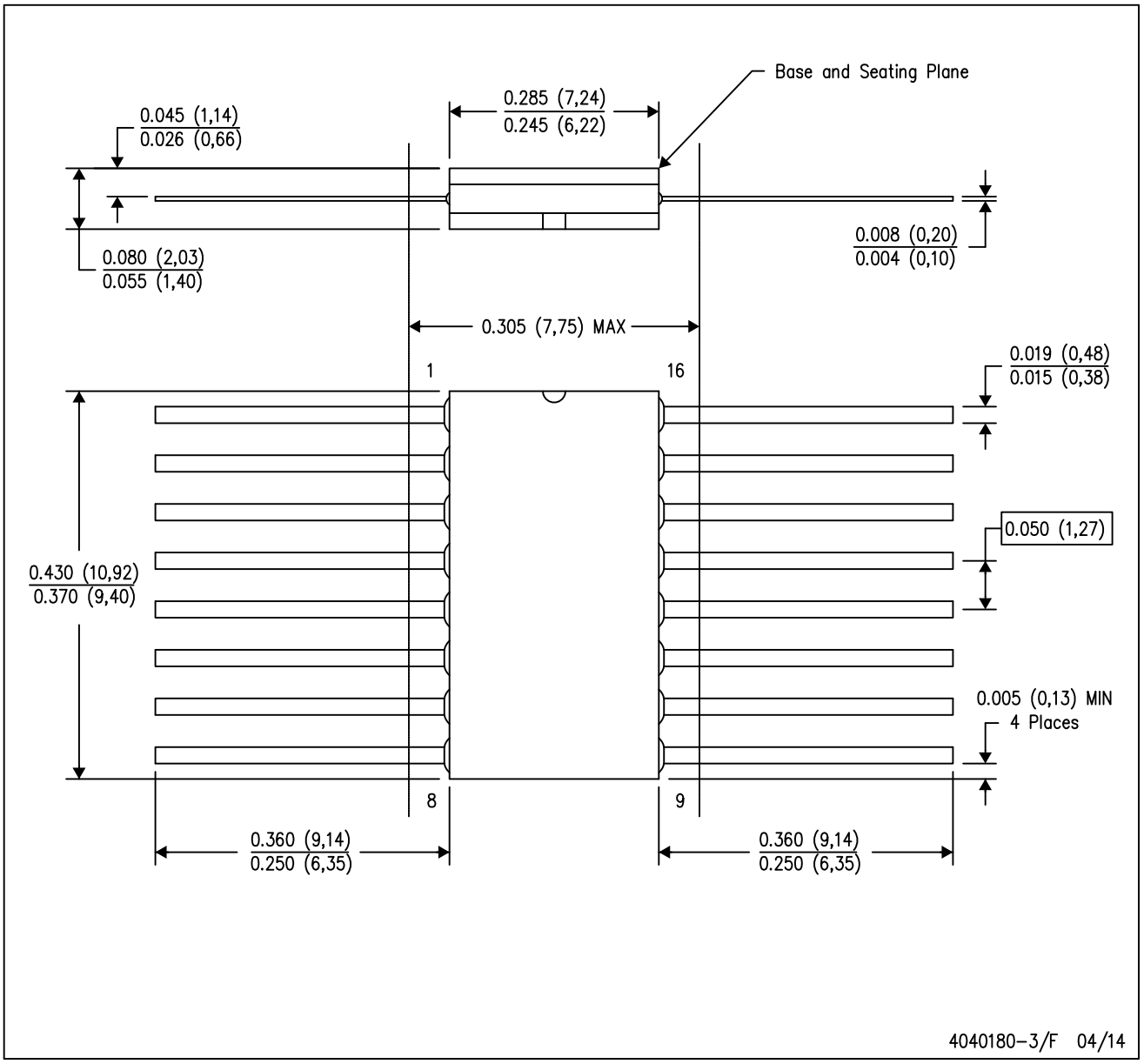


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

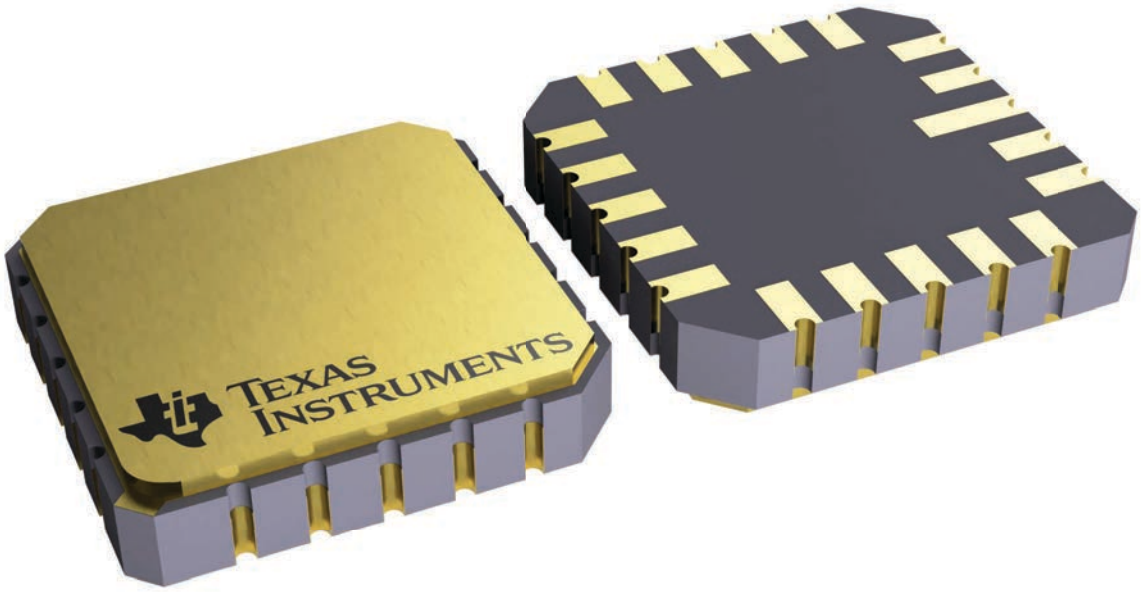
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

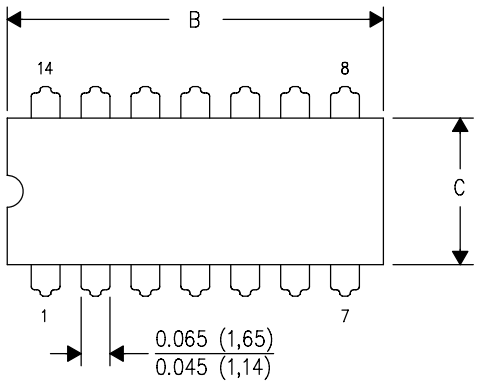


4229370VA\

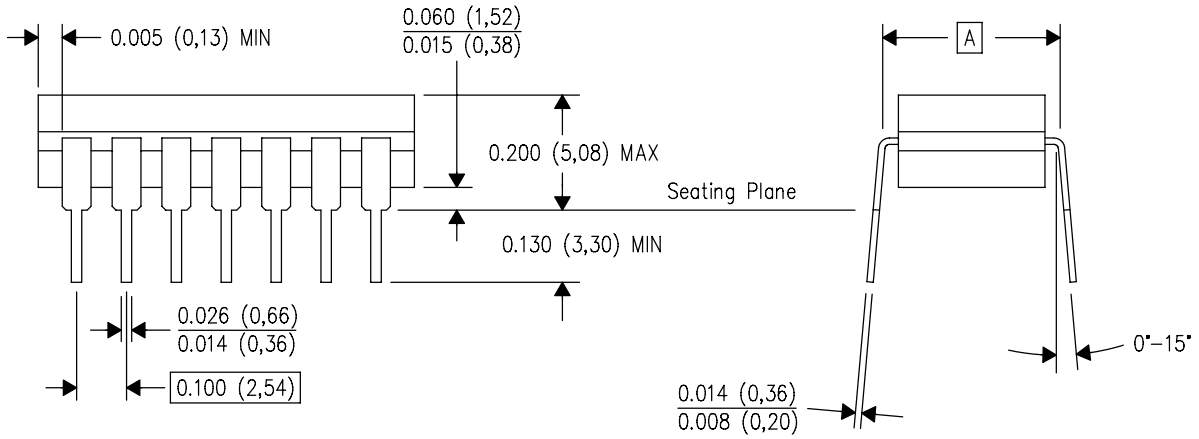
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



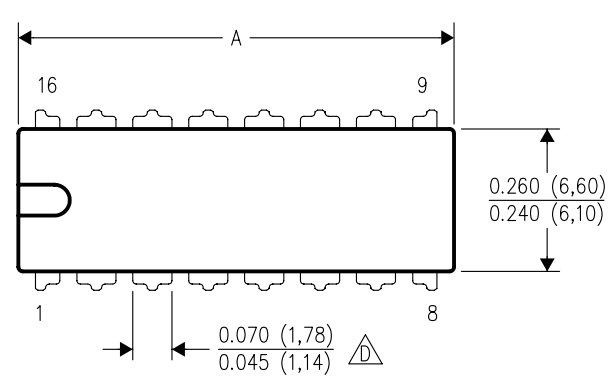
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

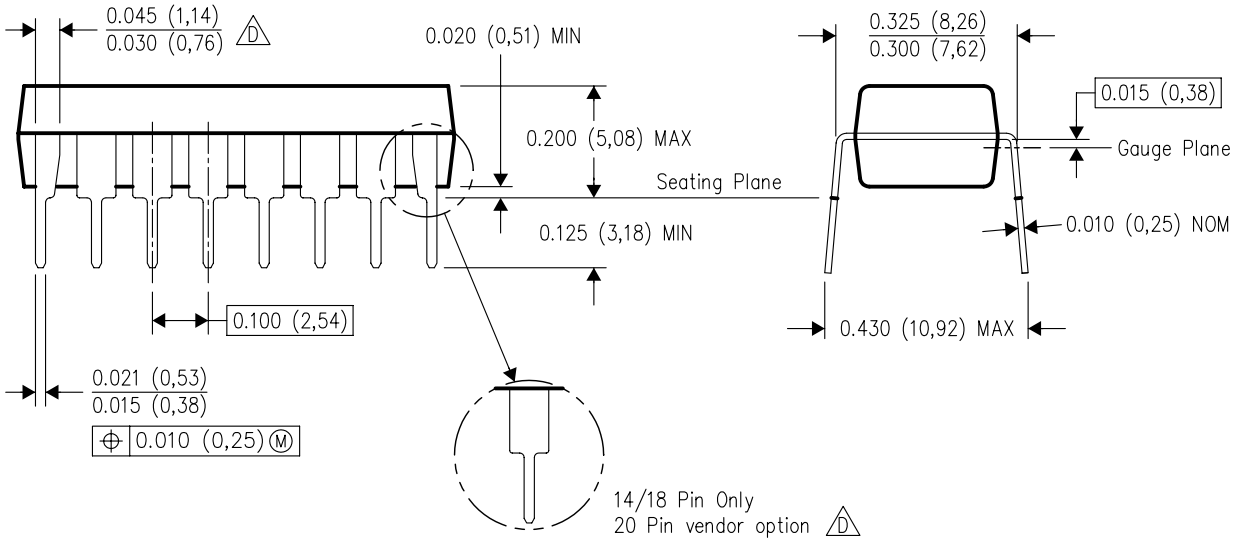
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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