bq2004

Fast-Charge IC

Features

- ➤ Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- ➤ Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- ➤ Easily integrated into systems or used as a stand-alone charger
- ➤ Pre-charge qualification of temperature and voltage
- ➤ Configurable, direct LED outputs display battery and charge status
- ➤ Fast-charge termination by Δ temperature/Δ time, peak volume detection, -ΔV, maximum voltage, maximum temperature, and maximum time
- ➤ Optional top-off charge and pulsed current maintenance charging
- ➤ Logic-level controlled low-power mode (< 5µA standby current)

General Description

The bq2004 Fast Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Integration of closed-loop current control circuitry allows the bq2004 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2004-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2004 as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2004 may alternatively be used to gate an externally regulated charging current.

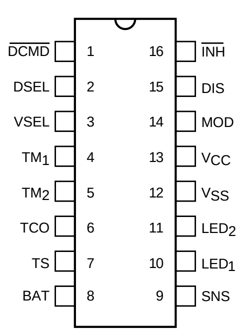
Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- ■ Rate of temperature time (ΔT/Δt)
- ■ Peak voltage detection (PVD)
- ■ Negative delta voltage (-ΔV)
- ■ Maximum voltage
- ■ Maximum temperature
- ■ Maximum time

After fast charge, optional top-off and pulsed current maintenance phases are available.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN2004E01.eps

Pin Names

$\overline{\text{DCMD}}$	Discharge command	SNS	Sense resistor input
DSEL	Display select	LED_1	Charge status output 1
VSEL	Voltage termination select	LED_2	Charge status output 2
TM_1	Timer mode select 1	V_{SS}	System ground
TM_2	Timer mode select 2	V_{CC}	5.0V ±10% power
TCO	Temperature cutoff	MOD	Charge current control
TS	Temperature sense	DIS	Discharge control output
BAT	Battery voltage	$\overline{\text{INH}}$	Charge inhibit input

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Pin Descriptions

$\overline{\text{DCMD}}$ **Discharge-before-charge control input**

The $\overline{\text{DCMD}}$ input controls the conditions that enable discharge-before-charge. $\overline{\text{DCMD}}$ is pulled up internally. A negative-going pulse on $\overline{\text{DCMD}}$ initiates a discharge to end-of-discharge voltage (EDV) on the BAT pin, followed by a new charge cycle start. Tying DCMD to ground enables automatic discharge-before-charge on every new charge cycle start.

DSEL **Display select input**

This three-state input configures the charge status display mode of the LED_1 and LED_2 outputs. See Table 2.

VSEL **Voltage termination select input**

This three-state input controls the voltage-termination technique used by the bq2004. When high, PVD is active. When floating, -ΔV is used. When pulled low, both PVD and -ΔV are disabled.

TM_1–TM_2 **Timer mode inputs**

TM_1 and TM_2 are three-state inputs that configure the fast charge safety timer, voltage termination hold-off time, "top-off", and trickle charge control. See Table 1.

TCO **Temperature cut-off threshold input**

Input to set maximum allowable battery temperature. If the potential between TS and SNS is less than the voltage at the TCO input, then fast charge or top-off charge is terminated.

TS **Temperature sense input**

Input, referenced to SNS, for an external thermister monitoring battery temperature.

BAT **Battery voltage input**

BAT is the battery voltage sense input, referenced to SNS. This is created by a high-impedance resistor-divider network connected between the positive and the negative terminals of the battery.

SNS **Charging current sense input**

SNS controls the switching of MOD based on an external sense resistor in the current path of the battery. SNS is the reference potential for both the TS and BAT pins. If SNS is connected to V_{SS}, then MOD switches high at the beginning of charge and low at the end of charge.

LED_1–LED_2 **Charge status outputs**

Push-pull outputs indicating charging status. See Table 2.

V_{SS} **Ground**

V_{CC} **V_{CC} supply input**

5.0V, ±10% power input.

MOD **Charge current control output**

MOD is a push-pull output that is used to control the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging current flow.

DIS **Discharge control output**

Push-pull output used to control an external transistor to discharge the battery before charging.

$\overline{\text{INH}}$ **Charge inhibit input**

When low, the bq2004 suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a new charge cycle is started.

Functional Description

Figure 3 shows a block diagram and Figure 4 shows a state diagram of the bq2004.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a two-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = \frac{N}{2} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1. Both the BAT and TS inputs are referenced to SNS, so the signals used inside the IC are:

$$V_{BAT} - V_{SNS} = V_{CELL}$$

and

$$V_{TS} - V_{SNS} = V_{TEMP}$$

Discharge-Before-Charge

The $\overline{\text{DCMD}}$ input is used to command discharge-before-charge via the DIS output. Once activated, DIS becomes active (high) until V_{CELL} falls below V_{EDV}, at which time DIS goes low and a new fast charge cycle begins.

The $\overline{\text{DCMD}}$ input is internally pulled up to V_{CC} (its inactive state). Leaving the input unconnected, therefore, results in disabling discharge-before-charge. A negative going pulse on $\overline{\text{DCMD}}$ initiates discharge-before-charge at any time regardless of the current state of the bq2004. If $\overline{\text{DCMD}}$ is tied to V_{SS}, discharge-before-charge will be the first step in all newly started charge cycles.

Starting a Charge Cycle

A new charge cycle (see Figure 2) is started by:

1. V_{CC} rising above 4.5V
2. V_{CELL} falling through the maximum cell voltage, V_{MCV} where:

$$V_{MCV} = 0.8 * V_{CC} \pm 30mV$$

3. A transition on the $\overline{\text{INH}}$ input from low to high.

If $\overline{\text{DCMD}}$ is tied low, a discharge-before-charge is executed as the first step of the new charge cycle. Otherwise, pre-charge qualification testing is the first step.

The battery must be within the configured temperature and voltage limits before fast charging begins.

The valid battery voltage range is $V_{EDV} < V_{BAT} < V_{MCV}$ where:

$$V_{EDV} = 0.4 * V_{CC} \pm 30mV$$

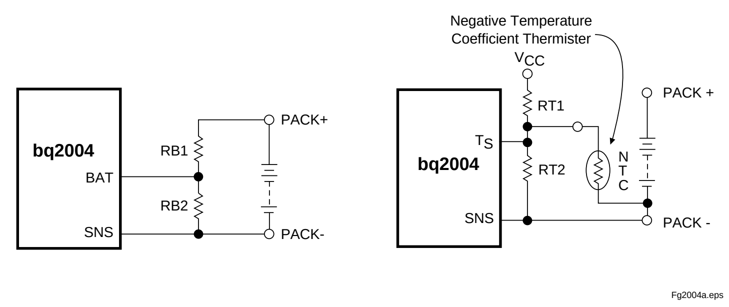


Figure 1. Voltage and Temperature Monitoring

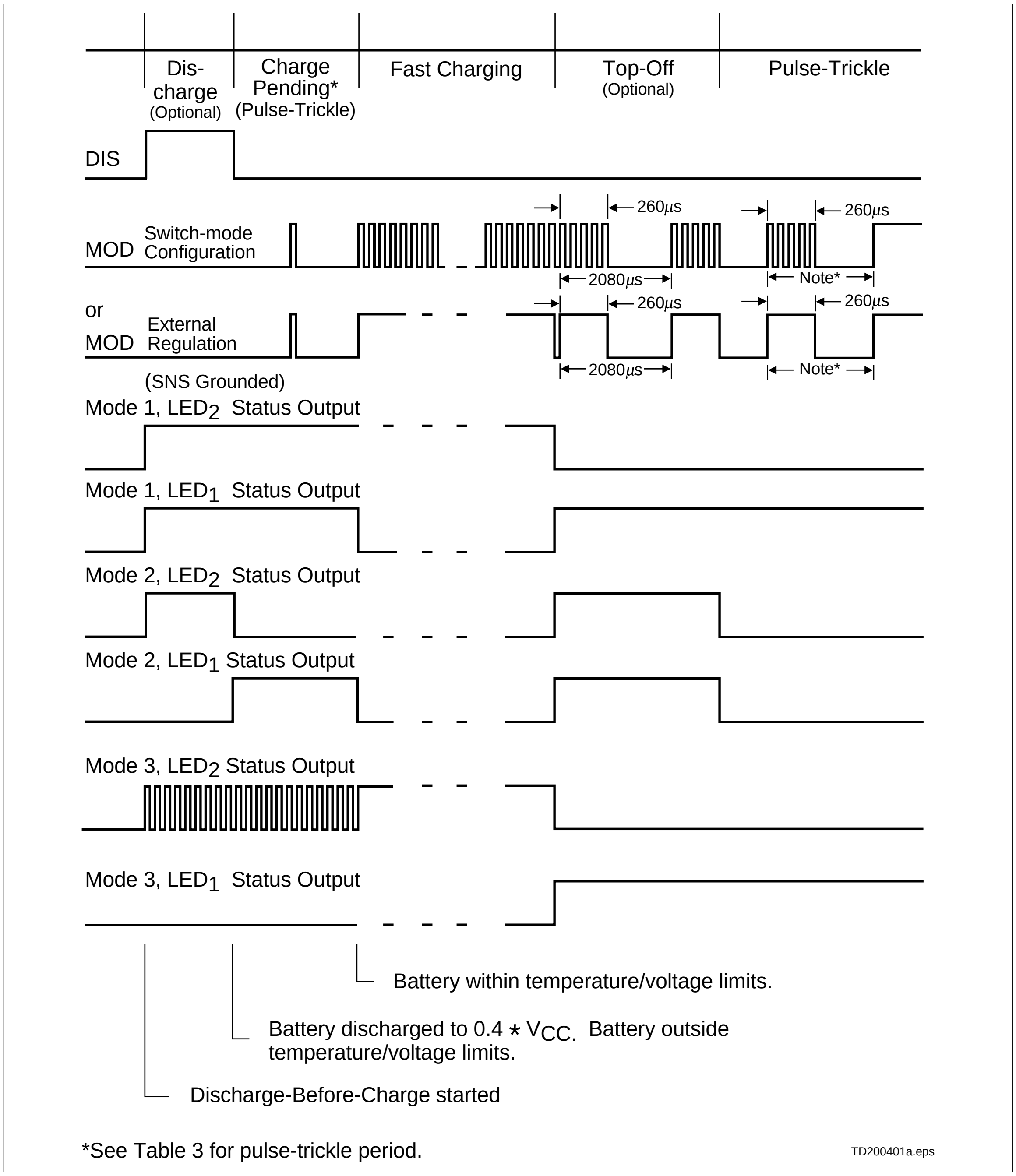


Figure 2. Charge Cycle Phases

The valid temperature range is $V_{HTF} < V_{TEMP} < V_{LTF}$, where:

$$V_{LTF} = 0.4 * V_{CC} \pm 30mV$$

$$V_{HTF} = [(1/4 * V_{LTF}) + (3/4 * V_{TCO})] \pm 30mV$$

Note: The low temperature fault (LTF) threshold is not enforced if the IC is configured for PVD termination (VSEL = high).

V_{TCO} is the voltage presented at the TCO input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to 0.4 $*$ V_{CC}.

If the temperature of the battery is out of range, or the voltage is too low, the chip enters the charge pending state and waits for both conditions to fall within their allowed limits. The MOD output is modulated to provide the configured trickle charge rate in the charge pending state. There is no time limit on the charge pending state; the charger remains in this state as long as the voltage or temperature conditons are outside of the allowed limits. If the voltage is too high, the chip goes to the battery absent state and waits until a new charge cycle is started.

Fast charge continues until termination by one or more of the six possible termination conditions:

- Delta temperature/delta time ($\Delta T/\Delta t$)
- Peak voltage detection (PVD)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

PVD and - V Termination

The bq2004 samples the voltage at the BAT pin once every 34s. When $-\Delta V$ termination is selected, if V_{CELL} is lower than any previously measured value by 12mV ±4mV (6mV/cell), fast charge is terminated. When PVD termination is selected, if V_{CELL} is lower than any previously measured value by 6mV ±2mV (3mV/cell), fast charge is terminated. The PVD and $-\Delta V$ tests are valid in the range $0.4 * V_{CC} < V_{CELL} < 0.8 * V_{CC}$.

VSEL Input	Voltage Termination
Low	Disabled
Float	$-\Delta V$
High	PVD

Voltage Sampling

Each sample is an average of voltage measurements taken 57µs apart. The IC takes 32 measurements in PVD mode and 16 measurements in $-\Delta V$ mode. The resulting sample periods (9.17ms and 18.18ms, respectively) filter out harmonics centered around 55Hz and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period, $-\Delta V$ termination is disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. $\Delta T/\Delta t$, maximum voltage and maximum temperature terminations are not affected by the hold-off period.

T/ t Termination

The bq2004 samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If V_{TEMP} has fallen 16mV ±4mV or more, fast charge is terminated. If VSEL = high, the $\Delta T/\Delta t$ termination test is valid only when $V_{TCO} < V_{TEMP} < V_{TCO} + 0.2 * V_{CC}$. Otherwise the $\Delta T/\Delta t$ termination test is valid only when $V_{TCO} < V_{TEMP} < V_{LTF}$.

Temperature Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Maximum Voltage, Temperature, and Time

Anytime V_{CELL} rises above V_{MCV}, the LEDs go off and charging ceases immediately. If V_{CELL} then falls back below V_{MCV} before t_{MCV} = 1.5s ±0.5s, the chip transitions to the Charge Complete state (maximum voltage termination). If V_{CELL} remains above V_{MCV} at the expiration of t_{MCV}, the bq2004 transitions to the Battery Absent state (battery removal). See Figure 4.

Maximum temperature termination occurs anytime V_{TEMP} falls below the temperature cutoff threshold V_{TCO}. Unless PVD termination is enabled (VSEL = high), charge will also be terminated if V_{TEMP} rises above the low temperature fault threshold, V_{LTF}, after fast charge begins. The V_{LTF} threshold is not enforced when the IC is configured for PVD termination.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time equal to the fast-charge safety time (See Table 1.) During top-off, the MOD pin is enabled at a duty cycle of 260µs active for every 1820µs inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle charging follows the fast charge and optional top-off charge phases to compensate for self-discharge of the battery while it is idle in the charger. The configured pulse-trickle rate is also applied in the charge pending state to raise the voltage of an over-discharged battery up to the minimum required before fast charge can begin.

In the pulse-trickle mode, MOD is active for 260µs of a period specified by the settings of TM1 and TM2. See Table 1. The resulting trickle-charge rate is C/64 when top-off is enabled and C/32 when top-off is disabled. Both pulse trickle and top-off may be disabled by tying TM1 and TM2 to V_{SS}.

Charge Status Indication

Charge status is indicated by the LED_1 and LED_2 outputs. The state of these outputs in the various charge cycle phases is given in Table 2 and illustrated in Figure 2.

In all cases, if V_{CELL} exceeds the voltage at the MCV pin, both LED_1 and LED_2 outputs are held low regardless of other conditions. Both can be used to directly drive an LED.

Charge Current Control

The bq2004 controls charge current through the MOD output pin. The current control circuitry is designed to support implementation of a constant-current switching regulator or to gate an externally regulated current source.

When used in switch mode configuration, the nominal regulated current is:

$$I_{REG} = 0.225V/R_{SNS}$$

Charge current is monitored at the SNS input by the voltage drop across a sense resistor, R_{SNS}, between the low side of the battery pack and ground. R_{SNS} is sized to provide the desired fast charge current.

Table 1. Fast-Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate	TM1	TM2	Typical Fast-Charge Safety Time (minutes)	Typical PVD, -ΔV Hold-Off Time (seconds)	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Period (Hz)
C/4	Low	Low	360	137	Disabled	Disabled	Disabled
C/2	Float	Low	180	820	Disabled	C/32	240
1C	High	Low	90	410	Disabled	C/32	120
2C	Low	Float	45	200	Disabled	C/32	60
4C	Float	Float	23	100	Disabled	C/32	30
C/2	High	Float	180	820	C/16	C/64	120
1C	Low	High	90	410	C/8	C/64	60
2C	Float	High	45	200	C/4	C/64	30
4C	High	High	23	100	C/2	C/64	15

Note: Typical conditions = 25°C, V_{CC} = 5.0V.

If the voltage at the SNS pin is less than V_{SNSLO}, the MOD output is switched high to pass charge current to the battery.

When the SNS voltage is greater than V_{SNSHI}, the MOD output is switched low—shutting off charging current to the battery.

$$V_{SNSLO} = 0.04 * V_{CC} \pm 25mV$$

$$V_{SNSHI} = 0.05 * V_{CC} \pm 25mV$$

When used to gate an externally regulated current source, the SNS pin is connected to V_{SS}, and no sense resisitor is required.

Table 2. bq2004 LED Status Display Options

Mode 1	Charge Status	LED_1	LED_2
DSEL = V_{SS}	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	High	High
	Fast charge in progress	Low	High
	Charge complete, top-off, and/or trickle	High	Low
Mode 2	**Charge Status**	**LED_1**	**LED_2**
DSEL = Floating	Battery absent, fast charge in progress or complete	Low	Low
	Fast charge pending	High	Low
	Discharge in progress	Low	High
	Top-off in progress	High	High
Mode 3	**Charge Status**	**LED_1**	**LED_2**
DSEL = V_{CC}	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	Low	1/8s high 1/8s low
	Fast charge in progress	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low

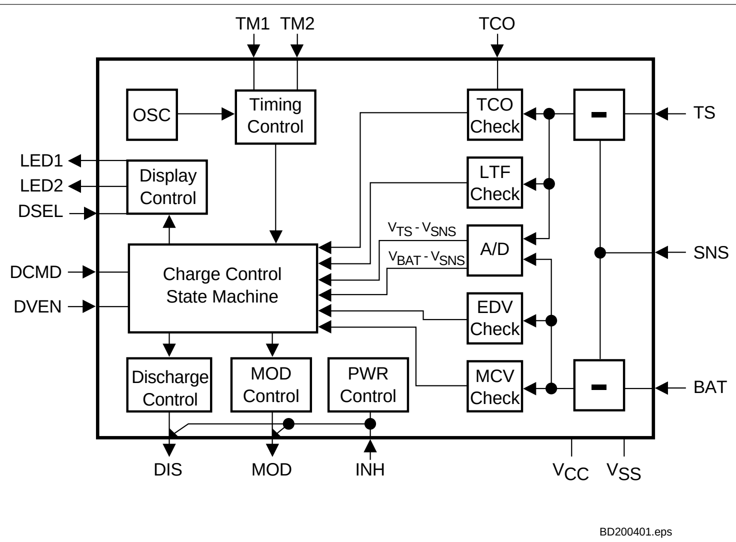


Figure 3. Block Diagram

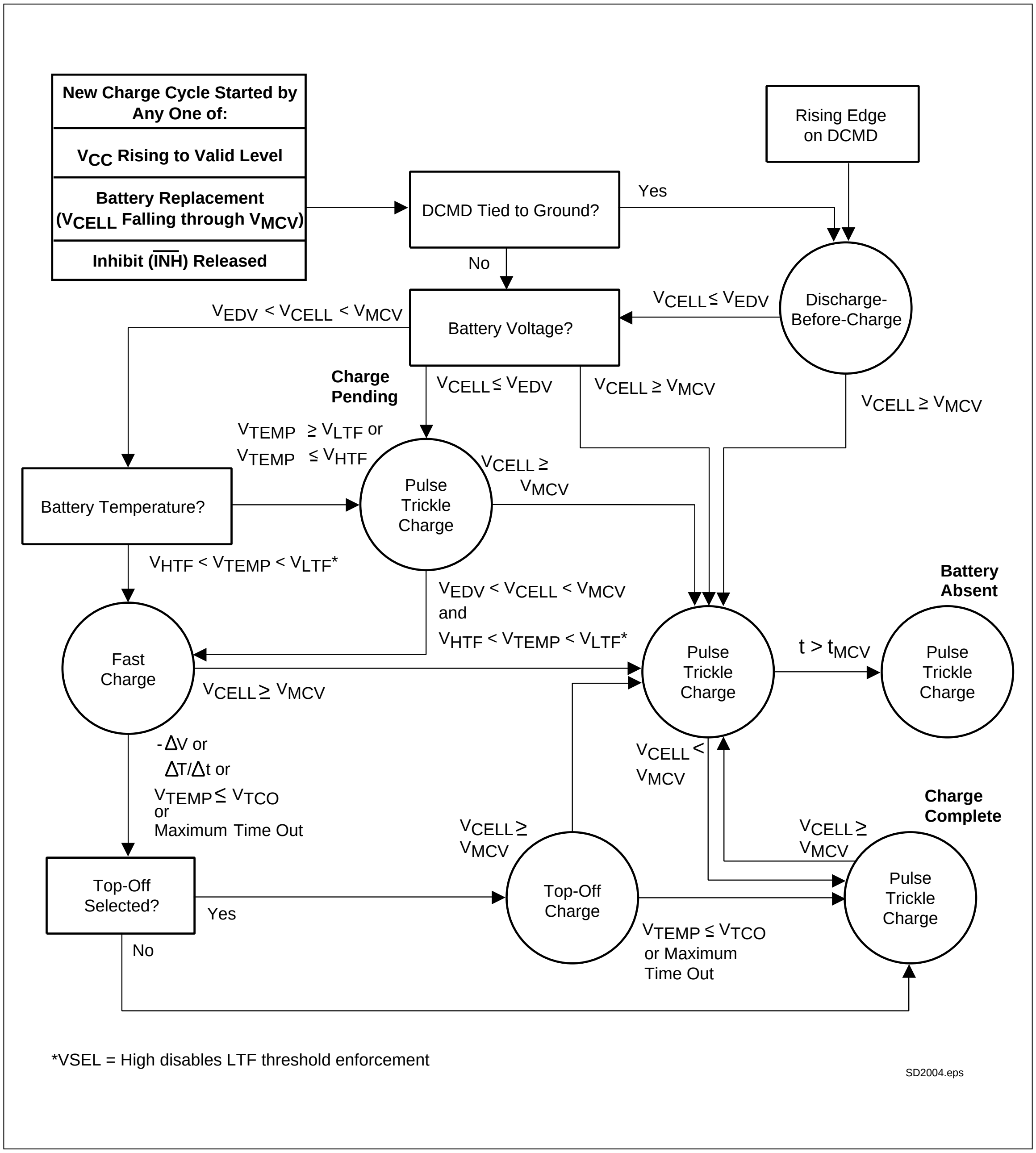


Figure 4. State Diagram

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	$0.05 * V_{CC}$	±0.025	V	
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	$0.04 * V_{CC}$	±0.025	V	
V_{LTF}	Low-temperature fault	$0.4 * V_{CC}$	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/terminates charge
V_{HTF}	High-temperature fault	$(1/4 * V_{LTF}) + (3/4 * V_{TCO})$	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	$0.4 * V_{CC}$	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{MCV}	Maximum cell voltage	$0.8 * V_{CC}$	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/terminates charge
V_{THERM}	TS input change for $\Delta T/\Delta t$ detection	-16	±4	mV	V_{CC} = 5V, T_A = 25°C
$-\Delta V$	BAT input change for $-\Delta V$ detection	-12	±4	mV	V_{CC} = 5V, T_A = 25°C
PVD	BAT input change for PVD detection	-6	±2	mV	V_{CC} = 5V, T_A = 25°C

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TCO}	Temperature cutoff	0.2 ∗ V_{CC}	-	0.4 ∗ V_{CC}	V	Valid $\Delta T/\Delta t$ range
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2, DSEL, VSEL
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input low	-	-	0.3	V	TM_1, TM_2, DSEL, VSEL
V_{OH}	Logic output high	V_{CC} - 0.8	-	-	V	DIS, MOD, LED_1, LED_2, $I_{OH} \leq$ -10mA
V_{OL}	Logic output low	-	-	0.8	V	DIS, MOD, LED_1, LED_2, $I_{OL} \leq$ 10mA
I_{CC}	Supply current	-	1	3	mA	Outputs unloaded
I_{SB}	Standby current	-	-	1	µA	$\overline{INH}$ = V_{IL}
I_{OH}	DIS, LED_1, LED_2, MOD source	-10	-	-	mA	@V_{OH} = V_{CC} - 0.8V
I_{OL}	DIS, LED_1, LED_2, MOD sink	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_L	Input leakage	-	-	±1	µA	$\overline{INH}$, BAT, V = V_{SS} to V_{CC}
	Input leakage	50	-	400	µA	$\overline{DCMD}$, V = V_{SS} to V_{CC}
I_{IL}	Logic input low source	-	-	70	µA	TM_1, TM_2, DSEL, VSEL, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70	-	-	µA	TM_1, TM_2, DSEL, VSEL, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	Tri-state	-2	-	2	µA	TM_1, TM_2, DSEL, and VSEL should be left disconnected (floating) for Z logic input state

Note: All voltages relative to V_{SS} except as noted.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
R_{SNS}	SNS input impedance	50	-	-	MΩ

Timing (T$_A$ = 0 to +70°C; V$_{CC}$ ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD}$ and $\overline{INH}$ pulse command	1	-	-	µs	Pulse start for charge or discharge before charge
d_{FCV}	Time base variation	-16	-	16	%	V_{CC} = 4.75V to 5.25V
f_{REG}	MOD output regulation frequency	-	-	300	kHz	
t_{MCV}	Maximum voltage termination time limit	1	-	2	s	Time limit to distinguish battery removed from charge complete.

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	10	Standby current ISB	Was 5 A max; is 1 A max
2	9	V_{BSNSLO} Rating	Was: V_{SNSHI} - (0.01 * V_{CC}) Is: 0.04 * V_{CC}
2	7	Correction in Peak Voltage Detect Termination section	Was VCELL; is VBAT
2	3	Added block diagram	Diagram insertion
2	7	Added VSEL/termination table	Table insertion
2	8	Added values to Table 3	Top-off rate values
3	7	VSEL/Termination	Low, High changed
4	All	Revised and expanded format of this data sheet	Clarification
5	9	Corrected V_{HTF} rating	Was: (1/3 V_{LTF}) + (2/3 V_{TCO}) Is: (1/4 V_{LTF}) + (3/4 V_{TCO})
6	9	T_{OPR}	Deleted industrial temperature range
7	9	Corrected V_{HTF} DC threshold	Was: (1/4 * V_{LTF}) + (2/3 * V_{TCO}) Is: (1/4 * V_{LTF}) + (3/4 * V_{TCO})
8	9	Corrected V_{SNSLO} tolerance	Was: ±0.010 Is: ±0.025

Notes: Change 1 = Apr. 1994 B "Final" changes from Dec. 1993 A "Preliminary."
Change 2 = Sept. 1996 C changes from Apr. 1994 B.
Change 3 = April 1997 C changes from Sept. 1996 C.
Change 4 = Oct. 1997 D changes from April 1997 C.
Change 5 = Jan. 1998 E changes from Oct. 1997 D.
Change 6 = June 1999 F changes from Jan. 1998 E.
Change 7 = Feb. 2001 G changes from June 1999 F.
Change 8 = Apr. 2005 H changes from Feb. 2001 G.

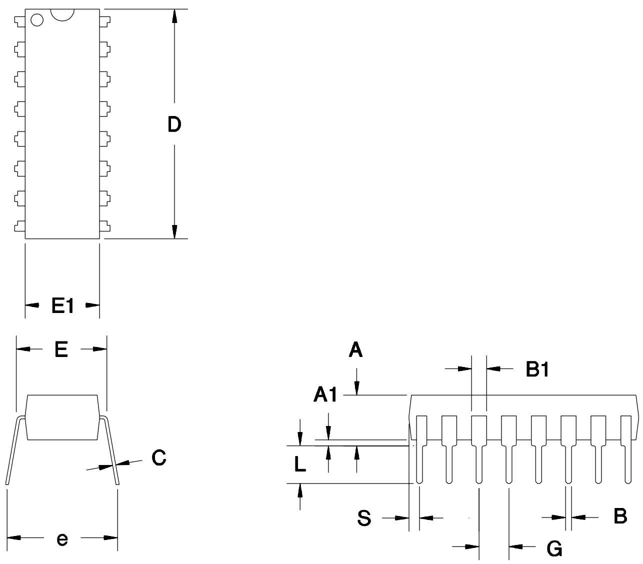
Ordering Information

bq2004 __

Package Option:
PN = 16-pin narrow plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2004 Fast-Charge IC

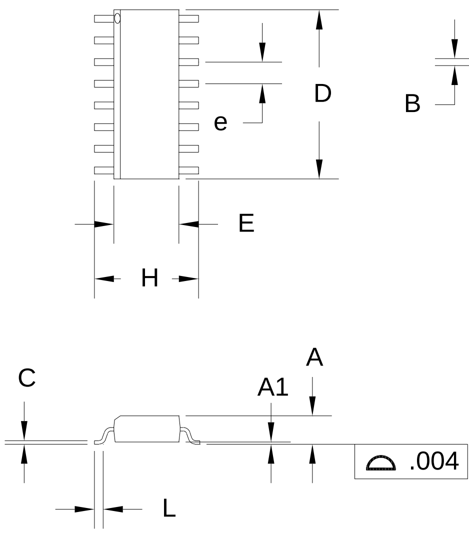
16-Pin DIP Narrow (PN)



16-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

16-Pin SOIC Narrow (SN)



16-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2004PN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-20 to 70	2004PN -A4	Samples
BQ2004SN	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004 (-A4, A4)	Samples
BQ2004SNG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004 (-A4, A4)	Samples
BQ2004SNTR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2004 (-A4, A4)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

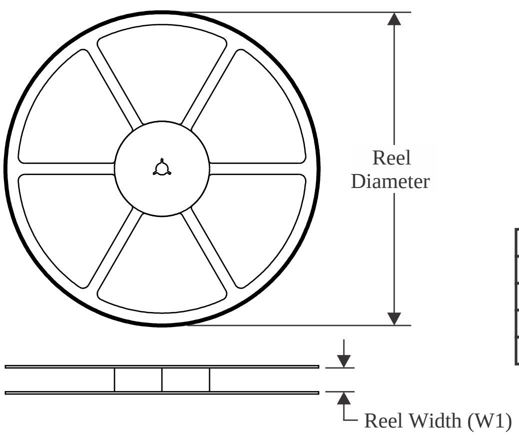
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

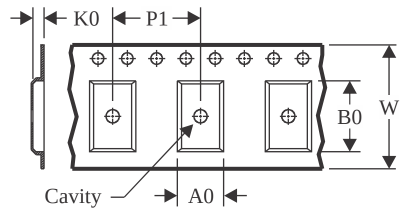
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

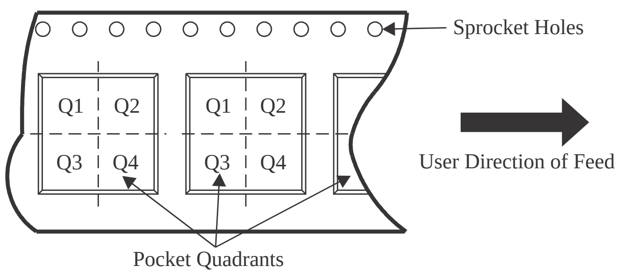


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

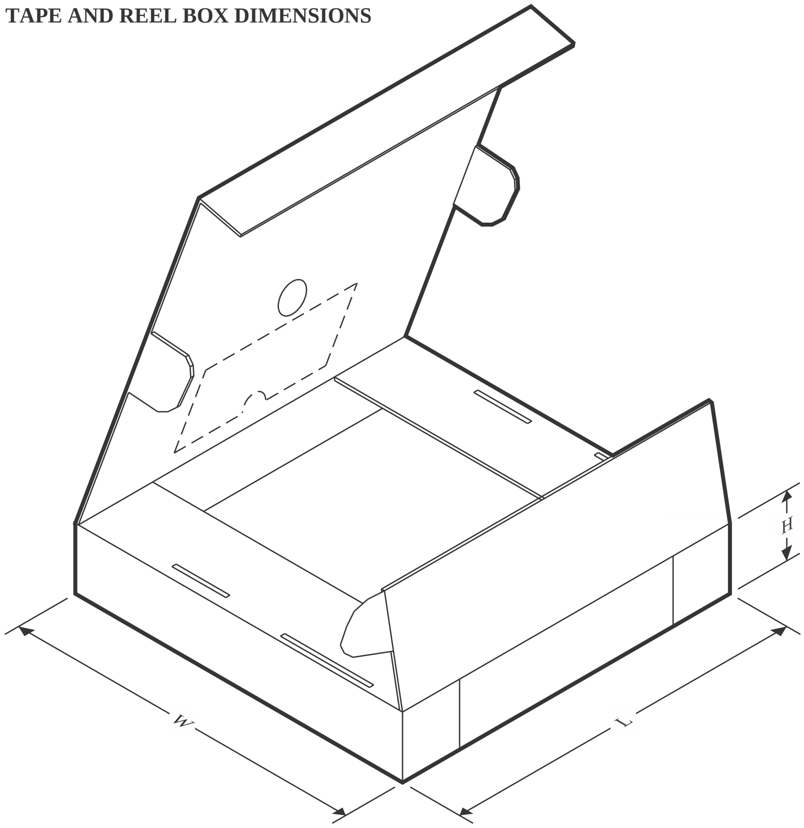
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2004SNTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

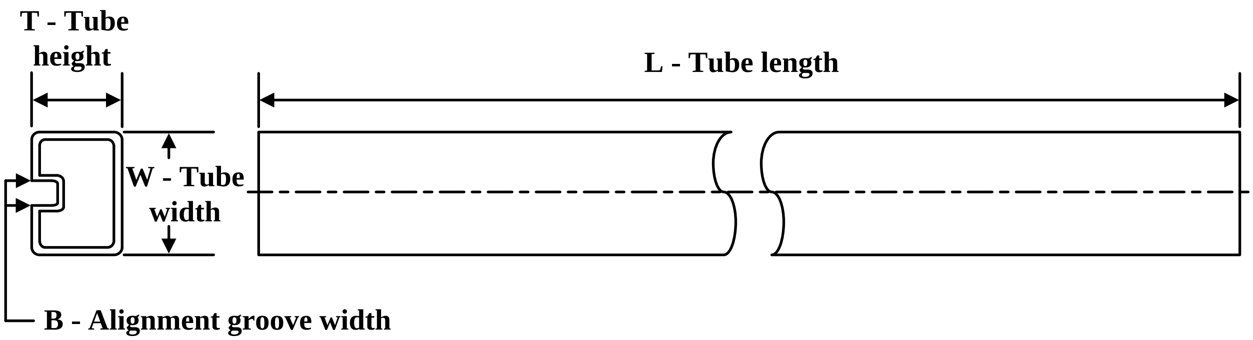
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2004SNTR	SOIC	D	16	2500	356.0	356.0	35.0

TUBE

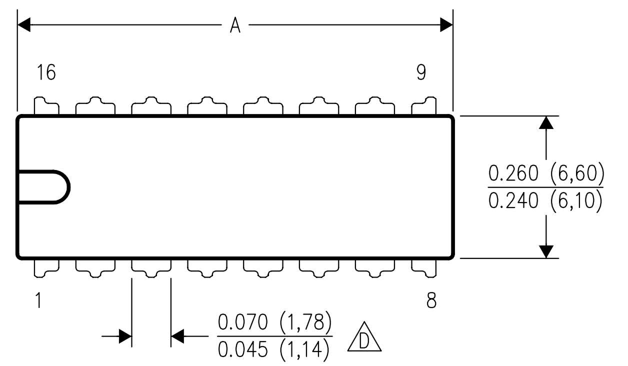


*All dimensions are nominal

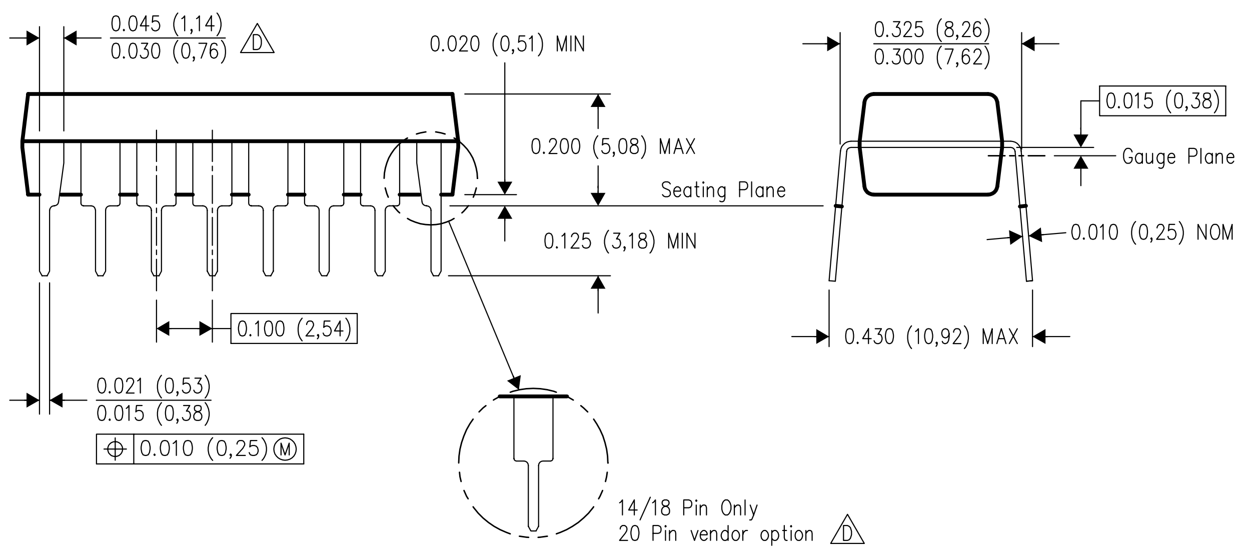
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ2004PN	N	PDIP	16	25	506	13.97	11230	4.32
BQ2004SN	D	SOIC	16	40	506.6	8	3940	4.32
BQ2004SNG4	D	SOIC	16	40	506.6	8	3940	4.32

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



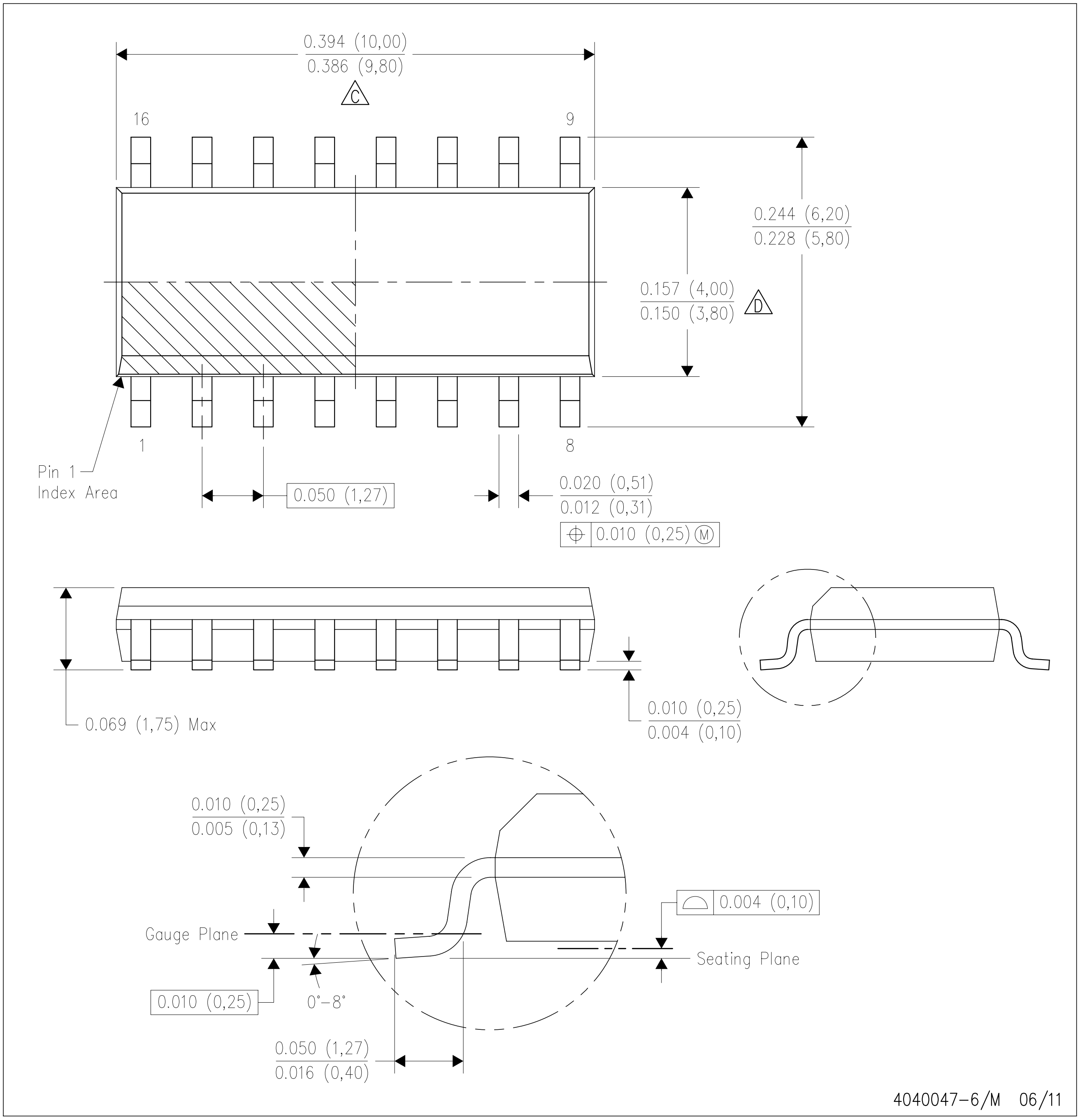
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

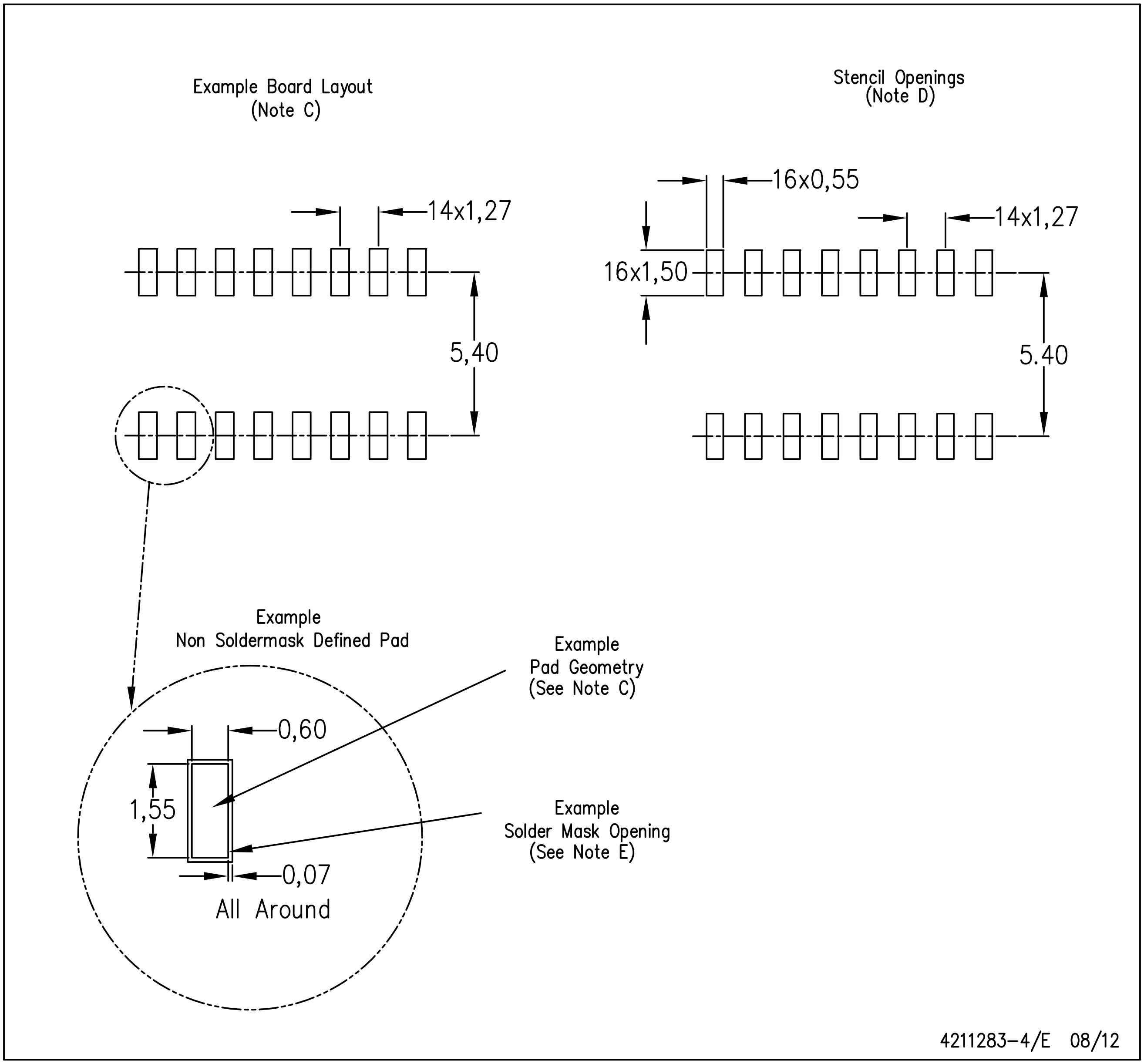
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.