

# bq4050 CEDVバッテリー残量計および保護ソリューション

## 1シリーズ～4シリーズ・セル・リチウムイオン・バッテリー・パック用

### 1 特長

- NチャネルFETドライブのハイサイド保護により、フォルト状況でもシリアル・バス通信が可能
- 内部バイパス付きのセル・バランス機能により、バッテリーの状態を最適化
- 診断用の寿命データ・モニタと、障害解析用のブラック・ボックス・レコーダ
- プログラミング可能な各種の保護機能: 電圧、電流、温度
- JEITA充電アルゴリズムによりスマート充電をサポート
- 2つの独立したADCを持つアナログ・フロント・エンド
  - 電流および電圧の同時サンプリング
  - 入力オフセット誤差1 $\mu$ V未満(標準値)の高精度クーロン・カウンタ
- バッテリー・トリップ・ポイント(BTP)機能のサポートによる Windows®統合
- 充電状態およびバッテリー状態の表示用LEDディスプレイ
- 100kHz SMBus v1.1通信インターフェイスによるプログラミングとデータ・アクセス、400kHzモードにも対応
- SHA-1認証レスポндаによるバッテリー・パックのセキュリティ強化
- 小型の32ピンVQFNパッケージ(RSM)

### 2 アプリケーション

- ノートブックPC
- 医療用およびテスト機器
- ポータブル機器
- コードレス掃除機およびロボット掃除機

### 3 概要

補償付き放電終止電圧(CEDV)技術を採用したテキサス・インスツルメンツのbq4050デバイスは、高度に統合された高精度の1シリーズ～4シリーズ・セル用バッテリー残量計および保護ソリューションであり、自律的な充電制御とセル・バランスを実現します。

bq4050デバイスは、フラッシュをプログラム可能なカスタムのRISC (Reduced Instruction Set CPU)を搭載し、安全保護機能や、リチウムイオンおよびリチウムポリマ・バッテリー・パック用の認証機能を備えた、完全に統合されたパック・ベースのソリューションです。

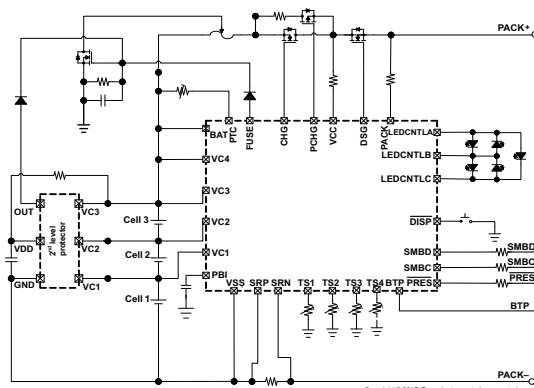
bq4050バッテリー残量計はSMBus準拠のインターフェイスで通信を行い、超低消費電力かつ高速のTI bqBMPプロセッサ、高精度のアナログ測定機能、内蔵のフラッシュ・メモリ、ペリフェラルおよび通信ポートのレイ、NチャネルFETドライブ、SHA-1認証変換レスポндаを組み合わせた、完全な高性能バッテリー管理ソリューションです。

#### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
bq4050	VQFN (32)	4.00mmx4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

#### 概略回路図



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## 4 改訂履歴

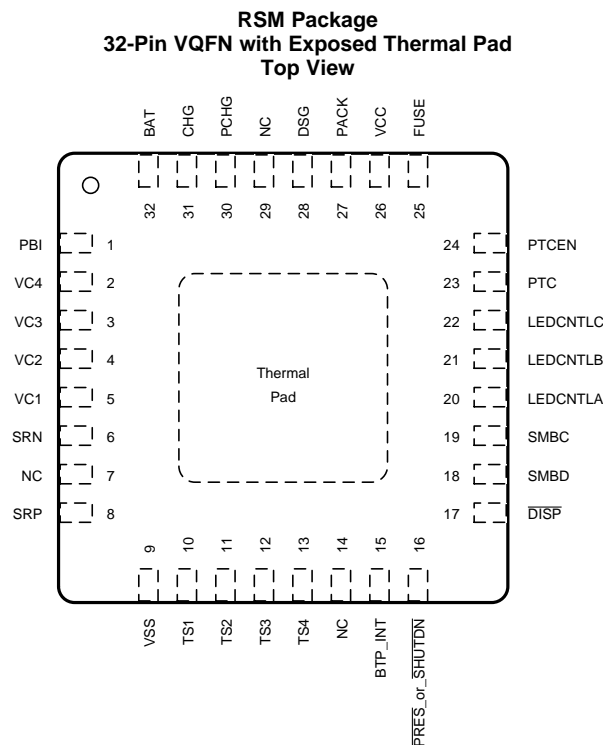
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (April 2016) から Revision B に変更

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## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
PBI	1	P <sup>(1)</sup>	Power supply backup input pin
VC4	2	IA	Sense voltage input pin for the most positive cell, and balance current input for the most positive cell
VC3	3	IA	Sense voltage input pin for the second most positive cell, balance current input for the second most positive cell, and return balance current for the most positive cell
VC2	4	IA	Sense voltage input pin for the third most positive cell, balance current input for the third most positive cell, and return balance current for the second most positive cell
VC1	5	IA	Sense voltage input pin for the least positive cell, balance current input for the least positive cell, and return balance current for the third most positive cell
SRN	6	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
NC	7	—	Not internally connected. Connect to V <sub>SS</sub> .
SRP	8	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
VSS	9	P	Device ground
TS1	10	IA	Temperature sensor 1 thermistor input pin
TS2	11	IA	Temperature sensor 2 thermistor input pin
TS3	12	IA	Temperature sensor 3 thermistor input pin
TS4	13	IA	Temperature sensor 4 thermistor input pin
NC	14	—	Not internally connected. Connect to V <sub>SS</sub> .
BTP_INT	15	O	Battery Trip Point (BTP) interrupt output
PRES or SHUTDN	16	I	Host system present input for removable battery pack or emergency system shutdown input for embedded packs

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

**Pin Functions (continued)**

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
DISP	17	—	Display control for LEDs
SMBD	18	I/OD	SMBus data pin
SMBC	19	I/OD	SMBus clock pin
LEDCNTLA	20	—	LED display segment that drives the external LEDs depending on the firmware configuration
LEDCNTLB	21	—	LED display segment that drives the external LEDs depending on the firmware configuration
LEDCNTLC	22	—	LED display segment that drives the external LEDs depending on the firmware configuration
PTC	23	IA	Safety PTC thermistor input pin. To disable, connect PTC and PTCEN to V <sub>SS</sub> .
PTCEN	24	IA	Safety PTC thermistor enable input pin. Connect to BAT. To disable, connect PTC and PTCEN to V <sub>SS</sub> .
FUSE	25	O	Fuse drive output pin
VCC	26	P	Secondary power supply input
PACK	27	IA	Pack sense input pin
DSG	28	O	NMOS Discharge FET drive output pin
NC	29	—	Not internally connected. Connect to V <sub>SS</sub> .
PCHG	30	O	PMOS Precharge FET drive output pin
CHG	31	O	NMOS Charge FET drive output pin
BAT	32	P	Primary power supply input pin

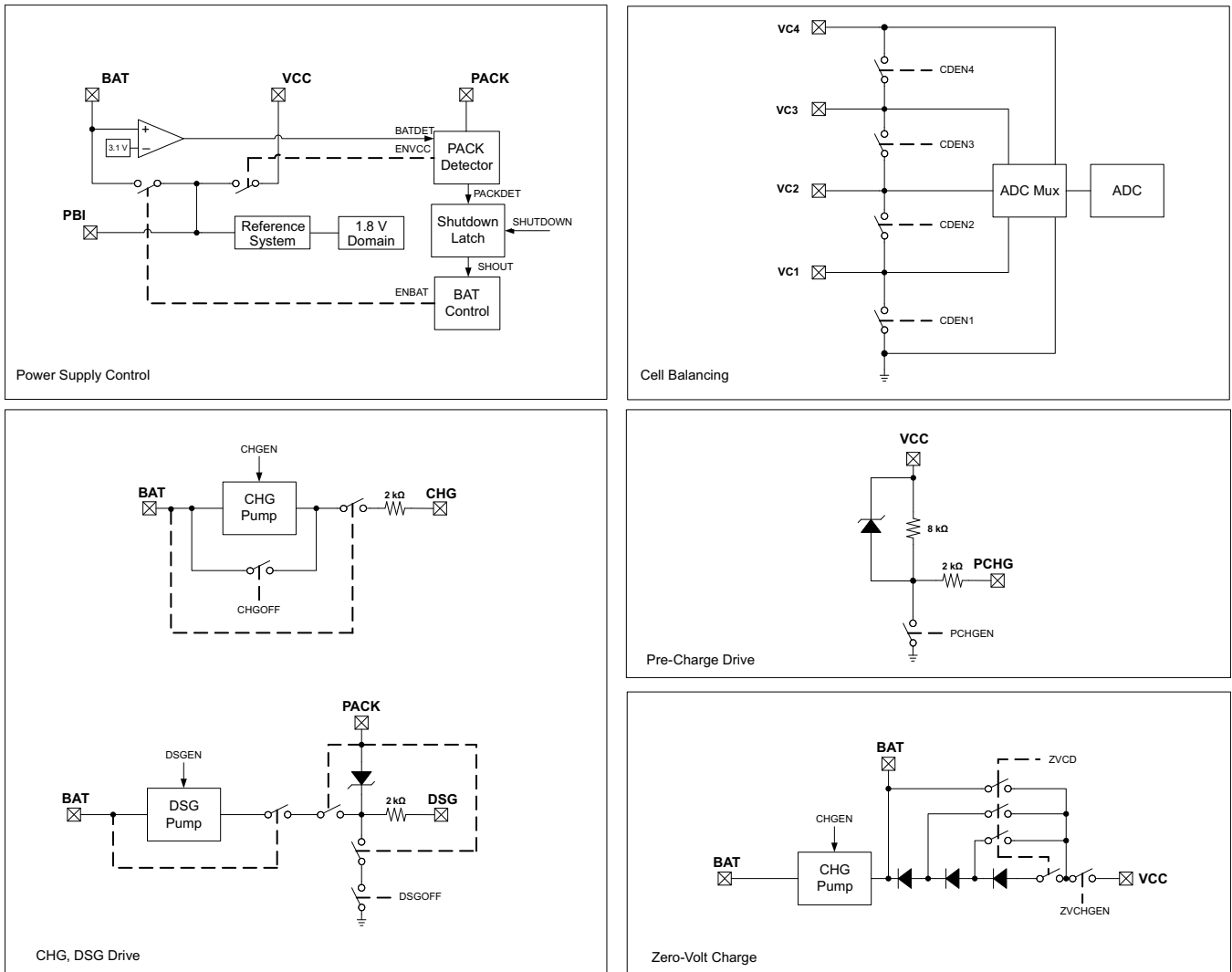
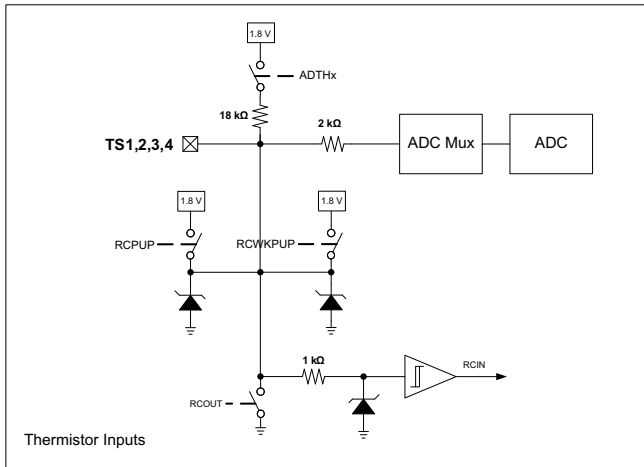
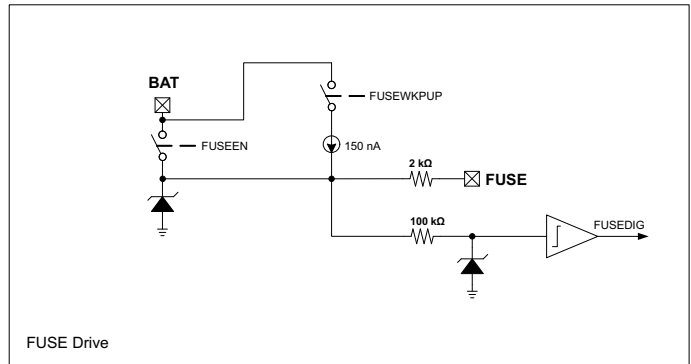


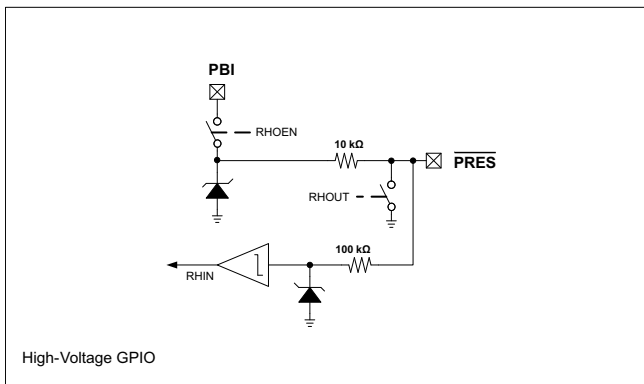
Figure 1. Pin Equivalent Diagram 1



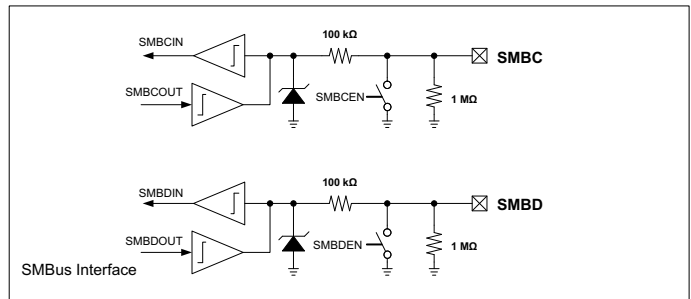
Thermistor Inputs



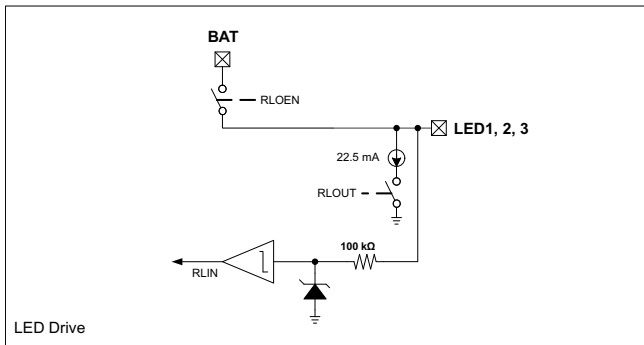
FUSE Drive



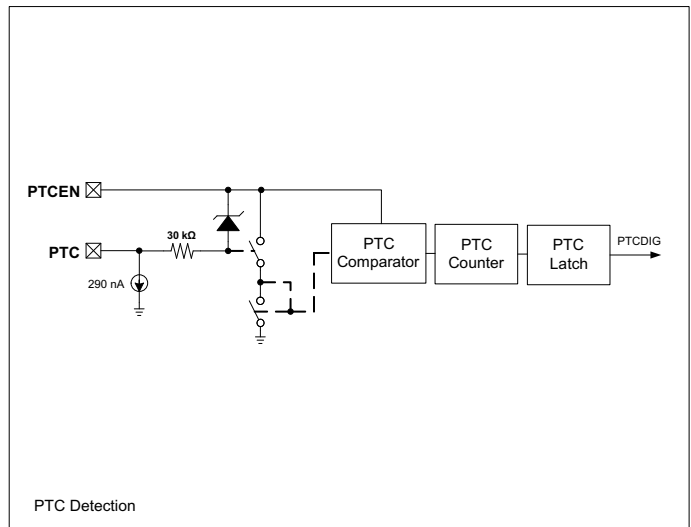
High-Voltage GPIO



SMBus Interface



LED Drive



PTC Detection

Figure 2. Pin Equivalent Diagram 2

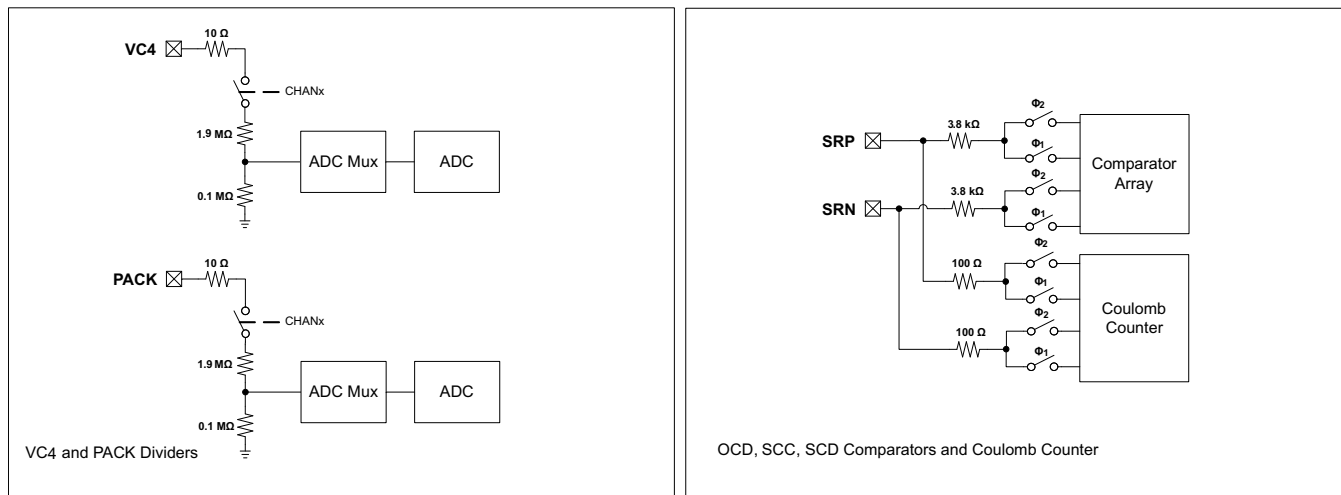


Figure 3. Pin Equivalent Diagram 3

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range, V <sub>CC</sub>	BAT, VCC, PBI	-0.3	30	V
Input voltage range, V <sub>IN</sub>	PACK, SMBC, SMBD, $\overline{\text{PRES}}$ or $\overline{\text{SHUTDN}}$ , BTP_INT, $\overline{\text{DISP}}$	-0.3	30	V
	TS1, TS2, TS3, TS4	-0.3	V <sub>REG</sub> + 0.3	V
	PTC, PTCEN, LEDCNTLA, LEDCNTLB, LEDCNTLC	-0.3	V <sub>BAT</sub> + 0.3	V
	SRP, SRN	-0.3	0.3	V
	VC4	VC3 - 0.3	VC3 + 8.5 V, or VSS + 30	V
	VC3	VC2 - 0.3	VC2 + 8.5 V, or VSS + 30	V
	VC2	VC1 - 0.3	VC1 + 8.5 V, or VSS + 30	V
Output voltage range, V <sub>O</sub>	CHG, DSG	-0.3	32	
	PCHG, FUSE	-0.3	30	V
Maximum VSS current, I <sub>SS</sub>			50	mA
T <sub>STG</sub>	Storage temperature	-65	150	°C
Lead temperature (soldering, 10 s), T <sub>SOLDER</sub>			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	BAT, VCC, PBI	2.2		26	V
$V_{SHUTDOWN-}$	Shutdown voltage	$V_{PACK} < V_{SHUTDOWN-}$	1.8	2.0	2.2	V
$V_{SHUTDOWN+}$	Start-up voltage	$V_{PACK} > V_{SHUTDOWN-} + V_{HYS}$	2.05	2.25	2.45	V
$V_{HYS}$	Shutdown voltage hysteresis	$V_{SHUTDOWN+} - V_{SHUTDOWN-}$		250		mV
$V_{IN}$	Input voltage range	PACK, SMBC, SMBD, $\overline{PRES}$ , BTP_IN, $\overline{DISP}$			26	V
		TS1, TS2, TS3, TS4			$V_{REG}$	
		PTC, PTCEN, LEDCNTLA, LEDCNTLB, LEDCNTLC			$V_{BAT}$	
		SRP, SRN	-0.2		0.2	
		VC4	$V_{VC3}$		$V_{VC3} + 5$	
		VC3	$V_{VC2}$		$V_{VC2} + 5$	
		VC2	$V_{VC1}$		$V_{VC1} + 5$	
	VC1	$V_{VSS}$		$V_{VSS} + 5$		
$V_O$	Output voltage range	CHG, DSG, PCHG, FUSE			26	V
$C_{PBI}$	External PBI capacitor		2.2			$\mu\text{F}$
$T_{OPR}$	Operating temperature		-40		85	$^\circ\text{C}$

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq4050		UNIT
		RSM (QFN)		
		32 PINS		
$R_{\theta JA, \text{High K}}$	Junction-to-ambient thermal resistance	47.4		$^\circ\text{C}/\text{W}$
$R_{\theta JC(\text{top})}$	Junction-to-case(top) thermal resistance	40.3		$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7		$^\circ\text{C}/\text{W}$
$\psi_{JT}$	Junction-to-top characterization parameter	0.8		$^\circ\text{C}/\text{W}$
$\psi_{JB}$	Junction-to-board characterization parameter	14.4		$^\circ\text{C}/\text{W}$
$R_{\theta JC(\text{bottom})}$	Junction-to-case(bottom) thermal resistance	3.8		$^\circ\text{C}/\text{W}$

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, [SPRA953](#).

### 6.5 Electrical Characteristics: Supply Current

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $20\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{NORMAL}$	NORMAL mode	CHG on, DSG on, no Flash write		336		$\mu\text{A}$
$I_{SLEEP}$	SLEEP mode	CHG off, DSG on, no SBS communication		75		$\mu\text{A}$
		CHG off, DSG off, no SBS communication		52		
$I_{SHUTDOWN}$	SHUTDOWN mode			1.6		$\mu\text{A}$



## 6.6 Electrical Characteristics: Power Supply Control

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{SWITCHOVER-}}$	BAT to $V_{CC}$ switchover voltage	$V_{\text{BAT}} < V_{\text{SWITCHOVER-}}$	1.95	2.1	2.2	V
$V_{\text{SWITCHOVER+}}$	$V_{CC}$ to BAT switchover voltage	$V_{\text{BAT}} > V_{\text{SWITCHOVER-}} + V_{\text{HYS}}$	2.9	3.1	3.25	V
$V_{\text{HYS}}$	Switchover voltage hysteresis	$V_{\text{SWITCHOVER+}} - V_{\text{SWITCHOVER-}}$		1000		mV
$I_{\text{LKG}}$	Input Leakage current	BAT pin, BAT = 0 V, $V_{CC} = 25\text{ V}$ , PACK = 25 V			1	$\mu\text{A}$
		PACK pin, BAT = 25 V, $V_{CC} = 0\text{ V}$ , PACK = 0 V			1	
		BAT and PACK terminals, BAT = 0 V, $V_{CC} = 0\text{ V}$ , PACK = 0 V, PBI = 25 V			1	
$R_{\text{PD}}$	Internal pulldown resistance	PACK	30	40	50	$\text{k}\Omega$

## 6.7 Electrical Characteristics: AFE Power-On Reset

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{REGIT-}}$	Negative-going voltage input	$V_{\text{REG}}$	1.51	1.55	1.59	V
$V_{\text{HYS}}$	Power-on reset hysteresis	$V_{\text{REGIT+}} - V_{\text{REGIT-}}$	70	100	130	mV
$t_{\text{RST}}$	Power-on reset time		200	300	400	$\mu\text{s}$

## 6.8 Electrical Characteristics: AFE Watchdog Reset and Wake Timer

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{WDT}}$	AFE watchdog timeout	$t_{\text{WDT}} = 500$	372	500	628	ms
		$t_{\text{WDT}} = 1000$	744	1000	1256	
		$t_{\text{WDT}} = 2000$	1488	2000	2512	
		$t_{\text{WDT}} = 4000$	2976	4000	5024	
$t_{\text{WAKE}}$	AFE wake timer	$t_{\text{WAKE}} = 250$	186	250	314	ms
		$t_{\text{WAKE}} = 500$	372	500	628	
		$t_{\text{WAKE}} = 1000$	744	1000	1256	
		$t_{\text{WAKE}} = 512$	1488	2000	2512	
$t_{\text{FETOFF}}$	FET off delay after reset	$t_{\text{FETOFF}} = 512$	409	512	614	ms

## 6.9 Electrical Characteristics: Current Wake Comparator

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{WAKE}}$	Wake voltage threshold	$V_{\text{WAKE}} = \pm 0.625\text{ mV}$	$\pm 0.3$	$\pm 0.625$	$\pm 0.9$	mV
		$V_{\text{WAKE}} = \pm 1.25\text{ mV}$	$\pm 0.6$	$\pm 1.25$	$\pm 1.8$	
		$V_{\text{WAKE}} = \pm 2.5\text{ mV}$	$\pm 1.2$	$\pm 2.5$	$\pm 3.6$	
		$V_{\text{WAKE}} = \pm 5\text{ mV}$	$\pm 2.4$	$\pm 5.0$	$\pm 7.2$	

### Electrical Characteristics: Current Wake Comparator (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{WAKE(DRIFT)}}$	Temperature drift of $V_{\text{WAKE}}$ accuracy		0.5%		$^\circ\text{C}$
$t_{\text{WAKE}}$	Time from application of current to wake interrupt			700	$\mu\text{s}$
$t_{\text{WAKE(SU)}}$	Wake comparator startup time		500	1000	$\mu\text{s}$

### 6.10 Electrical Characteristics: VC1, VC2, VC3, VC4, BAT, PACK

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
K	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3	0.1980	0.2000	0.2020	—	
	BAT–VSS, PACK–VSS	0.049	0.050	0.051		
	$V_{\text{REF2}}$	0.490	0.500	0.510		
$V_{\text{IN}}$	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3	–0.2		5	V	
	BAT–VSS, PACK–VSS	–0.2		20		
$I_{\text{LKG}}$	VC1, VC2, VC3, VC4, cell balancing off, cell detach detection off, ADC multiplexer off			1	$\mu\text{A}$	
$R_{\text{CB}}$	Internal cell balance resistance	$R_{\text{DS(ON)}}$ for internal FET switch at $2\text{ V} < V_{\text{DS}} < 4\text{ V}$			200	$\Omega$
$I_{\text{CD}}$	Internal cell detach check current	$V_{\text{Cx}} > V_{\text{SS}} + 0.8\text{ V}$	30	50	70	$\mu\text{A}$

### 6.11 Electrical Characteristics: SMBD, SMBC

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{\text{IH}}$	Input voltage high	SMBC, SMBD, $V_{\text{REG}} = 1.8\text{ V}$			1.3	V
$V_{\text{IL}}$	Input voltage low	SMBC, SMBD, $V_{\text{REG}} = 1.8\text{ V}$			0.8	V
$V_{\text{OL}}$	Output low voltage	SMBC, SMBD, $V_{\text{REG}} = 1.8\text{ V}$ , $I_{\text{OL}} = 1.5\text{ mA}$			0.4	V
$C_{\text{IN}}$	Input capacitance		5		pF	
$I_{\text{LKG}}$	Input leakage current			1	$\mu\text{A}$	
$R_{\text{PD}}$	Pulldown resistance	0.7	1.0	1.3	M $\Omega$	

### 6.12 Electrical Characteristics: $\overline{\text{PRES}}$ , $\overline{\text{BTP\_INT}}$ , $\overline{\text{DISP}}$

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{\text{IH}}$	High-level input				1.3	V
$V_{\text{IL}}$	Low-level input				0.55	V
$V_{\text{OH}}$	Output voltage high	$V_{\text{BAT}} > 5.5\text{ V}$ , $I_{\text{OH}} = -0\text{ }\mu\text{A}$			3.5	V
		$V_{\text{BAT}} > 5.5\text{ V}$ , $I_{\text{OH}} = -10\text{ }\mu\text{A}$			1.8	
$V_{\text{OL}}$	Output voltage low	$I_{\text{OL}} = 1.5\text{ mA}$			0.4	V
$C_{\text{IN}}$	Input capacitance		5		pF	
$I_{\text{LKG}}$	Input leakage current			1	$\mu\text{A}$	

**Electrical Characteristics:  $\overline{\text{PRES}}$ ,  $\overline{\text{BTP\_INT}}$ ,  $\overline{\text{DISP}}$  (continued)**

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_O$	Output reverse resistance Between $\overline{\text{PRES}}$ or $\overline{\text{BTP\_INT}}$ or $\overline{\text{DISP}}$ and PBI	8			k $\Omega$

**6.13 Electrical Characteristics: LEDCNTLA, LEDCNTLB, LEDCNTLC**

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input	1.45			V
$V_{IL}$	Low-level input			0.55	V
$V_{OH}$	Output voltage high $V_{BAT} > 3.0\text{ V}$ , $I_{OH} = -22.5\text{ mA}$	$V_{BAT} - 1.6$			V
$V_{OL}$	Output voltage low $I_{OL} = 1.5\text{ mA}$			0.4	V
$I_{SC}$	High level output current protection	-30	-45	-6 0	mA
$I_{OL}$	Low level output current $V_{BAT} > 3.0\text{ V}$ , $V_{OH} = 0.4\text{ V}$	15.75	22.5	29.25	mA
$I_{LEDCNTLx}$	Current matching between LEDCNTLx $V_{BAT} = V_{LEDCNTLx} + 2.5\text{ V}$		$\pm 1\%$		
$C_{IN}$	Input capacitance		20		pF
$I_{LKG}$	Input leakage current			1	$\mu\text{A}$
$f_{LEDCNTLx}$	Frequency of LED pattern		124		Hz

**6.14 Electrical Characteristics: Coulomb Counter**

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		-0.1		0.1	V
Full scale range		$-V_{REF1}/10$		$V_{REF1}/10$	V
Integral nonlinearity <sup>(1)</sup>	16-bit, best fit over input voltage range		$\pm 5.2$	$\pm 22.3$	LSB
Offset error	16-bit, Post-calibration		$\pm 5$	$\pm 10$	$\mu\text{V}$
Offset error drift	15-bit + sign, Post-calibration		0.2	0.3	$\mu\text{V}/^\circ\text{C}$
Gain error	15-bit + sign, over input voltage range		$\pm 0.2\%$	$\pm 0.8\%$	FSR
Gain error drift	15-bit + sign, over input voltage range			150	PPM/ $^\circ\text{C}$
Effective input resistance		2.5			M $\Omega$

(1)  $1\text{ LSB} = V_{REF1}/(10 \times 2^N) = 1.215/(10 \times 2^{15}) = 3.71\text{ }\mu\text{V}$

**6.15 Electrical Characteristics: CC Digital Filter**

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion time	Single conversion		250		ms
Effective resolution	Single conversion	15			Bits

## 6.16 Electrical Characteristics: ADC

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	Internal reference ( $V_{REF1}$ )	-0.2		1	V
	External reference ( $V_{REG}$ )	-0.2		$0.8 \times V_{REG}$	
Full scale range	$V_{FS} = V_{REF1}$ or $V_{REG}$	$-V_{FS}$		$V_{FS}$	V
Integral nonlinearity <sup>(1)</sup>	16-bit, best fit, $-0.1\text{ V}$ to $0.8 \times V_{REF1}$			$\pm 6.6$	LSB
	16-bit, best fit, $-0.2\text{ V}$ to $-0.1\text{ V}$			$\pm 13.1$	
Offset error <sup>(2)</sup>	16-bit, Post-calibration, $V_{FS} = V_{REF1}$		$\pm 67$	$\pm 157$	$\mu\text{V}$
Offset error drift	16-bit, Post-calibration, $V_{FS} = V_{REF1}$		0.6	3	$\mu\text{V}/^\circ\text{C}$
Gain error	16-bit, $-0.1\text{ V}$ to $0.8 \times V_{FS}$		$\pm 0.2\%$	$\pm 0.8\%$	FSR
Gain error drift	16-bit, $-0.1\text{ V}$ to $0.8 \times V_{FS}$			150	PPM/ $^\circ\text{C}$
Effective input resistance		8			$\text{M}\Omega$

(1)  $1\text{ LSB} = V_{REF1}/(2^N) = 1.225/(2^{15}) = 37.4\ \mu\text{V}$  (when  $t_{CONV} = 31.25\text{ ms}$ )

(2) For VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3, VC4–VSS, PACK–VSS, and  $V_{REF1}/2$ , the offset error is multiplied by (1/ADC multiplexer scaling factor (K)).

## 6.17 Electrical Characteristics: ADC Digital Filter

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion time	Single conversion		31.25		ms
	Single conversion		15.63		
	Single conversion		7.81		
	Single conversion		1.95		
Resolution	No missing codes	16			Bits
Effective resolution	With sign, $t_{CONV} = 31.25\text{ ms}$	14	15		Bits
	With sign, $t_{CONV} = 15.63\text{ ms}$	13	14		
	With sign, $t_{CONV} = 7.81\text{ ms}$	11	12		
	With sign, $t_{CONV} = 1.95\text{ ms}$	9	10		

## 6.18 Electrical Characteristics: CHG, DSG FET Drive

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage ratio	$\text{Ratio}_{\text{DSG}} = (V_{\text{DSG}} - V_{\text{BAT}})/V_{\text{BAT}}$ , $2.2\text{ V} < V_{\text{BAT}} < 4.92\text{ V}$ , $10\text{ M}\Omega$ between PACK and DSG	2.133	2.333	2.433	—
	$\text{Ratio}_{\text{CHG}} = (V_{\text{CHG}} - V_{\text{BAT}})/V_{\text{BAT}}$ , $2.2\text{ V} < V_{\text{BAT}} < 4.92\text{ V}$ , $10\text{ M}\Omega$ between BAT and CHG	2.133	2.333	2.433	
$V_{(\text{FETON})}$	Output voltage, CHG and DSG on $V_{\text{DSG}(\text{ON})} = V_{\text{DSG}} - V_{\text{BAT}}$ , $4.92\text{ V} \leq V_{\text{BAT}} \leq 18\text{ V}$ , $10\text{ M}\Omega$ between PACK and DSG	10.5	11.5	12	V
	$V_{\text{CHG}(\text{ON})} = V_{\text{CHG}} - V_{\text{BAT}}$ , $4.92\text{ V} \leq V_{\text{BAT}} \leq 18\text{ V}$ , $10\text{ M}\Omega$ between BAT and CHG	10.5	11.5	12	
$V_{(\text{FETOFF})}$	Output voltage, CHG and DSG off $V_{\text{DSG}(\text{OFF})} = V_{\text{DSG}} - V_{\text{PACK}}$ , $10\text{ M}\Omega$ between PACK and DSG	-0.4		0.4	V
	$V_{\text{CHG}(\text{OFF})} = V_{\text{CHG}} - V_{\text{BAT}}$ , $10\text{ M}\Omega$ between BAT and CHG	-0.4		0.4	
$t_R$	Rise time $V_{\text{DSG}}$ from 0% to 35% $V_{\text{DSG}(\text{ON})(\text{TYP})}$ , $V_{\text{BAT}} \geq 2.2\text{ V}$ , $C_L = 4.7\text{ nF}$ between DSG and PACK, $5.1\text{ k}\Omega$ between DSG and $C_L$ , $10\text{ M}\Omega$ between PACK and DSG		200	500	$\mu\text{s}$
	$V_{\text{CHG}}$ from 0% to 35% $V_{\text{CHG}(\text{ON})(\text{TYP})}$ , $V_{\text{BAT}} \geq 2.2\text{ V}$ , $C_L = 4.7\text{ nF}$ between CHG and BAT, $5.1\text{ k}\Omega$ between CHG and $C_L$ , $10\text{ M}\Omega$ between BAT and CHG		200	500	

## Electrical Characteristics: CHG, DSG FET Drive (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_F$ Fall time	$V_{DSG}$ from $V_{DSG(ON)(TYP)}$ to $1\text{ V}$ , $V_{BAT} \geq 2.2\text{ V}$ , $C_L = 4.7\text{ nF}$ between DSG and PACK, $5.1\text{ k}\Omega$ between DSG and $C_L$ , $10\text{ M}\Omega$ between PACK and DSG		40	300	$\mu\text{s}$
	$V_{CHG}$ from $V_{CHG(ON)(TYP)}$ to $1\text{ V}$ , $V_{BAT} \geq 2.2\text{ V}$ , $C_L = 4.7\text{ nF}$ between CHG and BAT, $5.1\text{ k}\Omega$ between CHG and $C_L$ , $10\text{ M}\Omega$ between BAT and CHG		40	200	

## 6.19 Electrical Characteristics: PCHG FET Drive

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON)}$ Output voltage, PCHG on	$V_{PCHG(ON)} = V_{V_{CC}} - V_{PCHG}$ , $10\text{ M}\Omega$ between $V_{CC}$ and PCHG	6	7	8	V
$V_{(FETOFF)}$ Output voltage, PCHG off	$V_{PCHG(OFF)} = V_{V_{CC}} - V_{PCHG}$ , $10\text{ M}\Omega$ between $V_{CC}$ and PCHG	-0.4		0.4	V
$t_R$ Rise time	$V_{PCHG}$ from 10% to 90% $V_{PCHG(ON)(TYP)}$ , $V_{V_{CC}} \geq 8\text{ V}$ , $C_L = 4.7\text{ nF}$ between PCHG and $V_{CC}$ , $5.1\text{ k}\Omega$ between PCHG and $C_L$ , $10\text{ M}\Omega$ between $V_{CC}$ and CHG		40	200	$\mu\text{s}$
$t_F$ Fall time	$V_{PCHG}$ from 90% to 10% $V_{PCHG(ON)(TYP)}$ , $V_{V_{CC}} \geq 8\text{ V}$ , $C_L = 4.7\text{ nF}$ between PCHG and $V_{CC}$ , $5.1\text{ k}\Omega$ between PCHG and $C_L$ , $10\text{ M}\Omega$ between $V_{CC}$ and CHG		40	200	$\mu\text{s}$

## 6.20 Electrical Characteristics: FUSE Drive

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$ Output voltage high	$V_{BAT} \geq 8\text{ V}$ , $C_L = 1\text{ nF}$ , $I_{AFEFUSE} = 0\text{ }\mu\text{A}$	6	7	8.65	V
	$V_{BAT} < 8\text{ V}$ , $C_L = 1\text{ nF}$ , $I_{AFEFUSE} = 0\text{ }\mu\text{A}$	$V_{BAT} - 0.1$		$V_{BAT}$	
$V_{IH}$ High-level input		1.5	2.0	2.5	V
$I_{AFEFUSE(PU)}$ Internal pullup current	$V_{BAT} \geq 8\text{ V}$ , $V_{AFEFUSE} = V_{SS}$		150	330	nA
$R_{AFEFUSE}$ Output impedance		2	2.6	3.2	k $\Omega$
$C_{IN}$ Input capacitance			5		pF
$t_{DELAY}$ Fuse trip detection delay		128		256	$\mu\text{s}$
$t_{RISE}$ Fuse output rise time	$V_{BAT} \geq 8\text{ V}$ , $C_L = 1\text{ nF}$ , $V_{OH} = 0\text{ V}$ to $5\text{ V}$		5	20	$\mu\text{s}$

## 6.21 Electrical Characteristics: Internal Temperature Sensor

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TEMP}$ Internal temperature sensor voltage drift	$V_{TEMP}$	-1.9	-2.0	-2.1	mV/ $^\circ\text{C}$
	$V_{TEMP} - V_{TEMPN}$ , assured by design	0.177	0.178	0.179	

## 6.22 Electrical Characteristics: TS1, TS2, TS3, TS4

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range	TS1, TS2, TS3, TS4, $V_{BIAS} = V_{REF1}$	-0.2	$0.8 \times V_{REF1}$		V
		TS1, TS2, TS3, TS4, $V_{BIAS} = V_{REG}$	-0.2	$0.8 \times V_{REG}$		
$R_{NTC(PU)}$	Internal pullup resistance	TS1, TS2, TS3, TS4	14.4	18	21.6	k $\Omega$
$R_{NTC(DRIFT)}$	Resistance drift over temperature	TS1, TS2, TS3, TS4	-360	-280	-200	PPM/ $^\circ\text{C}$

## 6.23 Electrical Characteristics: PTC, PTCEN

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PTC(TRIP)}$	PTC trip resistance		1.2	2.5	3.95	M $\Omega$
$V_{PTC(TRIP)}$	PTC trip voltage	$V_{PTC(TRIP)} = V_{PTCEN} - V_{PTC}$	200	500	890	mV
$I_{PTC}$	Internal PTC current bias	$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	200	290	350	nA
$t_{PTC(Delay)}$	PTC delay time	$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	40	80	145	ms

## 6.24 Electrical Characteristics: Internal 1.8-V LDO

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REG}$	Regulator voltage		1.6	1.8	2.0	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG}/\Delta T_A$ , $I_{REG} = 10\text{ mA}$		$\pm 0.25\%$		
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG}/\Delta V_{BAT}$ , $V_{BAT} = 10\text{ mA}$	-0.6%		0.5%	
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG}/\Delta I_{REG}$ , $I_{REG} = 0\text{ mA}$ to $10\text{ mA}$	-1.5%		1.5%	
$I_{REG}$	Regulator output current limit	$V_{REG} = 0.9 \times V_{REG(NOM)}$ , $V_{IN} > 2.2\text{ V}$	20			mA
$I_{SC}$	Regulator short-circuit current limit	$V_{REG} = 0 \times V_{REG(NOM)}$	25	40	55	mA
$PSRR_{REG}$	Power supply rejection ratio	$\Delta V_{BAT}/\Delta V_{REG}$ , $I_{REG} = 10\text{ mA}$ , $V_{IN} > 2.5\text{ V}$ , $f = 10\text{ Hz}$		40		dB
$V_{SLEW}$	Slew rate enhancement voltage threshold	$V_{REG}$	1.58	1.65		V

## 6.25 Electrical Characteristics: High-Frequency Oscillator

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{HFO}$	Operating frequency			16.78		MHz
$f_{HFO(ERR)}$	Frequency error	$T_A = -20^\circ\text{C}$ to $70^\circ\text{C}$ , includes frequency drift	-2.5%	$\pm 0.25\%$	2.5%	
		$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , includes frequency drift	-3.5%	$\pm 0.25\%$	3.5%	
$t_{HFO(SU)}$	Start-up time	$T_A = -20^\circ\text{C}$ to $85^\circ\text{C}$ , oscillator frequency within $\pm 3\%$ of nominal			4	ms
		oscillator frequency within $\pm 3\%$ of nominal			100	$\mu\text{s}$

## 6.26 Electrical Characteristics: Low-Frequency Oscillator

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{LFO}$ Operating frequency			262.144		kHz
$f_{LFO(ERR)}$ Frequency error	$T_A = -20^\circ\text{C}$ to $70^\circ\text{C}$ , includes frequency drift	-1.5%	$\pm 0.25\%$	1.5%	
	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , includes frequency drift	-2.5	$\pm 0.25$	2.5	
$f_{LFO(FAIL)}$ Failure detection frequency		30	80	100	kHz

## 6.27 Electrical Characteristics: Voltage Reference 1

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REF1}$ Internal reference voltage	$T_A = 25^\circ\text{C}$ , after trim	1.21	1.215	1.22	V
$V_{REF1(DRIFT)}$ Internal reference voltage drift	$T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$ , after trim		$\pm 50$		PPM/ $^\circ\text{C}$
	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , after trim		$\pm 80$		

## 6.28 Electrical Characteristics: Voltage Reference 2

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REF2}$ Internal reference voltage	$T_A = 25^\circ\text{C}$ , after trim	1.22	1.225	1.23	V
$V_{REF2(DRIFT)}$ Internal reference voltage drift	$T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$ , after trim		$\pm 50$		PPM/ $^\circ\text{C}$
	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , after trim		$\pm 80$		

## 6.29 Electrical Characteristics: Instruction Flash

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data retention		10			Years
Flash programming write cycles		1000			Cycles
$t_{PROGWORD}$ Word programming time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			40	$\mu\text{s}$
$t_{MASSERASE}$ Mass-erase time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			40	ms
$t_{PAGEERASE}$ Page-erase time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			40	ms
$I_{FLASHREAD}$ Flash-read current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			2	mA
$I_{FLASHWRITE}$ Flash-write current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			5	mA
$I_{FLASHERASE}$ Flash-erase current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			15	mA

## 6.30 Electrical Characteristics: Data Flash

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data retention		10			Years
Flash programming write cycles		20000			Cycles
$t_{PROGWORD}$ Word programming time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			40	$\mu\text{s}$

## Electrical Characteristics: Data Flash (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{MASSERASE}}$	Mass-erase time $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			40	ms
$t_{\text{PAGEERASE}}$	Page-erase time $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			40	ms
$I_{\text{FLASHREAD}}$	Flash-read current $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			1	mA
$I_{\text{FLASHWRITE}}$	Flash-write current $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			5	mA
$I_{\text{FLASHERASE}}$	Flash-erase current $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$			15	mA

## 6.31 Electrical Characteristics: OCD, SCC, SCD1, SCD2 Current Protection Thresholds

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{OCD}}$	OCD detection threshold voltage range $V_{\text{OCD}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1	-16.6		-100	mV
	$V_{\text{OCD}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0	-8.3		-50	
$\Delta V_{\text{OCD}}$	OCD detection threshold voltage program step $V_{\text{OCD}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1		-5.56		mV
	$V_{\text{OCD}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0		-2.78		
$V_{\text{SCC}}$	SCC detection threshold voltage range $V_{\text{SCC}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1	44.4		200	mV
	$V_{\text{SCC}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0	22.2		100	
$\Delta V_{\text{SCC}}$	SCC detection threshold voltage program step $V_{\text{SCC}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1		22.2		mV
	$V_{\text{SCC}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0		11.1		
$V_{\text{SCD1}}$	SCD1 detection threshold voltage range $V_{\text{SCD1}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1	-44.4		-200	mV
	$V_{\text{SCD1}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0	-22.2		-100	
$\Delta V_{\text{SCD1}}$	SCD1 detection threshold voltage program step $V_{\text{SCD1}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1		-22.2		mV
	$V_{\text{SCD1}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0		-11.1		
$V_{\text{SCD2}}$	SCD2 detection threshold voltage range $V_{\text{SCD2}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1	-44.4		-200	mV
	$V_{\text{SCD2}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0	-22.2		-100	
$\Delta V_{\text{SCD2}}$	SCD2 detection threshold voltage program step $V_{\text{SCD2}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1		-22.2		mV
	$V_{\text{SCD2}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0		-11.1		
$V_{\text{OFFSET}}$	OCD, SCC, and SCDx offset error Post-trim	-2.5		2.5	mV
$V_{\text{SCALE}}$	OCD, SCC, and SCDx scale error No trim	-10%		10%	
	Post-trim	-5%		5%	



### 6.32 Timing Requirements: OCD, SCC, SCD1, SCD2 Current Protection Timing

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{\text{OCD}}$	OCD detection delay time		1		31	ms
$\Delta t_{\text{OCD}}$	OCD detection delay time program step			2		ms
$t_{\text{SCC}}$	SCC detection delay time		0		915	$\mu\text{s}$
$\Delta t_{\text{SCC}}$	SCC detection delay time program step			61		$\mu\text{s}$
$t_{\text{SCD1}}$	SCD1 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		915	$\mu\text{s}$
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		1850	
$\Delta t_{\text{SCD1}}$	SCD1 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		61		$\mu\text{s}$
		AFE PROTECTION CONTROL[SCDDx2] = 1		121		
$t_{\text{SCD2}}$	SCD2 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		458	$\mu\text{s}$
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		915	
$\Delta t_{\text{SCD2}}$	SCD2 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		30.5		$\mu\text{s}$
		AFE PROTECTION CONTROL[SCDDx2] = 1		61		
$t_{\text{DETECT}}$	Current fault detect time	$V_{\text{SRP}} - V_{\text{SRN}} = V_T - 3\text{ mV}$ for OCD, SCD1, and SC2, $V_{\text{SRP}} - V_{\text{SRN}} = V_T + 3\text{ mV}$ for SCC			160	$\mu\text{s}$
$t_{\text{ACC}}$	Current fault delay time accuracy	Max delay setting	-10%		10%	

### 6.33 Timing Requirements: SMBus

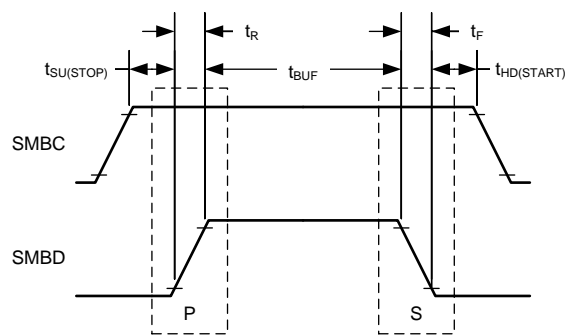
Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$f_{\text{SMB}}$	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
$f_{\text{MAS}}$	SMBus master clock frequency	MASTER mode, no clock low slave extend		51.2		kHz
$t_{\text{BUF}}$	Bus free time between start and stop		4.7			$\mu\text{s}$
$t_{\text{HD(START)}}$	Hold time after (repeated) start		4.0			$\mu\text{s}$
$t_{\text{SU(START)}}$	Repeated start setup time		4.7			$\mu\text{s}$
$t_{\text{SU(STOP)}}$	Stop setup time		4.0			$\mu\text{s}$
$t_{\text{HD(DATA)}}$	Data hold time		300			ns
$t_{\text{SU(DATA)}}$	Data setup time		250			ns
$t_{\text{TIMEOUT}}$	Error signal detect time		25		35	ms
$t_{\text{LOW}}$	Clock low period		4.7			$\mu\text{s}$
$t_{\text{HIGH}}$	Clock high period		4.0		50	$\mu\text{s}$
$t_{\text{R}}$	Clock rise time	10% to 90%			1000	ns
$t_{\text{F}}$	Clock fall time	90% to 10%			300	ns
$t_{\text{LOW(SEXT)}}$	Cumulative clock low slave extend time				25	ms
$t_{\text{LOW(MEXT)}}$	Cumulative clock low master extend time				10	ms

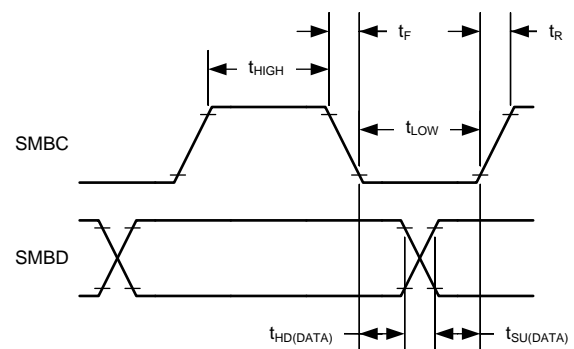
### 6.34 Timing Requirements: SMBus XL

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

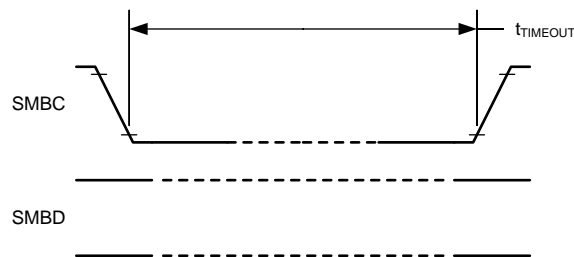
			MIN	NOM	MAX	UNIT
$f_{\text{SMBXL}}$	SMBus XL operating frequency	SLAVE mode	40		400	kHz
$t_{\text{BUF}}$	Bus free time between start and stop		4.7			$\mu\text{s}$
$t_{\text{HD(START)}}$	Hold time after (repeated) start		4.0			$\mu\text{s}$
$t_{\text{SU(START)}}$	Repeated start setup time		4.7			$\mu\text{s}$
$t_{\text{SU(STOP)}}$	Stop setup time		4.0			$\mu\text{s}$
$t_{\text{TIMEOUT}}$	Error signal detect time		5		20	ms
$t_{\text{LOW}}$	Clock low period				20	$\mu\text{s}$
$t_{\text{HIGH}}$	Clock high period				20	$\mu\text{s}$



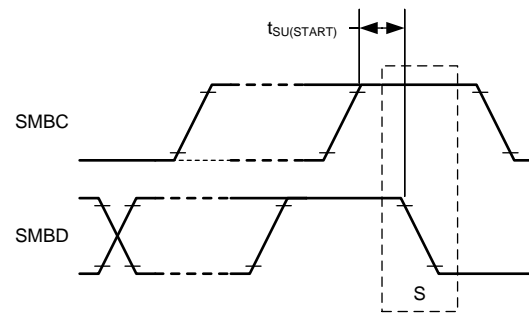
Start and Stop Condition



Wait and Hold Condition



Timeout Condition



Repeated Start Condition

Figure 4. SMBus Timing Diagram

### 6.35 Typical Characteristics

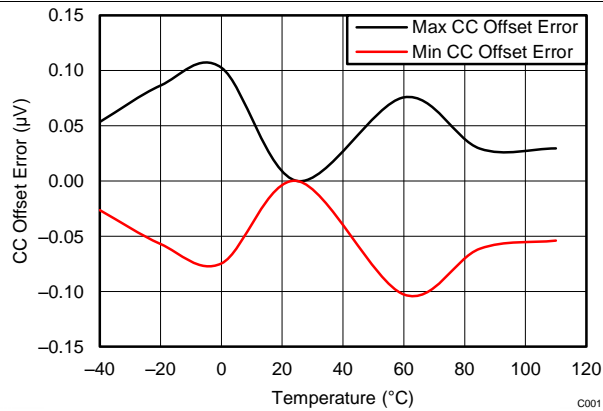


Figure 5. CC Offset Error vs. Temperature

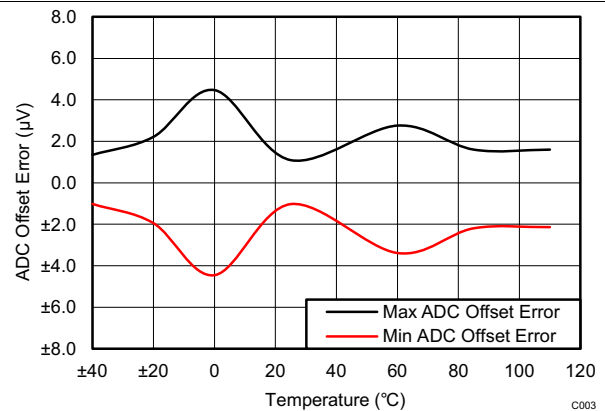


Figure 6. ADC Offset Error vs. Temperature

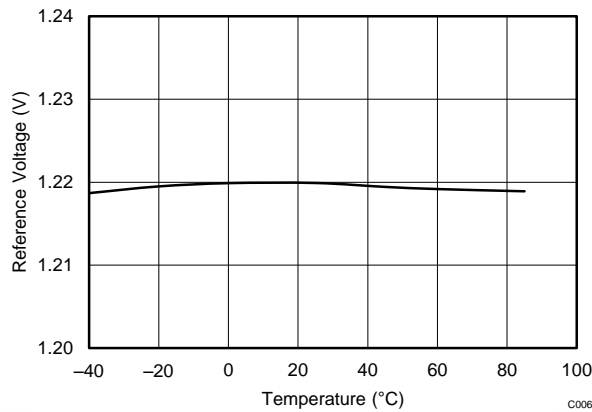


Figure 7. Reference Voltage vs. Temperature

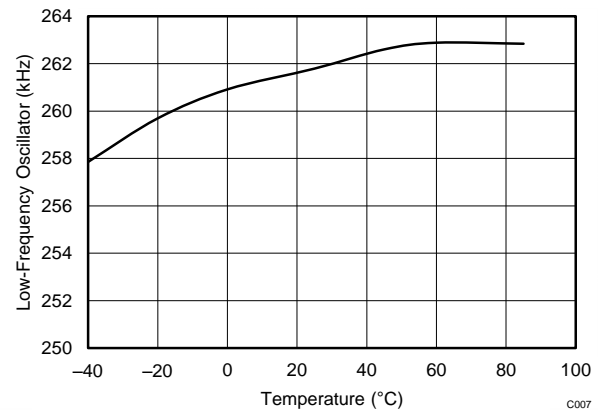


Figure 8. Low-Frequency Oscillator vs. Temperature

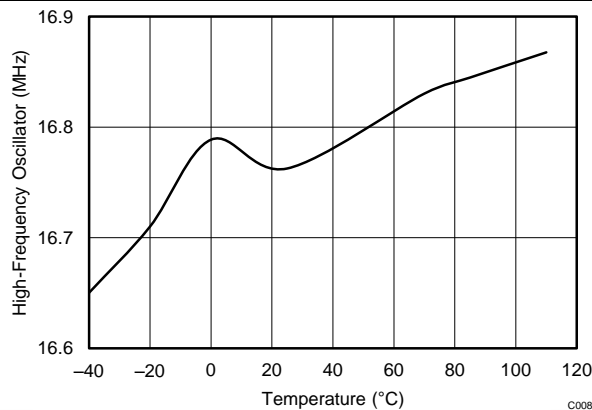
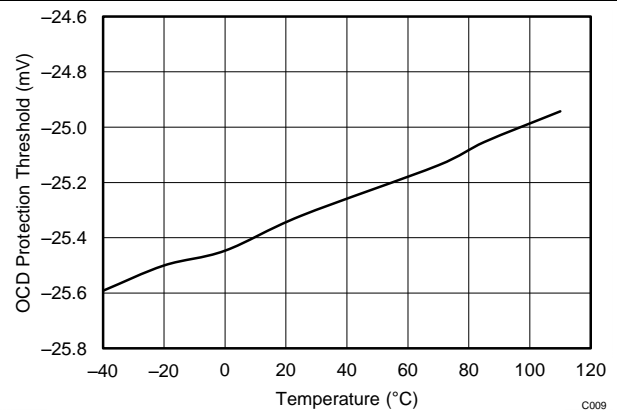


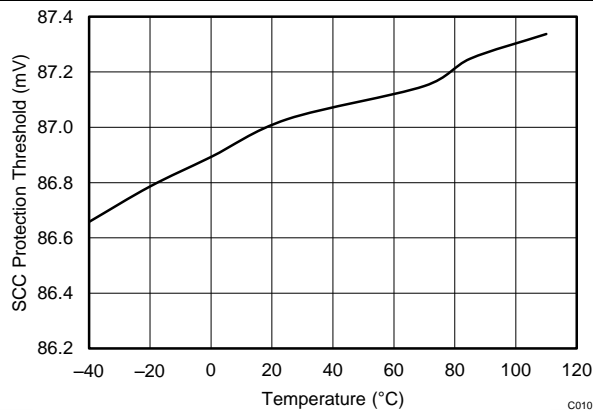
Figure 9. High-Frequency Oscillator vs. Temperature



Threshold setting is -25 mV.

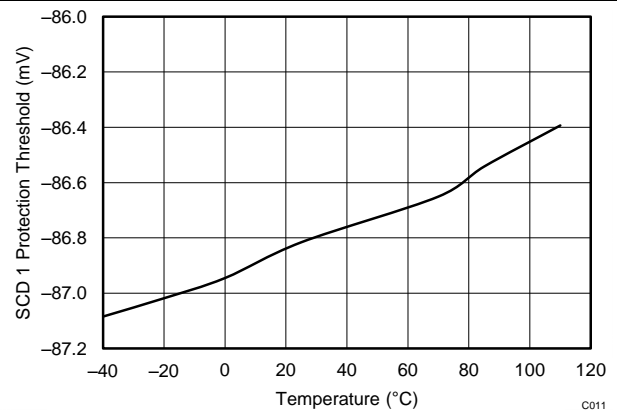
Figure 10. Overcurrent Discharge Protection Threshold vs. Temperature

Typical Characteristics (continued)



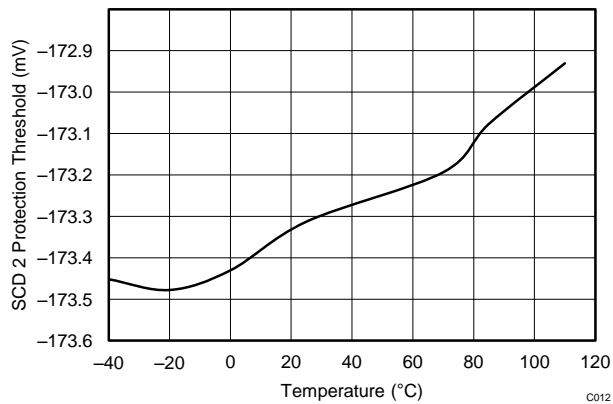
Threshold setting is 88.85 mV.

Figure 11. Short Circuit Charge Protection Threshold vs. Temperature



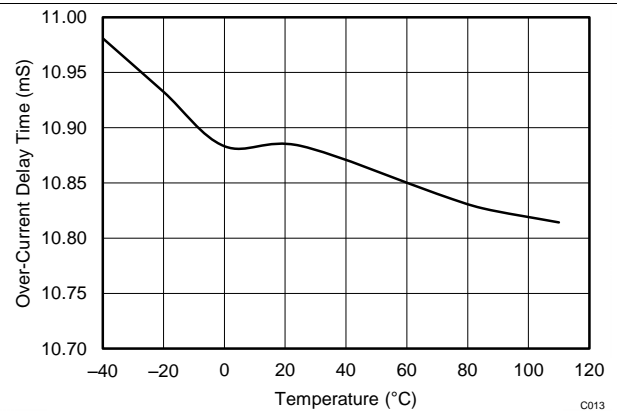
Threshold setting is -88.85 mV.

Figure 12. Short Circuit Discharge 1 Protection Threshold vs. Temperature



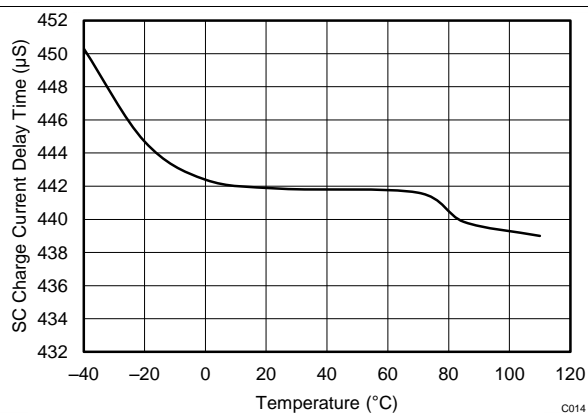
Threshold setting is -177.7 mV.

Figure 13. Short Circuit Discharge 2 Protection Threshold vs. Temperature



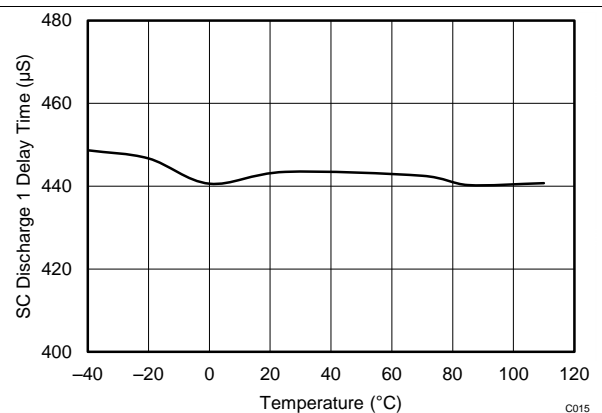
Threshold setting is 11 ms.

Figure 14. Overcurrent Delay Time vs. Temperature



Threshold setting is 465 µs.

Figure 15. Short Circuit Charge Current Delay Time vs. Temperature



Threshold setting is 465 µs (including internal delay).

Figure 16. Short Circuit Discharge 1 Delay Time vs. Temperature

Typical Characteristics (continued)

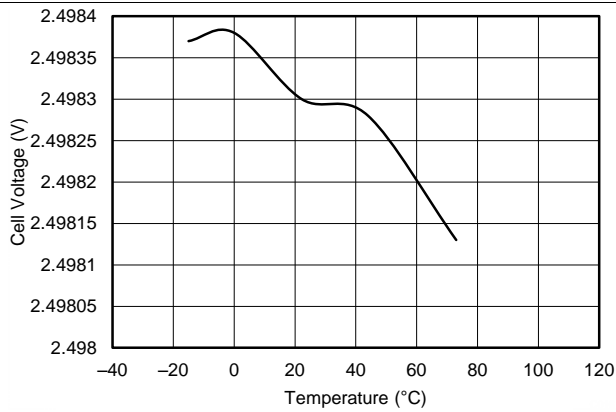
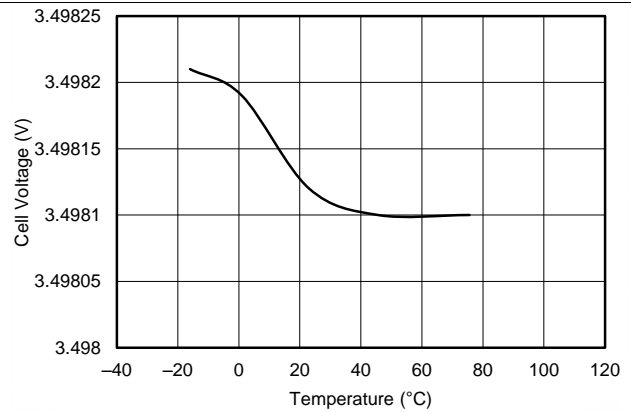
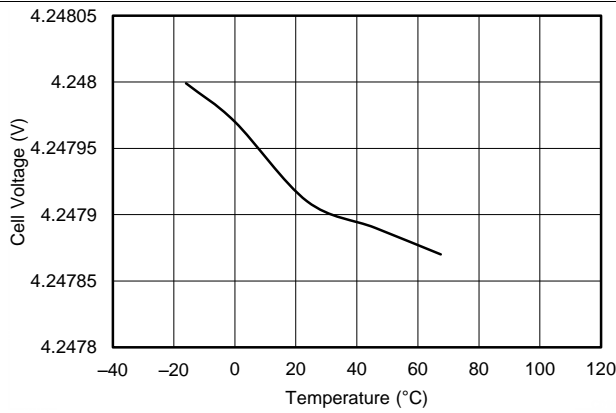


Figure 17.  $V_{CELL}$  Measurement at 2.5-V vs. Temperature



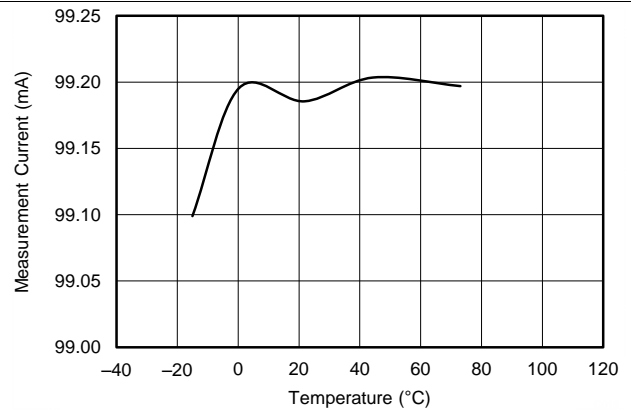
This is the  $V_{CELL}$  average for single cell.

Figure 18.  $V_{CELL}$  Measurement at 3.5-V vs. Temperature



This is the  $V_{CELL}$  average for single cell.

Figure 19.  $V_{CELL}$  Measurement at 4.25-V vs. Temperature



$I_{SET} = 100 \text{ mA}$

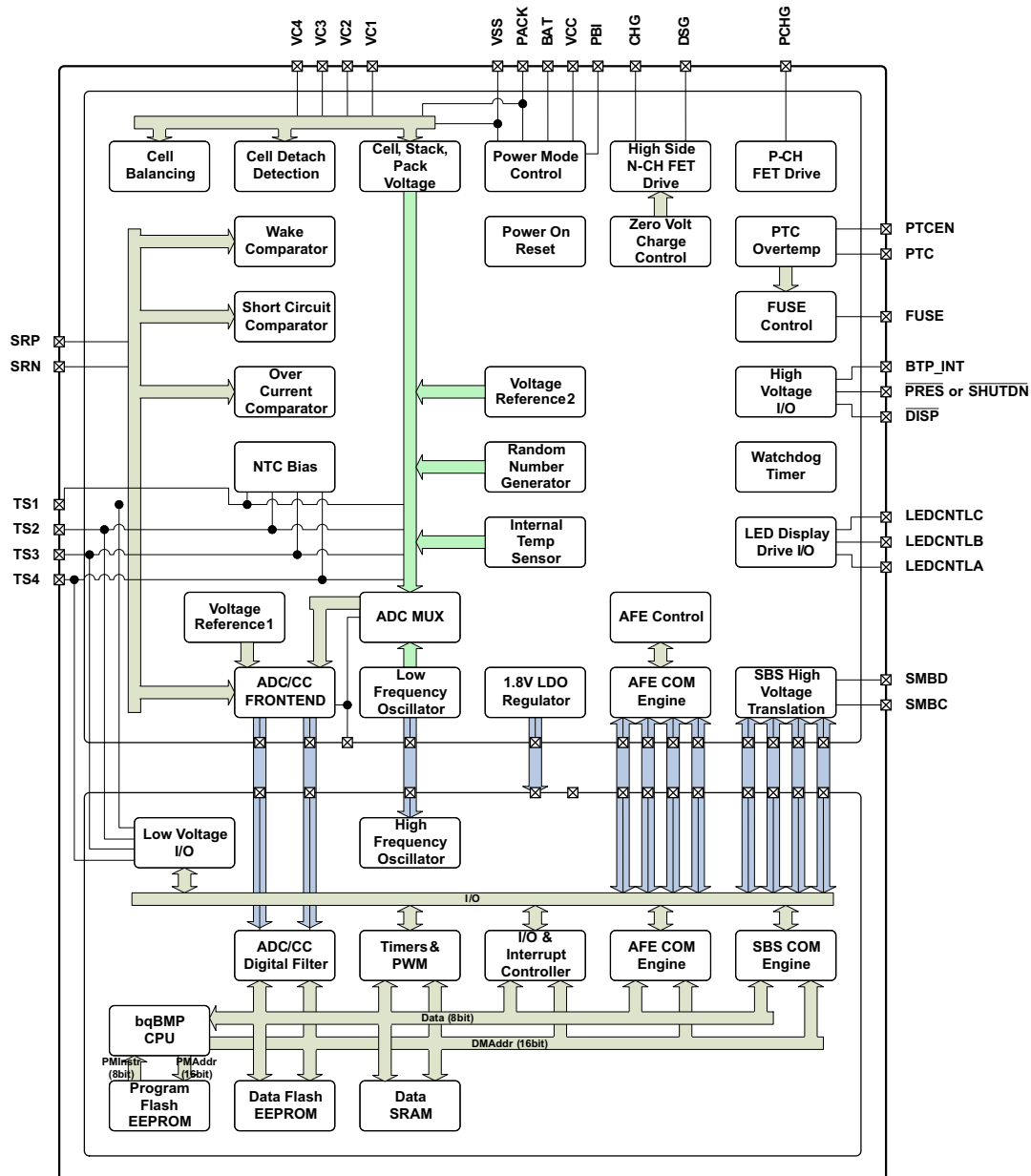
Figure 20.  $I$  Measured vs. Temperature

## 7 Detailed Description

### 7.1 Overview

The bq4050 device, incorporating Compensated End-of-Discharge Voltage (CEDV) technology, provides cell balancing while charging or at rest. This fully integrated, single-chip, pack-based solution, including a diagnostic lifetime data monitor and black box recorder, provides a rich array of features for gas gauging, protection, and authentication for 1-series, 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs.

### 7.2 Functional Block Diagram



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## 7.3 Feature Description

### 7.3.1 Primary (1st Level) Safety Features

The bq4050 gas gauge supports a wide range of battery and system protection features that can easily be configured. See the *bq4050 Technical Reference Manual* ([SLUUAQ3](#)) for detailed descriptions of each protection function.

The primary safety features include:

- Cell Overvoltage Protection
- Cell Undervoltage Protection
- Overcurrent in Charge Protection
- Overcurrent in Discharge Protection
- Overload in Discharge Protection
- Short Circuit in Charge Protection
- Short Circuit in Discharge Protection
- Overtemperature in Charge Protection
- Overtemperature in Discharge Protection
- Undertemperature in Charge Protection
- Undertemperature in Discharge Protection
- Overtemperature FET protection
- Precharge Timeout Protection
- Host Watchdog Timeout Protection
- Overcharge Protection
- Overcharging Voltage Protection
- Overcharging Current Protection
- Over Precharge Current Protection

### 7.3.2 Secondary (2nd Level) Safety Features

The secondary safety features of the bq4050 gas gauge can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. See the *bq4050 Technical Reference Manual* ([SLUUAQ3](#)) for detailed descriptions of each protection function.

The secondary safety features provide protection against:

- Safety Overvoltage Permanent Failure
- Safety Undervoltage Permanent Failure
- Safety Overtemperature Permanent Failure
- Safety FET Overtemperature Permanent Failure
- Fuse Failure Permanent Failure
- PTC Permanent Failure
- Voltage Imbalance at Rest (VIMR) Permanent Failure
- Voltage Imbalance Active (VIMA) Permanent Failure
- Charge FET Permanent Failure
- Discharge FET Permanent Failure
- AFE Register Permanent Failure
- AFE Communication Permanent Failure
- Second Level Protector Permanent Failure
- Instruction Flash Checksum Permanent Failure
- Open Cell Connection Permanent Failure
- Data Flash Permanent Failure
- Open Thermistor Permanent Failure

## Feature Description (continued)

### 7.3.3 Charge Control Features

The bq4050 gas gauge charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two subranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduces the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports precharging/0-volt charging
- Supports charge inhibit and charge suspend if the battery pack temperature is out of temperature range
- Reports charging fault and also indicates charge status via charge and discharge alarms

### 7.3.4 Gas Gauging

The bq4050 gas gauge uses the Compensated End-of-Discharge Voltage (CEDV) algorithm to measure and calculate the available capacity in battery cells. The bq4050 device accumulates a measure of charge and discharge currents, estimates self-discharge of the battery, and adjusts the self-discharge estimation based on temperature. See the *bq4050 Technical Reference Manual (SLUUAQ3)* for further details.

### 7.3.5 Configuration

#### 7.3.5.1 Oscillator Function

The bq4050 gas gauge fully integrates the system oscillators and does not require any external components to support this feature.

#### 7.3.5.2 System Present Operation

The bq4050 gas gauge checks the  $\overline{\text{PRES}}$  pin periodically (1 s). If  $\overline{\text{PRES}}$  input is pulled to ground by the external system, the bq4050 device detects this as system present.

#### 7.3.5.3 Emergency Shutdown

For battery maintenance, the emergency shutdown feature enables a push button action connecting the SHUTDOWN pin to shut down an embedded battery pack system before removing the battery. A high-to-low transition of the SHUTDOWN pin signals the bq4050 gas gauge to turn off the CHG and DSG FETs, disconnecting the power from the system to safely remove the battery pack. The CHG and DSG FETs can be turned on again by another high-to-low transition detected by the SHUTDOWN pin or when a data flash configurable timeout is reached.

#### 7.3.5.4 1-Series, 2-Series, 3-Series, or 4-Series Cell Configuration

In a 1-series cell configuration, VC4 is shorted to VC, VC2, and VC1. In a 2-series cell configuration, VC4 is shorted to VC3 and VC2. In a 3-series cell configuration, VC4 is shorted to VC3.

#### 7.3.5.5 Cell Balancing

The device reduces the charge difference of the battery cells in a fully charged state of the battery pack by gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation, and increases the usable pack energy by preventing premature charge termination.



## Feature Description (continued)

### 7.3.6 Battery Parameter Measurements

#### 7.3.6.1 Charge and Discharge Counting

The bq4050 gas gauge uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN terminals. The integrating ADC measures bipolar signals from  $-0.1\text{ V}$  to  $0.1\text{ V}$ . The bq4050 gauge detects charge activity when  $V_{SR} = V_{(SRP)} - V_{(SRN)}$  is positive, and discharge activity when  $V_{SR} = V_{(SRP)} - V_{(SRN)}$  is negative. The bq4050 gas gauge continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.26 nVh.

#### 7.3.7 Battery Trip Point (BTP)

Required for WIN8 OS, the battery trip point (BTP) feature indicates when the RSOC of a battery pack has depleted to a certain value set in a DF register. This feature enables a host to program two capacity-based thresholds that govern the triggering of a BTP interrupt on the BTP\_INT pin and the setting or clearing of the *OperationStatus[BTP\_INT]* on the basis of *RemainingCapacity()*.

An internal weak pullup is applied when the BTP feature is active. Depending on the system design, an external pullup may be required to put on the BTP\_INT pin. See *Electrical Characteristics: PRES, BTP\_INT, DISP* for details.

#### 7.3.8 Lifetime Data Logging Features

The bq4050 gas gauge offers lifetime data logging for several critical battery parameters. The following parameters are updated every 10 hours if a difference is detected between values in RAM and data flash:

- Maximum and Minimum Cell Voltages
- Maximum Delta Cell Voltage
- Maximum Charge Current
- Maximum Discharge Current
- Maximum Average Discharge Current
- Maximum Average Discharge Power
- Maximum and Minimum Cell Temperature
- Maximum Delta Cell Temperature
- Maximum and Minimum Internal Sensor Temperature
- Maximum FET Temperature
- Number of Safety Events Occurrences and the Last Cycle of the Occurrence
- Number of Valid Charge Termination and the Last Cycle of the Valid Charge Termination
- Number of Shutdown Events
- Cell Balancing Time for Each Cell  
(This data is updated every 2 hours if a difference is detected.)
- Total FW Runtime and Time Spent in Each Temperature Range  
(This data is updated every 2 hours if a difference is detected.)

#### 7.3.9 Authentication

The bq4050 gas gauge supports authentication by the host using SHA-1.

#### 7.3.10 LED Display

The bq4050 gas gauge can drive a 3-, 4-, or 5- segment LED display for remaining capacity indication and/or a permanent fail (PF) error code indication.

## Feature Description (continued)

### 7.3.11 Voltage

The bq4050 gas gauge updates the individual series cell voltages at 0.25-s intervals. The internal ADC of the bq4050 device measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the CEDV gas gauging.

### 7.3.12 Current

The bq4050 gas gauge uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 1-m $\Omega$  to 3-m $\Omega$  typ. sense resistor.

### 7.3.13 Temperature

The bq4050 gas gauge has an internal temperature sensor and inputs for four external temperature sensors. All five temperature sensor options can be individually enabled and configured for cell or FET temperature usage. Two configurable thermistor models are provided to enable monitoring of the cell temperature in addition to the FET temperature, which use a different thermistor profile.

### 7.3.14 Communications

The bq4050 gas gauge uses SMBus v1.1 with MASTER mode and packet error checking (PEC) options per the SBS specification.

#### 7.3.14.1 SMBus On and Off State

The bq4050 gas gauge detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing this state requires that either SMBC or SMBD transition high. The communication bus will resume activity within 1 ms.

#### 7.3.14.2 SBS Commands

See the *bq4050 Technical Reference Manual* ([SLUUAQ3](#)) for further details.

## 7.4 Device Functional Modes

The bq4050 gas gauge supports three power modes to reduce power consumption:

- In NORMAL mode, the bq4050 gauge performs measurements, calculations, protection decisions, and data updates in 250-ms intervals. Between these intervals, the bq4050 gauge is in a reduced power stage.
- In SLEEP mode, the bq4050 gauge performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq4050 gauge is in a reduced power stage. The bq4050 gauge has a wake function that enables exit from SLEEP mode when current flow or failure is detected.
- In SHUTDOWN mode, the bq4050 gauge is completely disabled.

## 8 Applications and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

---

### 8.1 Application Information

The bq4050 gas gauge has primary protection support to be used with a 1-series to 4-series Li-Ion/Li Polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, users need the Battery Management Studio ([bqStudio](#)) graphical user-interface tool installed on a PC during development. The firmware installed on the bqStudio tool has default values for this product, which are summarized in the *bq4050 Technical Reference Manual* ([SLUUAQ3](#)). Using the bqStudio tool, these default values can be changed to cater to specific application requirements during development once the system parameters, such as fault trigger thresholds for protection, enable/disable of certain features for operation, configuration of cells, chemistry that best matches the cell used, and more are known. This data is referred to as the "golden image."

## 8.2 Typical Applications

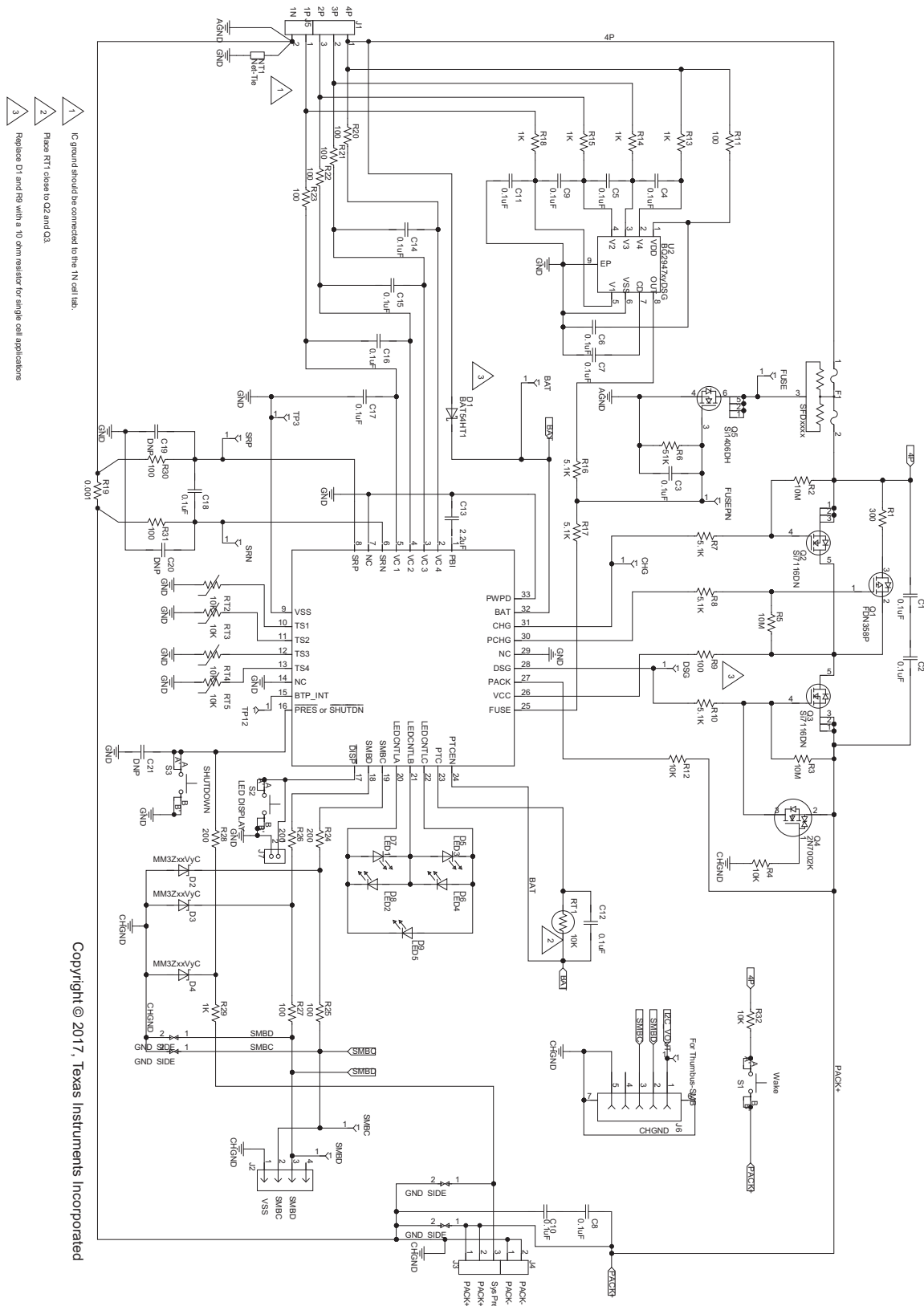


Figure 21. Application Schematic

## Typical Applications (continued)

### 8.2.1 Design Requirements

Table 1 shows the default settings for the main parameters. Use the [bqStudio](#) tool to update the settings to meet the specific application or battery pack configuration requirements.

The device should be calibrated before any gauging test. Follow the information in the bqStudio **Calibration** page to calibrate the device, and use the bqStudio **Chemistry** page to update the match chemistry profile to the device.

**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE
Cell Configuration	3s1p (3-series with 1 Parallel) <sup>(1)</sup>
Design Capacity	4400 mAh
Device Chemistry	1210 (LiCoO <sub>2</sub> /graphitized carbon)
Cell Overvoltage at Standard Temperature	4300 mV
Cell Undervoltage	2500 mV
Shutdown Voltage	2300 mV
Overcurrent in CHARGE Mode	6000 mA
Overcurrent in DISCHARGE Mode	–6000 mA
Short Circuit in CHARGE Mode	0.1 V/R <sub>sense</sub> across SRP, SRN
Short Circuit in DISCHARGE Mode	0.1 V/R <sub>sense</sub> across SRP, SRN
Safety Overvoltage	4500 mV
Cell Balancing	Disabled
Internal and External Temperature Sensor	External Temperature Sensors are used.
Undertemperature Charging	0°C
Undertemperature Discharging	0°C
BROADCAST Mode	Disabled
Battery Trip Point (BTP) with active high interrupt	Disabled

(1) When using the device the first time, if the a 1-s or 2-s battery pack is used, then a charger or power supply should be connected to the PACK+ terminal to prevent device shutdown. Then update the cell configuration (see the [bq4050 Technical Reference Manual \(SLUUAQ3\)](#) for details) before removing the charger connection.

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, and the sense resistor, and then returns to the PACK– terminal (see [Figure 22](#)). In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

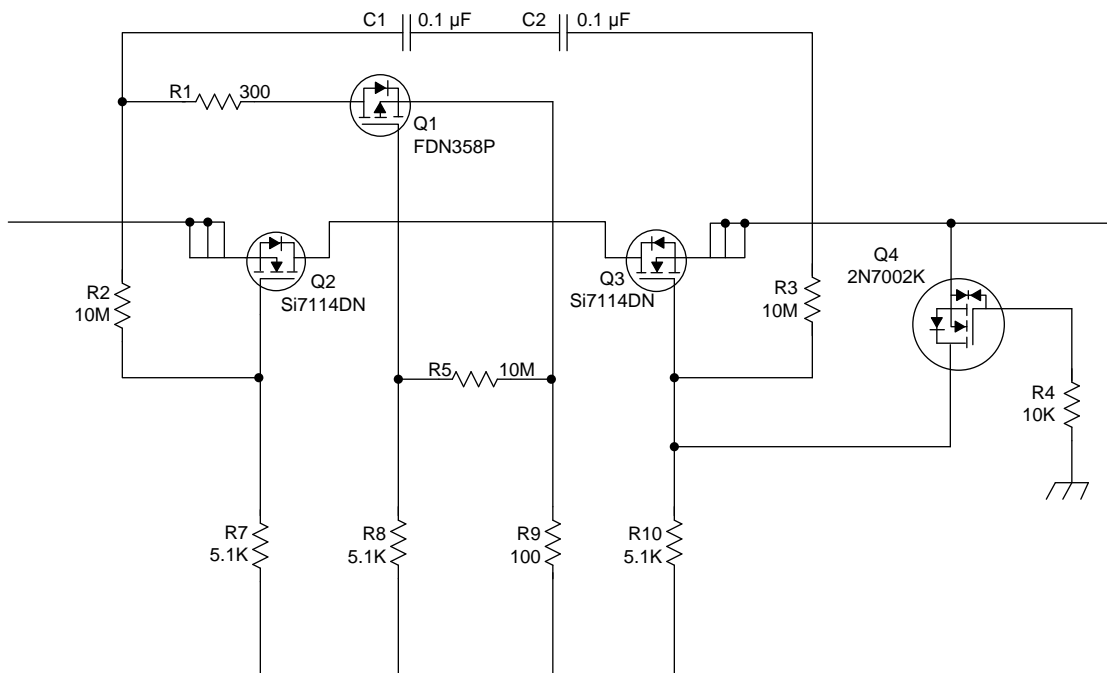
##### 8.2.2.1.1 Protection FETs

Select the N-CH charge and discharge FETs for a given application. Most portable battery applications are a good match for the CSD17308Q3. The TI CSD17308Q3 is a 47A, 30-V device with R<sub>ds(on)</sub> of 8.2 mΩ when the gate drive voltage is 8 V.

If a precharge FET is used, R1 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to  $(V_{\text{CHARGER}} - V_{\text{BAT}})/R1$  and maximum power dissipation is  $(V_{\text{charger}} - V_{\text{bat}})^2/R1$ .

The gates of all protection FETs are pulled to the source with a high-value resistor between the gate and source to ensure they are turned off if the gate drive is open.

Capacitors C1 and C2 help protect the FETs during an ESD event. Using two devices ensures normal operation if one becomes shorted. To have good ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage ratings of C1 and C2 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.



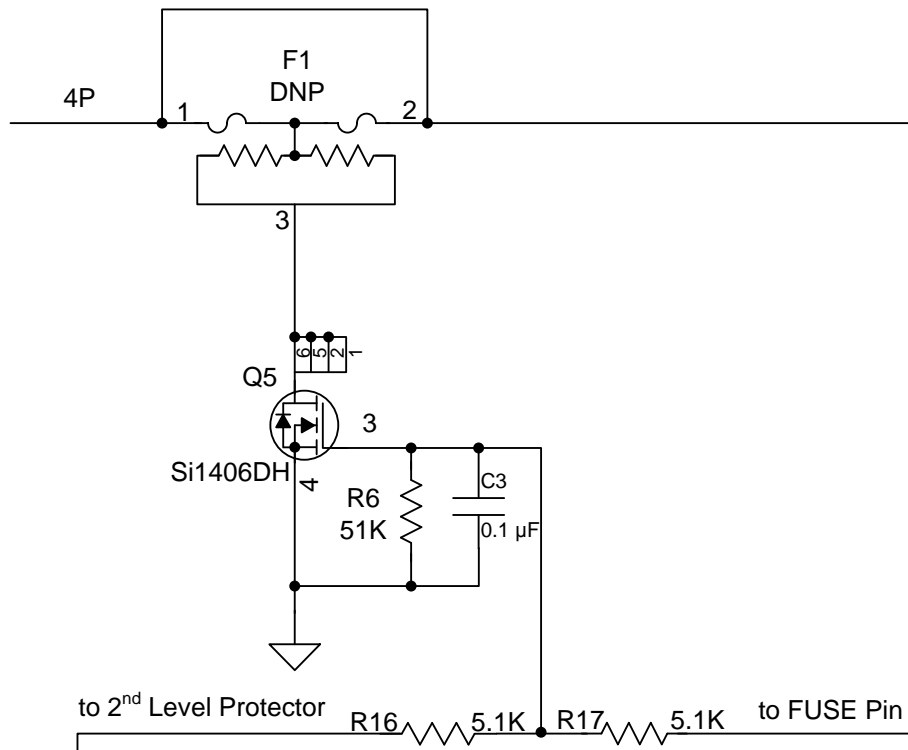
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**Figure 22. bq4050 Protection FETs**

### 8.2.2.1.2 Chemical Fuse

The chemical fuse (Dexerials, Uchihashi, and so on) is ignited under command from either the bq294700 secondary voltage protection IC or from the FUSE pin of the gas gauge. Either of these events applies a positive voltage to the gate of Q5, shown in [Figure 23](#), which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-CH FET. Ensure that the proper voltage, current, and  $R_{ds(on)}$  ratings are used for this device. The fuse control circuit is discussed in detail in [FUSE Circuitry](#).



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Figure 23. FUSE Circuit

### 8.2.2.1.3 Lithium-Ion Cell Connections

The important part to remember about the cell connections is that high current flows through the top and bottom connections; therefore, the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. The location marked 4P in Figure 24 indicates the Kelvin connection of the most positive battery node. The connection marked 1N is equally important. The VC5 pin (a ground reference for cell voltage measurement), which is in the older generation devices, is not in the bq4050 device. Therefore, the single-point connection at 1N to the low-current ground is needed to avoid an undesired voltage drop through long traces while the gas gauge is measuring the bottom cell voltage.

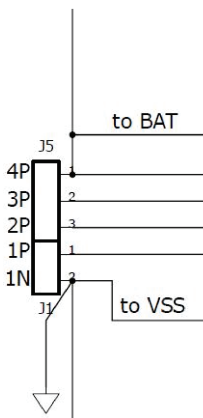
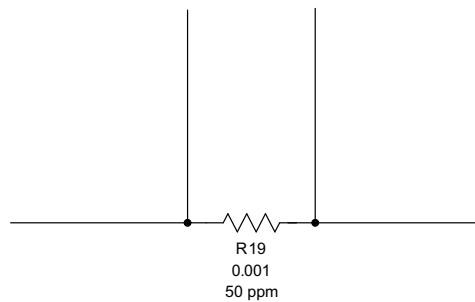


Figure 24. Lithium-Ion Cell Connections

#### 8.2.2.1.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq4050 gauge. Select the smallest value possible to minimize the negative voltage generated on the bq4050  $V_{SS}$  node(s) during a short circuit. This pin has an absolute minimum of  $-0.3$  V. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a  $1\text{-m}\Omega$  to  $3\text{-m}\Omega$  sense resistor.

The ground scheme of bq4050 gauge is different from the older generation devices. In previous devices, the device ground (or low current ground) is connected to the SRN side of the Rsense resistor pad. The bq4050 gauge, however, it connects the low-current ground on the SRP side of the Rsense resistor pad close to the battery 1N terminal (see [Lithium-Ion Cell Connections](#)). This is because the bq4050 gauge has one less VC pin (a ground reference pin VC5) compared to the previous devices. The pin was removed and was internally combined to SRP.



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**Figure 25. Sense Resistor**

#### 8.2.2.1.5 ESD Mitigation

A pair of series  $0.1\text{-}\mu\text{F}$  ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted.

Optionally, a tranzorb such as the SMBJ2A can be placed across the terminals to further improve ESD immunity.

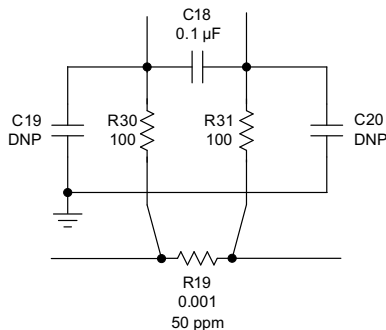
#### 8.2.2.2 Gas Gauge Circuit

The gas gauge circuit includes the bq4050 gauge and its peripheral components. These components are divided into the following groups: Differential Low-Pass Filter, PBI, system present, SMBus Communication, FUSE circuit, and LED.

##### 8.2.2.2.1 Coulomb-Counting Interface

The bq4050 gauge uses an integrating delta-sigma ADC for current measurements. Add a  $100\text{-}\Omega$  resistor from the sense resistor to the SRP and SRN inputs of the device. Place a  $0.1\text{-}\mu\text{F}$  (C18) filter capacitor across the SRP and SRN inputs. Optional  $0.1\text{-}\mu\text{F}$  filter capacitors (C19 and C20) can be added for additional noise filtering if required for a circuit.





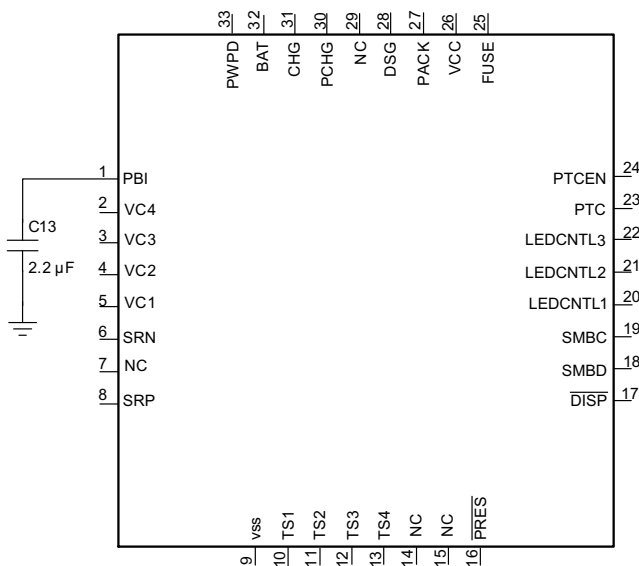
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Figure 26. Differential Filter

### 8.2.2.2.2 Power Supply Decoupling and PBI

The bq4050 gauge has an internal LDO that is internally compensated and does not require an external decoupling capacitor.

The PBI pin is used as a power supply backup input pin providing power during brief transient power outages. A standard 2.2-μF ceramic capacitor is connected from the PBI pin to ground as shown in Figure 27.

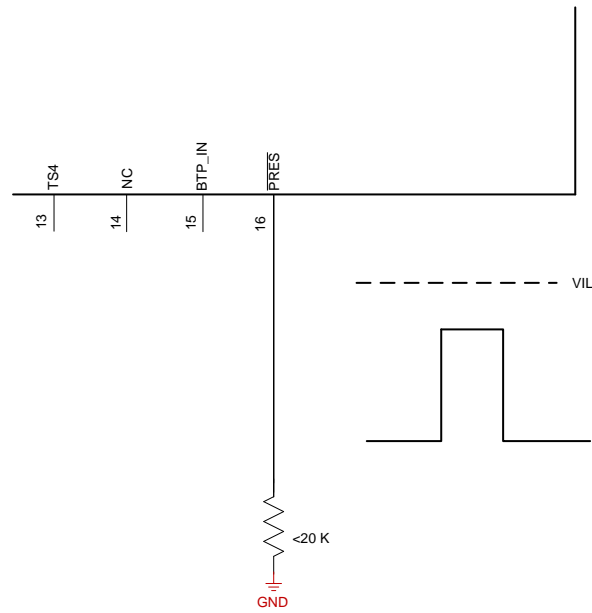


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Figure 27. Power Supply Decoupling

### 8.2.2.2.3 System Present

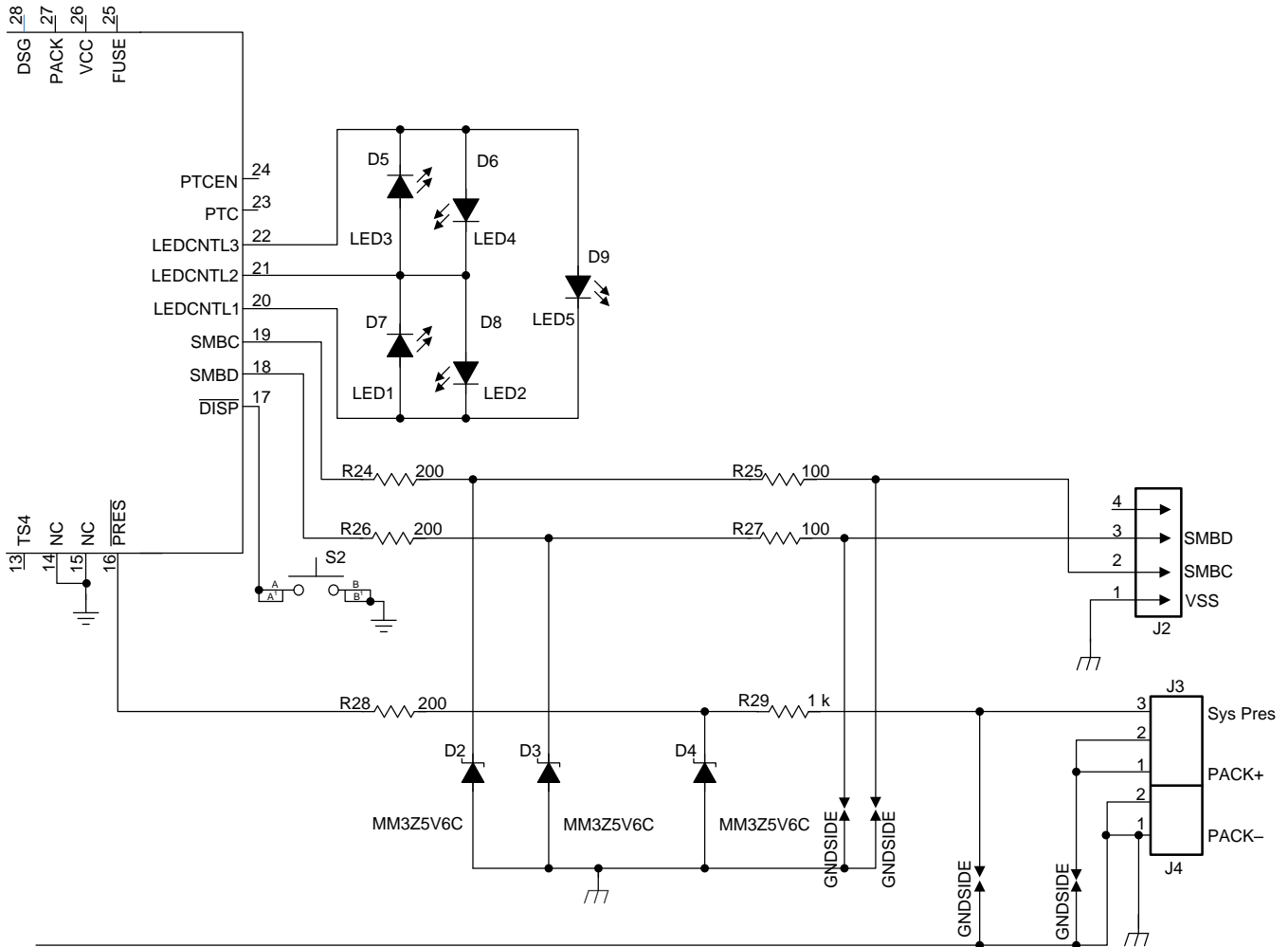
The system present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The PRES pin of the bq4050 gauge is occasionally sampled to test for system present. To save power, an internal pullup is provided by the gas gauge during a brief 4-μs sampling pulse once per second. A resistor can be used to pull the signal low and the resistance must be 20 kΩ or lower to ensure that the test pulse is lower than the VIL limit. The pullup current source is typically 10 μA to 20 μA.



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**Figure 28. System Present Pull-Down Resistor**

Because the system present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. An integrated ESD protection on the PRES device pin reduces the external protection requirement to just R29 for an 8-kV ESD contact rating. However, if it is possible that the system present signal may short to PACK+, then R28 and D4 must be included for high-voltage protection.



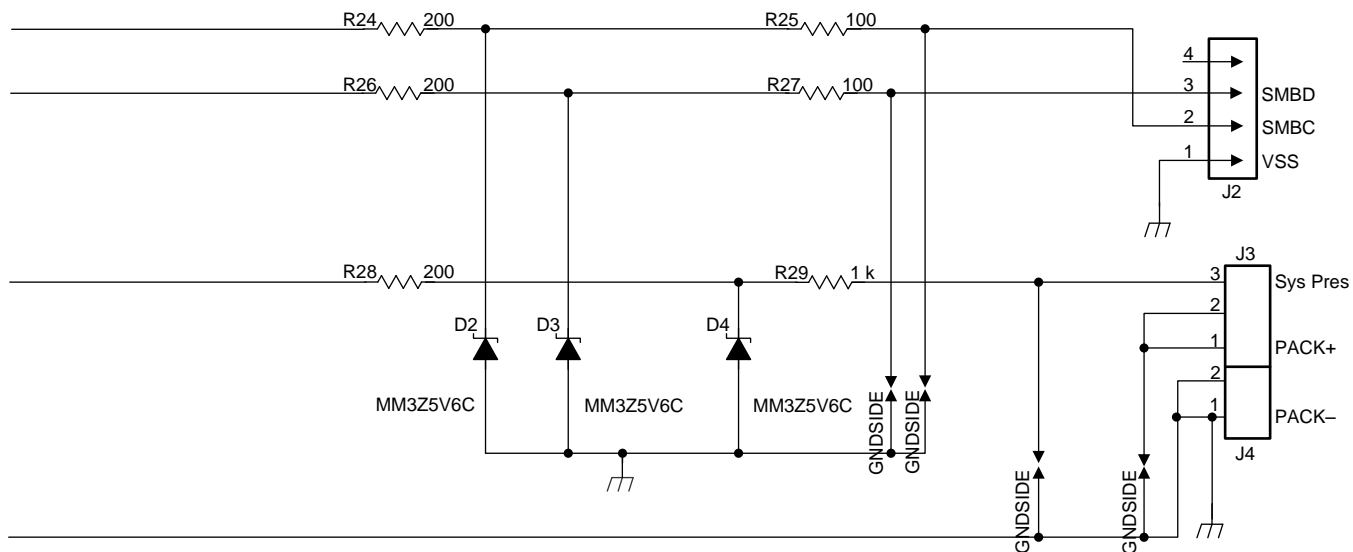
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Figure 29. System Present ESD and Short Protection

#### 8.2.2.2.4 SMBus Communication

The SMBus clock and data pins have integrated high-voltage ESD protection circuits; however, adding a Zener diode (D2 and D3) and series resistor (R24 and R26) provides more robust ESD performance.

The SMBus clock and data lines have internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into SLEEP mode to conserve power.



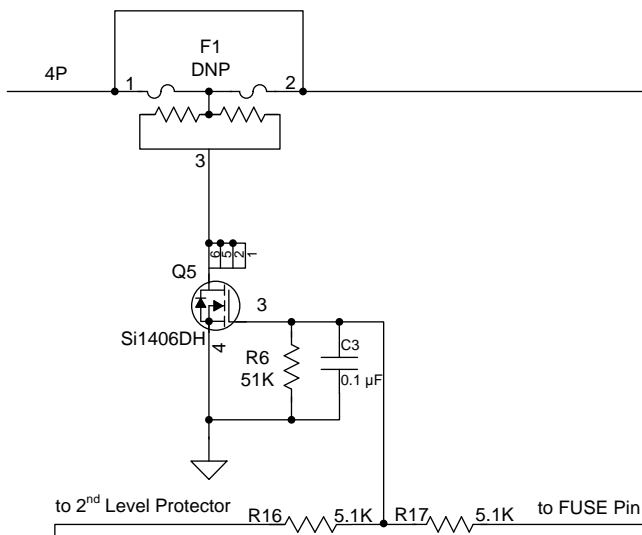
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**Figure 30. ESD Protection for SMB Communication**

**8.2.2.2.5 FUSE Circuitry**

The FUSE pin of the bq4050 gauge is designed to ignite the chemical fuse if one of the various safety criteria is violated. The FUSE pin also monitors the state of the secondary-voltage protection IC. Q5 ignites the chemical fuse when its gate is high. The 7-V output of the bq294700 is divided by R16 and R6, which provides adequate gate drive for Q5 while guarding against excessive back current into the bq294700 if the FUSE signal is high.

Using C3 is generally a good practice, especially for RFI immunity. C3 may be removed, if desired, because the chemical fuse is a comparatively slow device and is not affected by any submicrosecond glitches that come from the FUSE output during the cell connection process.



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**Figure 31. FUSE Circuit**

When the bq4050 gauge is commanded to ignite the chemical fuse, the FUSE pin activates to give a typical 8-V output. The new design makes it possible to use a higher Vgs FET for Q5. This improves the robustness of the system, as well as widens the choices for Q5.

### 8.2.2.3 Secondary-Current Protection

The bq4050 gauge provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, and voltage translation. The following discussion examines cell and battery inputs, pack and FET control, temperature output, and cell balancing.

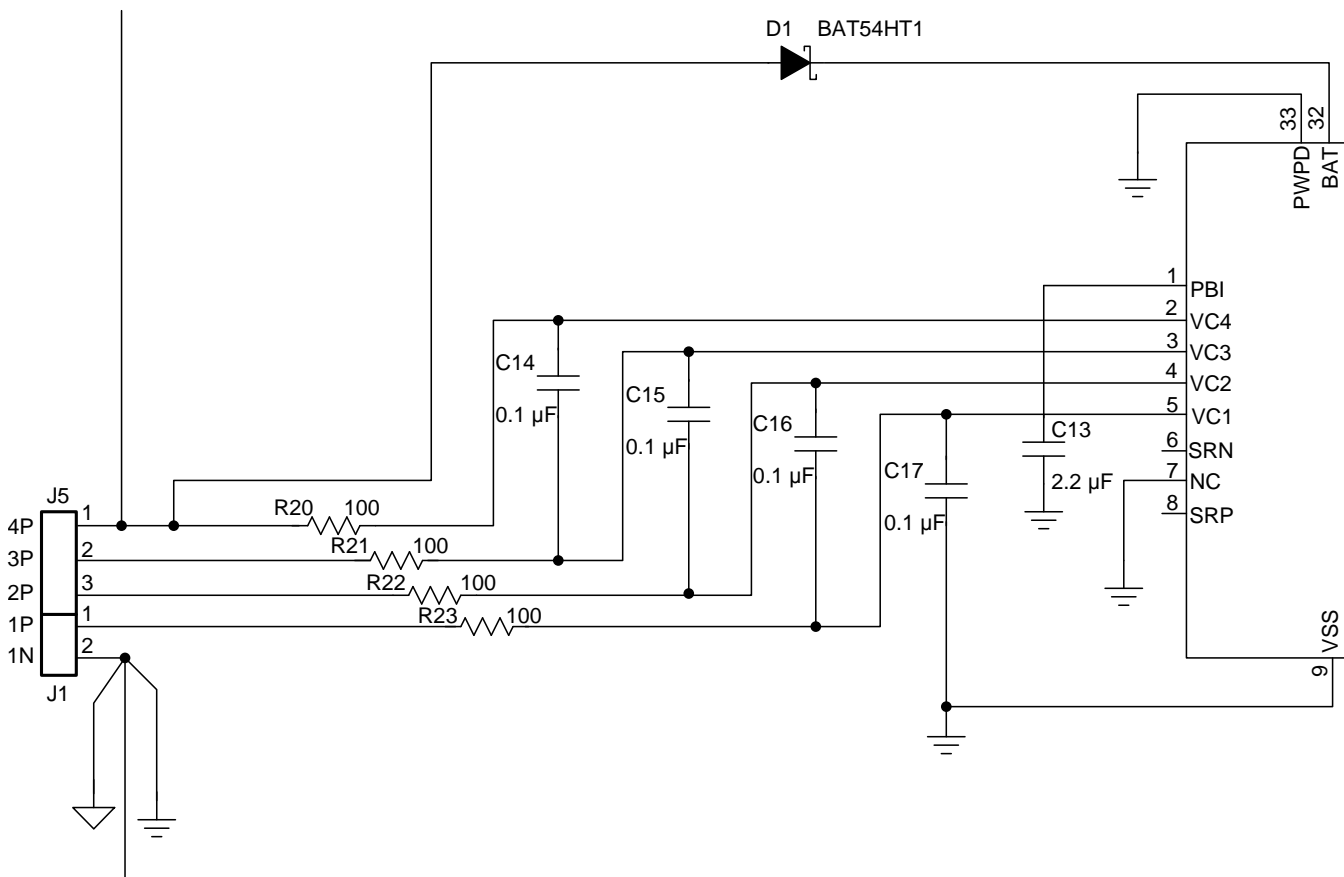
#### 8.2.2.3.1 Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter, which provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some trade-off for cell balancing versus safety protection.

The integrated cell balancing FETs allow the AFE to bypass cell current around a given cell or numerous cells, effectively balancing the entire battery stack. External series resistors placed between the cell connections and the VCx I/O pins set the balancing current magnitude. The internal FETs provide a 200-Ω resistance ( $2\text{ V} < \text{VDS} < 4\text{ V}$ ). Series input resistors between 100 Ω and 1 kΩ are recommended for effective cell balancing.

The BAT input uses a diode (D1) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

Also, as described in [High-Current Path](#), the top and bottom nodes of the cells must be sensed at the battery connections with a Kelvin connection to prevent voltage sensing errors caused by a drop in the high-current PCB copper.



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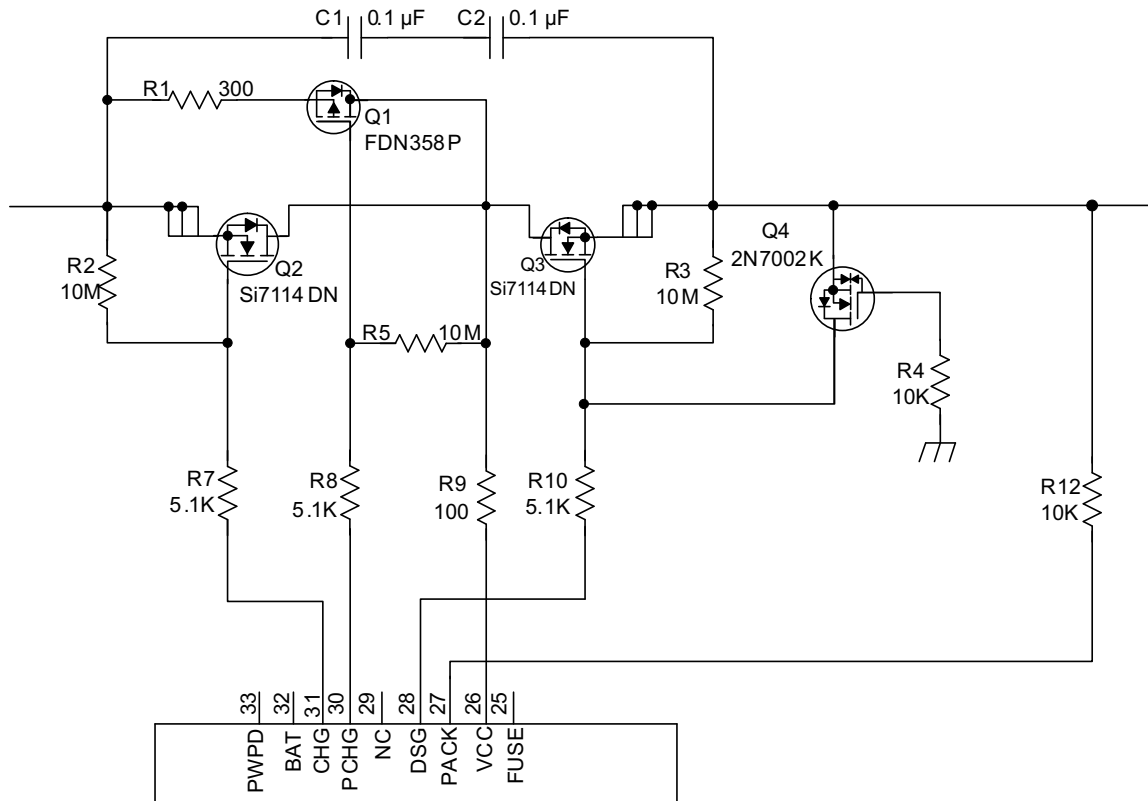
Figure 32. Cell and BAT Inputs

#### 8.2.2.3.2 External Cell Balancing

Internal cell balancing can only support up to 10 mA. External cell balancing is provided as another option for faster cell balancing. For details, refer to the application note, [Fast Cell Balancing Using External MOSFET \(SLUA420\)](#).

### 8.2.2.3.3 PACK and FET Control

The PACK and  $V_{CC}$  inputs provide power to the bq4050 gauge from the charger. The PACK input also provides a method to measure and detect the presence of a charger. The PACK input uses a 100- $\Omega$  resistor; whereas, the  $V_{CC}$  input uses a diode to guard against input transients and prevents misoperation of the data driver during short-circuit events.



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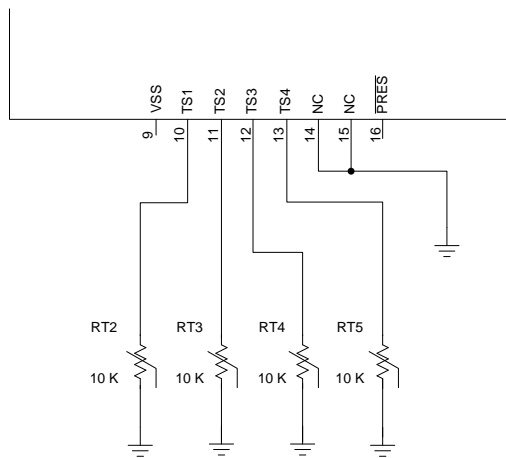
**Figure 33. bq4050 PACK and FET Control**

The N-CH charge and discharge FETs are controlled with 5.1-k $\Omega$  series gate resistors, which provide a switching time constant of a few microseconds. The 10-M $\Omega$  resistors ensure that the FETs are off in the event of an open connection to the FET drivers. Q4 is provided to protect the discharge FET (Q3) in the event of a reverse-connected charger. Without Q4, Q3 can be driven into its linear region and suffer severe damage if the PACK+ input becomes slightly negative.

Q4 turns on in that case to protect Q3 by shorting its gate to source. To use the simple ground gate circuit, the FET must have a low gate turn-on threshold. If it is desired to use a more standard device, such as the 2N7002 as the reference schematic, the gate should be biased up to 3.3 V with a high-value resistor. The bq4050 device has the capability to provide a current-limited charging path typically used for low battery voltage or low temperature charging. The bq4050 device uses an external P-channel, precharge FET controlled by PCHG.

### 8.2.2.3.4 Temperature Output

For the bq4050 device, TS1, TS2, TS3, and TS4 provide thermistor drive-under program control. Each pin can be enabled with an integrated 18-k $\Omega$  (typical) linearization pullup resistor to support the use of a 10-k $\Omega$  at 25 $^{\circ}$ C (103) NTC external thermistor, such as a Mitsubishi BN35-3H103. The reference design includes four 10-k $\Omega$  thermistors: RT1, RT2, RT3, and RT4. The bq4050 device supports up to four external thermistors. Connect unused thermistor pins to  $V_{SS}$ .

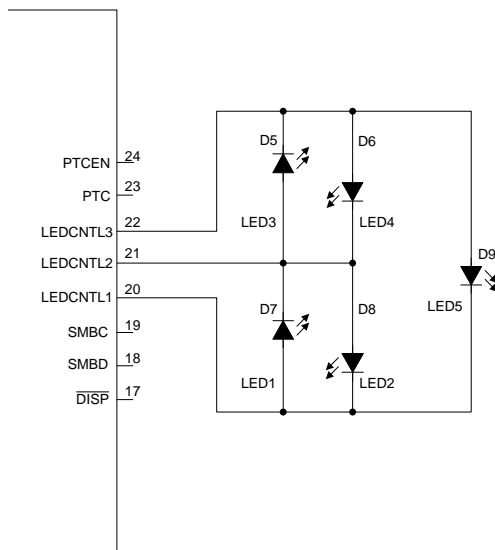


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Figure 34. Thermistor Drive

8.2.2.3.5 LEDs

Three LED control outputs provide constant current sinks for the driving external LEDs. These outputs are configured to provide voltage and control for up to 5 LEDs. No external bias voltage is required. Unused LEDCNTL pins can remain open or they can be connected to V<sub>SS</sub>. The  $\overline{\text{DISP}}$  pin should be connected to V<sub>SS</sub>, if the LED feature is not used.



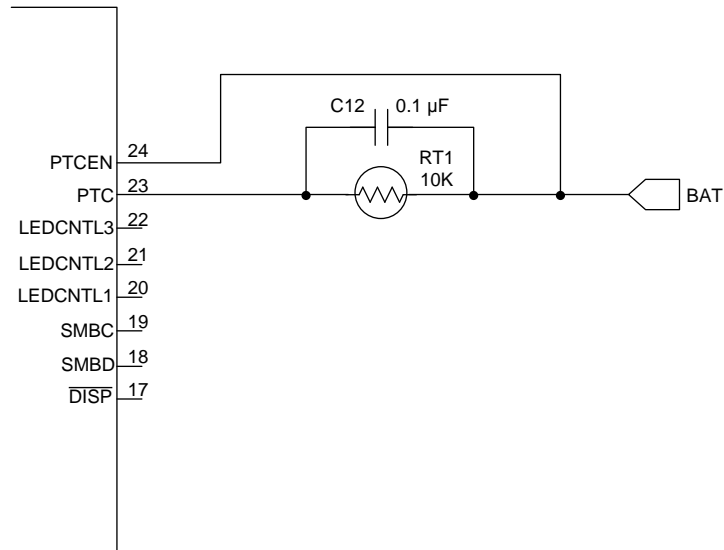
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Figure 35. LEDs

8.2.2.3.6 Safety PTC Thermistor

The bq4050 device provides support for a safety PTC thermistor. The PTC thermistor is connected between PTC and PTCEN, and PTCEN is connected to BAT. It can be placed close to the CHG/DSG FETs to monitor the temperature. A PTC fault is one of the permanent failure modes. It can only be cleared by a POR.

To disable, connect PTC and PTCEN to V<sub>SS</sub>.

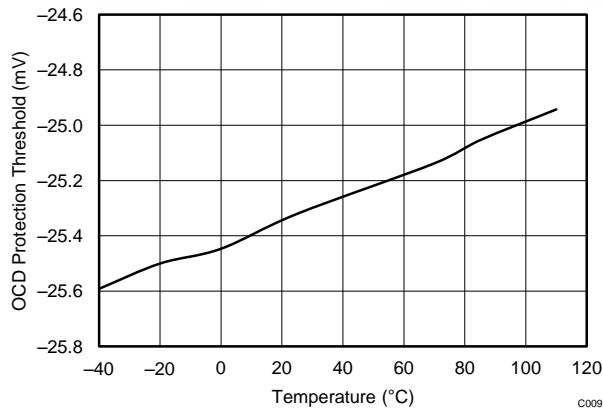


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**Figure 36. PTC Thermistor**

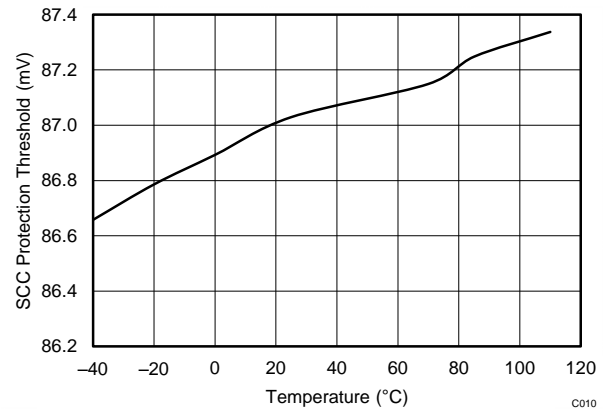


### 8.2.3 Application Curves



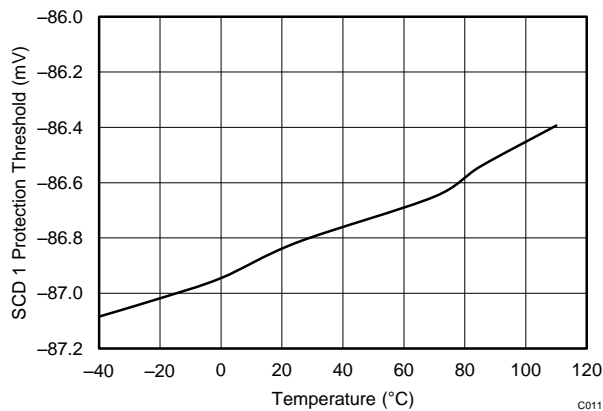
Threshold setting is -25 mV.

**Figure 37. Overcurrent Discharge Protection Threshold Vs. Temperature**



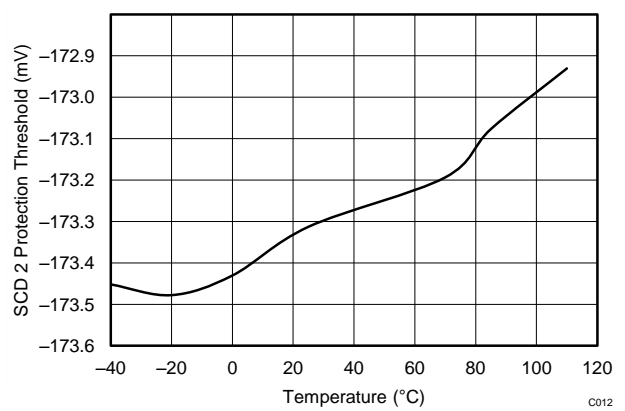
Threshold setting is 88.85 mV.

**Figure 38. Short Circuit Charge Protection Threshold Vs. Temperature**



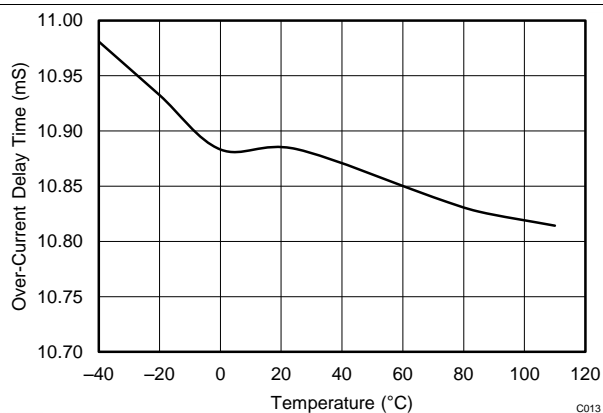
Threshold setting is -88.85 mV.

**Figure 39. Short Circuit Discharge 1 Protection Threshold Vs. Temperature**



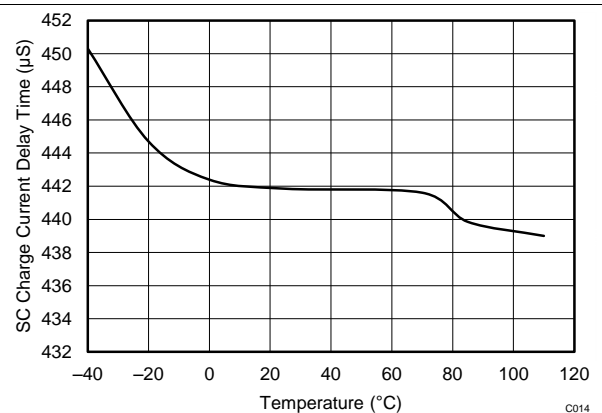
Threshold setting is -177.7 mV.

**Figure 40. Short Circuit Discharge 2 Protection Threshold Vs. Temperature**



Threshold setting is 11 ms.

**Figure 41. Overcurrent Delay Time Vs. Temperature**



Threshold setting is 465 µs.

**Figure 42. Short Circuit Charge Current Delay Time Vs. Temperature**

## 9 Power Supply Recommendations

The device manages its supply voltage dynamically according to the operation conditions. Normally, the BAT input is the primary power source to the device. The BAT pin should be connected to the positive termination of the battery stack. The input voltage for the BAT pin ranges from 2.2 V to 26 V.

The VCC pin is the secondary power input, which activates when the BAT voltage falls below minimum  $V_{CC}$ . This allows the device to source power from a charger (if present) connected to the PACK pin. The VCC pin should be connected to the common drain of the CHG and DSG FETs. The charger input should be connected to the PACK pin.

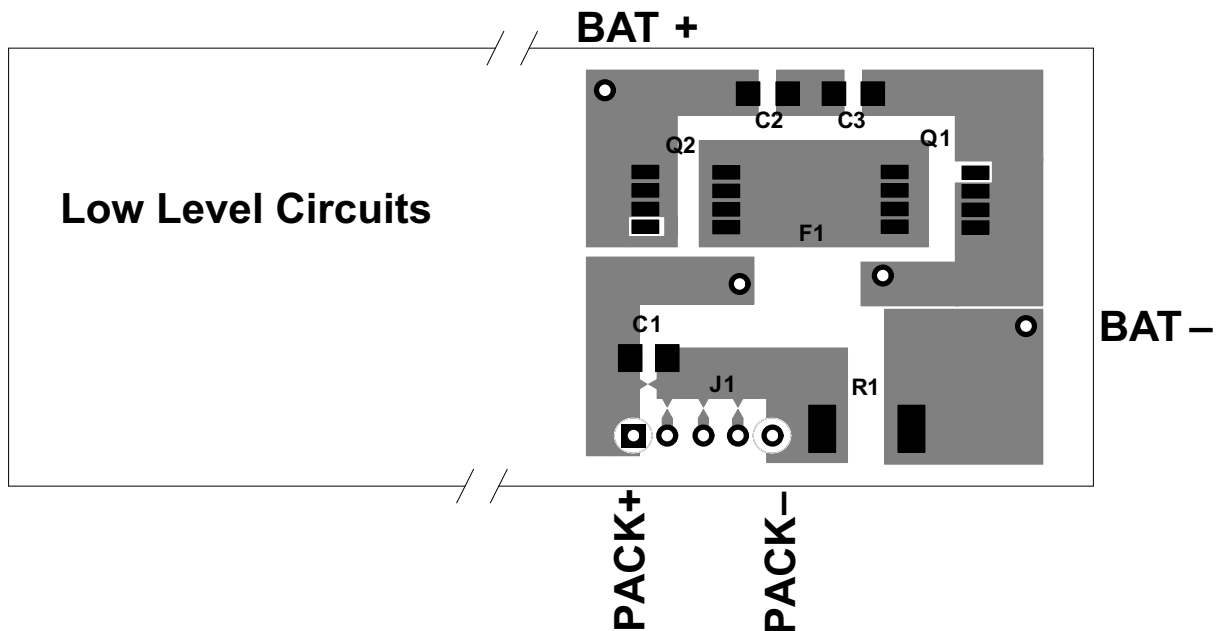
## 10 Layout

### 10.1 Layout Guidelines

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultra-low current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement, such as that shown in Figure 43, where the high-current section is on the opposite side of the board from the electronic devices. Clearly, this is not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high-current traces away from signal traces, which enter the bq4050 gauge directly. IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path.

**NOTE**

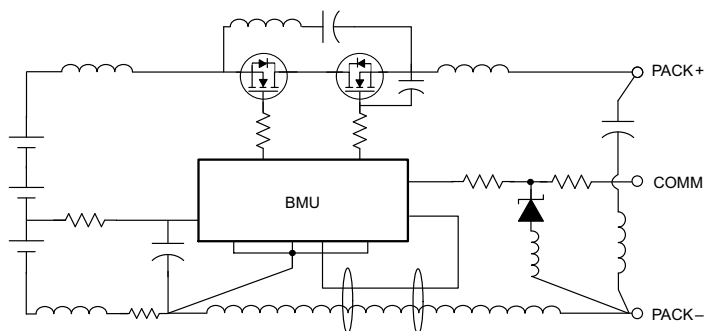
During surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics, as illustrated in Figure 44.



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**Figure 43. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity**

Layout Guidelines (continued)



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Figure 44. Avoid Close Spacing Between High-Current and Low-Level Signal Lines

Kelvin voltage sensing is important to accurately measure current and top and bottom cell voltages. Place all filter components as close as possible to the device. Route the traces from the sense resistor in parallel to the filter circuit. Adding a ground plane around the filter network can add additional noise immunity. Figure 45 and Figure 46 demonstrate correct kelvin current sensing.

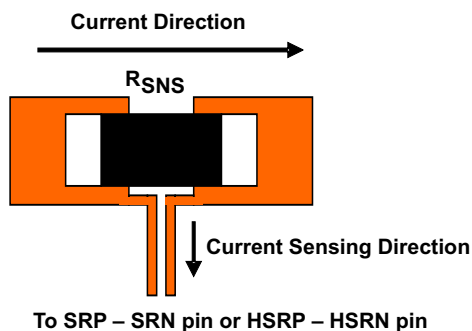


Figure 45. Sensing Resistor PCB Layout

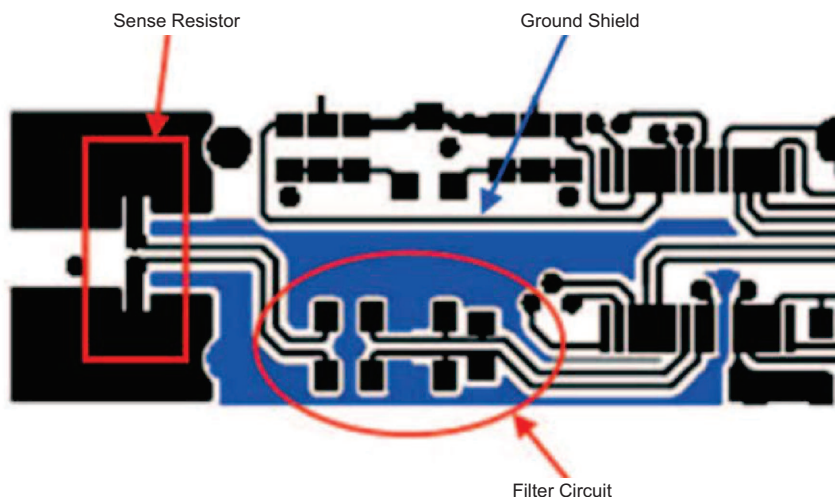
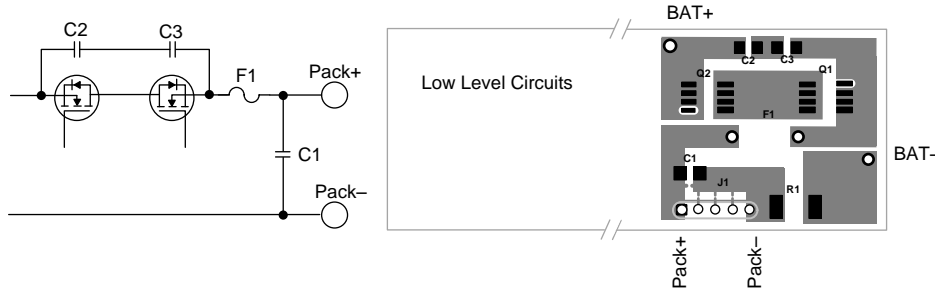


Figure 46. Sense Resistor, Ground Shield, and Filter Circuit Layout

**Layout Guidelines (continued)**

**10.1.1 Protector FET Bypass and Pack Terminal Bypass Capacitors**

Use wide copper traces to lower the inductance of the bypass capacitor circuit. In [Figure 47](#), an example layout demonstrates this technique.

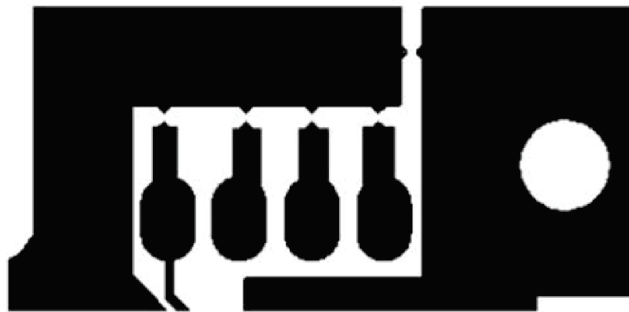


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**Figure 47. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, and C3**

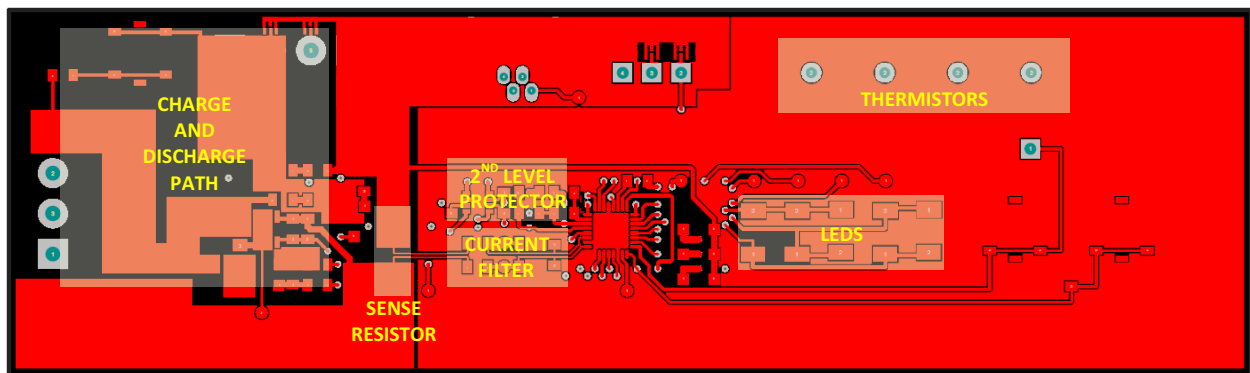
**10.1.2 ESD Spark Gap**

Protect the SMBus clock, data, and other communication lines from ESD with a spark gap at the connector. The pattern in [Figure 48](#) is recommended, with 0.2-mm spacing between the points.



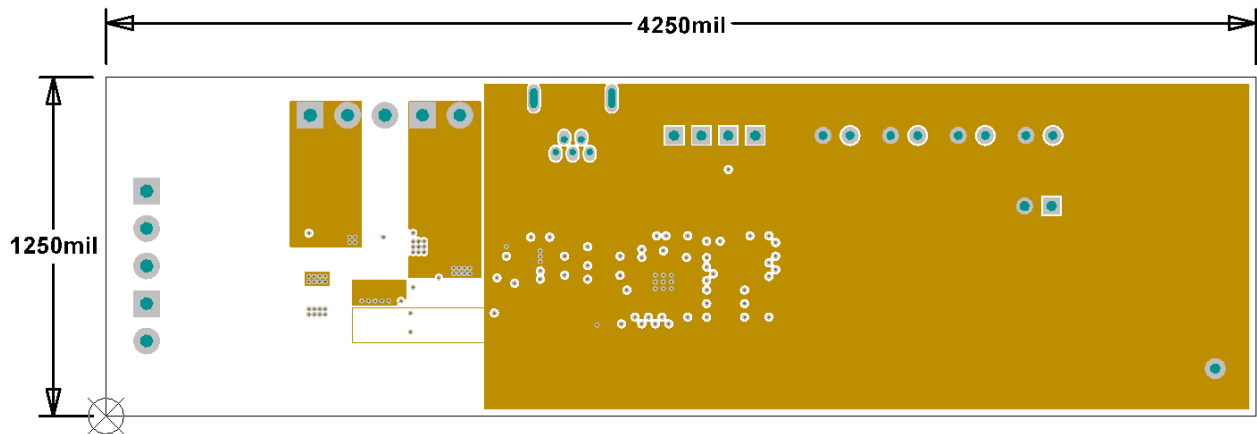
**Figure 48. Recommended Spark-Gap Pattern Helps Protect Communication Lines from ESD**

**10.2 Layout Example**

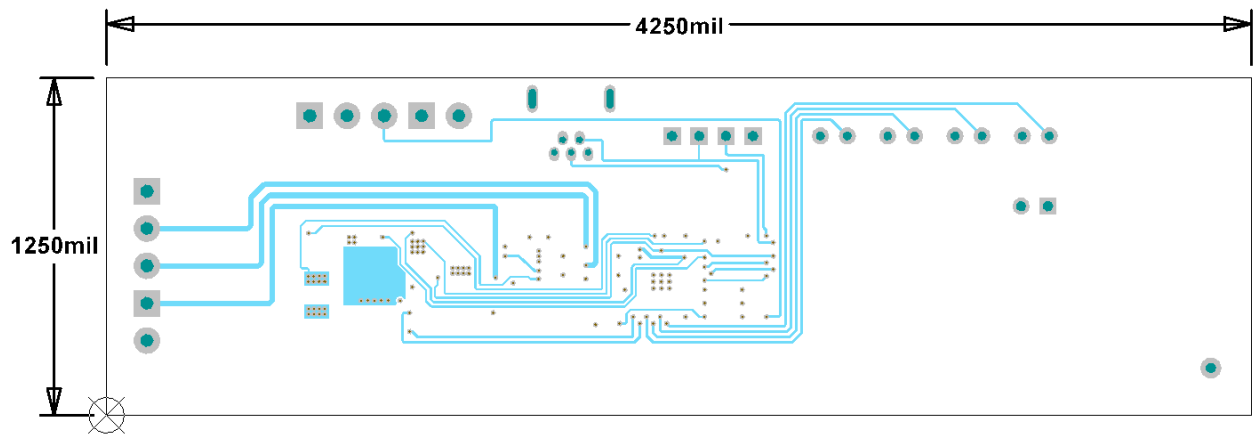


**Figure 49. Top Layer**

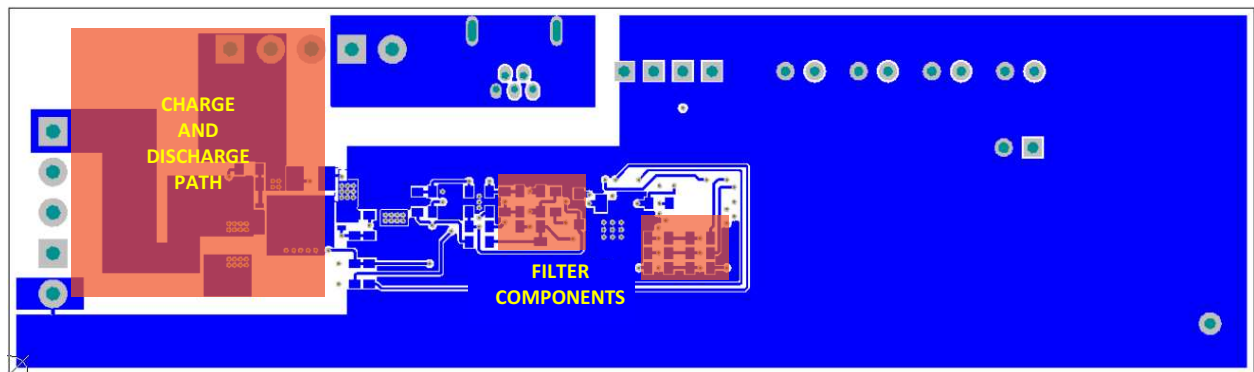
**Layout Example (continued)**



**Figure 50. Internal Layer 1**



**Figure 51. Internal Layer 2**



**Figure 52. Bottom Layer**

## 11 デバイスおよびドキュメントのサポート

### 11.1 ドキュメントのサポート

#### 11.1.1 関連資料

関連資料については、『[bq4050テクニカル・リファレンス・マニュアル](#)』([SLUUAQ3](#))を参照してください。

### 11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 11.3 商標

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### 11.4 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ4050RSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ4050	<a href="#">Samples</a>
BQ4050RSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ4050	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ4050RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ4050RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ4050RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
BQ4050RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

**RSM 32**

**VQFN - 1 mm max height**

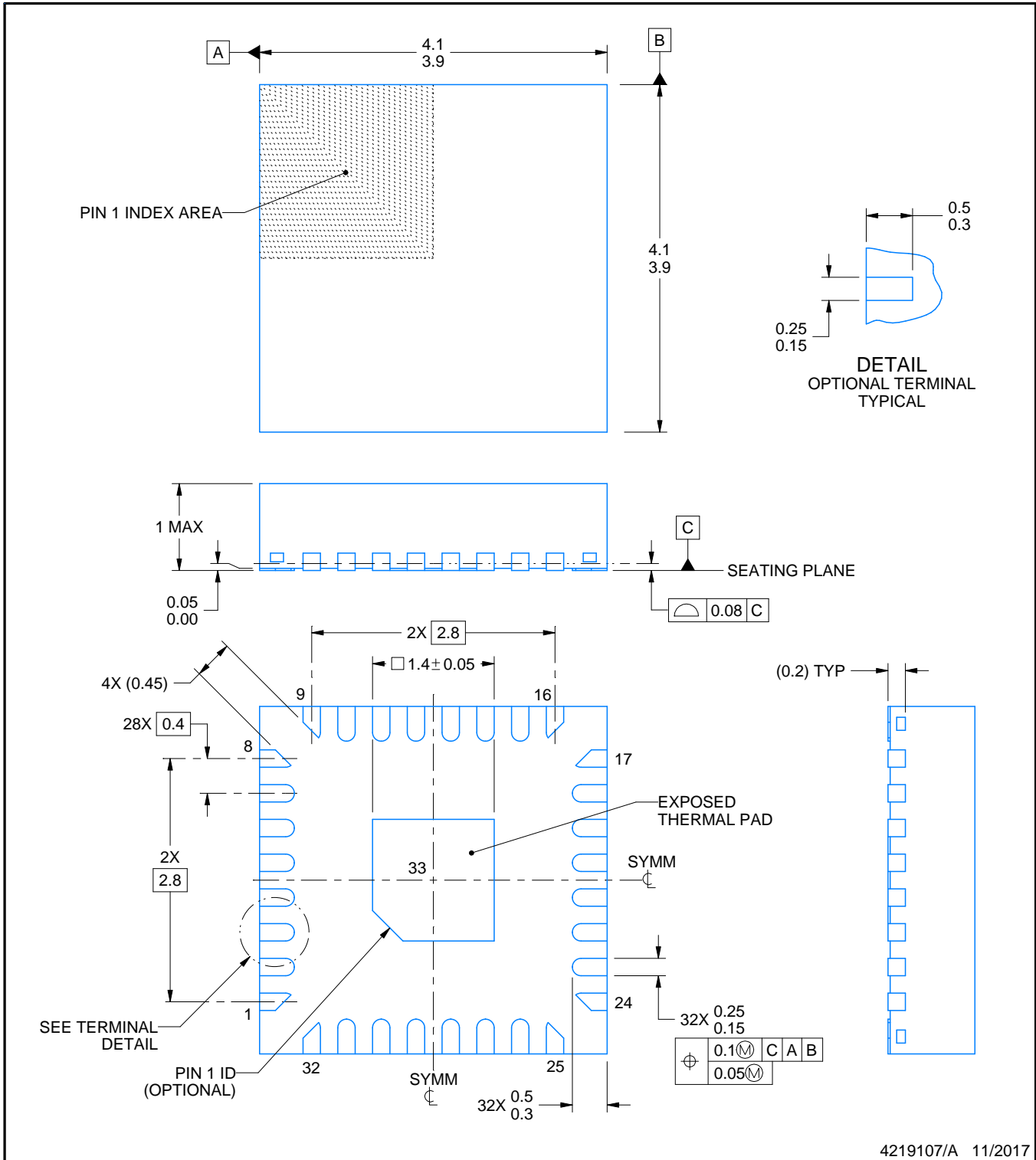
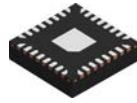
4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224982/A



NOTES:

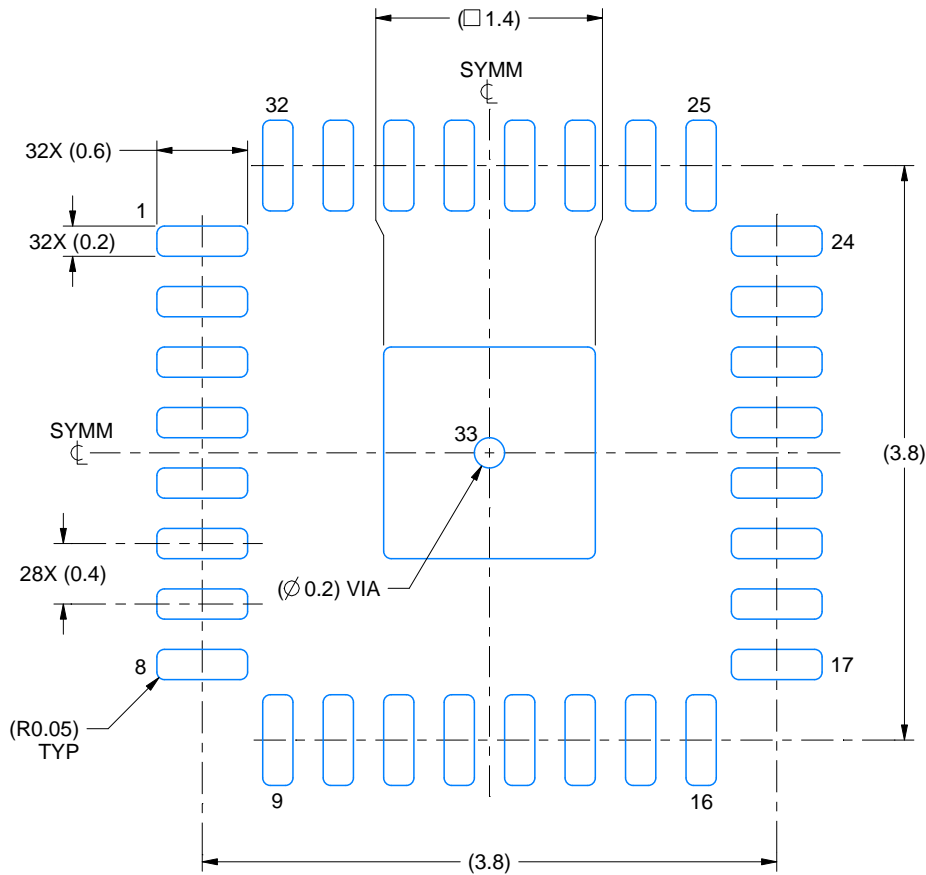
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

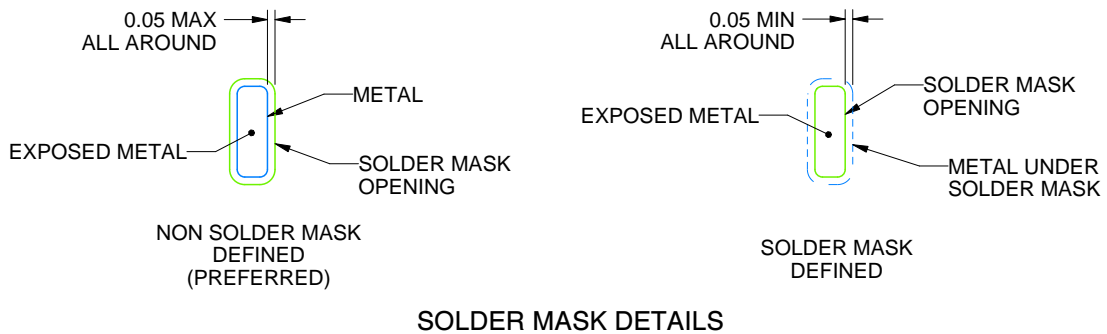
RSM0032A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

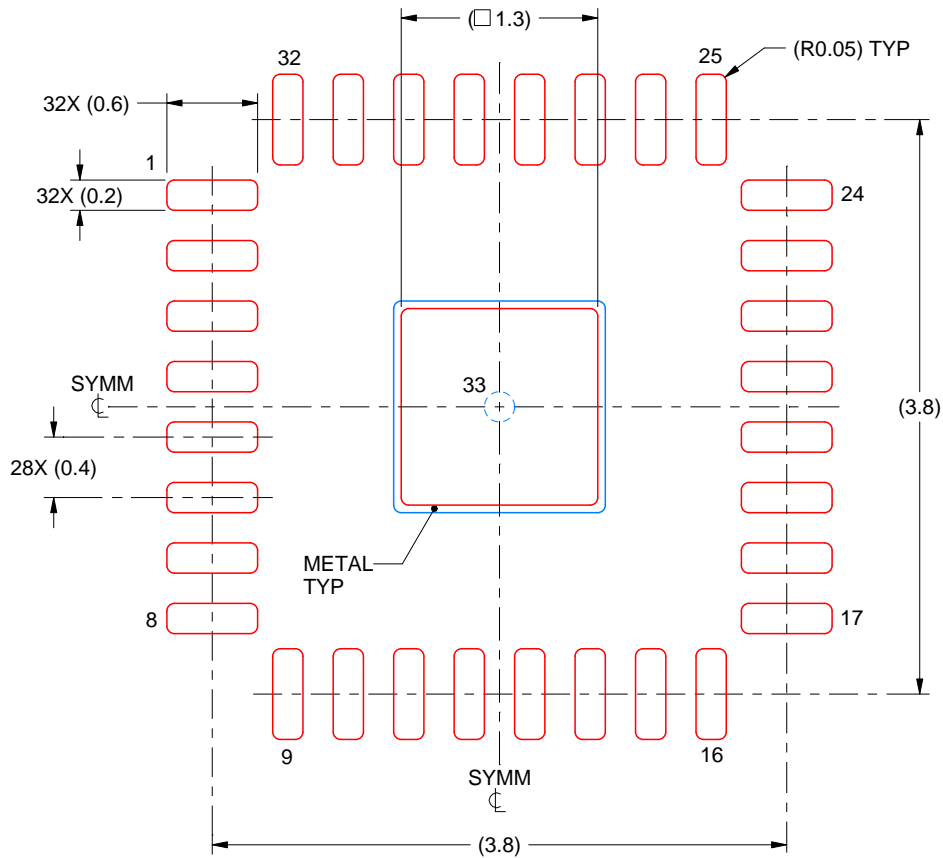
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSM0032A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:  
 86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

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NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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