

CDx4HC165/CDx4HCT165 ハイスピード CMOS ロジック、8 ビット、パラレル入力、シリアル出力、シフト・レジスタ

1 特長

- バッファ付き入力
- 非同期パラレル・ロード
- 相補出力
- ファンアウト (全温度範囲にわたって)
 - 標準出力: 10 の LSTTL 負荷
 - バス・ドライバ出力: 15 の LSTTL 負荷
- 広い動作温度範囲: -55°C ~ 125°C
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
 - 2V ~ 6V で動作
 - 優れたノイズ耐性: $N_{IL} = V_{CC}$ の 30%, $N_{IH} = V_{CC}$ の 30% ($V_{CC} = 5V$ の場合)
- HCT タイプ
 - 4.5V ~ 5.5V で動作
 - LSTTL 入力ロジックと直接互換、 $V_{IL} = 0.8V$ (最大値)、 $V_{IH} = 2V$ (最小値)
 - CMOS 入力互換、 V_{OL} 、 V_{OH} で $I_L \leq 1\mu A$

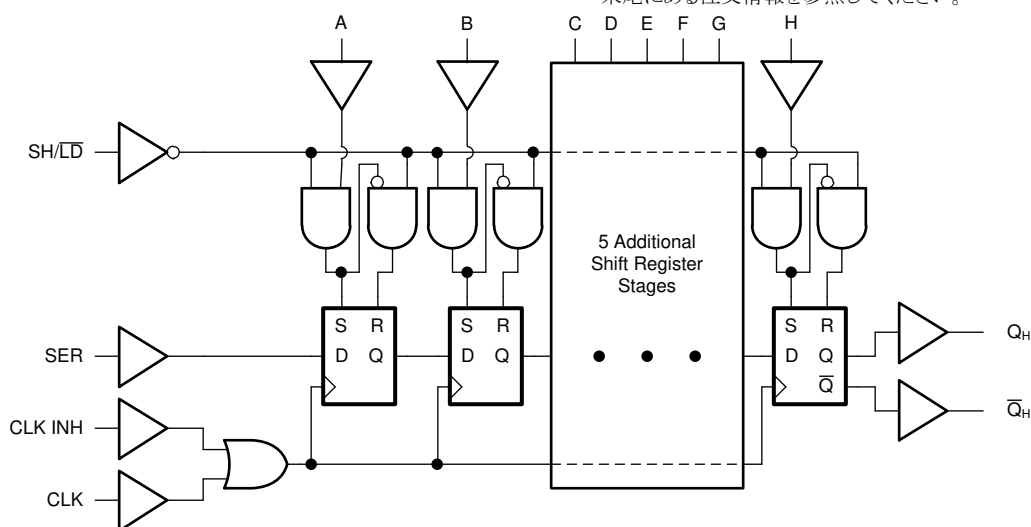
2 概要

'HC165 と 'HCT165 は、最終段から利用できる相補シリアル出力 (Q_H と \bar{Q}_H) を備えた 8 ビット・パラレルまたはシリアル入力シフト・レジスタです。パラレル・ロード (SH/LD) 入力が LOW の場合、A ~ H 入力のパラレル・データは非同期的にレジスタにロードされます。SH/LD が HIGH の場合、データは順次に SER 入力からレジスタに入り、クロックの立ち上がり遷移ごとに 1 つづつ右の位置 (A → B → C など) にシフトされます。この機能を使うと、 Q_H 出力を後続デバイスの SER 入力に接続することでパラレル入力シリアル出力コンバータを拡張できます。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
CD54HC165F3A	CDIP (16)	24.38mm × 6.92mm
CD74HC165M	SOIC (16)	9.90mm × 3.90mm
CD74HC165E	PDIP (16)	19.31mm × 6.35mm
CD54HCT165F3A	CDIP (16)	24.38mm × 6.92mm
CD74HCT165M	SOIC (16)	9.90mm × 3.90mm
CD74HCT165E	PDIP (16)	19.31mm × 6.35mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ダイアグラム



Table of Contents

1 特長	1	7.2 Functional Block Diagram.....	10
2 概要	1	7.3 Device Functional Modes.....	10
3 Revision History	2	8 Power Supply Recommendations	11
4 Pin Configuration and Functions	3	9 Layout	11
5 Specifications	4	9.1 Layout Guidelines.....	11
5.1 Absolute Maximum Ratings.....	4	10 Device and Documentation Support	12
5.2 Recommended Operating Conditions.....	4	10.1 Receiving Notification of Documentation Updates..	12
5.3 Thermal Information.....	4	10.2 サポート・リソース.....	12
5.4 Electrical Characteristics.....	5	10.3 Trademarks.....	12
5.5 Prerequisite for Switching Characteristics.....	6	10.4 Electrostatic Discharge Caution.....	12
5.6 Switching Characteristics.....	7	10.5 Glossary.....	12
6 Parameter Measurement Information	8	11 Mechanical, Packaging, and Orderable Information	12
7 Detailed Description	10		
7.1 Overview.....	10		

3 Revision History

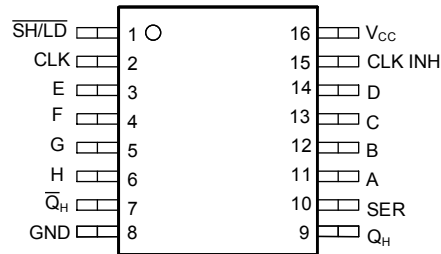
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2003) to Revision D (November 2021)

Page

- 最新のデータシート規格を反映するように、文書全体の表、図、相互参照の採番と書式設定を更新..... 1
- 現行の TI の命名規則に合わせてピン名を以下のように更新。 \overline{PL} を $\overline{SH/LD}$ 、CP を CLK、D4 を E、D5 を F、D6 を G、D7 を H、 $\overline{Q_7}$ を $\overline{Q_H}$ 、 Q_7 を Q_H 、DS を SER、D0 を A、D1 を B、D2 を C、D3 を D、 \overline{CE} を CLK INH。..... 1

4 Pin Configuration and Functions



J, N, or D package
16-Pin CDIP, PDIP, SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
I _{IK}	Input diode current	For V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20 mA
I _{OK}	Output diode current	For V _O < -0.5 V or V _O > V _{CC} + 0.5 V		±20 mA
I _O	Drain current per output	For V _O < -0.5 V or V _O > V _{CC} + 0.5 V		±25 mA
I _O	Output source or sink current per output pin	For V _O > -0.5 V or V _O < V _{CC} + 0.5 V		±25 mA
	Continuous current through V _{CC} or GND			±50 mA
T _J	Junction temperature			150 °C
T _{stg}	Storage temperature	-65	150	°C
	Lead temperature (Soldering 10s) (SOIC- Lead tips only)			300 °C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V _I , V _O	Input or output voltage	0	V _{CC}	V	
t _t	Input rise and fall time	2 V	1000		ns
		4.5 V	500		
		6 V	400		
T _A	Temperature range	-55	125	°C	

5.3 Thermal Information

THERMAL METRIC		CD74HC165, CD74HCT165		UNIT
		D (SOIC)	N (PDIP)	
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	73	67	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER	TEST CONDITIONS ⁽²⁾	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HC TYPES											
V _{IH}	High level input voltage		2	1.5		1.5		1.5		V	
			4.5	3.15		3.15		3.15		V	
			6	4.2		4.2		4.2		V	
V _{IL}	Low level input voltage		2		0.5		0.5		0.5	V	
			4.5		1.35		1.35		1.35	V	
			6		1.8		1.8		1.8	V	
V _{OH}	High level output voltage	I _{OH} = -20 μA	2	1.9		1.9		1.9		V	
		I _{OH} = -20 μA	4.5	4.4		4.4		4.4		V	
		I _{OH} = -20 μA	6	5.9		5.9		5.9		V	
	High level output voltage	I _{OH} = -4 mA	4.5	3.98		3.84		3.7		V	
		I _{OH} = -5.2 mA	6	5.48		5.34		5.2		V	
V _{OL}	Low level output voltage	I _{OL} = 20 μA	2		0.1		0.1		0.1	V	
		I _{OL} = 20 μA	4.5		0.1		0.1		0.1	V	
		I _{OL} = 20 μA	6		0.1		0.1		0.1	V	
	Low level output voltage	I _{OL} = 4 mA	4.5		0.26		0.33		0.4	V	
		I _{OL} = 5.2 mA	6		0.26		0.33		0.4	V	
I _I	Input leakage current	V _I = V _{CC} or GND	6		±0.1		±1		±1	μA	
I _{CC}	Supply current	V _I = V _{CC} or GND	6		8		80		160	μA	
HCT TYPES											
V _{IH}	High level input voltage		4.5 to 5.5	2		2		2		V	
V _{IL}	Low level input voltage		4.5 to 5.5		0.8		0.8		0.8	V	
V _{OH}	High level output voltage	I _{OH} = -20 μA	4.5	4.4		4.4		4.4		V	
	High level output voltage	I _{OH} = -4 mA	4.5	3.98		3.84		3.7		V	
V _{OL}	Low level output voltage	I _{OL} = 20 μA	4.5		0.1		0.1		0.1	V	
	Low level output voltage	I _{OL} = 4 mA	4.5		0.26		0.33		0.4	V	
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1		±1	μA	
I _{CC}	Supply current	V _I = V _{CC} or GND	5.5		8		80		160	μA	
ΔI _{CC} ⁽¹⁾	Additional quiescent device current per input pin	SER, A to H inputs held at V _{CC} - 2.1	4.5 to 5.5		100	126		157.5		171.5	μA
		CLK and SH/LD inputs held at V _{CC} - 2.1	4.5 to 5.5		100	234		292.5		318.5	

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(2) V_I = V_{IH} or V_{IL}.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V _{CC} (V)	25°C		-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{WL} , t _{WH}	CLK Pulse Width	2	80		100		120	ns	
		4.5	16		20		24		
		6	14		17		20		
t _{WL}	SH/ $\overline{\text{LD}}$ Pulse Width	2	80		100		120	ns	
		4.5	16		20		24		
		6	14		17		20		
t _{SU}	Set-up Time SER to CLK	2	80		100		120	ns	
		4.5	16		20		24		
		6	14		17		20		
t _{SU(L)}	CLK INH to CLK	2	80		100		120	ns	
		4.5	16		20		24		
		6	14		17		20		
t _{SU}	A-H to SH/ $\overline{\text{LD}}$	2	80		100		120	ns	
		4.5	16		20		24		
		6	14		17		20		
t _H	Hold Time SER to CLK or CLK INH	2	35		45		55	ns	
		4.5	7		9		11		
		6	6		8		9		
t _H	CLK INH to CLK	2	0		0		0	ns	
		4.5	0		0		0		
		6	0		0		0		
t _{REC}	Recovery Time SH/ $\overline{\text{LD}}$ to CLK	2	100		125		150	ns	
		4.5	20		25		30		
		6	17		21		26		
f _{MAX}	Maximum Clock Pulse Frequency	2	6		5		4	MHz	
		4.5	30		24		20		
		6	35		28		24		
HCT TYPES									
t _{WL} , t _{WH}	CLK Pulse Width	4.5	18		23		27	ns	
t _{WL}	SH/ $\overline{\text{LD}}$ Pulse Width	4.5	20		25		30	ns	
t _{SU}	Set-up Time SER to CLK	4.5	20		25		30	ns	
t _{SU(L)}	CLK INH to CLK	4.5	20		25		30	ns	
t _{SU}	A-H to SH/ $\overline{\text{LD}}$	6	20		25		30	ns	
t _H	Hold Time SER to CLK or CLK INH	4.5	7		9		11	ns	
t _S , t _H	CLK INH to CLK	4.5	0		0		0	ns	
t _{REC}	Recovery Time SH/ $\overline{\text{LD}}$ to CLK	4.5	20		25		30	ns	
f _{MAX}	Maximum Clock Pulse Frequency	4.5	27		22		18	MHz	

5.6 Switching Characteristics

Input t_r , $t_f = 6$ ns. Unless otherwise specified, $C_L = 50$ pF

PARAMETER		$V_{CC}(V)$	25°C		-40°C to 85°C	-55°C to 125°C	UNIT
			TYP	MAX	MAX	MAX	
HC TYPES							
t_{pd}	CLK or CLK INH to Q_H or \bar{Q}_H	2		165	205	250	ns
		4.5	13 ⁽³⁾	33	41	50	ns
		6		28	35	43	ns
	SH/ \bar{LD} to Q_H or \bar{Q}_H	2		175	220	265	ns
		4.5	14 ⁽³⁾	35	44	53	ns
		6		30	37	45	ns
	H to Q_H or \bar{Q}_H	2		150	190	225	ns
		4.5	12 ⁽³⁾	30	38	45	ns
		6		26	33	38	ns
t_t	Output Transition Times	2		75	95	110	ns
		4.5		15	19	22	ns
		6		13	16	19	ns
C_{IN}	Input Capacitance			10	10	10	pF
C_{PD}	Power Dissipation Capacitance ^{(1) (2)}	5	17				pF
HCT TYPES							
t_{pd}	CLK or CLK INH to Q_H or \bar{Q}_H	4.5	17 ⁽³⁾	40	50	60	ns
	SH/ \bar{LD} to Q_H or \bar{Q}_H	4.5	17 ⁽³⁾	40	50	60	ns
	H to Q_H or \bar{Q}_H	4.5	14 ⁽³⁾	35	44	53	ns
t_t	Output Transition Times	4.5		15	19	22	ns
C_{IN}	Input Capacitance			10	10	10	pF
C_{PD}	Power Dissipation Capacitance ^{(1) (2)}	5	24				pF

(1) C_{PD} is used to determine the dynamic power consumption, per package.

(2) $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_o)$ where f_i = Input Frequency, f_o = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

(3) $C_L = 15$ pF and $V_{CC} = 5$ V.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_f < 6 \text{ ns}$.

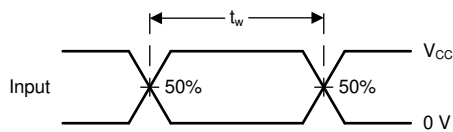
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

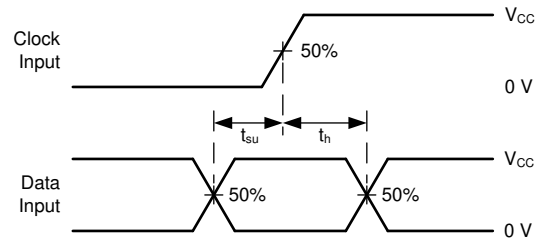


(1) C_L includes probe and test-fixture capacitance.

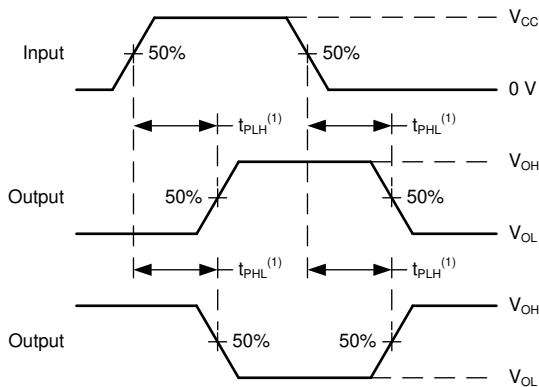
6-1. Load Circuit for Push-Pull Outputs



6-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

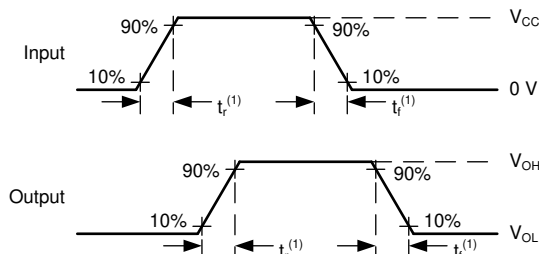


6-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

6-4. Voltage Waveforms, Standard CMOS Inputs Setup Propagation Delays




(1) The greater between t_r and t_f is the same as t_t .

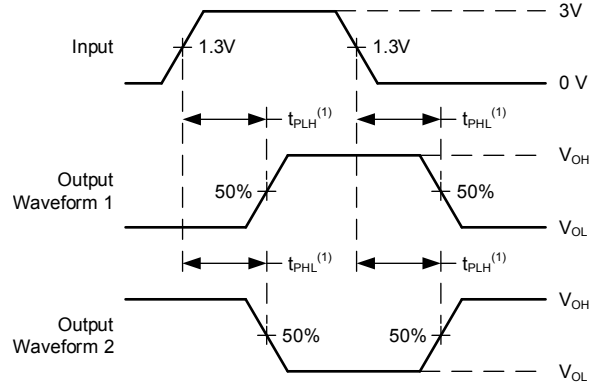
6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Input Devices




6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration




6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .


6-8. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays

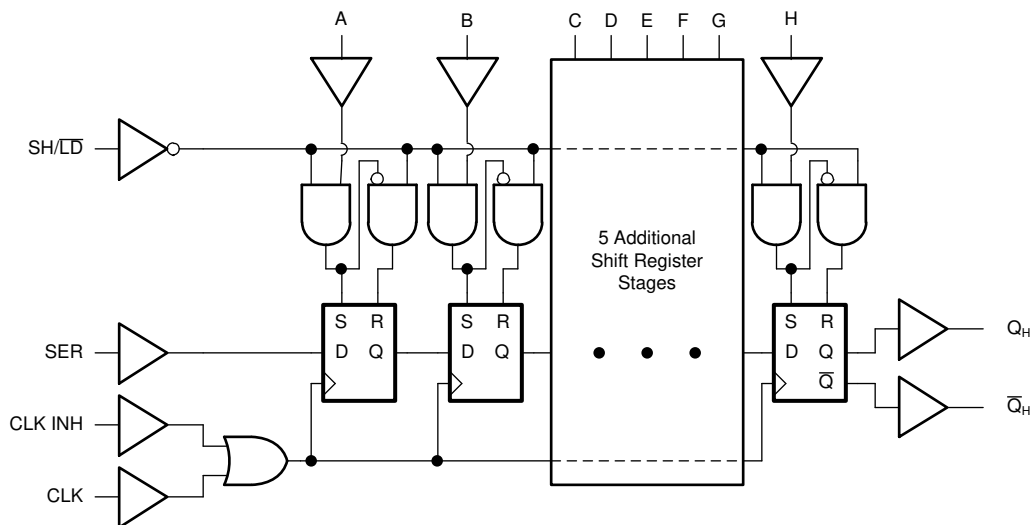
7 Detailed Description

7.1 Overview

The 'HC165 and 'HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs (Q_H and \bar{Q}_H) available from the last stage. When the parallel load (SH/\bar{LD}) input is LOW, parallel data from the A to H inputs are loaded into the register asynchronously. When the SH/\bar{LD} is HIGH, data enters the register serially at the SER input and shifts one place to the right ($A \rightarrow B \rightarrow C$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by connecting the Q_H output to the SER input of the succeeding device.

For predictable operation the LOW-to-HIGH transition of CLK INH should only take place while CLK is HIGH. Also, CLK and CLK INH should be LOW before the LOW-to-HIGH transition of SH/\bar{LD} to prevent shifting the data when SH/\bar{LD} goes HIGH.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Truth Table⁽¹⁾

OPERATING MODE	INPUTS					QnREGISTER		OUTPUTS	
	SHLD	CLK INH	CLK	SER	A - H	QA	QB - QG	QH	QH-bar
Parallel Load	L	X	X	X	L	L	L-L	L	H
	L	X	X	X	H	H	H-H	H	L
Serial Shift	H	L	↑	l	X	L	qA - qF	qG	qG-bar
	H	L	↑	h	X	H	qA - qF	qG	qG-bar
Hold (Do Nothing)	H	H	X	X	X	qA	qB - qG	qH	qH-bar

- (1) H = High voltage level.
 h = High voltage level one set-up time prior to the low-to-high clock transition.
 l = Low voltage level one set-up time prior to the low-to-high clock transition.
 L = Low voltage level.
 X = Don't care.
 ↑ = Transition from low to high level.
 q_n = Lower case letters indicate the state of the reference output clock transition.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8685501EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8685501EA CD54HCT165F3A	Samples
CD54HC165F3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409501EA CD54HC165F3A	Samples
CD54HCT165F3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8685501EA CD54HCT165F3A	Samples
CD74HC165E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC165E	Samples
CD74HC165M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC165M	Samples
CD74HCT165E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT165E	Samples
CD74HCT165M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HCT165M	Samples
CD74HCT165M96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT165M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC165, CD54HCT165, CD74HC165, CD74HCT165 :

- Catalog : [CD74HC165](#), [CD74HCT165](#)
- Military : [CD54HC165](#), [CD54HCT165](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC165M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC165M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT165M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT165M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC165M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC165M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HCT165M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HCT165M96G4	SOIC	D	16	2500	340.5	336.1	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC165E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC165E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT165E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT165E	N	PDIP	16	25	506	13.97	11230	4.32

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated