

# CDx4HC(T)245 高速 CMOS ロジック、オクタール・バス・トランシーバ、スリー・ステート、非反転型

## 1 特長

- バッファ付き入力
- スリー・ステート出力
- バス・ライン駆動能力
- $V_{CC} = 5V$ 、 $C_L = 15pF$ 、 $T_A = 25^\circ C$ で標準伝搬遅延 9ns (A から B、B から A)
- ファンアウト (全温度範囲にわたって)
  - バス・ドライバ出力は 15 個の LSTTL 負荷を駆動可能
- 広い動作温度範囲:  $-55^\circ C \sim 125^\circ C$
- 平衡のとれた伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
  - 2V~6V で動作
  - 優れたノイズ耐性:  $V_{CC}$  に対して  $N_{IL} = 30\%$ 、 $N_{IH} = 30\%$  ( $V_{CC} = 5V$  時)
- HCT タイプ
  - 4.5V~5.5V で動作
  - LSTTL 入力ロジックと直接互換、 $V_{IL} = 0.8V$  (最大値)、 $V_{IH} = 2V$  (最小値)
  - CMOS 入力互換、 $V_{OL}$ 、 $V_{OH}$  で  $I_L \leq 1\mu A$

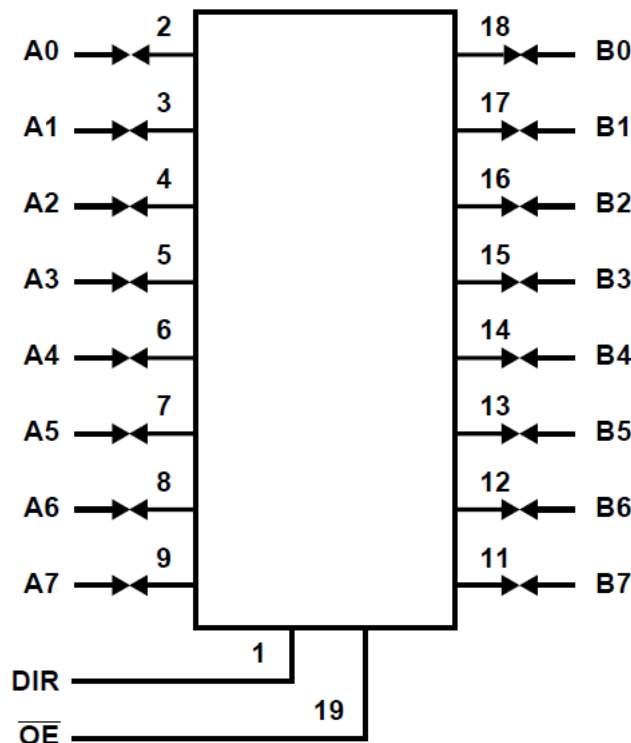
## 2 概要

CDx4HC(T)245 は、スリー・ステート出力を備えたオクタール・バス・トランシーバです。8 つのチャネルはすべて、方向 (DIR) ピンと出力イネーブル ( $\overline{OE}$ ) ピンにより制御されます。

### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
CD54HC245F	J (CDIP, 20)	26.92mm × 6.92mm
CD74HC245	N (PDIP, 20)	25.40mm × 6.35mm
	DW (SOIC, 20)	12.80mm × 7.50mm
CD54HCT245F	J (CDIP, 20)	26.92mm × 6.92mm
CD74HCT245	N (PDIP, 20)	25.40mm × 6.35mm
	DW (SOIC, 20)	12.80mm × 7.50mm

(1) すべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



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### 3 Revision History

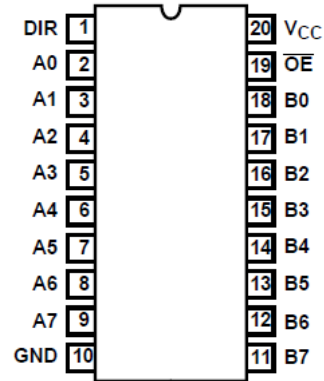
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

#### Changes from Revision A (April 2003) to Revision B (July 2022)

Page

- 最新のデータシート規格を反映するように、文書全体にわたって採番方式、書式、表、図、相互参照を更新..... 1

## 4 Pin Configuration and Functions



**J, N and DW Package  
20-Pin CDIP, PDIP or SOIC  
Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input diode current	For V <sub>I</sub> < -0.5V or V <sub>I</sub> > V <sub>CC</sub> + 0.5V		±20 mA
I <sub>OK</sub>	Output diode current	For V <sub>O</sub> < -0.5V or V <sub>O</sub> > V <sub>CC</sub> + 0.5V		±20 mA
I <sub>O</sub>	Drain current, per output	For -0.5V < V <sub>O</sub> < V <sub>CC</sub> + 0.5V		±35 mA
I <sub>O</sub>	Output source or sink current per output pin	For V <sub>O</sub> > -0.5V or V <sub>O</sub> < V <sub>CC</sub> + 0.5V		±25 mA
Continuous current through V <sub>CC</sub> or GND				±50 mA
T <sub>J</sub>	Junction temperature			150 °C
T <sub>stg</sub>	Storage temperature range	-65	150	°C
Lead temperature (Soldering 10s)(SOIC - lead tips only)				300 °C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V	
t <sub>t</sub>	Input rise and fall time	V <sub>CC</sub> = 2V	1000		ns
		V <sub>CC</sub> = 4.5V	500		
		V <sub>CC</sub> = 6V	400		
T <sub>A</sub>	Temperature range	-55	125	°C	

### 5.3 Thermal Information

THERMAL METRIC		DW (SOIC)	N (PDIP)	UNIT
		20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	58	69	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	V <sub>CC</sub> (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
V <sub>IH</sub>	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V <sub>IL</sub>	Low-level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		V
			6	1.8			1.8		1.8		V
V <sub>OH</sub>	High-level output voltage CMOS loads	I <sub>OH</sub> = -20 μA	2	1.9			1.9		1.9		V
		I <sub>OH</sub> = -20 μA	4.5	4.4			4.4		4.4		V
		I <sub>OH</sub> = -20 μA	6	5.9			5.9		5.9		V
	High-level output voltage TTL loads	I <sub>OH</sub> = -4 mA	4.5	3.98			3.84		3.7		V
I <sub>OH</sub> = -5.2 mA		6	5.48			5.48		5.2		V	
V <sub>OL</sub>	Low-level output voltage CMOS loads	I <sub>OL</sub> = 20 μA	2	0.1			0.1		0.1		V
		I <sub>OL</sub> = 20 μA	4.5	0.1			0.1		0.1		V
		I <sub>OL</sub> = 20 μA	6	0.1			0.1		0.1		V
	Low-level output voltage TTL	I <sub>OL</sub> = 4 mA	4.5	0.26			0.33		0.4		V
		I <sub>OL</sub> = 5.2 mA	6	0.26			0.33		0.4		V
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6	±0.1			±1		±1		μA
I <sub>CC</sub>	Quiescent device current	V <sub>I</sub> = V <sub>CC</sub> or GND	6	8			80		160		μA
I <sub>OZ</sub>	Three-state leakage current	V <sub>O</sub> = V <sub>CC</sub> or GND	6	±0.5			±5		±10		μA
<b>HCT TYPES</b>											
V <sub>IH</sub>	High-level input voltage		4.5 to 5.5	2			2		2		V
V <sub>IL</sub>	Low-level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V <sub>OH</sub>	High-level output voltage CMOS loads	I <sub>OH</sub> = -20 μA	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL	I <sub>OH</sub> = -4 mA	4.5	3.98			3.84		3.7		V
V <sub>OL</sub>	Low-level output voltage CMOS	I <sub>OL</sub> = 20 μA	4.5	0.1			0.1		0.1		V
	Low-level output voltage TTL	I <sub>OH</sub> = 4 mA	4.5	0.26			0.33		0.4		V
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> and GND	5.5	±0.1			±1		±1		μA
I <sub>CC</sub>	Quiescent device current	V <sub>I</sub> = V <sub>CC</sub> and GND	5.5	8			80		160		μA
I <sub>OZ</sub>	Three-state leakage current	V <sub>O</sub> = V <sub>CC</sub> or GND	6	±0.5			±5		±10		μA
ΔI <sub>CC</sub> <sup>(1)</sup>	Additional quiescent device current per input pin	An or Bn input held at V <sub>CC</sub> - 2.1 V	4.5 to 5.5	100 144			180		196		μA
		OE input held at V <sub>CC</sub> - 2.1 V	4.5 to 5.5	100 540			675		735		μA
		DIR input held at V <sub>CC</sub> - 2.1 V	4.5 to 5.5	100 324			405		441		μA

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA

## 5.5 Switching Characteristics

Input  $t_f = 6\text{ns}$ . Unless otherwise specified,  $C_L = 50\text{pF}^{(2)}$

PARAMETER		V <sub>CC</sub> (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
t <sub>pd</sub>	Propagation delay data to output	2		110		140		165	ns	
		4.5		22		28		33		
		6		19		24		28		
t <sub>dis</sub>	Output disable to output	2		150		190		225	ns	
		4.5		30		38		45		
		6		26		33		38		
t <sub>en</sub>	Output enable to output	2		150		190		225	ns	
		4.5		30		38		45		
		6		26		33		38		
t <sub>t</sub>	Output transition time	2		60		75		90	ns	
		4.5		12		15		18		
		6		10		13		15		
C <sub>i</sub>	Input capacitance		10	10		10		10	pF	
C <sub>io</sub>	Three-state output capacitance			20		20		20	pF	
C <sub>pd</sub>	Power dissipation capacitance	5		53					pF	
<b>HCT TYPES</b>										
t <sub>pd</sub>	Data to output	4.5		26		33		39	ns	
t <sub>dis</sub>	Output disable to output	4.5		30		38		45	ns	
t <sub>en</sub>	Output enable to output	4.5		32		40		48	ns	
t <sub>t</sub>	Output transition time	4.5		12		15		18	ns	
C <sub>i</sub>	Input capacitance		10	10		10		10	pF	
C <sub>io</sub>	Three-state output capacitance			20		20		20	pF	
C <sub>pd</sub>	Power dissipation capacitance <sup>(1) (2)</sup>	5		55					pF	

(1) C<sub>PD</sub> is used to determine the dynamic power consumption, per channel.

(2)  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## 6 Parameter Measurement Information

$t_{pd}$  is the maximum between  $t_{PLH}$  and  $t_{PHL}$

$t_t$  is the maximum between  $t_{TLH}$  and  $t_{THL}$

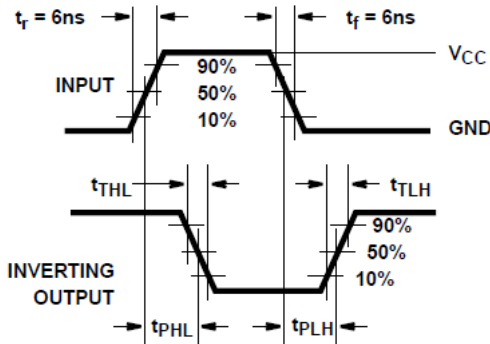


FIG 6-1. HC transition times and propagation delay times, combination logic

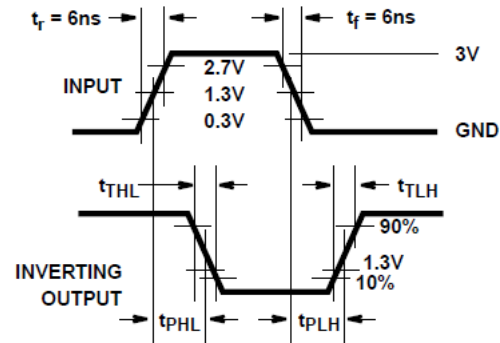


FIG 6-2. HCT transition times and propagation delay times, combination logic

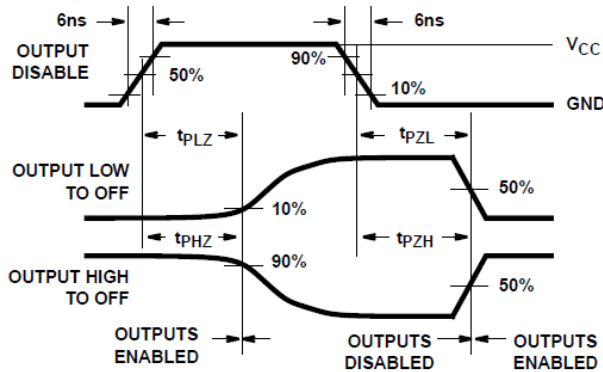


FIG 6-3. HC three-state propagation delay waveform

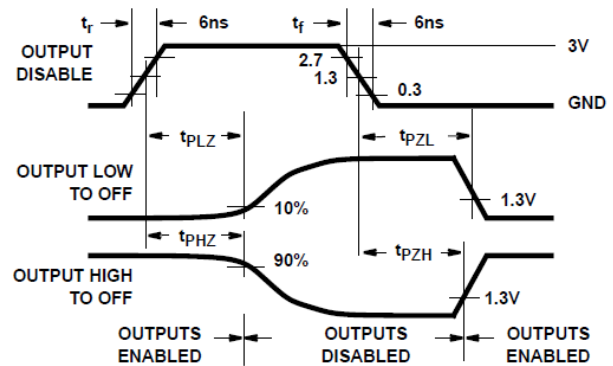


FIG 6-4. HCT three-state propagation delay waveform

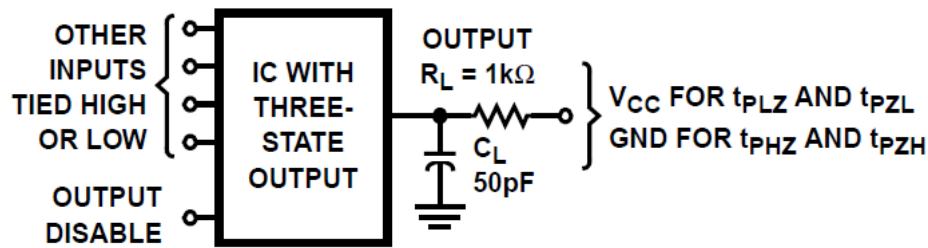


FIG 6-5. HC and HCT three-state propagation delay test circuit

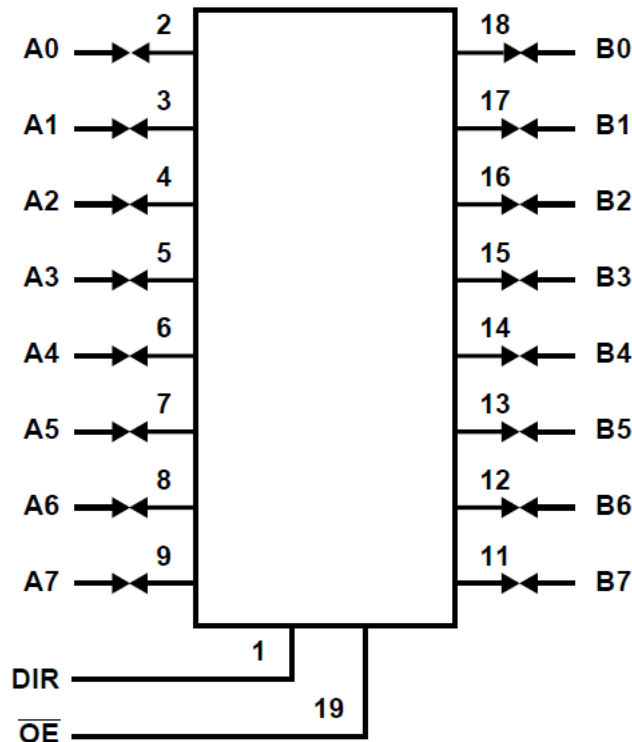
## 7 Detailed Description

### 7.1 Overview

The CD54HC245, CD54HCT245, and CD74HC245, CD74HCT245 are high-speed octal three-state bidirectional transceivers intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation while driving large bus capacitances. They provide the low power consumption of standard CMOS circuits with speeds and drive capabilities comparable to that of LSTTL circuits.

The CD54HC245, CD54HCT245, CD74HC245 and CD74HCT245 allow data transmission of the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the direction. The output enable input (OE), when high, puts the I/O ports in the high-impedance state.

The HC/HCT245 is similar in operation to the HC/HCT640 and the HC/HCT643.



Functional Block Diagram

### 7.2 Device Functional Modes

表 7-1. Truth Table

Control Inputs <sup>(1)</sup>		Operation
OE	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

(1) H = High Level, L = Low Level, X = Irrelevant



## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC245F	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC245F	<a href="#">Samples</a>
CD54HC245F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408501RA CD54HC245F3A	<a href="#">Samples</a>
CD54HCT245F	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT245F	<a href="#">Samples</a>
CD54HCT245F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8550601RA CD54HCT245F3A	<a href="#">Samples</a>
CD74HC245E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC245E	<a href="#">Samples</a>
CD74HC245M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	HC245M	
CD74HC245M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC245M	<a href="#">Samples</a>
CD74HCT245E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT245E	<a href="#">Samples</a>
CD74HCT245EE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT245E	<a href="#">Samples</a>
CD74HCT245M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	HCT245M	
CD74HCT245M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT245M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC245, CD54HCT245, CD74HC245, CD74HCT245 :**

- Catalog : [CD74HC245](#), [CD74HCT245](#)
- Military : [CD54HC245](#), [CD54HCT245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC245M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HC245M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT245M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT245M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC245M96	SOIC	DW	20	2000	356.0	356.0	41.0
CD74HC245M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT245M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT245M96	SOIC	DW	20	2000	356.0	356.0	41.0

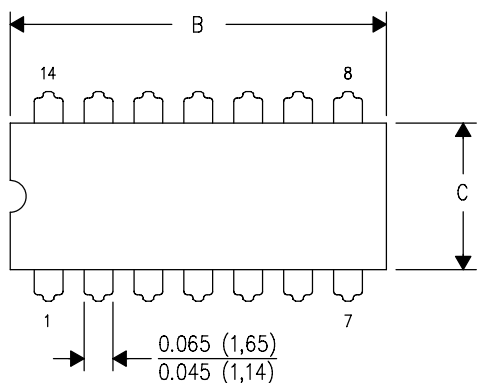
**TUBE**


\*All dimensions are nominal

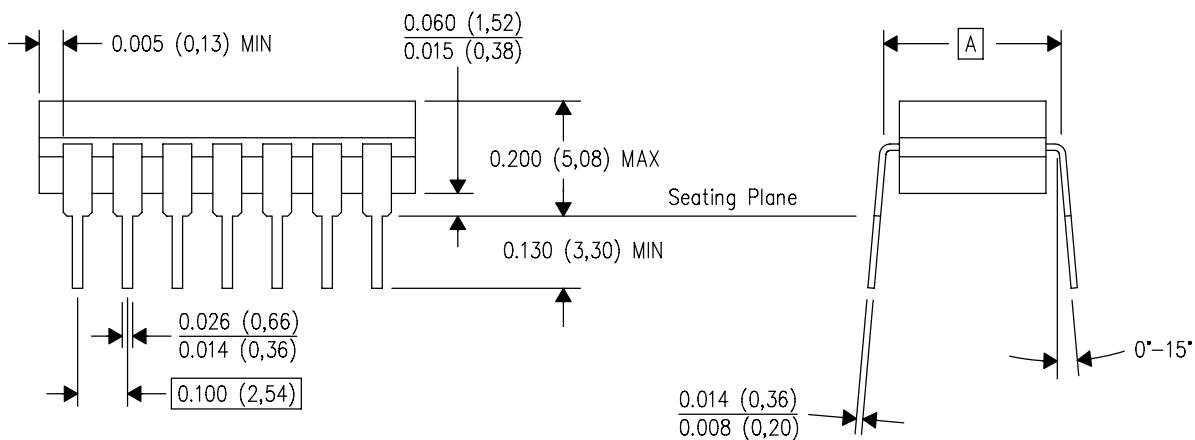
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC245E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT245E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT245EE4	N	PDIP	20	20	506	13.97	11230	4.32

J (R-GDIP-T\*\*)  
 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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