ISO35T トランス・ドライバ内蔵、絶縁型 3.3V RS-485 トランシーバ

1 特長

- RS-485 および RS-422 アプリケーション用に設計
- 最大 1Mbps の信号速度
- 1/8 ユニット負荷 - 1 個のバスに最大 256 個のノード
- サーマル・シャットダウン保護
- 標準的な効率が 60% 超 (I_{LOAD} = 100mA) - SLUU470 を参照
- 16pF の低ドライバ・バス容量 (標準値)
- バスの開放、短絡、アイドル時のフェイルセーフを備えるレシーバ
- ロジック入力は 5V 許容
- 50kV/μs の標準過渡耐性
- バス・ピンの ESD 保護
  - バス・ピンと GND2 の間に 16kV HBM
  - バス・ピンと GND1 の間に 6kV HBM
- 安全および規制の認定
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した 4242 V_{PK} の基本絶縁
  - UL 1577 に準拠した 2500 V_{RMS} での 1 分間の絶縁
  - CSA Component Acceptance Notice 5A、IEC 60950-1、および IEC 61010-1 規格

2 アプリケーション

- 絶縁型 RS-485/RS-422 インターフェイス
- ファクトリ・オートメーション
- モーター / モーション制御
- HVAC およびビルディング・オートメーション・ネットワーク
- ネットワーク接続セキュリティ・ステーション

3 概要

ISO35T は、絶縁トランスに 1 次電圧を供給する発振器出力を内蔵した絶縁型差動ライン・トランシーバです。このデバイスは RS-485 および RS-422 アプリケーション向けの全二重差動ライン・トランシーバで、ピン 11 をピン 14、ピン 12 をピン 13 に接続することで簡単に半二重用に構成できます。

これらのデバイスは、はるかに大きな同相電圧範囲を許容するようにグランド・ループが切断されているため、長い伝送ラインに理想的です。デバイスの対称型絶縁バリアは、バスライン・トランシーバとロジックレベル・インターフェイスとの間で、VDE に従い、4242V_{PK} で 60 秒間の絶縁を行うことがテスト済みです。

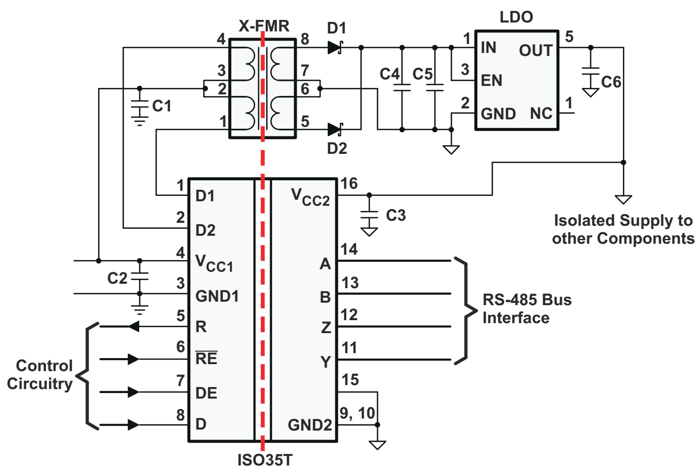
ケーブル接続されたすべての I/O は、各種ノイズ源からの電気的ノイズの過渡現象にさらされる可能性があります。このようなノイズ過渡は、十分な大きさと持続時間を持つ場合、トランシーバや隣接する敏感な回路に損傷を与える可能性があります。ISO35T は、データの破損や高価な制御回路の損傷が発生する危険性を大幅に低減できます。

ISO35T は、-40℃～85℃での使用が規定されています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
ISO35T	SOIC (16)	10.30mm × 7.50mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (October 2015) to Revision E (August 2023) **Page**

- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations......6
- Updated electrical and switching characteristics to match device performance......8

Changes from Revision C (July 2011) to Revision D (October 2015) **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加......1
- VDE 規格を DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 に変更......1

Changes from Revision B (June 2011) to Revision C (July 2011) **Page**

Changes from Revision A (March 2011) to Revision B (May 2011) **Page**

- Changed pin 16 From: V_{CC1} To: V_{CC2} in the DW Package drawing......3

Changes from Revision * (November 2010) to Revision A (March 2011) **Page**

- データシートを「製品プレビュー」から「量産データ」に変更......1
- Changed the designator of common mode voltage in Recommended operating condition to V_I......4

5 Pin Configuration and Functions

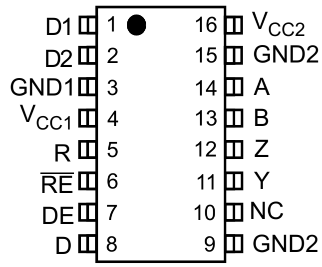


図 5-1. DW Package 16-Pin SOIC Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	14	I	Non-inverting Receiver Input
B	13	I	Inverting Receiver Input
D	8	I	Driver Input
D1	1	O	Transformer Driver Terminal 1, Open-Drain Output
D2	2	O	Transformer Driver Terminal 2, Open-Drain Output
DE	7	I	Driver Enable Input
GND1	3	–	Logic-side Ground
GND2	9, 15	–	Bus-side Ground. Both pins are internally connected.
NC	10	–	No Connect. This pin is not connected to any internal circuitry.
R	5	O	Receiver Output
$\overline{RE}$	6	I	Receiver Enable Input. This pin has complementary logic.
V_{CC1}	4	–	Logic-side Power Supply
V_{CC2}	16	–	Bus-side Power Supply
Y	11	O	Non-inverting Driver Output
Z	12	O	Inverting Driver Output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{CC} [(2)]	Supply voltage, V_{CC1}, V_{CC2}	-0.3	6	V
V_A , V_B , V_Y , V_Z	Voltage at any bus I/O terminal (A,B,Y,Z)	-9	14	V
V_{D1}, V_{D2}	Voltage at D1, D2		14	V
$V_{(TRANS)}$	Voltage input, transient pulse, A, B, Y, and Z (through 100Ω, see Figure 27)	-50	50	V
V_I	Voltage input at any D, DE or $\overline{RE}$ terminal	-0.5	6	V
I_O	Receiver output current	-10	10	mA
I_{D1}, I_{D2}	Transformer Driver Output Current		450	mA
T_J	Junction temperature		150	℃
T_{STG}	Storage temperature	-65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001[(1)]	Bus pins and GND1	±6000	V
$V_{(ESD)}$	Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001[(1)]	Bus pins and GND2	±16000	V
$V_{(ESD)}$	Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001[(1)]	All pins	±4000	V
$V_{(ESD)}$	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]		±1500	V
$V_{(ESD)}$	Machine model (MM), ANSI/ ESDS5.2-1996		±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC1}	Supply Voltage, Side 1	3	3.3	3.6	V
V_{CC2}	Supply Voltage, Side 2	3	3.3	3.6	V
V_I	Common Mode voltage at any bus terminal: A or B	-7		12	V
V_{IH}	High-level input voltage (D, DE, $\overline{RE}$ inputs)	2		V_{CC1}	V
V_{IL}	Low-level input voltage (D, DE, $\overline{RE}$ inputs)	0		0.8	V
V_{ID}	Differential input voltage, A with respect to B	-12		12	V
R_L	Differential load resistance	54	60		Ω
I_O	Output current, Driver	-60		60	mA
I_O	Output current, Receiver	-8		8	mA
T_A	Ambient temperature	-40		85	℃

		MIN	TYP	MAX	UNIT
$1/t_{UI}$	Signaling rate			1	Mbps

6.4 Thermal Information

THERMAL METRIC[1]		ISO35T DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the no.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2}$ = 3.6 V, TJ = 150°C, CL = 15 pF, Input a 0.5 MHz 50% duty cycle square wave			373	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE DW-16	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	8	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) [2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	4242	V_{PK}
q_{pd}	Apparent charge[3]	Method b; At routine test (100% production) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤5	pC
C_{IO}	Barrier capacitance, input to output[4]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	2	pF
C_I	Input capacitance to ground	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, V_{CC} = 5 V	2	pF
R_{IO}	Isolation resistance[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/085/21	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the

isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

(2) This coupler is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Apparent charge is electrical discharge caused by a partial discharge (pd).

(4) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 60950-1 and IEC 61010-1	Certified according to UL 1577 Component Recognition Program
Basic insulation, Maximum Transient Isolation Voltage, 4242 V_{PK} Maximum Surge Isolation Voltage, 4000 V_{PK} Maximum repetitive peak Isolation Voltage, 566 V_{PK}	3000 V_{RMS} Isolation Rating; Reinforced insulation per CSA 61010-1 and IEC 61010-1 150 V_{RMS} working voltage; Basic insulation per CSA 61010-1 and IEC 61010-1 600 V_{RMS} working voltage; Basic insulation per CSA 60950-1 and IEC 60950-1 760 V_{RMS} working voltage	Single protection, 2500 V_{RMS}
Certificate number: 40047657	Master contract number: 220991	File number: E181974

6.8 Safety Limiting Values

Safety limiting[(1)] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 80.5°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see #none#			431	mA
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Driver differential-output voltage magnitude	I_O = 0 mA, no load	2.5		V_{CC2}	V
		R_L = 54 Ω, See Figure 11	1.5	2		V
		R_L = 100 Ω (RS-422), See Figure 11	2	2.3		V
		V_{test} from –7 V to +12 V, See Figure 12	1.5			V
$\Delta \lvert V_{OD} \rvert$	Change in differential output voltage between two states	See Figure 11 and Figure 12	–200		200	mV
$V_{OC(SS)}$	Common-mode output voltage	See Figure 13	1	2.6	3	V
$\Delta V_{OC(SS)}$	change in steady-state common-mode output voltage between two states	See Figure 13	–100		100	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 13		0.5		V
I_I	Input current	D, DE, V_I at 0 V or V_{CC1}	–10		10	µA
I_{OZ}	High-impedance state output current	V_Y or V_Z = 12 V, V_{CC} = 0V or 3V, DE = 0V; other input at 0 V			90	µA
		V_Y or V_Z = -7 V, V_{CC} = 0V or 3V, DE = 0V; other input at 0 V	-10			µA
$I_{OS(P)}$ (1)	Short-circuit output current	V_Y or V_Z = –7 V to +12 V, Figure 14; Other input at 0 V		300		mA
$I_{OS(ss)}$ (1)	Short-circuit output current	V_Y or V_Z = –7 V to +12 V, Figure 14; Other input at 0 V	–250		250	mA
C_{OD}	Differential output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		16		pF

(1) This device has thermal shutdown and output current-limiting features to protect in short-circuit fault condition.

6.10 Electrical Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA			–20	mV
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA	–200			mV
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_O = -8 mA	2.4			V
V_{OL}	Low-level output voltage	V_{ID} = -200 mV, I_O = 8 mA			0.4	V
$I_{O(Z)}$	Output high-impedance current	V_O = 0 or V_{CC1}, $\overline{RE}$ = V_{CC1}	–1		1	µA
I_A or I_B	Bus input current	V_A or V_B = 12 V, Other input at 0 V		50	100	µA
		V_A or V_B = 12 V, VCC = 0, Other input at 0 V		60	100	µA
		V_A or V_B = –7 V, Other input at 0 V	-100	-40		µA
		V_A or V_B = –7 V, V_{CC} = 0, Other input at 0 V	-100	-30		µA
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V	-10		10	µA

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V	-10		10	µA
R_{ID}	Differential input resistance	Measured between A & B	96			kohm
C_{ID}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		15		pF

6.11 Supply Current

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER ENABLED, RECEIVER DISABLED					
I_{CC1} (1)	DE & $\overline{RE}$ = 0V or V_{CC1} (Driver and Receiver Enabled or Disabled), D = 0 V or V_{CC1}, No load		4.5	8	mA
I_{CC2} (1)	$\overline{RE}$ = 0 V or V_{CC1}, DE = 0 V (driver disabled), No load		7.5	13	mA
I_{CC2} (1)	$\overline{RE}$ = 0 V or V_{CC1}, DE = V_{CC1} (driver enabled), D = 0 V or V_{CC1}, No load		9	16	mA
CMTI	See Figure 23	25	50		kV/us

(1) I_{CC1} and I_{CC2} are measured when device is connected to external power supplies, V_{CC1} & V_{CC2}. In this case, D1 & D2 are open and disconnected from external transformer.

6.12 Transformer Driver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	V_{CC1} = 3.3 V ± 10%, D1 and D2 connected to transformer	300	400	550	kHz
R_{ON}	Switch on resistance	D1 and D2 connected to 50Ω pullup resistors		1	2.5	ohm
t_{r_D}	D1, D2 output rise time	V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		70		ns
t_{f_D}	D1, D2 output fall time	V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		80		ns
f_{St}	Startup frequency	V_{CC1} = 2.4 V, D1 and D2 connected to transformer		350		kHz
t_{BBM}	Break before make time delay	V_{CC1} = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		140		ns

6.13 Switching Characteristics: Driver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
500-kbps DEVICES						
t_{PHL}, t_{PLH}	Propagation delay	See Figure 15		205	340	ns
PWD	Pulse width distortion[(1)], $\|t_{PHL} – t_{PLH}\|$	See Figure 15		1.5		ns
t_r, t_f	Differential output rise time and fall time	See Figure 15	120	180	300	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output	See Figure 16			530	ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 16			205	ns
t_{PLZ}	Propagation delay, low-level to high-impedance output	See Figure 17			330	ns
t_{PZL}	Propagation delay, standby-to-low-level output	See Figure 17			530	ns

(1) Also known as pulse skew.

6.14 Switching Characteristics: Receiver

All typical specs are at V_{CC1}=3.3V, V_{CC2}=5V, T_A=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
500-kbps DEVICES						
t_{PHL}, t_{PLH}	Propagation delay	See Figure 19		85	115	ns
PWD	Pulse Skew, $\|t_{PHL} – t_{PLH}\|$	See Figure 19			13	ns
t_r, t_f	Differential output rise time and fall time	See Figure 19		1	4	ns
t_{PHZ}, t_{PLZ}	Propagation delay, high-impedance-to-high-level output, Propagation delay, high-impedance-to-low-level output	See Figure 20, DE at 0 V		13	25	ns
t_{PZH}, t_{PZL}	Propagation delay, high-level-to-high-impedance output, Propagation delay, low-level to high-impedance output	See Figure 21, DE at 0 V		13	25	ns

6.15 Insulation Characteristics Curves

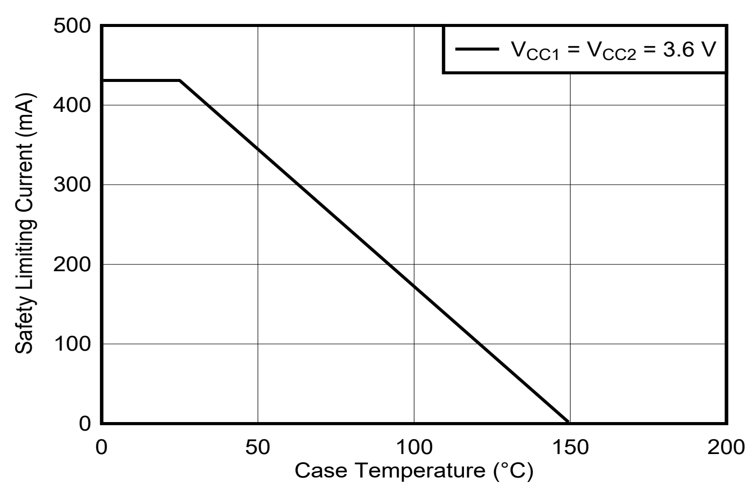
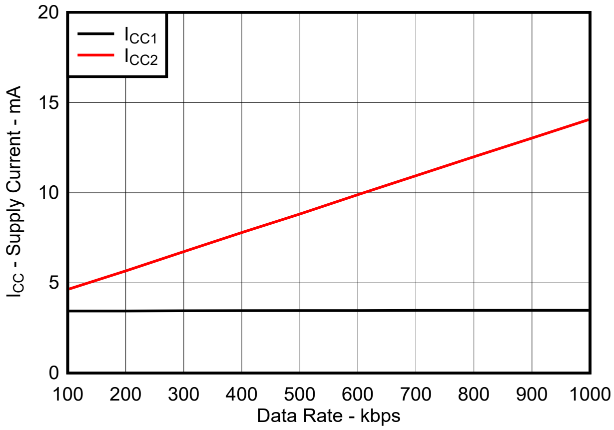


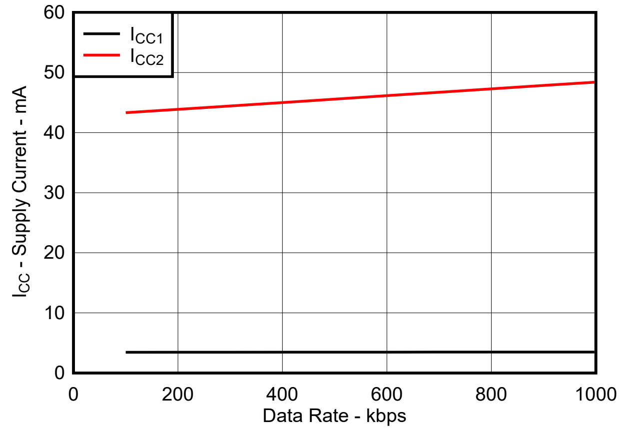
図 6-1. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

6.16 Typical Characteristics



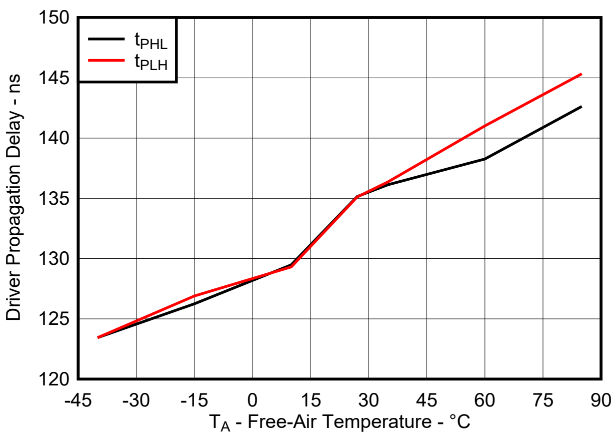
T_A = 25 °C V_{CC1} = V_{CC2} = 3.3 V   PRBS Data 2^{16} - 1

図 6-2. Supply Current vs Data Rate With No Load



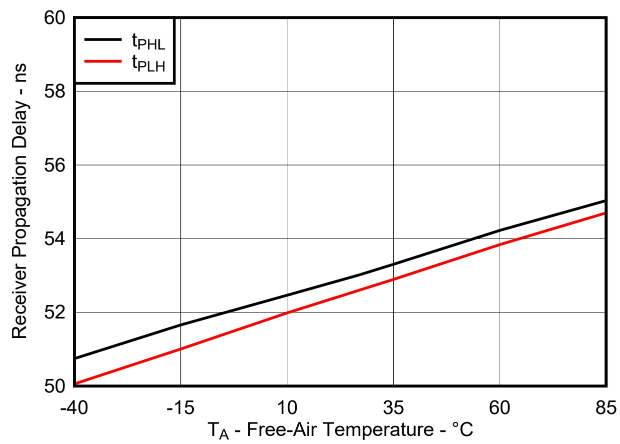
T_A = 25 °C   Receiver C_L = 15 pF   PRBS Data 2^{16} - 1
Driver C_L = 50 pF   Driver R_L = 54 Ω V_{CC1} = V_{CC2} = 3.3 V

図 6-3. Supply Current vs Data Rate With Load



V_{CC1} = V_{CC2} = 3.3 V C_L = 50 pF R_L = 54 Ω

図 6-4. Driver Propagation Delay vs Free-Air Temperature



V_{CC1} = V_{CC2} = 3.3 V C_L = 15 pF

図 6-5. Receiver Propagation Delay vs Free-Air Temperature

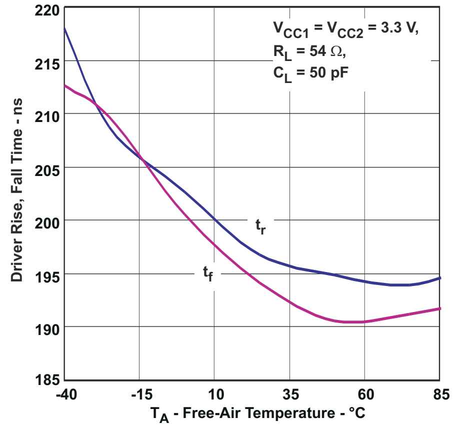


図 6-6. Driver Rise, Fall Time vs Free-Air Temperature

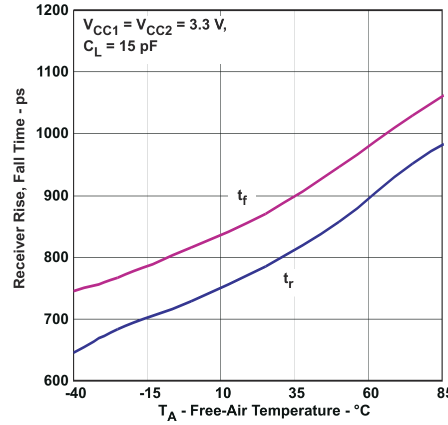


図 6-7. Receiver Rise, Fall Time vs Free-Air Temperature

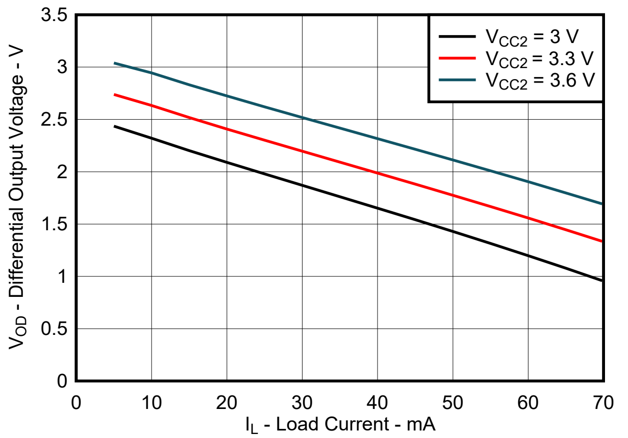


図 6-8. Differential Output Voltage vs Load Current

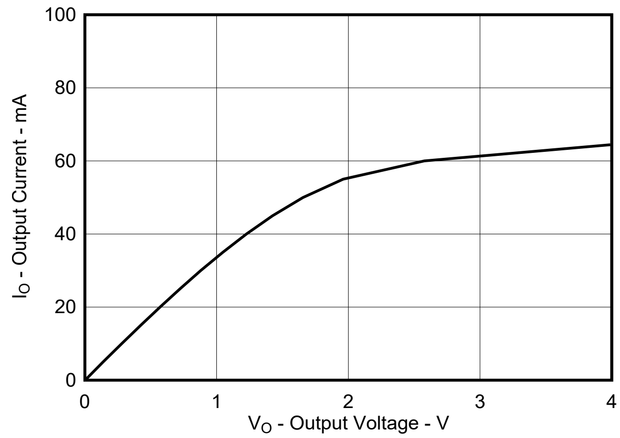


図 6-9. Receiver Low-Level Output Current vs Low-Level Output Voltage

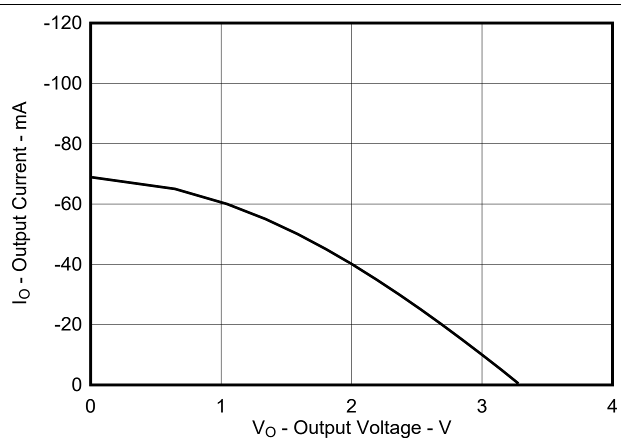


図 6-10. Receiver High-Level Output Current vs High-Level Output Voltage

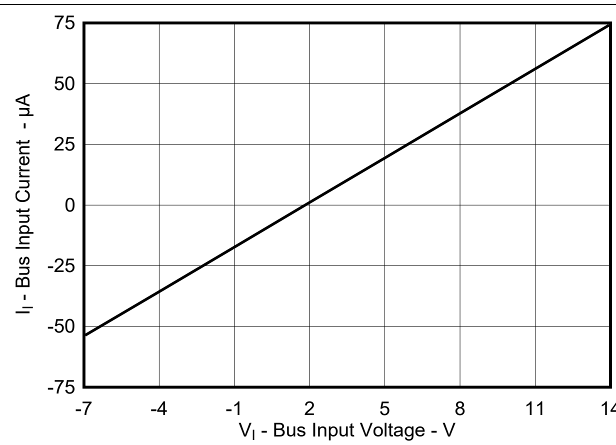


図 6-11. Bus Input Current vs Input Voltage

7 Parameter Measurement Information

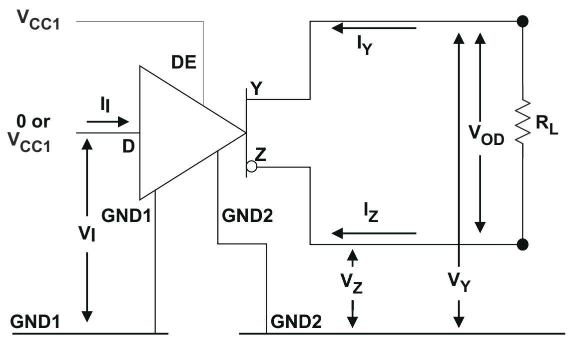


図 7-1. Driver V_{OD} Test and Current Definitions

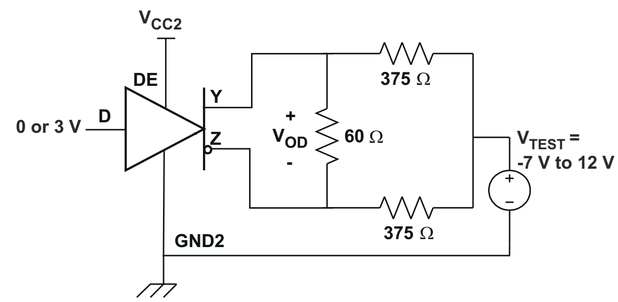


図 7-2. Driver V_{OD} With Common-Mode Loading Test Circuit

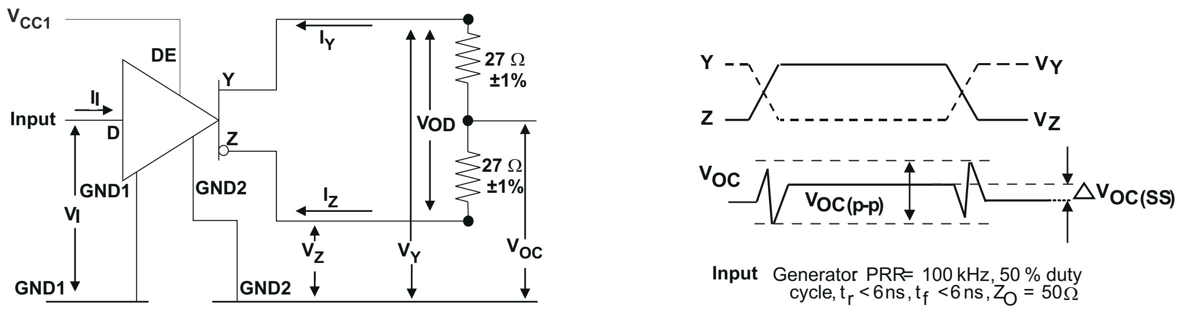


図 7-3. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage

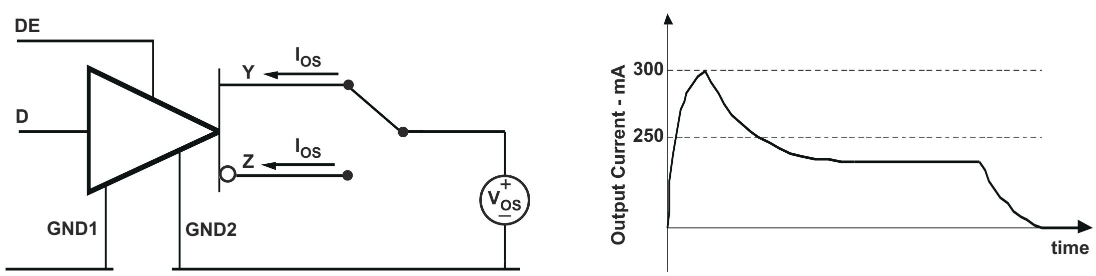


図 7-4. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t=0

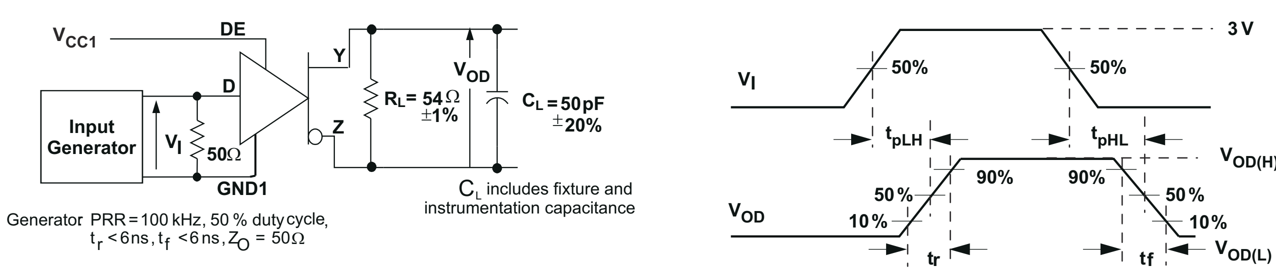


図 7-5. Driver Switching Test Circuit and Voltage Waveforms

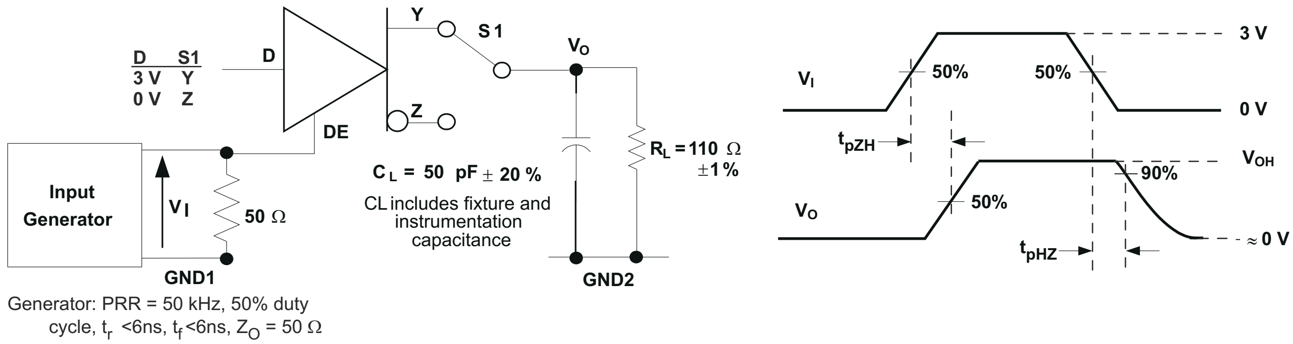


図 7-6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

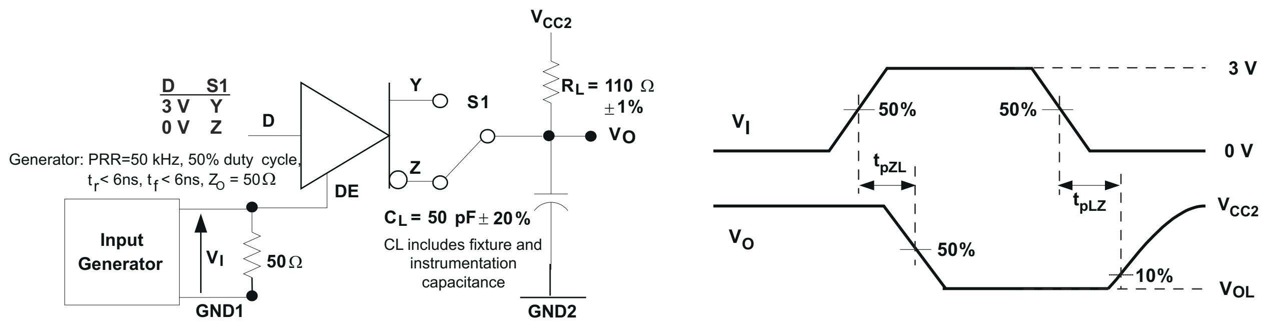


図 7-7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

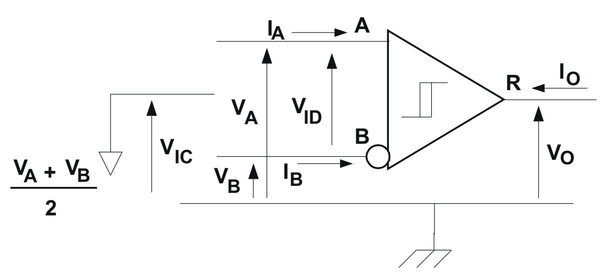


図 7-8. Receiver Voltage and Current Definitions

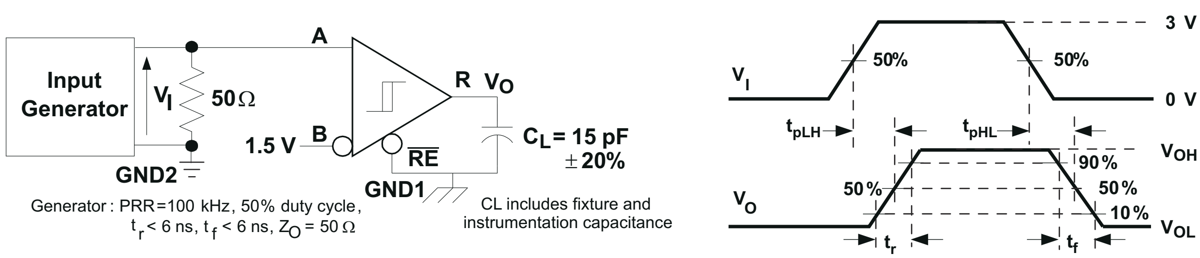


図 7-9. Receiver Switching Test Circuit and Waveforms

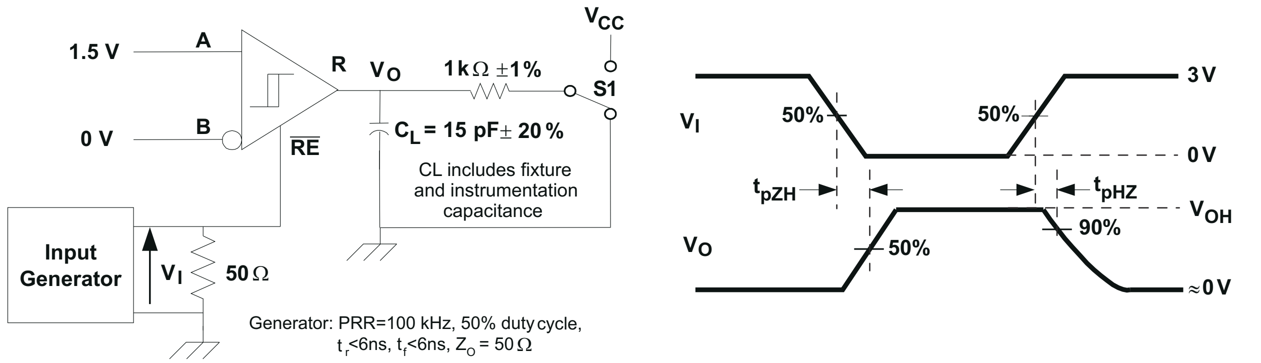


図 7-10. Receiver Enable Test Circuit and Waveforms, Data Output High

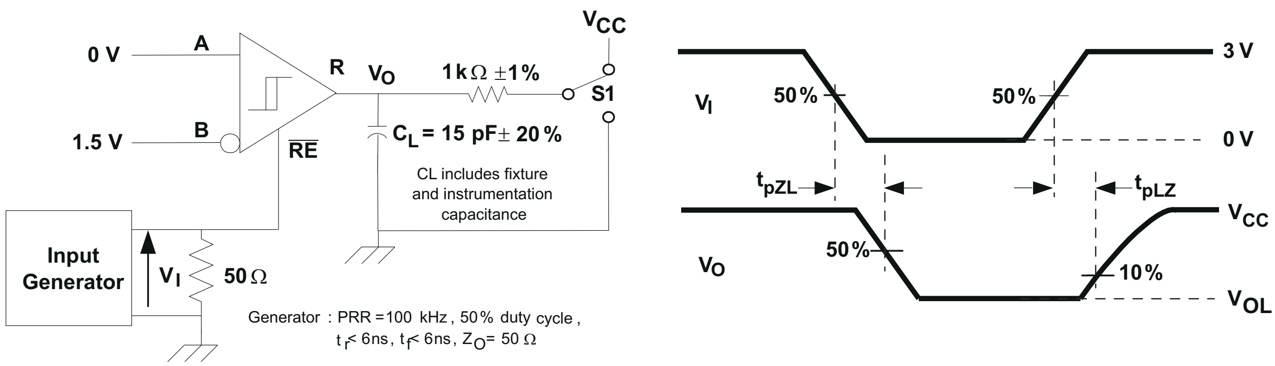


図 7-11. Receiver Enable Test Circuit and Waveforms, Data Output Low

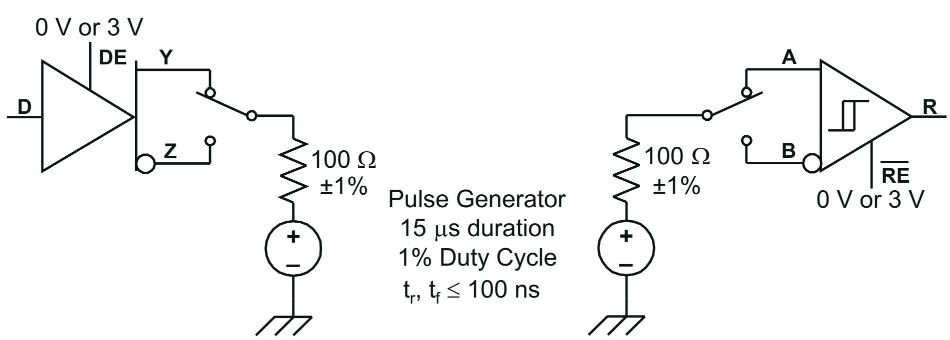


図 7-12. Transient Over-Voltage Test Circuit

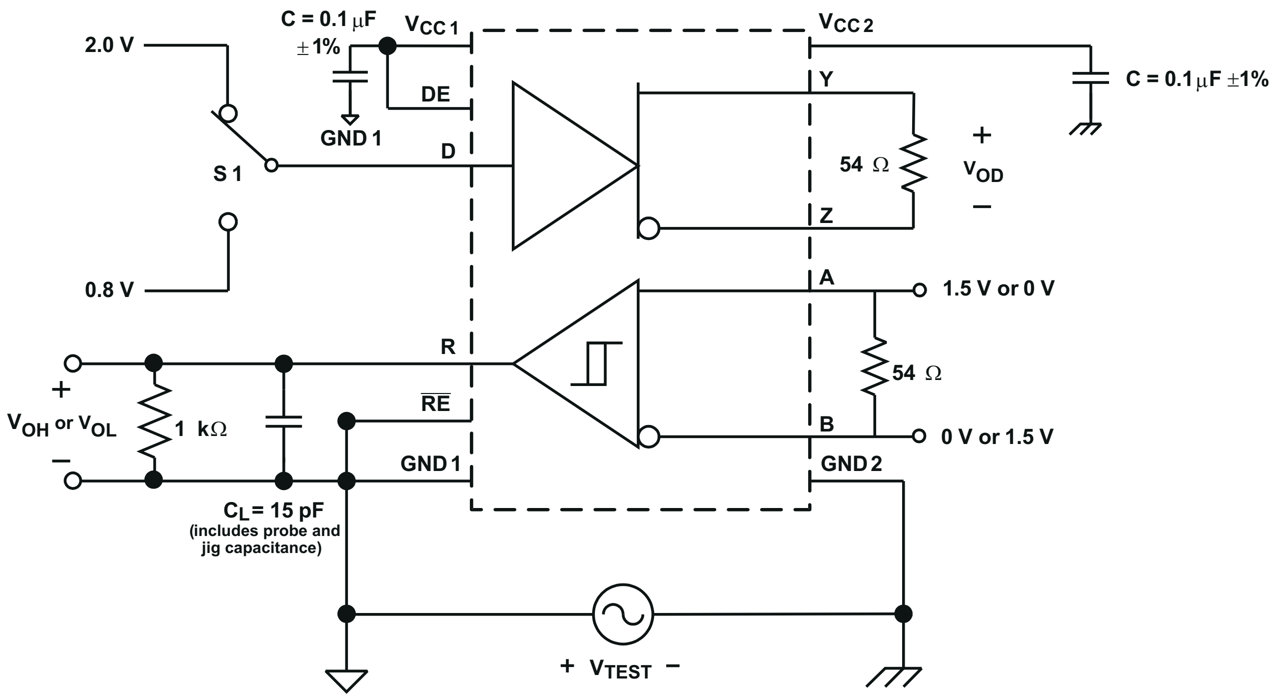


図 7-13. Common-Mode Transient Immunity Test Circuit

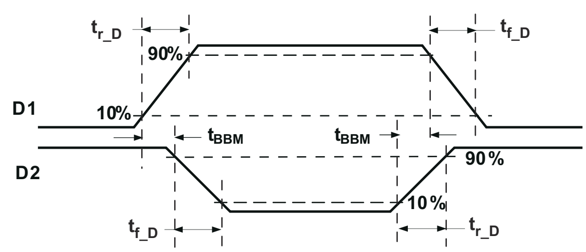


図 7-14. Transition Times and Break-Before-Make Time Delay for D1, D2 Outputs

8 Detailed Description

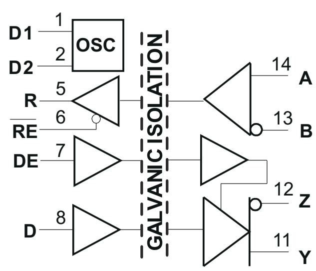
8.1 Overview

ISO35T is an isolated full-duplex differential transceiver with integrated transformer driver. The integrated transformer driver supports elegant secondary power supply design. This device is rated to provide galvanic isolation up to 4242 V_{PK} per VDE and 2500 V_{RMS} per UL. It has active-high driver enable and active-low receiver enable to control the data flow. It is suitable for data transmission up to 1 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

8.2 Functional Block Diagram



8.3 Device Functional Modes

表 8-1 and 表 8-2 are the function tables for the ISO35T driver and receiver.

表 8-1. Driver Function Table(1)

INPUT	ENABLE	OUTPUTS	
(D)	(DE)	Y	Z
H	H	H	L
L	H	L	H
X	L	hi-Z	hi-Z
X	OPEN	hi-Z	hi-Z
OPEN	H	H	L

(1) H = High Level, L= Low Level, X = Don't Care, hi-Z = High Impedance (Off)

表 8-2. Receiver Function Table(1)

DIFFERENTIAL INPUT $V_{ID} = (V_A – V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
$–0.02\ V \le V_{ID}$	L	H
$–0.2\ V < V_{ID}$ –0.02 V	L	?
$V_{ID} \le –0.2\ V$	L	L

表 8-2. Receiver Function Table[1] (続き)

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
X	H	hi-Z
X	OPEN	hi-Z
Open circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

(1) H = High Level, L= Low Level, X = Don't Care, hi-Z = High Impedance (Off), ? = Indeterminate

8.3.1 Device I/O Schematics

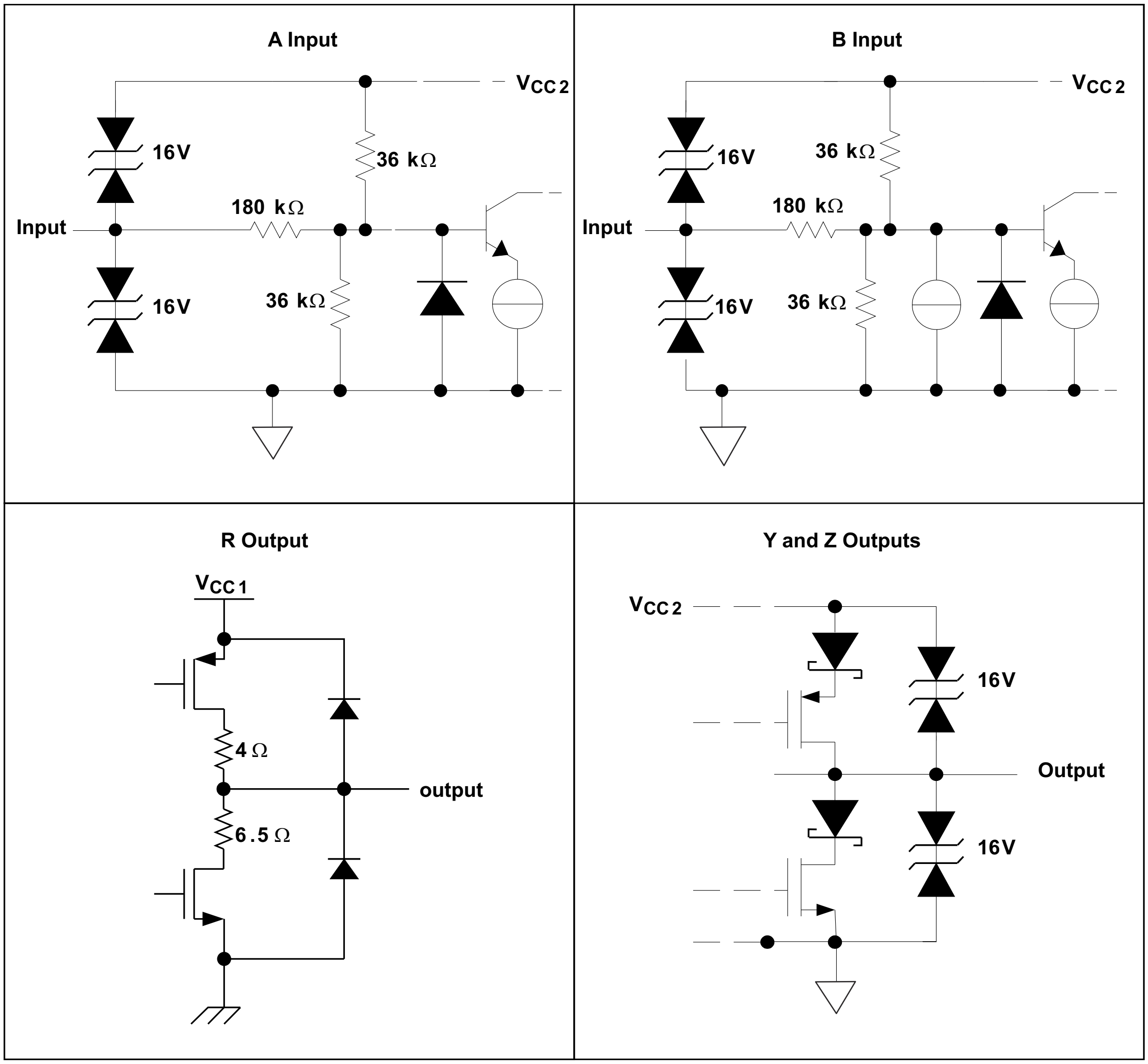


図 8-1. Equivalent Circuit Schematics

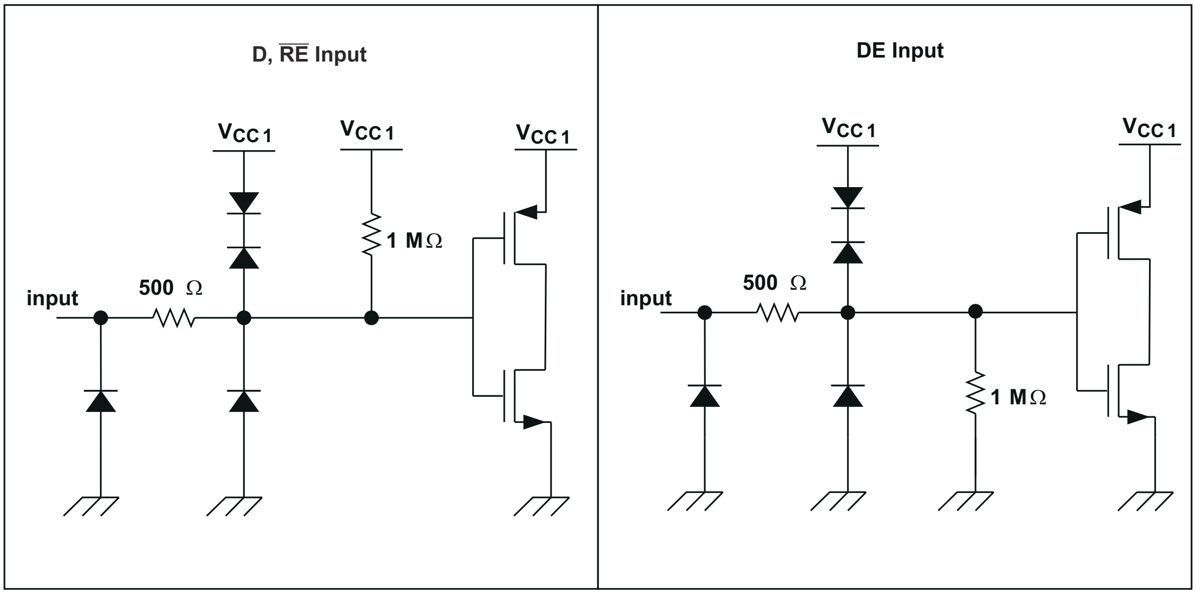


図 8-2. Equivalent Circuit Schematics

9 Application and Implementation

注

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9.1 Application Information

ISO35T is a full-duplex RS-485 transceiver commonly used for asynchronous data transmission. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

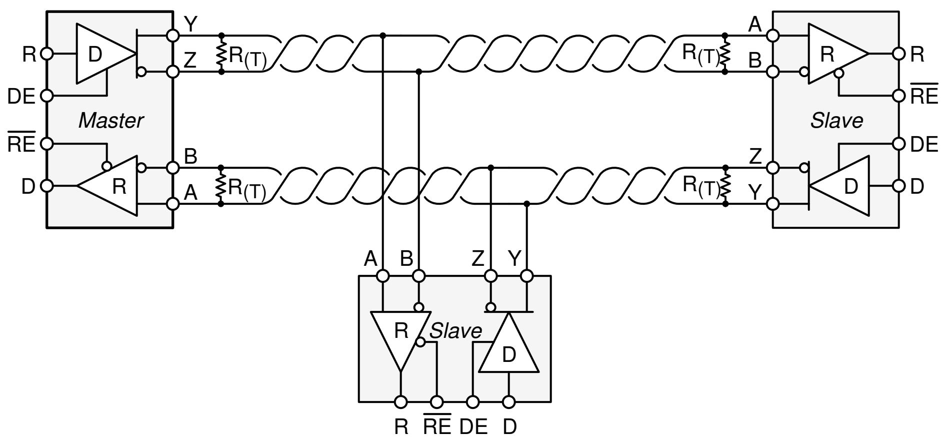

図 9-1. Typical RS-485 Network With Full-Duplex Transceivers

9.2 Typical Application

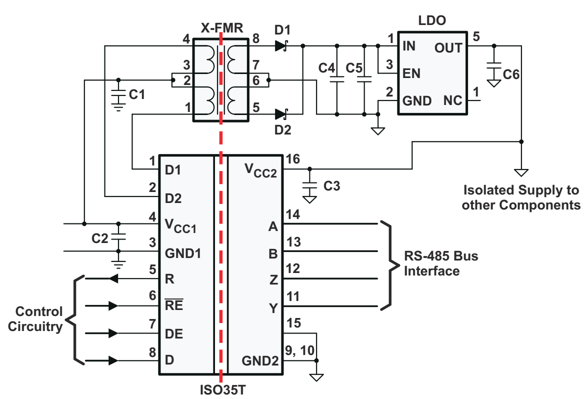

図 9-2. Typical Application Circuit

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

表 9-1. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

9.2.2 Detailed Design Procedure

9.2.2.1 Transient Voltages

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation and the transient ratings of ISO35T are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment and can easily exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but very high voltage transients.

図 9-3 models the ISO35T bus IO connected to a noise generator. C_{IN} and R_{IN} is the device and any other stray or added capacitance or resistance across the A or B pin to GND2, C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of ISO35T plus those of any other insulation (transformer, etc.), and we assume stray inductance negligible. From this model, the voltage at the isolated bus return is shown in 式 1 and will always be less than 16 V from V_N.

$$v_{GND2} = v_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}} \tag{1}$$

If ISO35T is tested as a stand-alone device, R_{IN}= 6 × 10^4Ω, C_{IN}= 16 × 10^{-12} F, R_{ISO}= 10^9Ω and C_{ISO}= 10^{-12} F.

In 図 9-3 the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency, use 式 2, or essentially all noise appears across the barrier.

$$\frac{v_{GND2}}{v_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4} \tag{2}$$

At very high frequency, 式 3 is true and 94% of V_N appears across the barrier.

$$\frac{v_{GND2}}{v_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94 \tag{3}$$

As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN}, most of transient noise appears across the isolation barrier, as it should.

We recommend the reader not test equipment transient susceptibility with ESD generators or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.

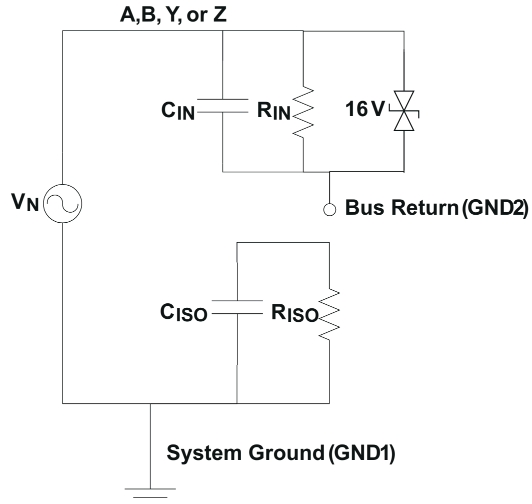

図 9-3. Noise Model

9.2.3 Application Curve

At maximum working voltage, ISO3086T isolation barrier has more than 28 years of life.

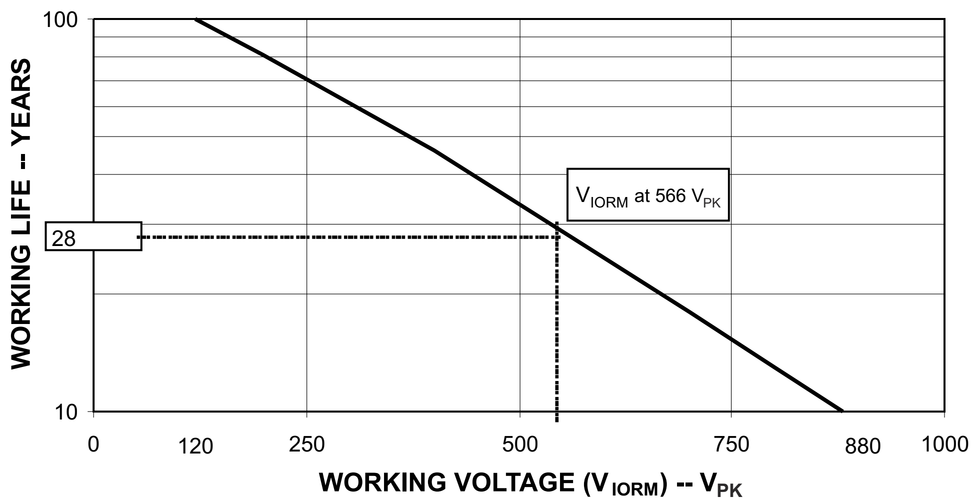

図 9-4. Time-Dependent Dielectric Breakdown Test Results

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends a 0.1-μF bypass capacitor at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. This device is used in applications where only a single primary-side power supply is available. Isolated power can be generated for the secondary-side with the help of integrated transformer driver.

11 Layout

11.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see 図 11-1).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1-μF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

注

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

11.2 Layout Example

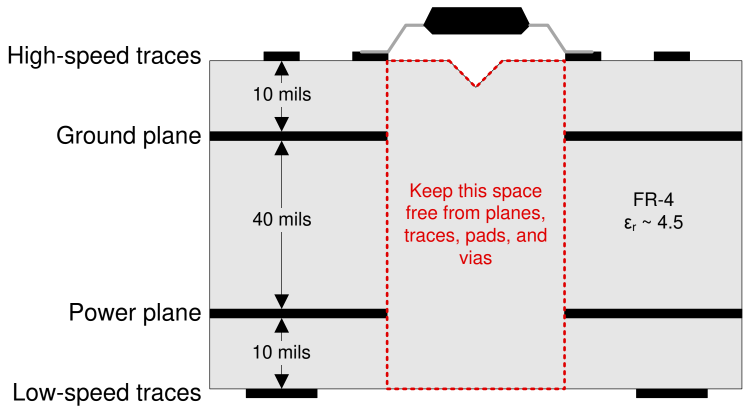

図 11-1. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Isolated, Full-Duplex, 1-Mbps, 3.3-V to 3.3-V RS-485 Interface* (*SLUU470*)
- *Digital Isolator Design Guide* (SLLA284)
- *Isolation Glossary* (SLLA353)

12.2 Community Resources

12.3 Trademarks

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12.4 静電気放電に関する注意事項

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12.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO35TDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85	ISO35TDW	
ISO35TDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35TDW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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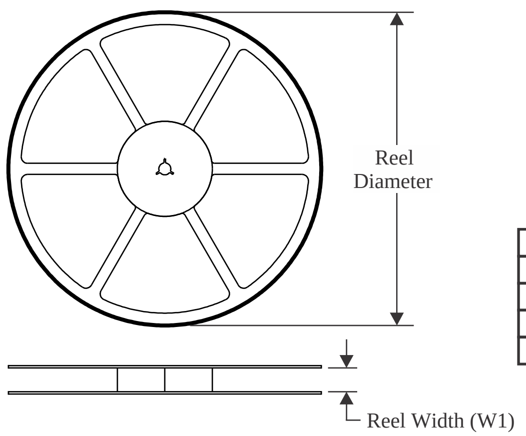
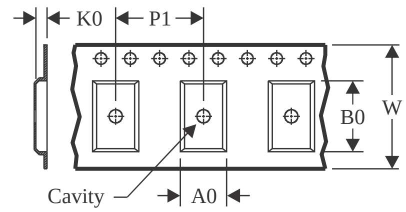
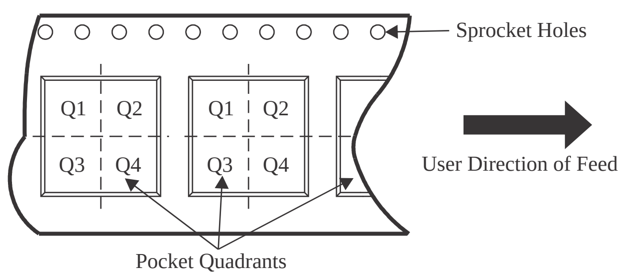
TAPE AND REEL INFORMATION





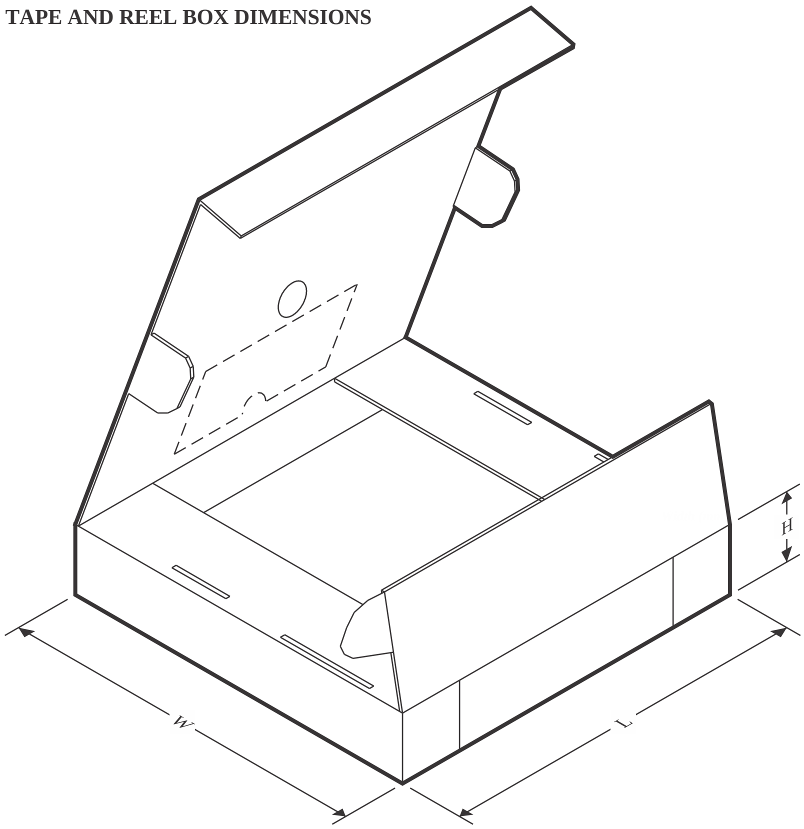
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO35TDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

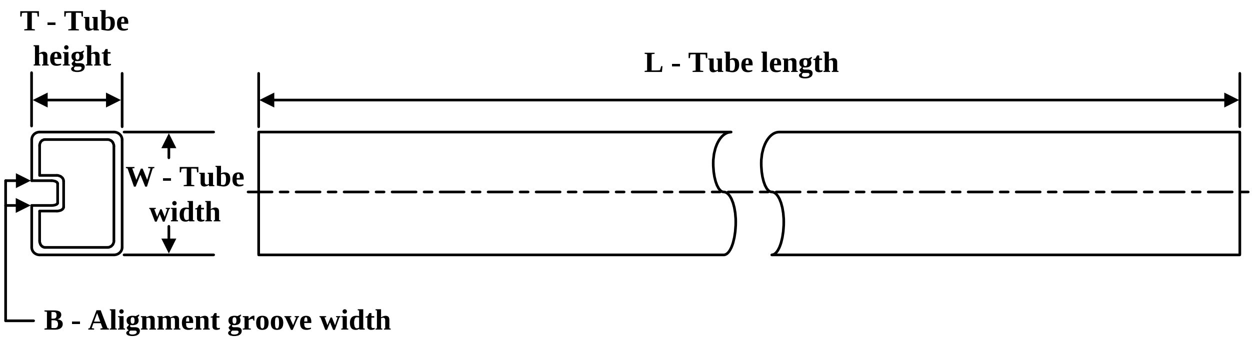
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO35TDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO35TDW	DW	SOIC	16	40	506.98	12.7	4826	6.6

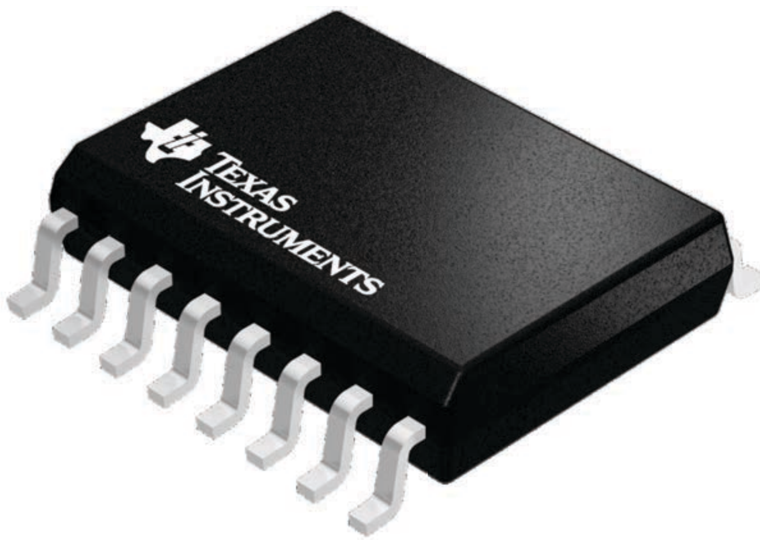
DW 16

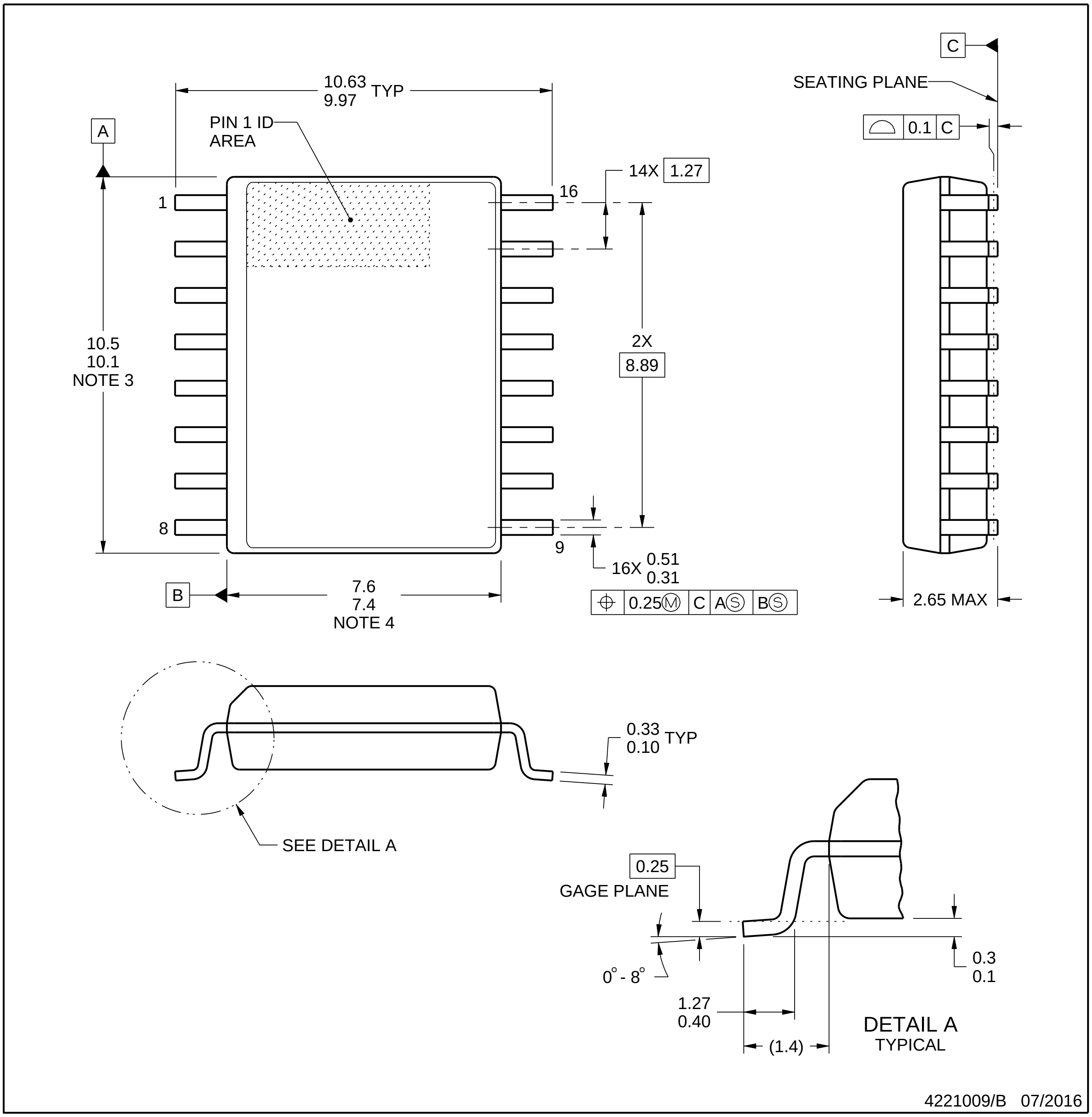
SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





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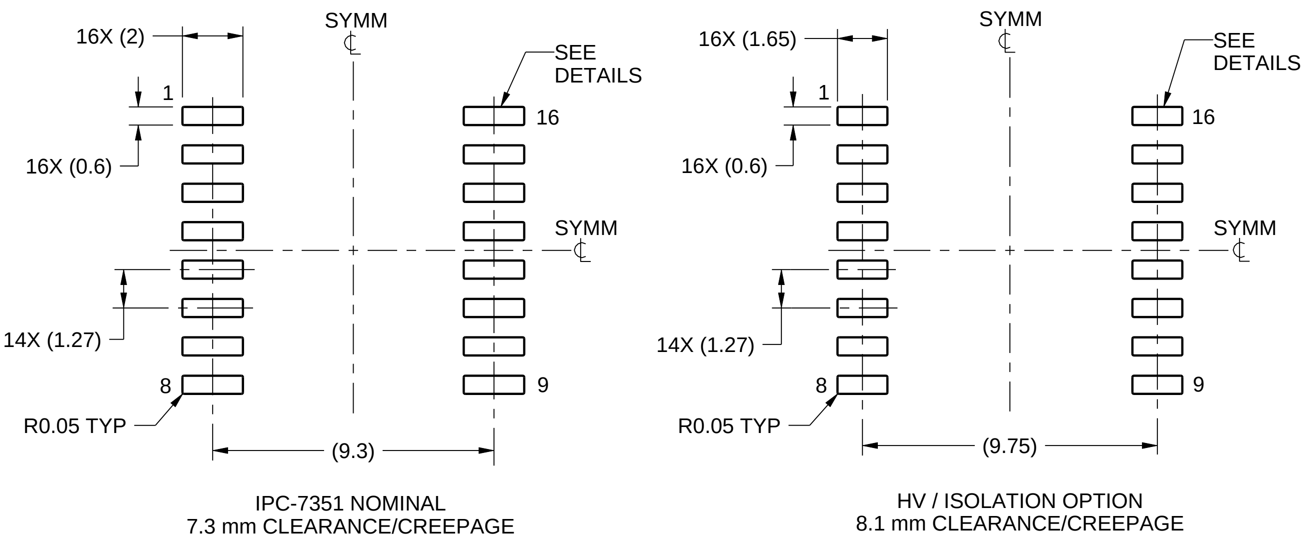
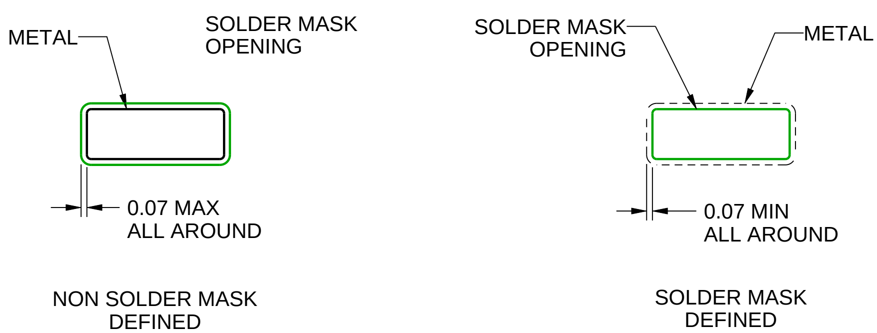
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

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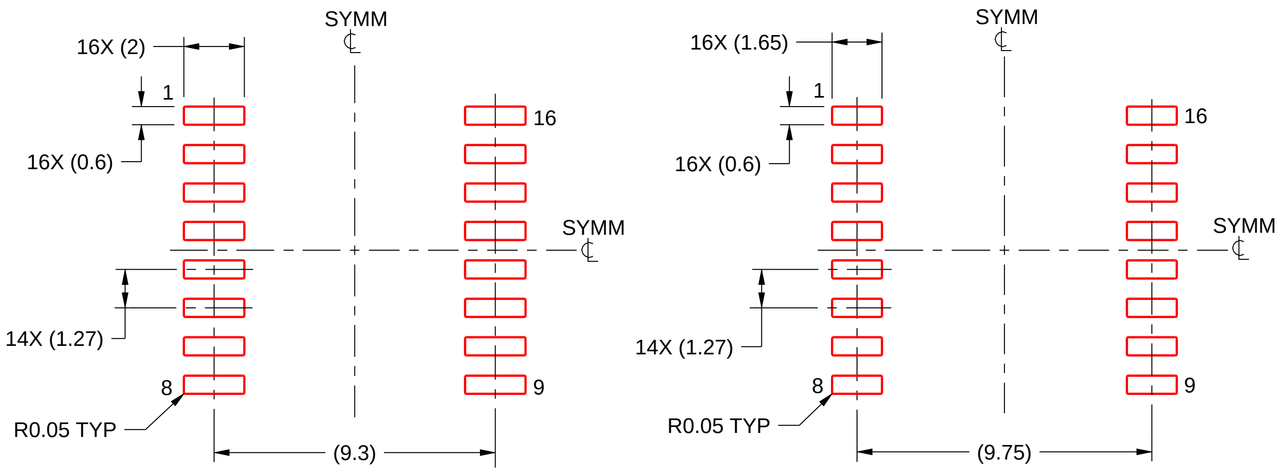
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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