

LM339B、LM2901B、LM339、LM239、LM139、LM2901 クワッド差動コンパレータ

1 特長

- 新しい **LM339B** および **LM2901B**
- B バージョンの仕様を改善
 - 最大定格: 最大 38V
 - ESD 定格 (HBM): 2kV
 - 低入力オフセット: 0.37mV
 - 低入力バイアス電流: 3.5nA
 - 低消費電流: 200 μ A (コンパレータあたり)
 - 短い応答時間: 1 μ s
 - 拡張温度範囲 (LM339B)
- B バージョンは、LM239、LM339、LM2901 の A および V バージョンをそのまま置き換えることが可能
- 同相入力電圧範囲にグランドを含む
- 差動入力電圧範囲が最大定格電源電圧と同じ: $\pm 38V$
- 低い出力飽和電圧
- TTL、MOS、CMOS 互換出力
- シングル・バージョンについては、**TL331B** を参照してください
- デュアル・バージョンについては、**LM393B** または **LM2903B** を参照してください

2 アプリケーション

- ロボット掃除機
- 単相 UPS
- サーバー PSU
- コードレス電動工具
- ワイヤレス・インフラ
- 電化製品
- ビル・オートメーション
- ファクトリ・オートメーションおよび制御
- モーター・ドライブ
- インフォテインメントおよびクラスタ

3 概要

LM339B および **LM2901B** デバイスは、業界標準の **LM339** および **LM2901** コンパレータ・ファミリの次世代バージョンです。これらの次世代 B バージョン・コンパレータは、小さいオフセット電圧、高い電源電圧への対応、小さい消費電流、小さい入力バイアス電流、短い伝搬遅延、および専用の ESD クランプによる優れた 2kV の ESD 性能と入力の耐久性が特長です。LM339B および LM2901B は、LM239、LM339 および LM2901 (「A」および「V」グレード) をそのまま置き換えることができます。

すべてのデバイスは、広い電圧範囲にわたって単一電源で動作するように設計された 4 つの独立した電圧コンパレータで構成されています。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
LM139x	CDIP (14)	21.30mm × 7.60mm
LM139x、LM239x、LM339x、LM2901x、LM339B、LM2901B	SOIC (14)	8.70mm × 3.90mm
LM239、LM339x、LM2901	PDIP (14)	19.30mm × 6.40mm
LM239、LM2901、LM339B、LM2901B	TSSOP (14)	5.00mm × 4.40mm
LM339x、LM2901、LM339B、LM2901B	SO (14)	10.20mm × 5.30mm
LM339x、LM339B	SSOP (14)	6.50mm × 5.30mm
LM2901B	SOT-23 (14)	4.20mm × 2.00mm
LM339B、LM2901B	WQFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ファミリ比較表

仕様	LM339B	LM2901B	LM339 LM339A	LM2901 LM2901A	LM2901V LM2901AV	LM139 LM139A	LM239 LM239A	単位
電源電圧	2~36	2~36	2~30	2~30	2~32	2~30	2~30	V
総電源電流 (5V~36V、最大値)	0.8~1	0.8~1	1~2.5	1~2.5	1~2.5	1~2.5	1~2.5	mA
温度範囲	-40~85	-40~125	0~70	-40~125	-40~125	-55~125	-25~85	°C
ESD (HBM)	2000	2000	1000	1000	1000	1000	1000	V
オフセット電圧 (全温度範囲での最大値)	± 5.5	± 5.5	± 9 ± 4	± 15 ± 4	± 15 ± 4	± 9 ± 4	± 9 ± 4	mV
入力バイアス電流 (標準値 / 最大値)	3.5/25	3.5/25	25/250	25/250	25/250	25/100	25/250	nA
応答時間 (標準値)	1	1	1.3	1.3	1.3	1.3	1.3	μ sec



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision W (October 2023) to Revision X (October 2023)	Page
<ul style="list-style-type: none"> SOT-23/QFN の「製品情報」表に LM339B および LM2901B を追加..... 	1
Changes from Revision V (December 2022) to Revision W (October 2023)	Page
<ul style="list-style-type: none"> Updated thermal tables for new package releases..... Changed Apps Input Voltage Range text to reference appnote..... 	6 24
Changes from Revision U (November 2018) to Revision V (December 2022)	Page
<ul style="list-style-type: none"> 文書全体にわたって表、図、相互参照の採番方法を更新..... 全体を通して「B」バージョンを追加「製品ファミリ」表を追加..... 	1 1
Changes from Revision T (June 2015) to Revision U (November 2018)	Page
<ul style="list-style-type: none"> 「概要」セクションで LM239x の最大温度仕様を 125°C から 85°C に変更..... データシートのタイトルを変更..... Changed LM293AD to LM239AD in <i>Device Comparison Table</i> Added Input Current and related footnote in <i>Absolute Maximum Ratings</i> Changed layout of <i>Recommended Operating Conditions</i> temperatures to separate rows..... Changed values in the Thermal Information table to align with JEDEC standards..... Added LM2901V and LMV2901AV to LM2901 Elect Char Table title to make more clear which devices are covered..... Changed "Dual" to "Quad" and removed "Absolute Maximum" wording and mention of Q100 in <i>Overview</i> section text..... Changed and corrected text in <i>Feature Description</i> section..... Changed Example Values in <i>Typical Application Design Parameters</i> table Added <i>Receiving Notification of Documentation Updates</i> section..... 	1 1 4 6 7 8 13 23 23 24 27
Changes from Revision S (August 2012) to Revision T (June 2015)	Page
<ul style="list-style-type: none"> 「注文情報」表を削除 「<i>特長</i>」の一覧に軍事利用についての免責事項を追加..... 「アプリケーション」、「製品情報」表、「ピン構成および機能」セクション、「ESD 定格」表、「熱に関する情報」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。仕様の変更はなし..... 	1 1 1

5 Other Versions

OTHER QUALIFIED VERSIONS OF LM139-SP, LM239A, LM2901, LM2901AV, LM2901V:

- Automotive Q100: [LM239A-Q1](#), [LM2901B-Q1](#), [LM2901-Q1](#), [LM2901AV-Q1](#), [LM2901V-Q1](#)
- Enhanced Product: [LM239A-EP](#)
- Space: [LM139-SP](#)

6 Pin Configuration and Functions



图 6-1. D, DB, N, NS, PW, DYY, J Packages
14-Pin SOIC, SSOP, PDIP, SO, TSSOP, SOT-23,
CDIP
Top View



NOTE: Connect exposed thermal pad directly to GND pin.

图 6-2. RTE Package
16-Pad WQFN With Exposed Thermal Pad
Top View

表 6-1. Pin Functions

NAME ⁽¹⁾	PIN		I/O	DESCRIPTION
	D, DB, N, NS, PW, DYY, J	WQFN		
OUT1 ⁽¹⁾	1	16	Output	Output pin of the comparator 2
OUT2 ⁽¹⁾	2	15	Output	Output pin of the comparator 1
V _{CC}	3	1	—	Positive supply
IN2- ⁽¹⁾	4	5	Input	Negative input pin of the comparator 1
IN2+ ⁽¹⁾	5	6	Input	Positive input pin of the comparator 1
IN1- ⁽¹⁾	6	2	Input	Negative input pin of the comparator 2
IN1+ ⁽¹⁾	7	4	Input	Positive input pin of the comparator 2
IN3- ⁽¹⁾	8	7	Input	Negative input pin of the comparator 3
IN3+ ⁽¹⁾	9	8	Input	Positive input pin of the comparator 3
IN4- ⁽¹⁾	10	9	Input	Negative input pin of the comparator 4
IN4+ ⁽¹⁾	11	11	Input	Positive input pin of the comparator 4
GND	12	12	—	Negative supply
OUT4	13	13	Output	Output pin of the comparator 4
OUT3	14	14	Output	Output pin of the comparator 3
NC	—	3	—	No Internal Connection - Leave floating or GND
NC	—	10	—	No Internal Connection - Leave floating or GND
Thermal Pad	—	PAD	—	Connect directly to GND pin

(1) Some manufacturers transpose the names of channels 1 & 2. Electrically the pinouts are identical, just a difference in the channel naming convention.

7 Specifications

7.1 Absolute Maximum Ratings for LM339B and LM2901B

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage: $V_S = (V+) - (V-)$	-0.3	38	V
Differential input voltage: V_{ID} ⁽²⁾		±38	V
Input pins (IN+, IN-)	-0.3	38	V
Current into input pins (IN+, IN-)		-50	mA
Output pin (OUT)	-0.3	38	V
Output sink current		25	mA
Output short-circuit duration ⁽³⁾		Unlimited	s
Junction temperature, T_J	TBD	150	°C
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Differential voltages are at IN+ with respect to IN-.
- (3) Short circuits from outputs to V+ can cause excessive heating and eventual destruction.

7.2 Absolute Maximum Ratings for Non-B Versions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
V_{CC} Supply voltage ⁽²⁾		36	V
V_{ID} Differential input voltage ⁽³⁾		±36	V
V_I Input voltage range (either input)	-0.3	36	V
I_K Input current ⁽⁵⁾		-50	mA
V_O Output voltage		36	V
I_O Output current		20	mA
Duration of output short circuit to ground ⁽⁴⁾		Unlimited	
T_J Operating virtual-junction temperature		150	°C
Case temperature for 60 s		260	°C
Lead temperature 1.6 mm (1/16 in) from case for 60 s		300	°C
T_{stg} Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at xIN+ with respect to xIN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
- (5) Input current flows through parasitic diode to ground and will turn on parasitic transistors that will increase I_{CC} and may cause output to be incorrect. Normal operation resumes when input is removed.

7.3 ESD Ratings for LM339B and LM2901B

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Human-body model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

7.4 ESD Ratings, Non-B Versions

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.5 Recommended Operating Conditions for LM339B and LM2901B

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V _S = (V+) – (V–)	2	36	V
Ambient temperature, T _A , LM339B	–40	85	°C
Ambient temperature, T _A , LM2901B	–40	125	°C
Input Voltage Range, V _{IVR}	(V–) – 0.1	(V+) – 2.0	V

7.6 Recommended Operating Conditions, Non-B Versions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Non-V devices	2	30	V
		V devices	2	32	V
T _J	Junction temperature	LM139x	–55	125	°C
		LM239x	–25	85	
		LM339x	–0	70	
		LM2901x	–40	125	

7.7 Thermal Information for LM339B and LM2901B

THERMAL METRIC ⁽¹⁾		LM339B, LM2901B					UNIT
		D (SOIC)	PW (TSSOP)	DDY (SOT-23)	RUC (QFN)	RTE (QFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	111.2	136.6			67.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	66.9	66.6			72.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	67.8	79.8			43.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	28.0	17.8			6.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	67.4	79.3			42.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	-	-	-		26.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report, [SPRA953](#).

7.8 Thermal Information for Non-B Versions

THERMAL METRIC ⁽¹⁾		LMx39, LM2901x							UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	J (CDIP)	W (CFP)	
R _{θJA}	Junction-to-ambient thermal resistance	98.8	111.8	79	96.2	120	89.5	156.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	64.3	63.6	73.4	56.1	59	46.1	86.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	59.7	60.5	58.7	56.9	68.8	78.7	154.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	25.7	26.2	48.3	24.8	9.9	3	56.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	59.3	59.8	58.5	56.4	68.2	71.8	133.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	24.2	14.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.9 Electrical Characteristics for LM339B

$V_S = 5\text{ V}$, $V_{CM} = (V-)$; $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_S = 5\text{ to }36\text{V}$	-3.5	± 0.37	3.5	mV
		$V_S = 5\text{ to }36\text{V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$	-5.5		5.5	
I_B	Input bias current			-3.5	-25	nA
		$T_A = -40^\circ\text{C to }+85^\circ\text{C}$			-50	nA
I_{OS}	Input offset current		-25	± 0.5	25	nA
		$T_A = -40^\circ\text{C to }+85^\circ\text{C}$	-50		50	nA
V_{CM}	Common mode range ⁽¹⁾	$V_S = 3\text{ to }36\text{V}$	(V-)		(V+) - 1.5	V
		$V_S = 3\text{ to }36\text{V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$	(V-)		(V+) - 2.0	V
A_{VD}	Large signal differential voltage amplification ⁽²⁾	$V_S = 15\text{V}$, $V_O = 1.4\text{V to }11.4\text{V}$; $R_L \geq 15\text{k to }(V+)$	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V-)}	$I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$		110	400	mV
		$I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$ $T_A = -40^\circ\text{C to }+85^\circ\text{C}$			550	mV
I_{OH-LKG}	High-level output leakage current	$(V+) = V_O = 5\text{V}$; $V_{ID} = 1\text{V}$		0.1	50	nA
		$(V+) = V_O = 36\text{V}$; $V_{ID} = 1\text{V}$			100	nA
I_{OL}	Low level output current	$V_{OL} = 1.5\text{V}$; $V_{ID} = -1\text{V}$; $V_S = 5\text{V}$	6	21		mA
I_Q	Quiescent current (all comparators)	$V_S = 5\text{ V}$, no load		0.8	1.2	mA
		$V_S = 36\text{ V}$, no load, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$		1	1.6	mA

- (1) The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by $V_{CC} - 2\text{V}$. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.
- (2) This parameter is ensured by design and/or characterization and is not tested in production.

7.10 Electrical Characteristics for LM2901B

$V_S = 5\text{ V}$, $V_{CM} = (V-)$; $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_S = 5\text{ to }36\text{V}$	-3.5	± 0.37	3.5	mV
		$V_S = 5\text{ to }36\text{V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$	-5.5		5.5	
I_B	Input bias current			-3.5	-25	nA
		$T_A = -40^\circ\text{C to }+125^\circ\text{C}$			-50	nA
I_{OS}	Input offset current		-25	± 0.5	25	nA
		$T_A = -40^\circ\text{C to }+125^\circ\text{C}$	-50		50	nA
V_{CM}	Common mode range ⁽¹⁾	$V_S = 3\text{ to }36\text{V}$	(V-)		(V+) - 1.5	V
		$V_S = 3\text{ to }36\text{V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$	(V-)		(V+) - 2.0	V
A_{VD}	Large signal differential voltage amplification ⁽²⁾	$V_S = 15\text{V}$, $V_O = 1.4\text{V to }11.4\text{V}$; $R_L \geq 15\text{k to }(V+)$	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V-)}	$I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$		110	400	mV
		$I_{SINK} \leq 4\text{mA}$, $V_{ID} = -1\text{V}$ $T_A = -40^\circ\text{C to }+125^\circ\text{C}$			550	mV
I_{OH-LKG}	High-level output leakage current	(V+) = $V_O = 5\text{ V}$; $V_{ID} = 1\text{ V}$		0.1	50	nA
		(V+) = $V_O = 36\text{V}$; $V_{ID} = 1\text{ V}$			100	nA
I_{OL}	Low level output current	$V_{OL} = 1.5\text{V}$; $V_{ID} = -1\text{V}$; $V_S = 5\text{V}$	6	21		mA
I_Q	Quiescent current (all comparators)	$V_S = 5\text{ V}$, no load		0.8	1.2	mA
		$V_S = 36\text{ V}$, no load, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$		1	1.6	mA

- (1) The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by $V_{CC} - 2\text{V}$. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.
- (2) This parameter is ensured by design and/or characterization and is not tested in production.

7.11 Electrical Characteristics for LM139 and LM139A

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	T_A ⁽²⁾	LM139			LM139A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{CC} = 5\text{ V to }30\text{ V}$, $V_{IC} = V_{ICR}\text{ min}$, $V_O = 1.4\text{ V}$	25°C		2	5		1	2	mV
		Full range			9			4	
I_{IO} Input offset current	$V_O = 1.4\text{ V}$	25°C		3	25		3	25	nA
		Full range			100			100	
I_{IB} Input bias current	$V_O = 1.4\text{ V}$	25°C		-25	-100		-25	-100	nA
		Full range			-300			-300	
V_{ICR} Common-mode input-voltage range ⁽³⁾		25°C		0 to $V_{CC} - 1.5$			0 to $V_{CC} - 1.5$		V
		Full range		0 to $V_{CC} - 2$			0 to $V_{CC} - 2$		
A_{VD} Large-signal differential-voltage amplification	$V_{CC+} = \pm 7.5\text{ V}$, $V_O = -5\text{ V to }5\text{ V}$	25°C		200		50	200	V/mV	
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$	$V_{OH} = 5\text{ V}$	25°C		0.1		0.1	nA	
		$V_{OH} = 30\text{ V}$	Full range			1		1	μA
V_{OL} Low-level output voltage	$V_{ID} = -1\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C		150	400		150	400	mV
		Full range			700			700	
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$	25°C		6	16		6	16	mA
I_{CC} Supply current (four comparators)	$V_O = 2.5\text{ V}$, No load	25°C		0.8	2		0.8	2	mA

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) Full range (MIN to MAX) for LM139 and LM139A is -55°C to $+125^\circ\text{C}$. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (3) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$; however, one input can exceed V_{CC} , and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30 V without damage.

7.12 Electrical Characteristics for LMx39 and LMx39A

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	T_A ⁽²⁾	LM239 LM339			LM239A LM339A			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO} Input offset voltage	$V_{CC} = 5\text{ V to }30\text{ V}$, $V_{IC} = V_{ICR\text{ min}}$, $V_O = 1.4\text{ V}$	25°C		2	5		1	3	mV	
		Full range			9			4		
I_{IO} Input offset current	$V_O = 1.4\text{ V}$	25°C		5	50		5	50	nA	
		Full range			150			150		
I_{IB} Input bias current	$V_O = 1.4\text{ V}$	25°C		-25	-250		-25	-250	nA	
		Full range			-400			-400		
V_{ICR} Common-mode input-voltage range ⁽³⁾		25°C		0 to $V_{CC} - 1.5$			0 to $V_{CC} - 1.5$		V	
		Full range		0 to $V_{CC} - 2$			0 to $V_{CC} - 2$			
A_{VD} Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V to }11.4\text{ V}$, $R_L \geq 15\text{ k}\Omega\text{ to }V_{CC}$	25°C		50	200		50	200	V/mV	
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$	$V_{OH} = 5\text{ V}$	25°C		0.1	50		0.1	50	nA
		$V_{OH} = 30\text{ V}$	Full range			1			1	μA
V_{OL} Low-level output voltage	$V_{ID} = -1\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C		150	400		150	400	mV	
		Full range			700			700		
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$	25°C		6	16		6	16	mA	
I_{CC} Supply current (four comparators)	$V_O = 2.5\text{ V}$, No load	25°C		0.8	2		0.8	2	mA	

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) Full range (MIN to MAX) for LM239/LM239A is -25°C to $+85^\circ\text{C}$, and for LM339/LM339A is 0°C to 70°C . All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (3) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$; however, one input can exceed V_{CC} , and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30 V without damage.

7.13 Electrical Characteristics for LM2901, LM2901V and LM2901AV

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾		T_A ⁽²⁾	LM2901			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = V_{ICR\text{ min}}$, $V_O = 1.4\text{ V}$, $V_{CC} = 5\text{ V to MAX}^{(3)}$	Non-A devices	25°C	2	7	mV	
			Full range		15		
		A-suffix devices	25°C	1	2		
			Full range		4		
I_{IO} Input offset current	$V_O = 1.4\text{ V}$		25°C	5	50	nA	
			Full range		200		
I_{IB} Input bias current	$V_O = 1.4\text{ V}$		25°C	-25	-250	nA	
			Full range		-500		
V_{ICR} Common-mode input-voltage range ⁽⁴⁾			25°C	0 to $V_{CC} - 1.5$		V	
			Full range	0 to $V_{CC} - 2$			
A_{VD} Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V to } 11.4\text{ V}$, $R_L \geq 15\text{ k}\Omega\text{ to } V_{CC}$		25°C	25	100	V/mV	
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$		$V_{OH} = 5\text{ V}$	25°C	0.1	50	nA
			$V_{OH} = V_{CC}\text{ MAX}^{(3)}$	Full range		1	μA
V_{OL} Low-level output voltage	$V_{ID} = -1\text{ V}$, $I_{OL} = 4\text{ mA}$	Non-V devices	25°C	150	500	mV	
		V-suffix devices		150	400		
		All devices	Full range		700		
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$		25°C	6	16	mA	
I_{CC} Supply current (four comparators)	$V_O = 2.5\text{ V}$, No load		$V_{CC} = 5\text{ V}$	25°C	0.8	2	mA
			$V_{CC} = \text{MAX}^{(3)}$		1	2.5	

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) Full range (MIN to MAX) for LM2901 is -40°C to $+125^\circ\text{C}$. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (3) $V_{CC}\text{ MAX} = 30\text{ V}$ for non-V devices, and 32 V for V-suffix devices
- (4) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$; however, one input can exceed V_{CC} , and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to $V_{CC}\text{ MAX}$ without damage.

7.14 Switching Characteristics for LM139 and LM139A

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		LM139 LM139A	UNIT
			TYP	
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}$ ^{(1) (2)}	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

- (1) C_L includes probe and jig capacitance.
 (2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

7.15 Switching Characteristics for LM339B and LM2901B

$V_S = 5\text{ V}$, $V_{O_PULLUP} = 5\text{ V}$, $V_{CM} = V_S/2$, $C_L = 15\text{ pF}$, $R_L = 5.1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{response}	Propagation delay time, high-to-low; Small scale input signal ⁽¹⁾	Input overdrive = 5mV, Input step = 100mV		1000		ns
t_{response}	Propagation delay time, high-to-low; TTL input signal ⁽¹⁾	TTL input with $V_{\text{ref}} = 1.4\text{ V}$		300		ns

- (1) High-to-low and low-to-high refers to the transition at the input.

7.16 Switching Characteristics for LMx39 and LMx39A

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		LM239 LM239A LM339 LM339A	UNIT
			TYP	
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}$ ^{(1) (2)}	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

- (1) C_L includes probe and jig capacitance.
 (2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

7.17 Switching Characteristics for LM2901

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		LM2901	UNIT
			TYP	
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}$ ^{(1) (2)}	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

- (1) C_L includes probe and jig capacitance.
 (2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

7.18 Typical Characteristics for LM339B and LM2901B Only

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.

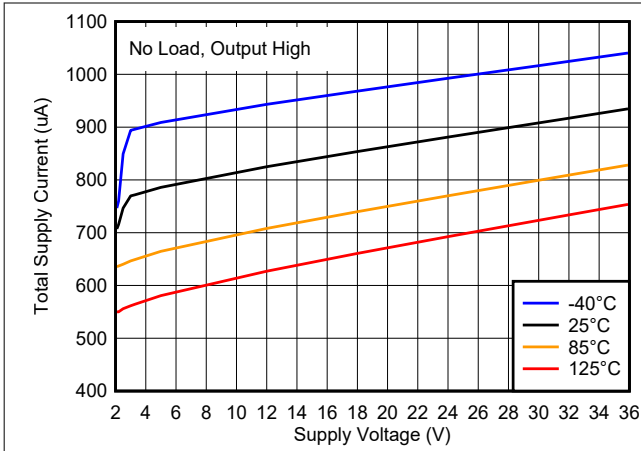


Figure 7-1. Total Supply Current vs. Supply Voltage

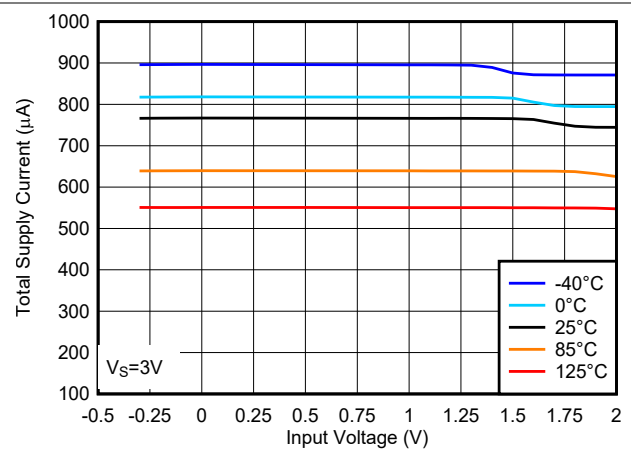


Figure 7-2. Total Supply Current vs. Input Voltage at 3V

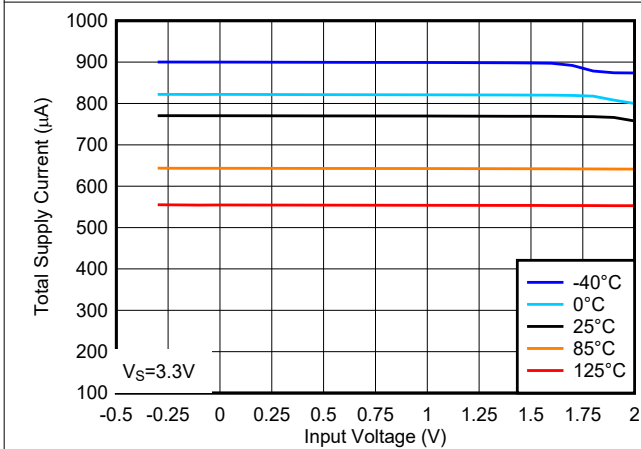


Figure 7-3. Total Supply Current vs. Input Voltage at 3.3V

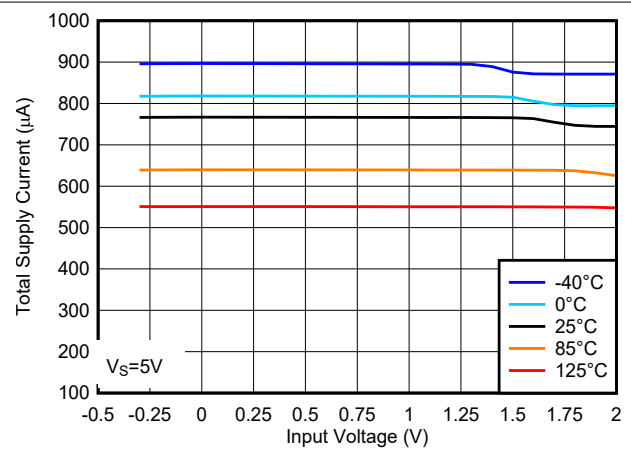


Figure 7-4. Total Supply Current vs. Input Voltage at 5V

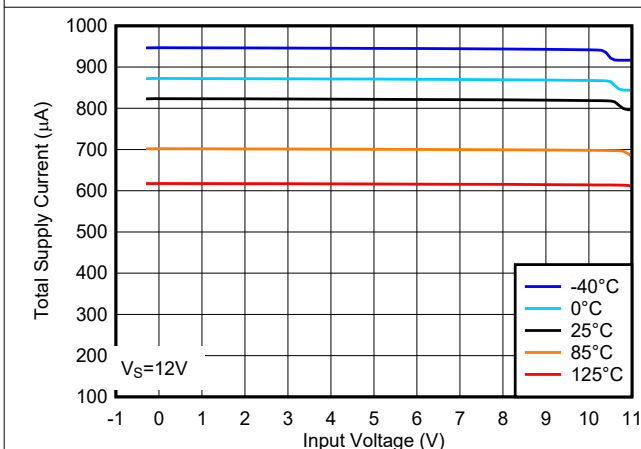


Figure 7-5. Total Supply Current vs. Input Voltage at 12V

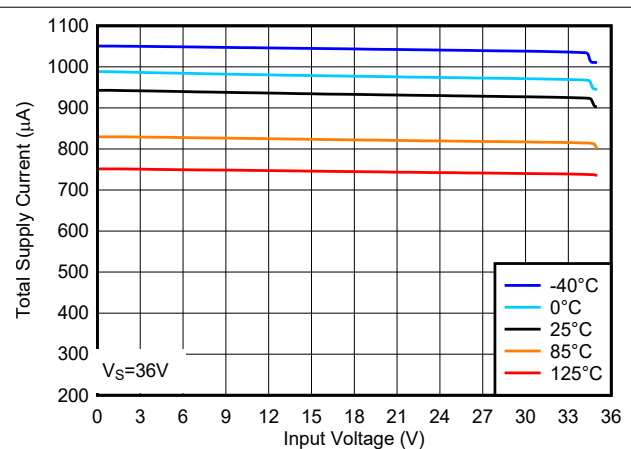
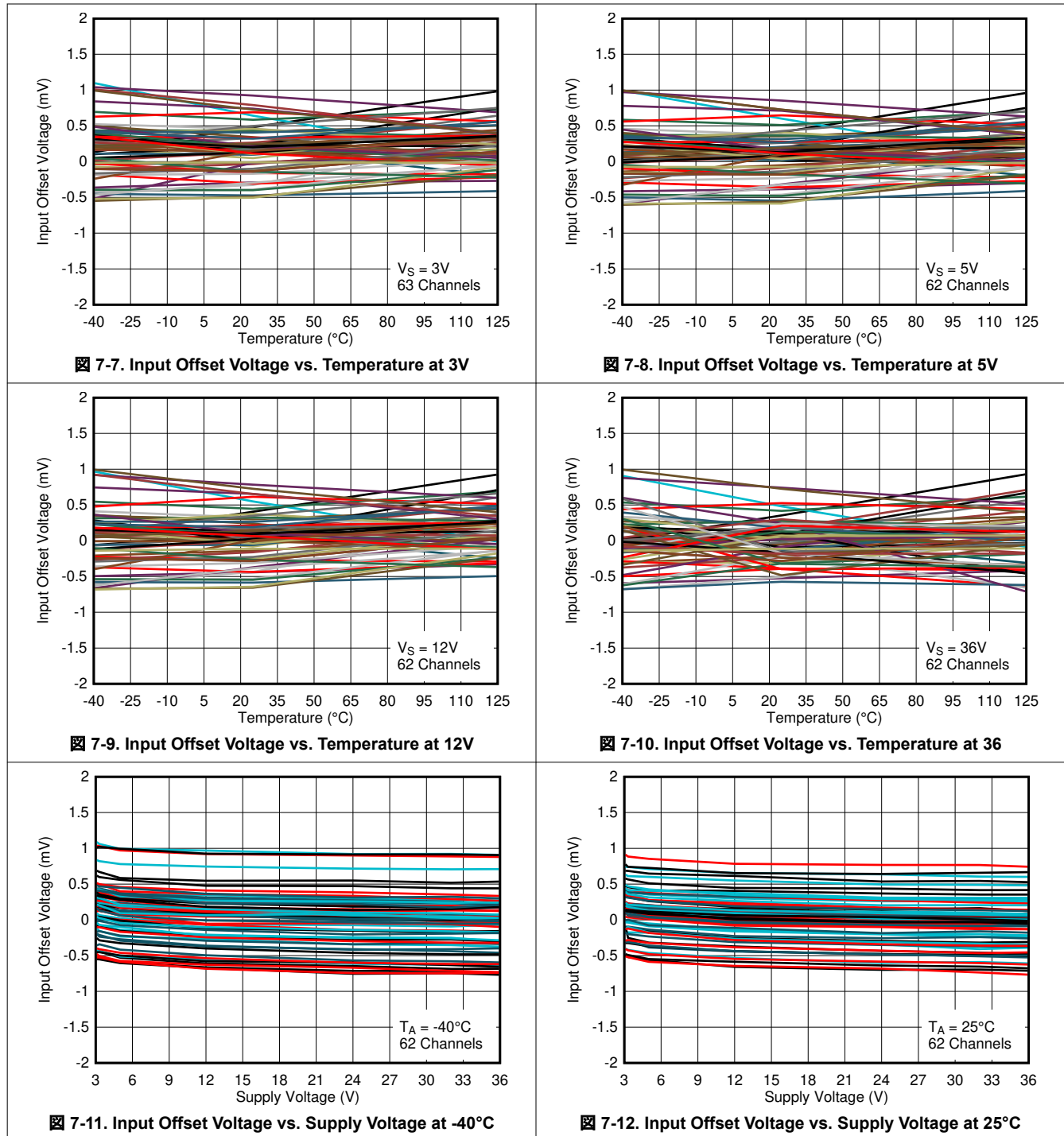


Figure 7-6. Total Supply Current vs. Input Voltage at 36V

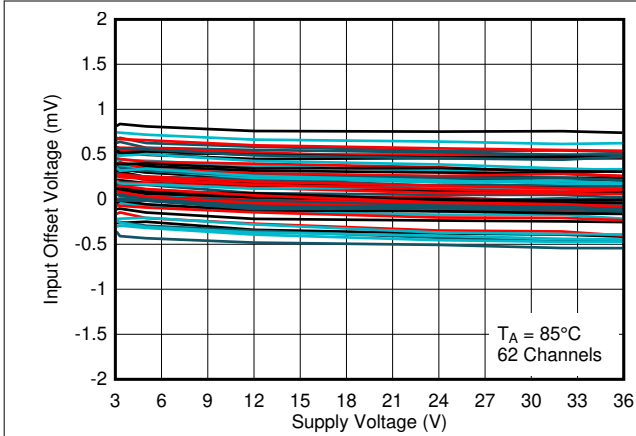
7.18 Typical Characteristics for LM339B and LM2901B Only (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.

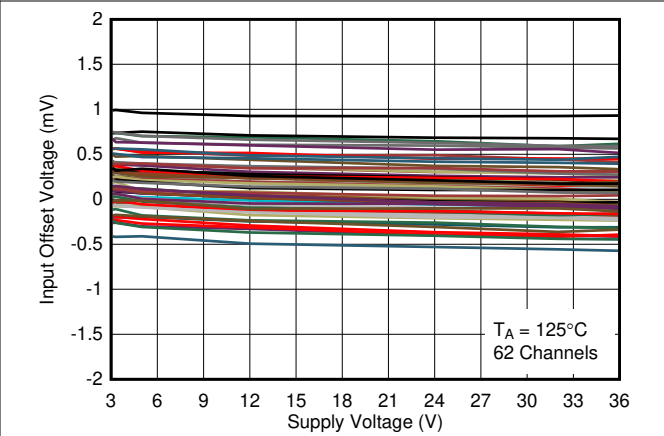


7.18 Typical Characteristics for LM339B and LM2901B Only (continued)

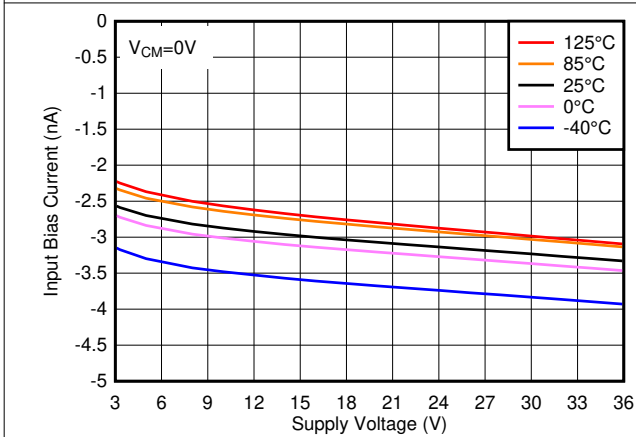
$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.



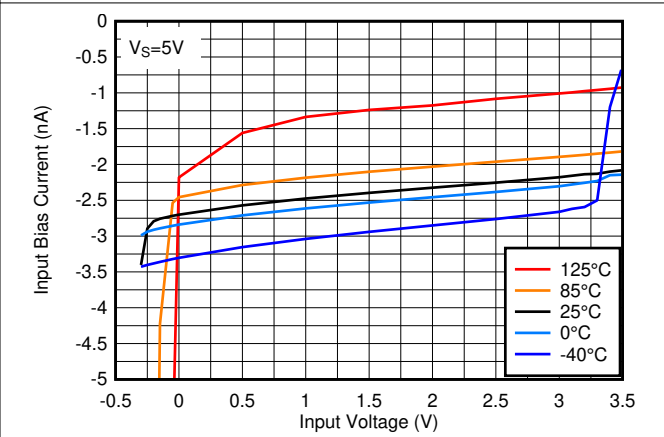
7-13. Input Offset Voltage vs. Supply Voltage at 85°C



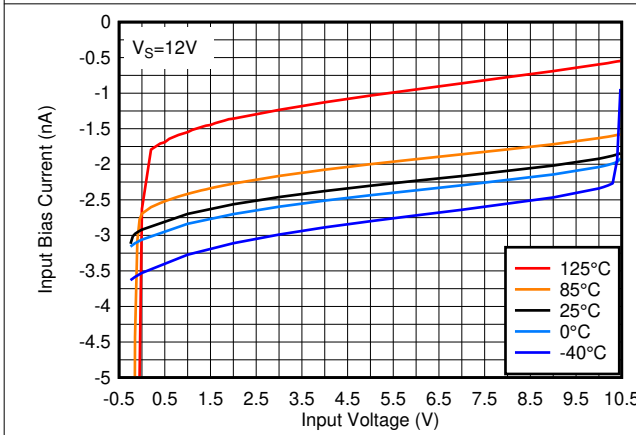
7-14. Input Offset Voltage vs. Supply Voltage at 125°C



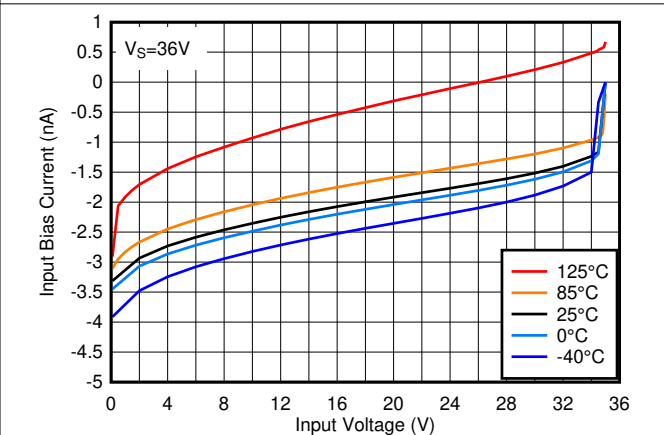
7-15. Input Bias Current vs. Supply Voltage



7-16. Input Bias Current vs. Input Voltage at 5V



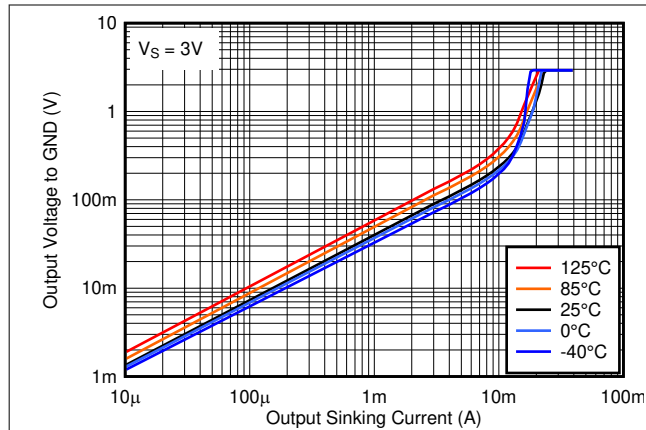
7-17. Input Bias Current vs. Input Voltage at 12V



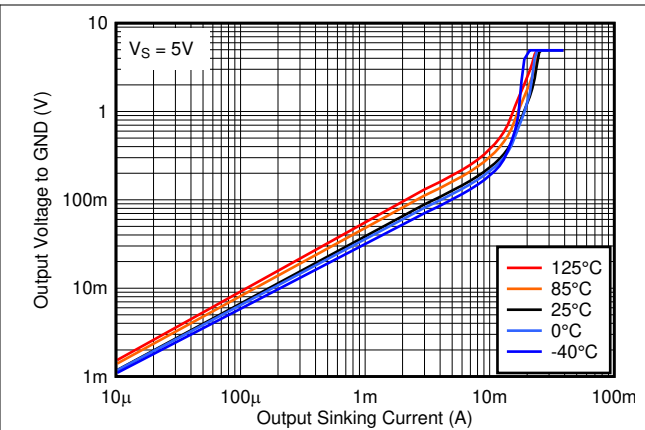
7-18. Input Bias Current vs. Input Voltage at 36V

7.18 Typical Characteristics for LM339B and LM2901B Only (continued)

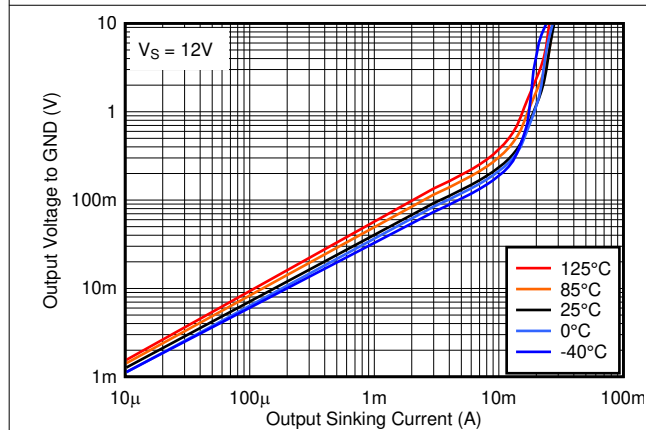
$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.



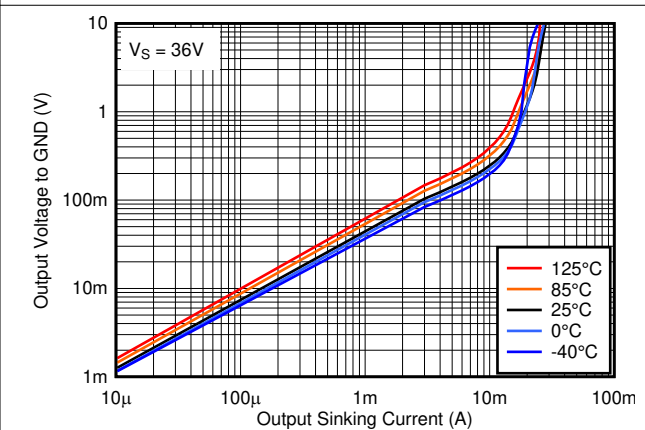
7-19. Output Low Voltage vs. Output Sinking Current at 3V



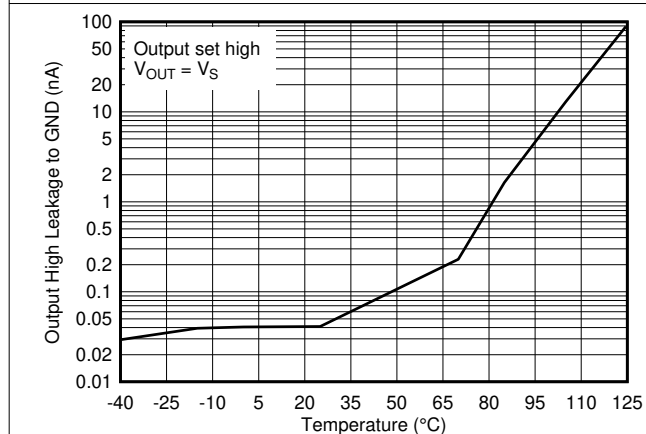
7-20. Output Low Voltage vs. Output Sinking Current at 5V



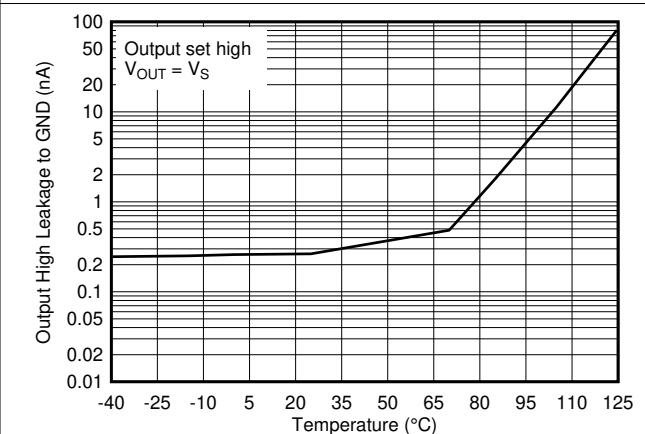
7-21. Output Low Voltage vs. Output Sinking Current at 12V



7-22. Output Low Voltage vs. Output Sinking Current at 36V



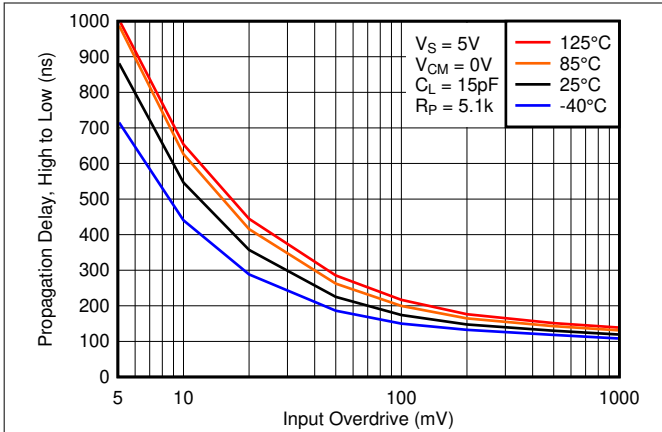
7-23. Output High Leakage Current vs. Temperature at 5V



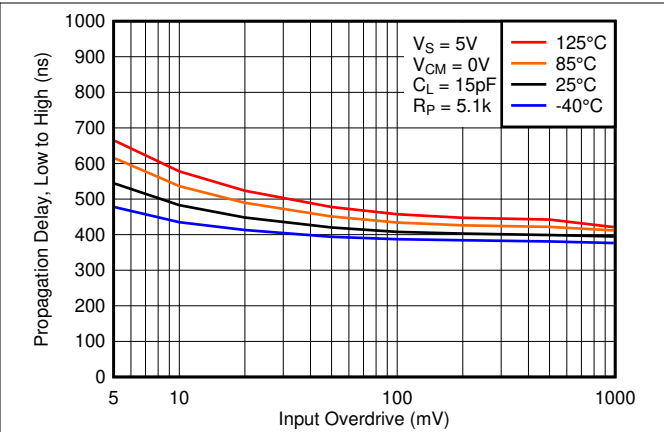
7-24. Output High Leakage Current vs. Temperature at 36V

7.18 Typical Characteristics for LM339B and LM2901B Only (continued)

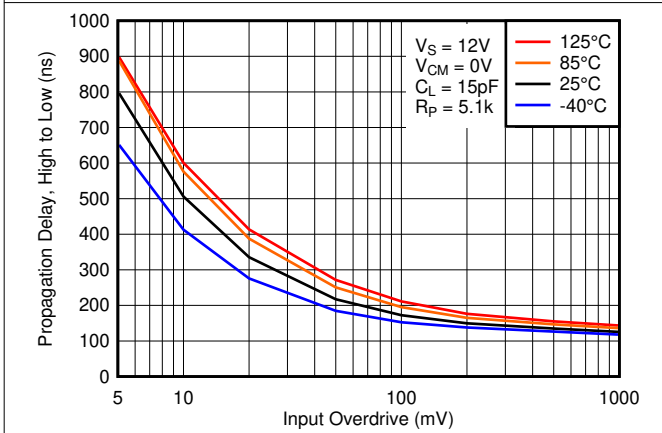
$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.



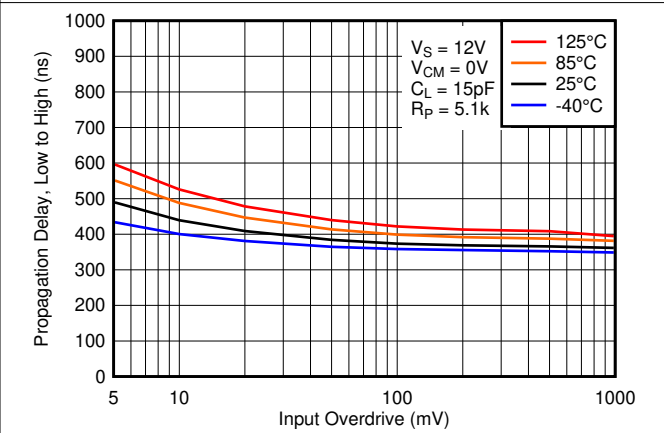
7-25. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V



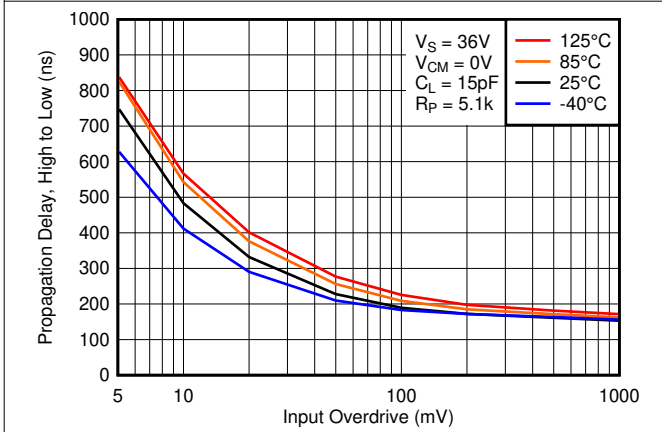
7-26. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V



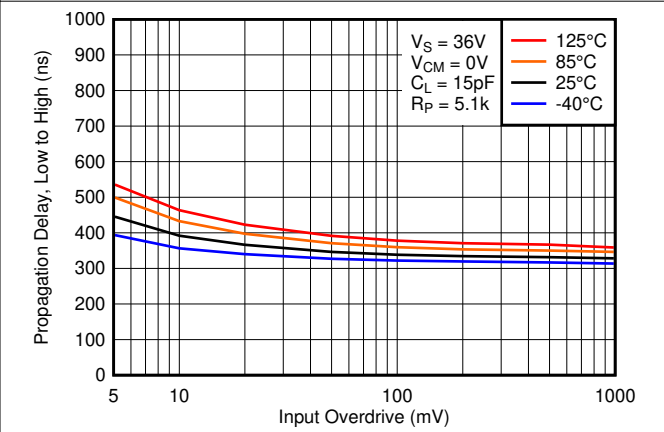
7-27. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V



7-28. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V



7-29. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V



7-30. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V

7.18 Typical Characteristics for LM339B and LM2901B Only (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}$, $C_L = 15\text{ pF}$, $V_{\text{CM}} = 0\text{ V}$, $V_{\text{UNDERDRIVE}} = 100\text{ mV}$, $V_{\text{OVERDRIVE}} = 100\text{ mV}$ unless otherwise noted.

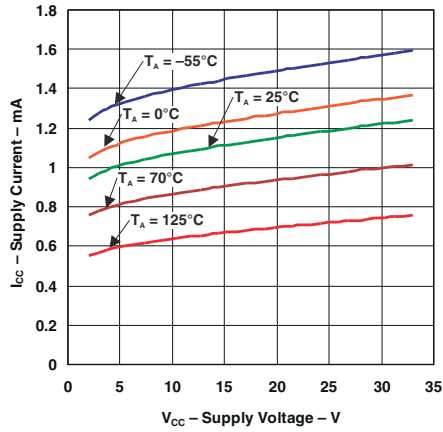


7-31. Response Time for Various Overdrives, High-to-Low Transition

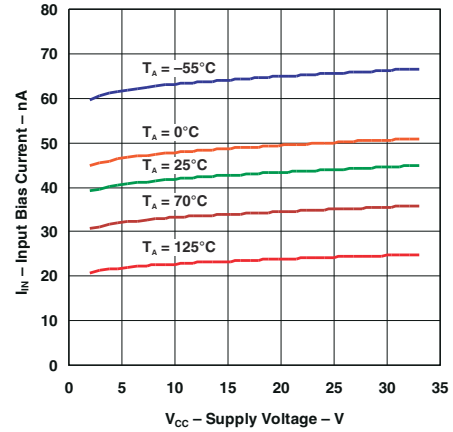


7-32. Response Time for Various Overdrives, Low-to-High Transition

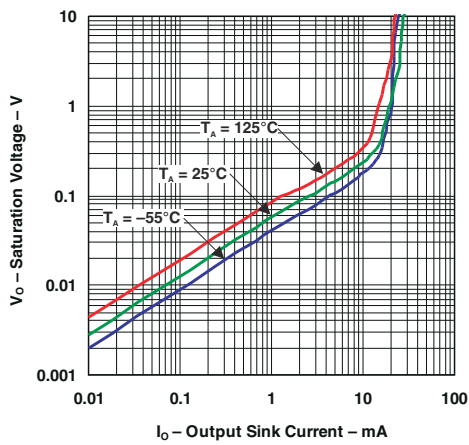
7.19 Typical Characteristics, Non-B Versions



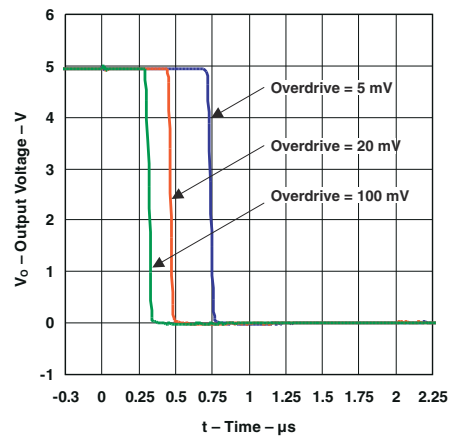
7-33. Supply Current vs Supply Voltage



7-34. Input Bias Current vs Supply Voltage



7-35. Output Saturation Voltage



7-36. Response Time for Various Overdrives Negative Transition



図 7-37. Response Time for Various Overdrives Positive Transition

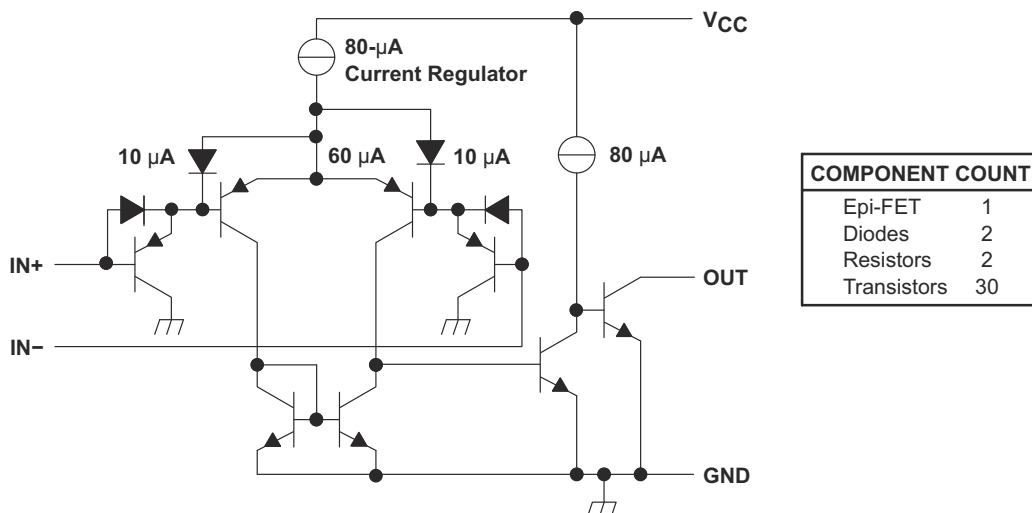
8 Detailed Description

8.1 Overview

The LMx39 and LM2901x are quad comparators with the ability to operate up to an absolute maximum of 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 V up to 32 V), low I_q , and fast response of the device.

The open-drain output allows the user to configure the output logic low voltage (V_{OL}) and allows the comparator to be used in AND functionality.

8.2 Functional Block Diagram



☒ 8-1. Schematic (Each Comparator)

8.3 Feature Description

The comparator consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common-mode voltage capability, allowing the comparator to accurately function from ground to ($V_{CC} - 1.5\text{ V}$) differential input. Allow for ($V_{CC} - 2\text{ V}$) at cold temperature.

The output consists of an open-collector NPN (pulldown or low-side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. See the [セクション 7](#) section for V_{OL} values with respect to the output current.

8.4 Device Functional Modes

8.4.1 Voltage Comparison

The comparator operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

Typically, a comparator compares either a single signal to a reference, or to two different signals. Many users take advantage of the open-drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LMx39 or LM2901x optimal for level shifting to a higher or lower voltage.

9.2 Typical Application

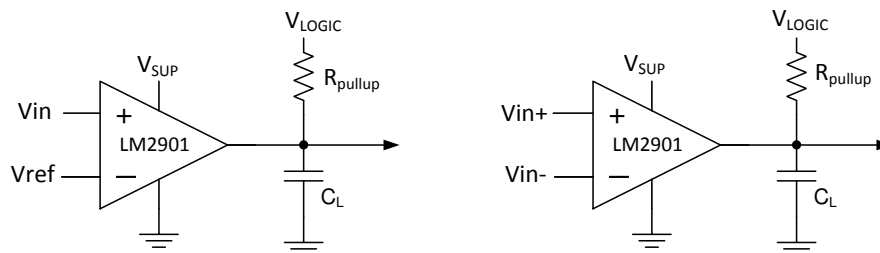


図 9-1. Single-ended and Differential Comparator Configurations

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to $V_{sup}-1.5$ V
Supply Voltage	4.5 V to V_{CC} maximum
Logic Supply Voltage	0 V to V_{CC} maximum
Output Current (R_{PULLUP})	1 μ A to 4 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

9.2.2 Detailed Design Procedure

When using the LMx39 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

9.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common-mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to $V_{CC}-2$ V. This limits the input voltage range to as high as $V_{CC}-2$ V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

The following list describes the outcomes of some input voltage situations.

- When both IN– and IN+ are both within the common-mode range:
 - If IN– is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - If IN– is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
- When IN– is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
- When IN+ is higher than common mode and IN– is within common mode, the output is high impedance and the output transistor is not conducting
- When IN– and IN+ are both higher than common mode, see Section 2 of [Application Design Guidelines for LM339, LM393, TL331 Family Comparators Including the New B-versions](#)

9.2.2.2 Minimum Overdrive Voltage

Overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison, the overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. [Figure 9-2](#) and [Figure 9-3](#) show positive and negative response times with respect to overdrive voltage.

9.2.2.3 Output and Drive Current

Output current is determined by the load and pullup resistance and logic and pullup voltage. The output current produces a low-level output voltage (V_{OL}) from the comparator, where V_{OL} is proportional to the output current.

The output current can also effect the transient response.

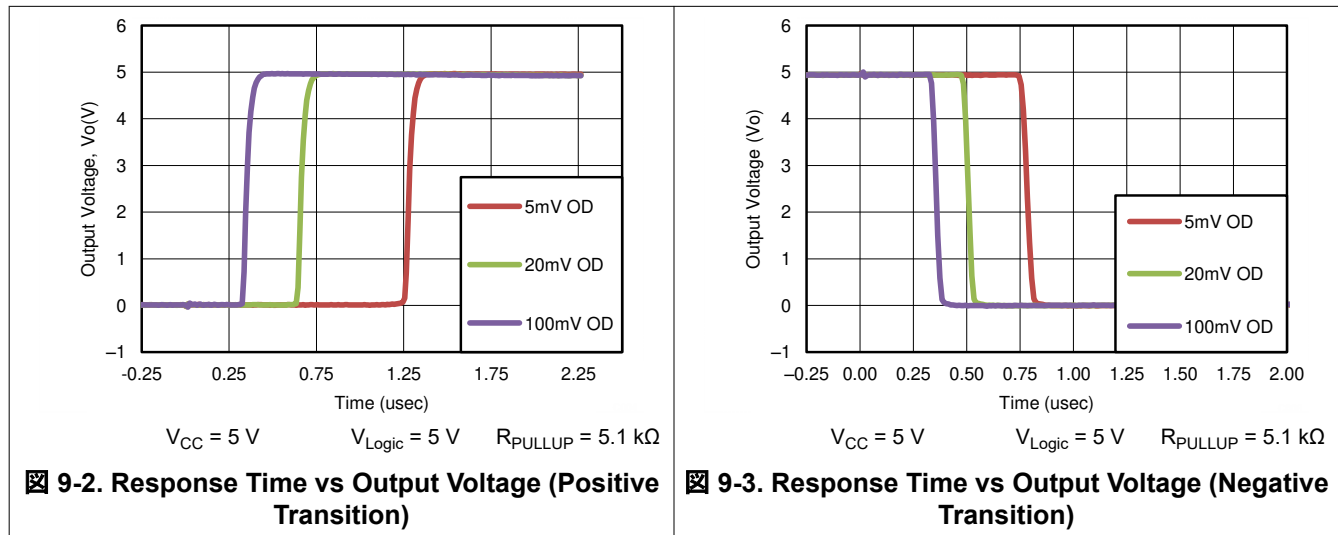
9.2.2.4 Response Time

Response time is a function of input over-drive. See the [Section 7.19](#) graphs for typical response times. The rise and fall times can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (T_R) is approximately $T_R \sim R_{PULLUP} \times C_L$
- The fall time (T_F) is approximately $T_F \sim R_{CE} \times C_L$
 - R_{CE} can be determined by taking the slope of [Figure 7-35](#) in its linear region at the desired temperature, or by dividing the V_{OL} by I_{OUT}

9.2.3 Application Curves

☒ 9-2 and ☒ 9-3 were generated with scope probe parasitic capacitance of 50 pF.



9.3 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can affect the common-mode range of the comparator input and create an inaccurate comparison.

9.4 Layout

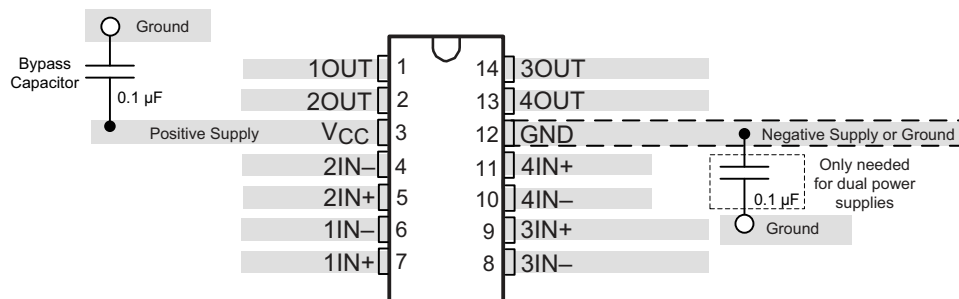
9.4.1 Layout Guidelines

To create an accurate comparator application without hysteresis, maintain a stable power supply with minimized noise and glitches, which can affect the high level input common-mode voltage range. To achieve this accuracy, add a bypass capacitor between the supply voltage and ground. Place a bypass capacitor on the positive power supply and negative supply (if available).

注

If a negative supply is not being used, do not place a capacitor between the GND pin of the device and system ground.

9.4.2 Layout Example



☒ 9-4. LMx39 Layout Example

10 Device and Documentation Support

10.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM139	Click here	Click here	Click here	Click here	Click here
LM239	Click here	Click here	Click here	Click here	Click here
LM339	Click here	Click here	Click here	Click here	Click here
LM139A	Click here	Click here	Click here	Click here	Click here
LM239A	Click here	Click here	Click here	Click here	Click here
LM339A	Click here	Click here	Click here	Click here	Click here
LM2901	Click here	Click here	Click here	Click here	Click here
LM2901AV	Click here	Click here	Click here	Click here	Click here
LM2901V	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM139AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	LM139A	
LM139ADG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	LM139A	
LM139ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A	Samples
LM139ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A	Samples
LM139D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	LM139	
LM139DG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	LM139	
LM139DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139	Samples
LM139DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139	Samples
LM239AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-25 to 85	LM239A	
LM239ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239A	Samples
LM239ADRE4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-25 to 85		Samples
LM239ADRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-25 to 85		Samples
LM239D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-25 to 85	LM239	
LM239DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM239	Samples
LM239DRG4	LIFEBUY	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239	
LM239N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU SN	N / A for Pkg Type	-25 to 85	LM239N	Samples
LM239NE4	ACTIVE	PDIP	N	14	25	TBD	Call TI	Call TI	-25 to 85		Samples
LM239PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-25 to 85	L239	
LM239PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	L239	Samples
LM239PWRG4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-25 to 85	L239	
LM2901AVQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901AV	Samples
LM2901AVQDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901AV	Samples
LM2901AVQPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901AV	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2901AVQPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901AV	Samples
LM2901BIDR	ACTIVE	SOIC	D	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901B	Samples
LM2901BIPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901B	Samples
LM2901BIRTER	ACTIVE	WQFN	RTE	16	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M2901B	Samples
LM2901D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LM2901	
LM2901DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2901N	Samples
LM2901NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	L2901	
LM2901PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L2901	Samples
LM2901PWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L2901	Samples
LM2901PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901	Samples
LM2901VQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V	Samples
LM2901VQPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V	Samples
LM2901VQPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V	Samples
LM339AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LM339A	
LM339ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A	Samples
LM339ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339ADRG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LM339A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM339AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	LM339AN	Samples
LM339ANE4	ACTIVE	PDIP	N	14	25	TBD	Call TI	Call TI	0 to 70		Samples
LM339ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339APW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	L339A	
LM339APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L339A	Samples
LM339APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A	Samples
LM339BIDR	ACTIVE	SOIC	D	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM339B	Samples
LM339BIPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM339B	Samples
LM339BIRTER	ACTIVE	WQFN	RTE	16	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM339B	Samples
LM339D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LM339	
LM339DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	LM339N	Samples
LM339NE3	ACTIVE	PDIP	N	14	25	RoHS & Non-Green	SN	N / A for Pkg Type	0 to 70	LM339N	Samples
LM339NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM339N	Samples
LM339NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	L339	
LM339PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L339	Samples
LM339PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339	Samples
LM339PWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L339	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM339PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM139, LM239A, LM2901, LM2901AV, LM2901B, LM2901V :

- Automotive : [LM239A-Q1](#), [LM2901-Q1](#), [LM2901AV-Q1](#), [LM2901B-Q1](#), [LM2901V-Q1](#)

- Enhanced Product : [LM239A-EP](#)
- Space : [LM139-SP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM139ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM139ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM139DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM139DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901AVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901AVQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901BIDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901BIPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901BIRTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM2901DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2901DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM2901DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM2901PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM339ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM339APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339BIDR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339BIPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339BIRTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM339DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM339DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM339PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM139ADR	SOIC	D	14	2500	350.0	350.0	43.0
LM139ADRG4	SOIC	D	14	2500	350.0	350.0	43.0
LM139DR	SOIC	D	14	2500	350.0	350.0	43.0
LM139DRG4	SOIC	D	14	2500	350.0	350.0	43.0
LM239ADR	SOIC	D	14	2500	356.0	356.0	35.0
LM239ADR	SOIC	D	14	2500	353.0	353.0	32.0
LM239DR	SOIC	D	14	2500	353.0	353.0	32.0
LM239DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM239DRG4	SOIC	D	14	2500	340.5	336.1	32.0
LM239PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901AVQPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901AVQPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901BIDR	SOIC	D	14	3000	356.0	356.0	35.0
LM2901BIPWR	TSSOP	PW	14	3000	356.0	356.0	35.0
LM2901BIRTER	WQFN	RTE	16	5000	367.0	367.0	35.0
LM2901DR	SOIC	D	14	2500	353.0	353.0	32.0
LM2901DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM2901DRG4	SOIC	D	14	2500	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2901DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM2901NSR	SO	NS	14	2000	356.0	356.0	35.0
LM2901PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
LM2901PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901VQPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901VQPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
LM339ADR	SOIC	D	14	2500	353.0	353.0	32.0
LM339ANSR	SO	NS	14	2000	356.0	356.0	35.0
LM339APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339BIDR	SOIC	D	14	3000	356.0	356.0	35.0
LM339BIPWR	TSSOP	PW	14	3000	356.0	356.0	35.0
LM339BIRTER	WQFN	RTE	16	5000	367.0	367.0	35.0
LM339DBR	SSOP	DB	14	2000	356.0	356.0	35.0
LM339DR	SOIC	D	14	2500	353.0	353.0	32.0
LM339DRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM339DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM339NSR	SO	NS	14	2000	356.0	356.0	35.0
LM339PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
LM339PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM239N	N	PDIP	14	25	506	13.97	11230	4.32
LM239N	N	PDIP	14	25	506.1	9	600	5.4
LM2901N	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN	N	PDIP	14	25	506.1	9	600	5.4
LM339N	N	PDIP	14	25	506.1	9	600	5.4
LM339N	N	PDIP	14	25	506	13.97	11230	4.32
LM339N	N	PDIP	14	25	506	13.97	11230	4.32
LM339N	N	PDIP	14	25	506	13.97	11230	4.32
LM339N	N	PDIP	14	25	506	13.97	11230	4.32
LM339NE3	N	PDIP	14	25	506.1	9	600	5.4
LM339NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM339NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM339NE4	N	PDIP	14	25	506	13.97	11230	4.32

D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

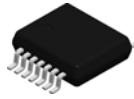
PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

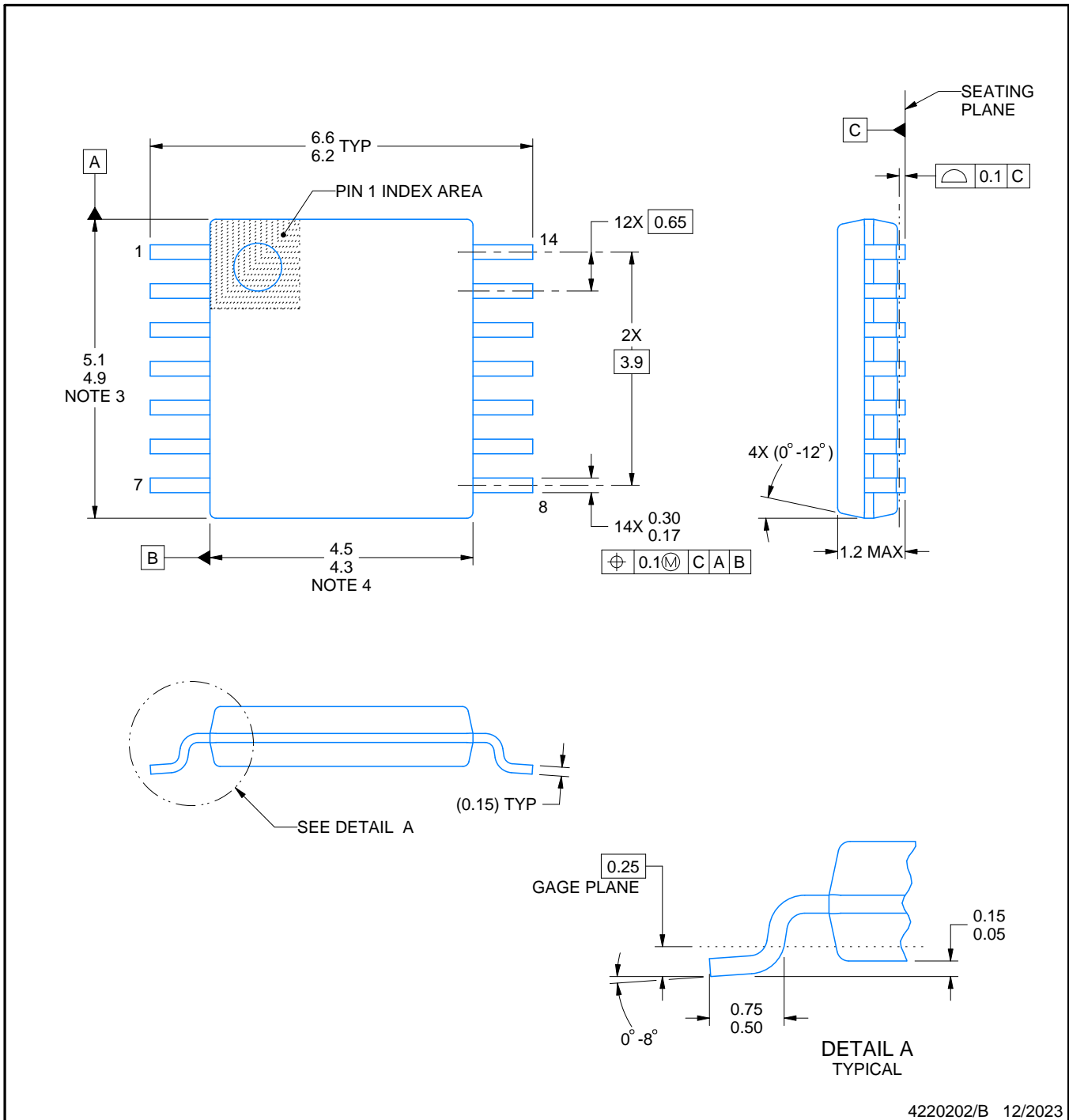
PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RTE 16

WQFN - 0.8 mm max height

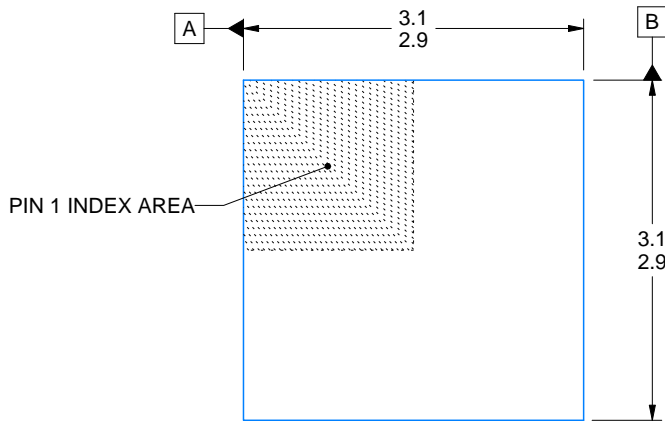
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

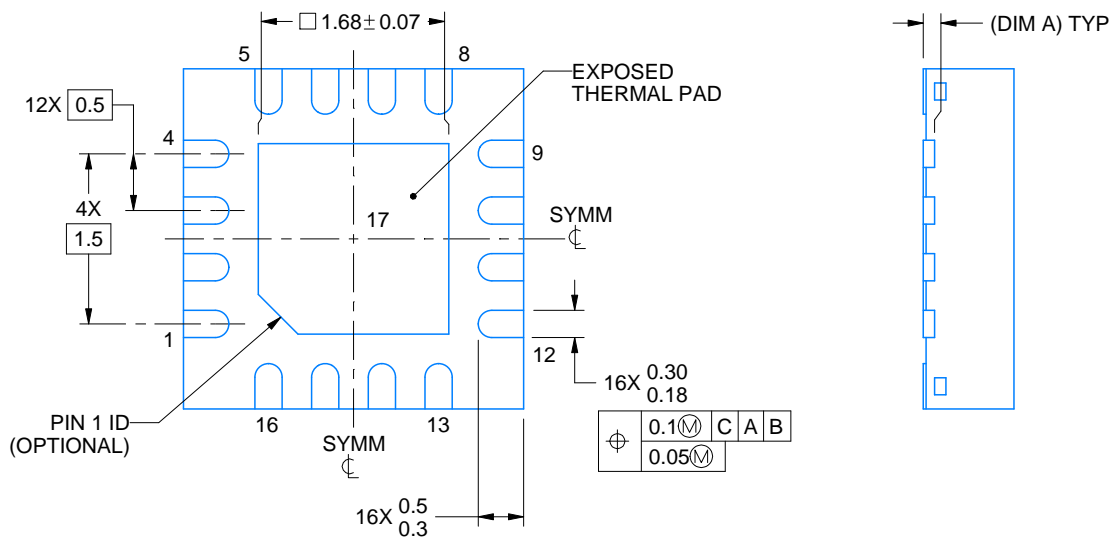
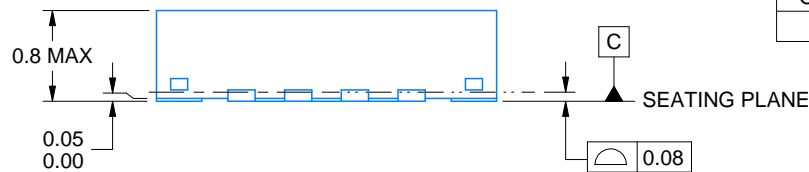
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4219117/B 04/2022

NOTES:

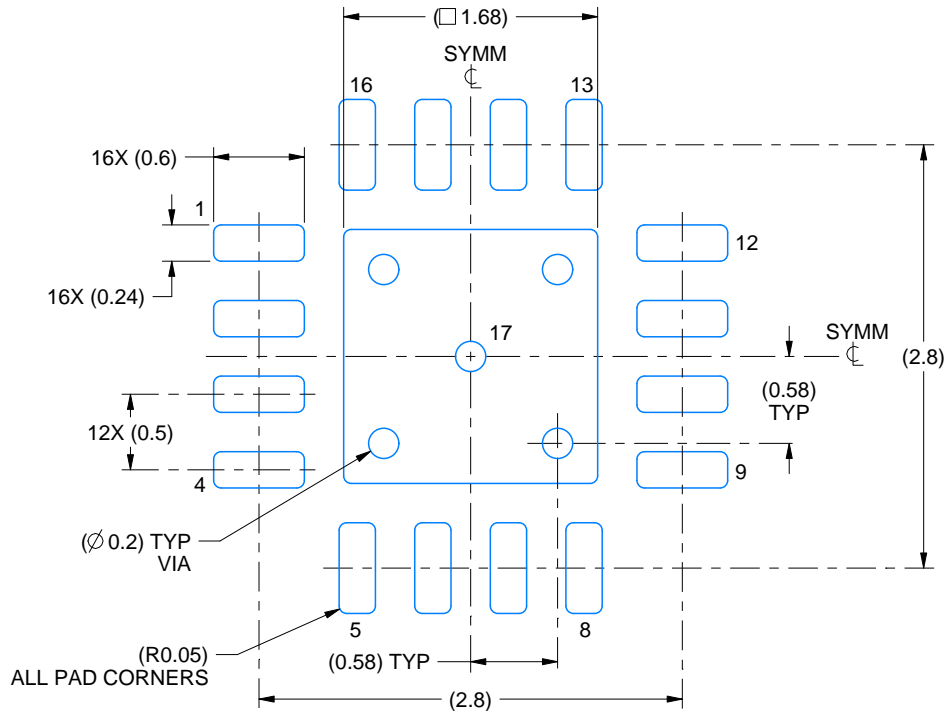
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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